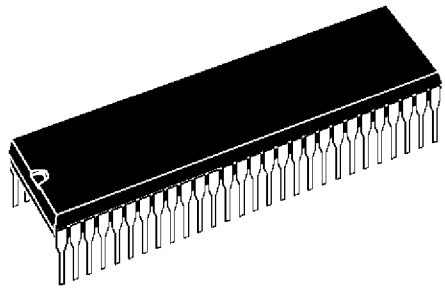
SGS-THOMSON MICROELECTRONICS

ST7272

8-BIT MCU WITH 24K ROM, EEPROM, ADC, PWM/BRM DACs, SYNC PROCESSOR, EWPCC, TIMER AND DDC INTERFACE

PRELIMINARY DATA

- 4.5V to 5.5V Supply Operating Range
- 8MHz Maximum Oscillator Frequency
- Fully Static operation
- 0°C to + 70°C Operating Temperature Range
- Run, Wait, and Halt modes
- User ROM: 24Kbytes
- Data RAM: 384 bytes
- EEPROM: 640 + 256 bytes
- 56 pin Shrink Dual-in-Line plastic package
- 27 multifunctional bidirectional I/O lines:
  - 8 lines with 12V open-drain drive capability
  - 8 Programmable Interrupt inputs
  - 8 Analog inputs
- 16-bit Timer, featuring:
  - 2 Input Captures
  - 2 Output Compares (1 output pin)
- 8-bit Analog-to-Digital converter
- Programmable Watchdog Timer
- 16 10-bit PWM/BRM Digital to Analog outputs
- 2 12-bit PWM/BRM Digital to Analog outputs
- EWPCC circuit with on-chip EEPROM
- New upgraded Sync processor for Mode Recognition, Power Management and Composite Video Blanking generation
- DDC 1/2/AB interface with built-in DMA and I^2C Master/Slave Modes
- Master Reset and Power-On Reset
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS Real-Time Emulator
- Full Software Package (C-Compiler, Cross-Assembler, Debugger)



PSDIP56

(See end of Datasheet for Ordering Information)

This is advance information from SGS-THOMSON. Details are subject to change without notice.

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1 GENERAL DESCRIPTION

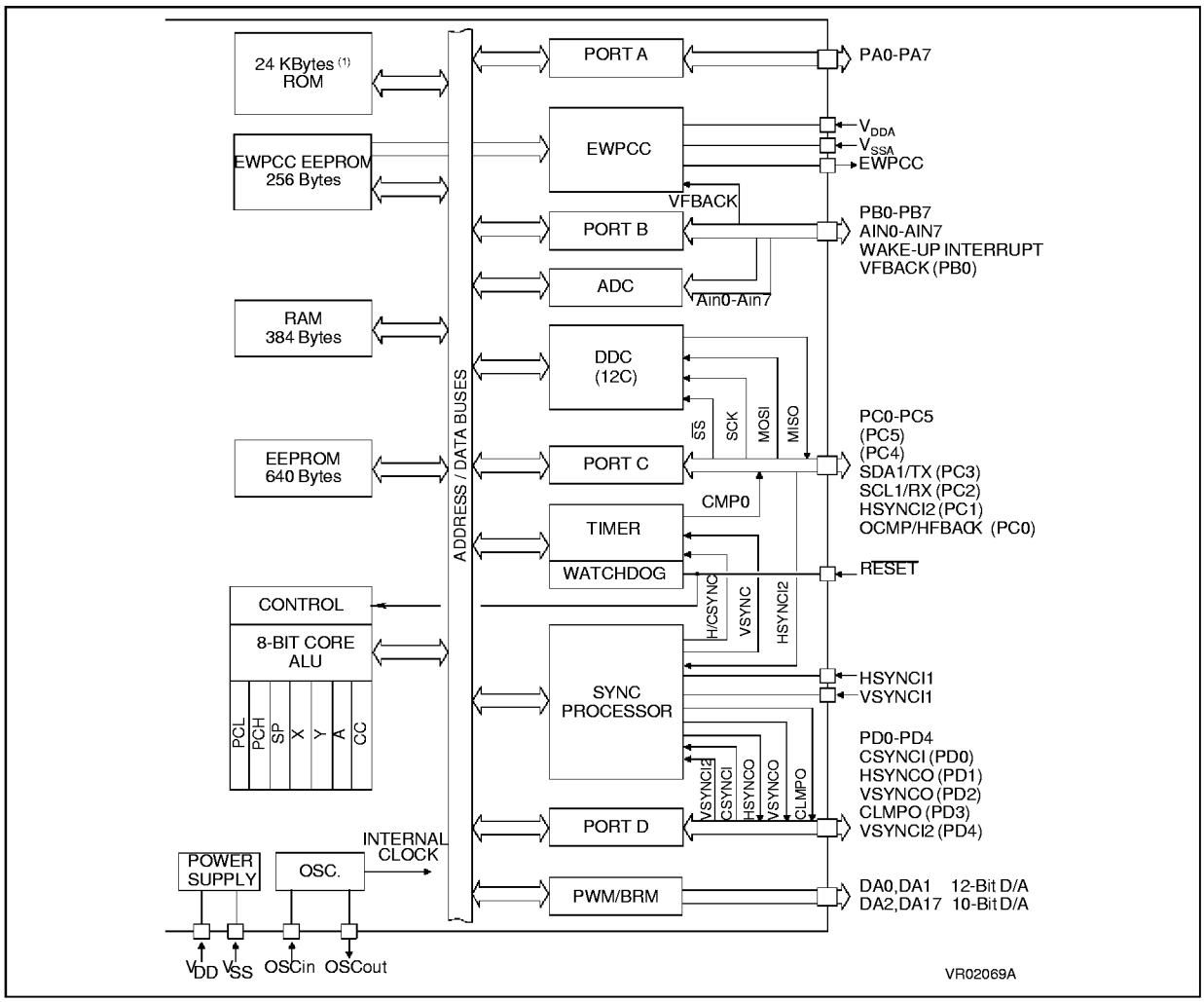
1.1 INTRODUCTION

The ST7272 HCMOS Microcontroller Unit is a member of the ST7 family of Microcontrollers. The device is based on an industry-standard 8-bit core and features an enhanced instruction set. Oscillator frequency can be as high as 8MHz, however, thanks to the fully static design, operation is possible down to DC. Under software control, the ST7272 may be placed in either WAIT or HALT modes, thus reducing power consumption.

The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST7272 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

The device features an on-chip oscillator, CPU, ROM, RAM, EEPROM, 27 multifunctional I/O lines, 12 of which with 12V open-drain drive capability, and the following on-chip peripherals: Analog-to-Digital converter with 8 multiplexed analog inputs, sixteen 10-bit and two 12-bit PWM/BRM analog outputs, EWPCC circuit with EEPROM and analog output, DDC 1/2AB interface with I²C functionality and built-in DMA, digital Watchdog Timer, 16-bit multipurpose Timer featuring 2 Input Captures and 2 Output Compares, and an upgraded Sync Processor offering Mode Recognition, Power Management and Composite Video Blanking generation.

Figure 1. ST7272 Block Diagram



Note1: EPROM/OTP versions also available

1.2 PIN DESCRIPTION

V_{DD} Power supply

V_{SS} Digital Ground

V_{DDA} Analog V_{DD} and reference for EWPCC Digital to Analog Converter (typically 8 Volts).

V_{SSA} Analog V_{SS} for EWPCC DAC.

OSCin, OSCout Oscillator input and output pins; usually connected to a parallel resonant crystal or ceramic resonator. Altenatively an external clock source may also be input via OSCin.

EWPCC Analog correction signal output from East-West Pin Cushion Correction circuit.

SCL1/RX DDC Serial Clock or RX (Falling edge detector with interrupt).

SDA1/TX DDC Serial Data or TX.

OCMP / HFBACK Output compare signal from the Timer.

HSYNCI1 Horizontal Synchronization Input 1.

VSYNCI1 Vertical Synchronization Input 1.

HSYNCI2 Sync Processor Horizontal or complete Synchronization Input 2.

VSYNCI2 Vertical Synchronization Input 2.

CSYNCI Composite Synchronization Input. This pin accepts the composite synchronization input when the Sync Processor I/O functions are enabled.

VFBACK Vertical Flyback signal used for timing correlation for the East-West Pin Cushion correction.

HFBACK Horizontal Flyback Input.

BLANK OUT Video Blanking Output.

HSYNCO Horizontal Synchronization Output from the Sync Processor.

VSYNCO Vertical Synchronization Output from the Sync Processor.

CLMPO Clamp Output. This pin outputs the clamping (back porch) output signal from the Sync Processor .

DA0, DA1 12-bit PWM/BRM outputs (for Analog Controls, after external filtering).

DA2-DA17 10-bit PWM/BRM outputs (for Analog controls, after external filtering).

PORT A 8 I/O lines, bit programmable, accessed through PADDR and PADR Registers. Each bit can be defined as a standard input port bit without pull-up resistor or as an open drain output port (up to 12V).

PORT B 8 Standard bit-programmable I/O lines accessed through the PBDDR and PBDR Registers. Each bit can be programmed as an analog input (by control bits in the PORT B Configuration register), digital input (with internal pull-up resistor), push-pull digital output or as interrupt wake-up (with pull-up). These negative edge or low-level sensitive interrupt lines can wake-up the MCU from WAIT or HALT mode. PB0 is used for the East-West Pin cushion controller VFBACK input when the EWPCC is used.

PORT C 6 Standard bit-programmable I/O lines accessed through the PCDDR and PCDR Registers. PC 0,1 are Inputs with Pull-Up or Push-Pull Outputs, PC 2,3 are Open Drain outputs or Inputs without Pull-Up, PC 4,5 are Open Drain outputs or Digital Inputs with or without Pull-Up internal resistor. The pull-up resistor is enabled for all bits by one control bit in the Programmable Input/Output Configuration Register. PC0 can also be configured as Timer Output Compare pin or Horizontal Flyback Input. PC1 can be programmed as HSYNCI2 sync input for the Sync Processor. PC2/SCL1 and PC3/SDA1 are alternate functions with the DDC cell.

PORT D 5 Standard bit-programmable I/O lines accessed through PDDDR and PDDR Registers. Each bit can be programmed as an input (with internal pull-up resistor), push-pull output or Synchronization inputs and outputs to/from the Sync Processor. When programmed as inputs, Video Synchronization signals can be directly inspected. The inputs may also be passed through the Sync Processor to the Timer Input Captures.

$\overline{\text{RESET}}$ An active-low signal on this pin forces initialization of the MCU. This is the top priority non maskable interrupt. This pin is driven low if the Watchdog Timer has been triggered. The resulting pulse can be used to reset external peripherals.

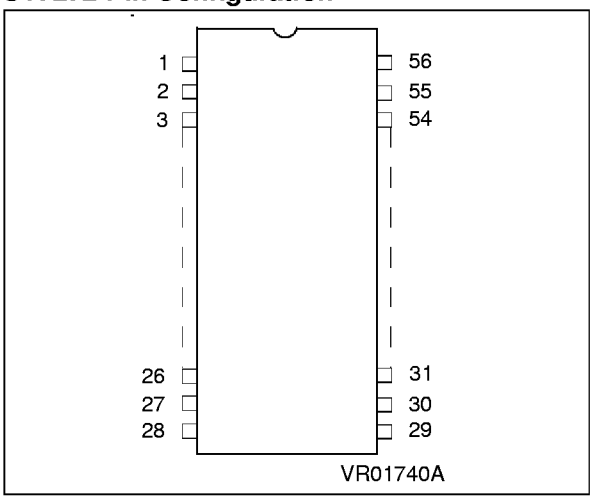
TEST This pin must be held low for normal operation.

CAUTION: *The TEST pin MUST be connected directly to the V_{SS} pin on the device in order to ensure correct operation.*

PIN DESCRIPTION (Cont'd)

The following table describes basic and alternate functions for each pin. Relevant ancillary information is given in the Remarks column. The pin configuration is illustrated for convenience.

ST7272 Pin Configuration

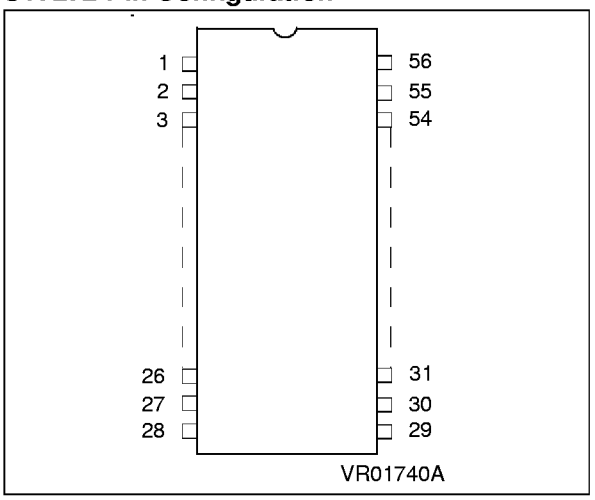


Pin Name(s)	Basic Function	Alternate Function	Pin	Remarks
V_{DDA}	Analog power supply	-	1	Typically +8V
EWPCC	EWPCC circuit analog output	-	2	2 - 6V
DA0	12-bit DAC PWM outputs	--	3	Generated by PWM/BRM circuitry, need external filtering.
DA1			4	
DA2	10-bit DAC PWM outputs	--	5	
DA3			6	
DA4			7	
DA5			8	
DA6			9	
DA7			10	
DA8			11	
DA9			12	
PB7	Port B I/Os	Analog input	13	Standard I/O or alternate function. The I/O configuration is software programmable as input with pull-ups, wake-up interrupt input, or push-pull output.
PB6			14	
PB5			15	
PB4			16	
PB3			17	
PB2			18	
PB1			19	
PB0 / VFBACK		Analog input or VFBACK	20	As above, or input for EWPCC circuit, when active.
PD4 / VSYNCI2	Port D I/O	VSYNCI2	21	Vertical Sync input 2 (TTL with pull-up).
PD3 / CLMPO	Port D I/O	CLMPO	22	Clamp output from Sync circuit.
DA10	10-bit DAC PWM outputs	-	23	Generated by PWM/BRM circuitry, need external filtering.
DA11			24	

PIN DESCRIPTION (Cont'd)

The following table describes basic and alternate functions for each pin. Relevant ancillary information is given in the Remarks column. The pin configuration is illustrated for convenience.

ST7272 Pin Configuration

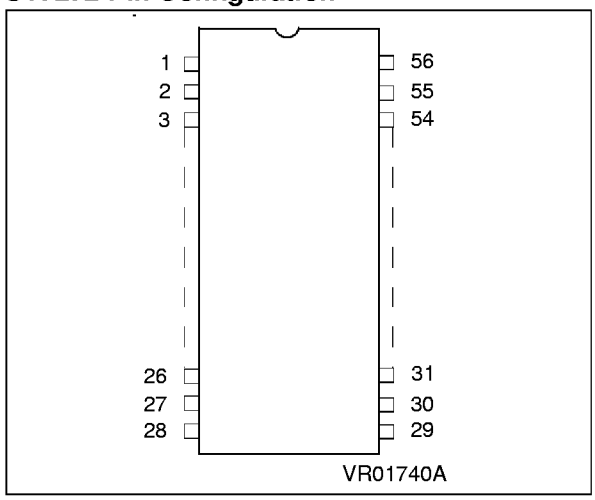


Pin Name(s)	Basic Function	Alternate Function	Pin	Remarks
$\overline{\text{RESET}}$	General reset input and output	-	25	As an input, a Reset is generated by an active low signal; when the Watchdog has triggered this pin will be driven low to reset external peripherals.
PD2 / VSYNCO	Port D I/O	VSYNCO	26	Vertical Sync output from Sync processor.
VSYNCI1	VSYNCI1		27	Vertical Sync input to Sync processor (TTL with pull-up).
V_{DD}	Power supply to digital circuits.	-	28	4.5 - 5.5V
HSYNCI1	HSYNCI1		29	Horizontal Sync input to Sync processor (TTL with pull-up).
PD1 / HSYNCO	Port D I/Os	HSYNCO	30	Horizontal Sync output from Sync processor.
PD0 / CSYNCI		CSYNCI	31	Composite Sync input (TTL with pull-up).
OSCOUT	Oscillator output	-	32	These pins may be connected to a parallel resonant crystal or ceramic resonator; alternatively an external clock source may be connected to OSCIN.
OSCIN	Oscillator input		33	
DA12	10-bit DAC PWM outputs	-	34	Generated by PWM/BRM circuitry, need external filtering.
DA13			35	
PA7 / BLANKOUT	Port A I/Os	BLANKOUT	36	Video blanking output from Sync processor.
PA6		-	37	Standard I/Os, bit programmable via PADDR and PADR registers as inputs without pull-ups or as open-drain outputs (up to 12V).
PA5			38	
PA4			39	
PA3			40	
PA2			41	
PA1			42	
PA0			43	

PIN DESCRIPTION (Cont'd)

The following table describes basic and alternate functions for each pin. Relevant ancillary information is given in the Remarks column. The pin configuration is illustrated for convenience.

ST7272 Pin Configuration



Pin Name(s)	Basic Function	Alternate Function	Pin	Remarks
DA14	10-bit DAC PWM outputs	-	44	Generated by PWM/BRM circuitry, need external filtering.
DA15			45	
DA16			46	
DA17			47	
TEST	TEST	-	48	This pin is for SGS-THOMSON internal use only and **MUST** be tied directly to V_{SS} for normal operation
PC0 / OCMP / HFBACK	Port C I/Os	OCMP or HFBACK	49	Output compare from Timer peripheral. or Horizontal flyback input (TTL with pull-up).
PC1 / HSYNCI2		HSYNCI2	50	Horizontal Sync input to Sync processor (TTL with pull-up).
PC2 / SCL1 / RX		SCL1 RX	51	DDC serial clock. Can generate interrupt on falling edge for RX Start detection for software SCI.
PC3 / SDA1 / TX		SDA1 TX	52	DDC serial data. OCMP can generate interrupt for TX bit timing for software SCI.
PC4		-	53	
PC5			54	
V_{SS}	Digital Ground	-	55	
V_{SSA}	Analog Ground	-	56	

1.3 MEMORY MAP

Table 1. ST7272 Memory Map

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0000h		PADR	Port A Data Register	XXh	R/W Register
0001h		PBDR	Port B Data Register	XXh	R/W Register
0002h		PCDR	Port C Data Register	XXh	R/W Register
0003h		PDDR	Port D Data Register	XXh	R/W Register
0004h		PADDR	Port A Data Direction Register	00h	R/W Register
0005h		PBDDR	Port B Data Direction Register	00h	R/W Register
0006h		PCDDR	Port C Data Direction Register	00h	R/W Register
0007h		PDDDR	Port D Data Direction Register	00h	R/W Register
0008h	ADC	DR	ADC Data Register	XX	Read Only Register
0009h		CR	ADC control/Status register	00h	R/W Register
000Ah	Reserved				
000Bh	EW	DACR	East/West DAC Register	00h	R/W Register
000Ch		PCC0	East/West Control 0	00h	R/W Register
000Dh		PCC1	East/West Control 1	C0h	R/W Register
000Eh	EEP	CR0	DDC EEPROM Control register	00h	R/W Register
000Fh		CR1	GP1 EEPROM Control register	00h	R/W Register
0010h		CR2	GP2 EEPROM Control register	00h	R/W Register
0011h		CR3	E/W EEPROM Control register	00h	R/W Register
0012h	TIM	CR	TIMER Control Register	00h & 02h	R/W Register
0013h		SR	TIMER Status Register	XXh	Read Only Register
0014h		IC1HR	TIMER Input Capture High Register 1	XXh	Read only
0015h		IC1LR	TIMER Input Capture Low Register 1	XXh	Read only
0016h		OC1HR	TIMER Output Compare High Register 1	XXh	R/W Register
0017h		OC1LR	TIMER Output Compare Low Register 1	XXh	R/W Register
0018h		CNTHR	TIMER Counter High Register	FFh	Read only
0019h		CNTLR	TIMER Counter Low Register	FCh	R/W Register
001Ah		ACNTHR	TIMER Alternate Counter High Register	FFh	Read only
001Bh		ACNTLR	TIMER Alternate Counter Low Register	FCh	R/W Register
001Ch		IC2HR	TIMER Input Capture High Register 2	XXh	Read only
001Dh		IC2LR	TIMER Input Capture Low Register 2	XXh	Read only
001Eh		OC2HR	TIMER Output Compare High Register 2	XXh	R/W Register
001Fh		OC2LR	TIMER Output Compare Low Register 2	XXh	R/W Register
0020h	PWM/BRM	PWM0	(12-BIT PWM) Register	80h	R/W Register
0021h		BRM0	(12-BIT BRM) Register	C0h	R/W Register
0022h		PWM1	(12-BIT PWM) Register	80h	R/W Register
0023h		BRM1	(12-BIT BRM) Register	C0h	R/W Register

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0024h	PWM/BRM	PWM2	10-BIT PWM/BRM Registers	80h	R/W Registers
0025h		BRM3 + BRM2		00h	
0026h		PWM3		80h	
0027h		PWM4		80h	
0028h		BRM5+ BRM4		00h	
0029h		PWM5		80h	
002Ah		PWM6		80h	
002Bh		BRM7 + BRM6		00h	
002Ch		PWM7		80h	
002Dh		PWM8		80h	
002Eh		BRM9+ BRM8		00h	
002Fh		PWM9		80h	
0030h		PWM10		80h	
0031h		BRM11 + BRM10		00h	
0032h		PWM11		80h	
0033h		PWM12		80h	
0034h		BRM13+ BRM12		00h	
0035h		PWM13		80h	
0036h		PWM14		80h	
0037h		BRM15 + BRM14		00h	
0038h		PWM15		80h	
0039h		PWM16		80h	
003Ah		BRM17+ BRM16		00h	
003Bh		PWM17		80h	
003Ch		PBICFGR	Port B Input Pull-Up Configuration Register	00h	R/W Register
003Dh		PIOCFGR	Programmable I/O Configuration Register	F8h	R/W Register
003Eh		WDOGR	Watchdog Register	7Fh	R/W Register
003Fh		MISCR	Miscellaneous Register	2Ah	R/W Register
0040h	SYNC	CFGR	SYNCHRO Configuration Register	00h	R/W Register
0041h		MCR	SYNCHRO Multiplexer Register	00h	R/W Register
0042h		CCR	SYNCHRO Counter Register	00h	R/W Register
0043h		POLR	SYNCHRO Polarity Register	00h	R/W Register
0044h		LATR	SYNCHRO Latch Register	00h	R/W Register
0045h		HGENR	SYNCHRO H Sync Generator Register	00h	R/W Register
0046h		VGENR	SYNCHRO V Sync Generator Register	00h	R/W Register
0047h		ENR	SYNCHRO Processor Enable Register	00h	R/W Register

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0048h	DMA	IADHR	DMA Initial High Address Register	XXh	R/W Register
0049h		IADLR	DMA Initial Low Address Register	XXh	R/W Register
004Ah		CADHR	DMA current High Address Register	XXh	R/W Register
004Bh		CADLR	DMA current Low Address Register	XXh	R/W Register
004Ch		ICTR	DMA Initial Counter Register	XXh	R/W Register
004Dh		CCTR	DMA current Counter Register	XXh	R/W Register
004Eh		CTLR	DMA Control Register	00h	R/W Register
004Fh	Reserved				
0050h	DDC	CR	DDC Control Register	00h	R/W Register
0051h		SR1	DDC 1st Status Register	00h	Read only
0052h		SR2	DDC 2nd Status Register	00h	Read only
0053h		CCR	DDC Clock Control Register	00h	R/W Register
0054h		OAR1	DDC 7 Bits Slave address Register	00h	R/W Register
0055h			Reserved		
0056h		DR	DDC Data Register	00h	R/W Register
0057h			Reserved		
0058h	CRC	CRCL	CRC Low register / Reserved	ST INTERNAL USE ONLY	
0059to		CRCH	CRC High register/ Reserved		
005Ah to 007Fh	Reserved				
0080h to 01BFh			User RAM 384 bytes, including stack		
01C0h to 01FFh			Stack 64bytes		
0200h to 027Fh	Reserved				
0280h to 02FFh		DDC-EEPROM	128 bytes dedicated for DDC EEPROM		EEPROM 896 bytes in 4 banks
0300h to 03FFh		GP1-EEPROM	256 bytes for Data GP1 EEPROM		
0400h to 04FFh		GP2-EEPROM	256 bytes for Data GP2 EEPROM		
0500h to 05FFh		EWPCC-EEP-ROM	256 bytes for either EWPCC or Data GP3 EEPROM		

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0600h to 07FFh	Unused				
0800h to 08FFh	Reserved				
0900h to 13FFh	Unused				
1400h to 1FFFh	Reserved				
2000h to 7EFFh			24K bytes ROM		
7F00h to 7FEFh	Reserved				
7FF0h to 7FFFh		7FF0-7FF1	DDC/DMA (OR wiring)		Internal Interrupts
		7FF2-7FF3	TIMER Overflow TOF		"
		7FF4-7FF5	TIMER Output compare OCMP		"
		7FF6-7FF7	TIMER Input capture ICAP		"
		7FF8-7FF9	RX falling edge		"
		7FFA-7FFB	Key Board (PORT B)		External Interrupts
		7FFC-7FFD	TRAP (software)		"
		7FFE-7FFF7	RESET vector		CPU Interrupt

2 CENTRAL PROCESSING UNIT

2.1 INTRODUCTION

The CPU has a full 8-bit architecture. Six internal registers allow efficient 8-bit data manipulations. The CPU is capable of executing 63 basic instructions and features 17 main addressing modes. The ST7272 device can address 24 Kbytes of program memory, as well as 384 bytes of data and register memory.

2.2 CPU REGISTERS

The 6 CPU registers are shown in the programming model in Figure 2. Following an interrupt, all registers except Y are pushed onto the stack in the order shown in Figure 3. They are popped from stack in the reverse order.

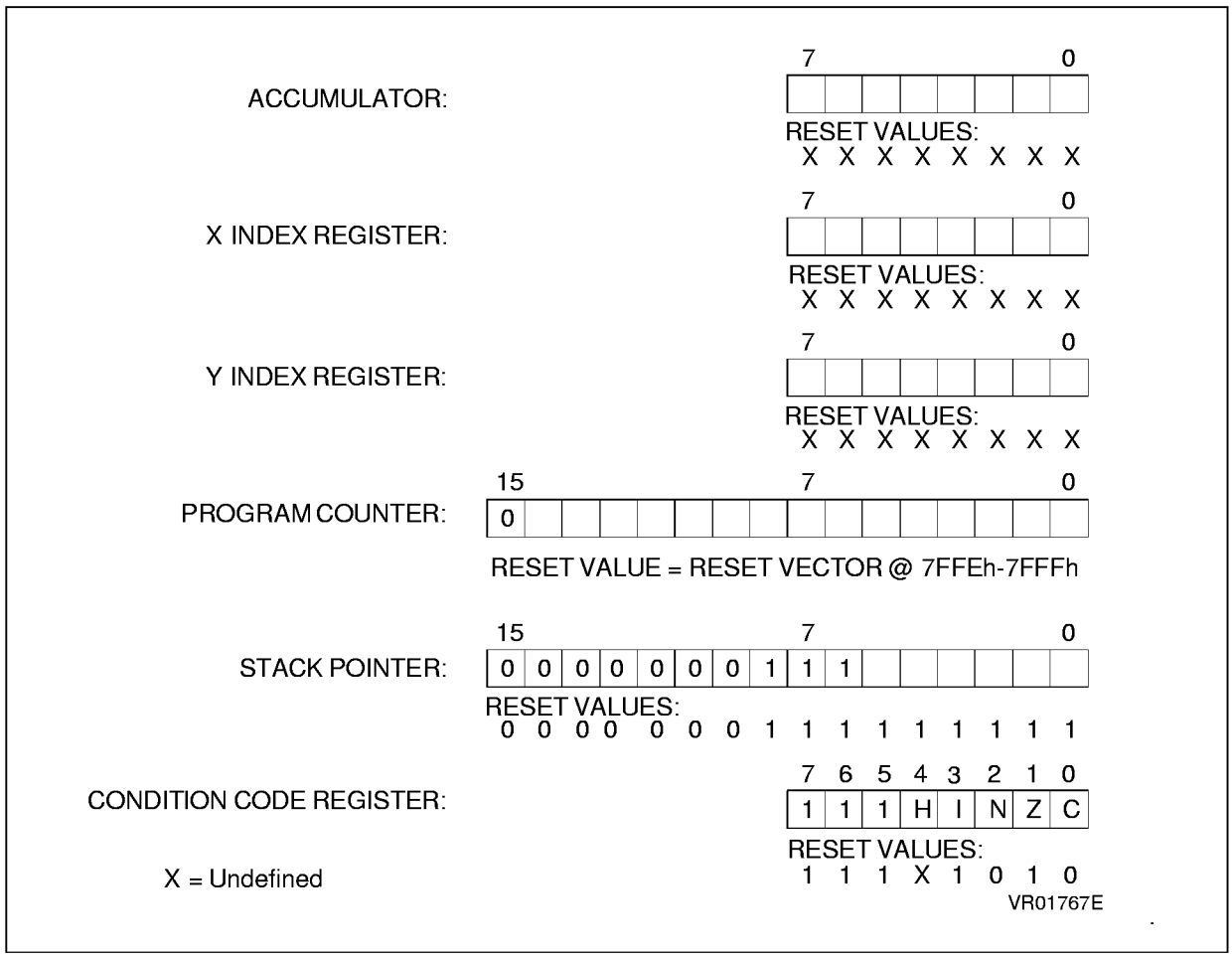
The Y register is not affected by these automatic procedures. The interrupt routine must therefore handle Y, if necessary, through the PUSH and POP instructions.

Accumulator (A). The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations as well as data manipulations.

Index Registers (X and Y). These 8-bit registers are used to create effective addresses or as temporary storage areas for data manipulation. The Cross-Assembler generates a PRECEDE instruction (PRE) to indicate that the following instruction refers to the Y register. The Y register is never automatically stacked. Interrupt routines must push or pop it by using the PUSH and POP instructions.

Program Counter (PC). The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU.

Figure 2. Organisation of Internal CPU Registers



CPU REGISTERS (Cont'd)

Stack Pointer (SP) The Stack Pointer is a 16-bit register. Since the stack is 64 bytes deep, the 10 most significant bits are forced as indicated inFigure 2 in order to address the stack as it is mapped in memory.

The stack is used to save the CPU context during subroutine calls or interrupts. The user may also directly manipulate the stack by means of the PUSH and POP instructions.

Following an MCU Reset, or after a Restore following a Reset Stack Pointer instruction (RSP), the Stack Pointer is set to point to the highest location in the stack. It is then decremented after data has been pushed onto the stack and incremented after data is popped from the stack. When the lower limit is exceeded, the Stack Pointer wraps around to the stack upper limit. The previously stored information is then overwritten and therefore lost. The upper and lower limits of the stack area are shown in the Memory Map, seeTable 1.

A subroutine call occupies two locations and an interrupt five locations in the stack area.

Condition Code Register (CC) The Condition Code register is a 5-bit register which indicates the result of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. The following paragraphs describe each bit of the CC register in turn.

Half carry bit (H) The H bit is set to 1 when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in BCD arithmetic subroutines.

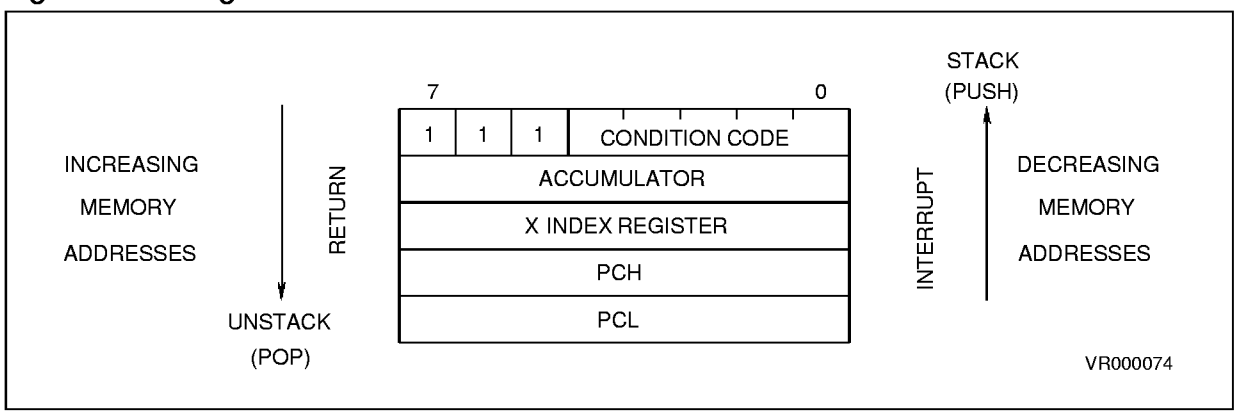
Interrupt mask (I) When the I bit is set to 1, all interrupts except the TRAP software interrupt are disabled. Clearing this bit enables interrupts to be passed to the processor core. Interrupts requested while I is set are latched and can be processed when I is cleared (only one interrupt request per interrupt enable flag can be latched).

Negative (N) When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is negative (i.e. the most significant bit is a logic 1).

Zero (Z) When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

Carry/Borrow (C) When set, C indicates that a carry or borrow out of the ALU occured during the last arithmetic operation. This bit is also affected during execution of bit test, branch, shift, rotate and store instructions.

Figure 3. Stacking Order



3 CLOCKS, RESET, INTERRUPTS & POWER SAVING MODES

3.1 CLOCK SYSTEM

3.1.1 General Description

The MCU accepts either a Crystal or Ceramic resonator, or an external clock signal to drive the internal oscillator. The internal clock (CPU CLK running at f_{CPU}) is derived from the external oscillator frequency (f_{OSC}). The external Oscillator clock is first divided by 2, and an additional division factor of 2, 4, 8, or 16 can be applied, in Slow Mode, to reduce the frequency of the CPU clock; this clock signal is also routed to the on-chip peripherals. The CPU clock signal consists of a square wave with a duty cycle of 50%. On Reset, Slow Mode with a division factor of 4 is selected.

3.1.2 Crystal Resonator

The internal oscillator is designed to operate with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{osc}. The circuit shown in Figure 6 is recommended when using a crystal, and Table 2 lists the recommended capacitance and feedback resistance values. The crystal and associated components should be mounted as close as possible to the input pins in order to minimize output distortion and start-up stabilisation time.

Use of an external CMOS oscillator is recommended when crystals outside the specified frequency ranges are to be used.

Figure 4. External Clock Source Connections

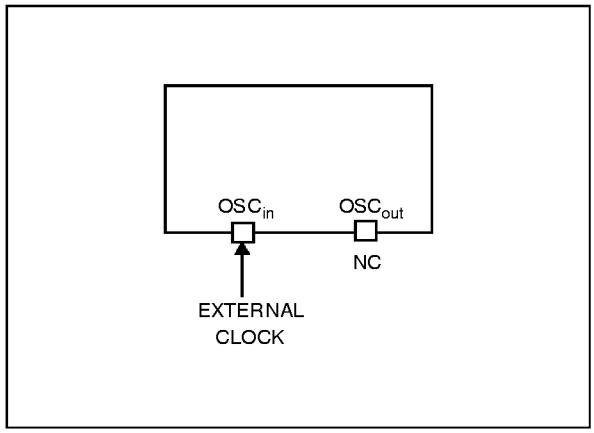


Figure 5. Clock Prescaler Block Diagram.

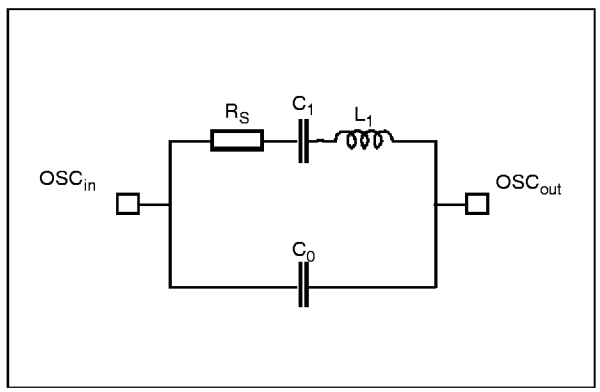


Figure 6. Crystal/Ceramic Resonator

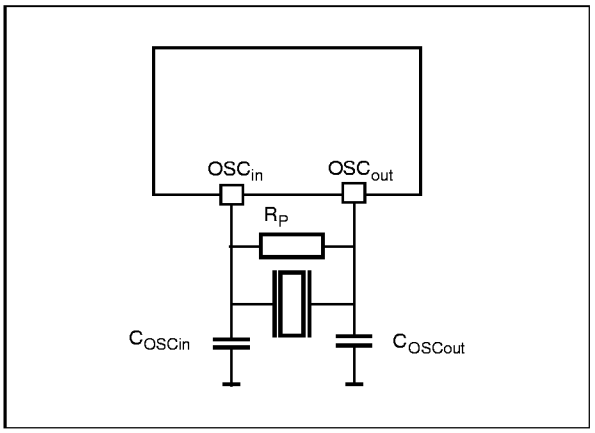
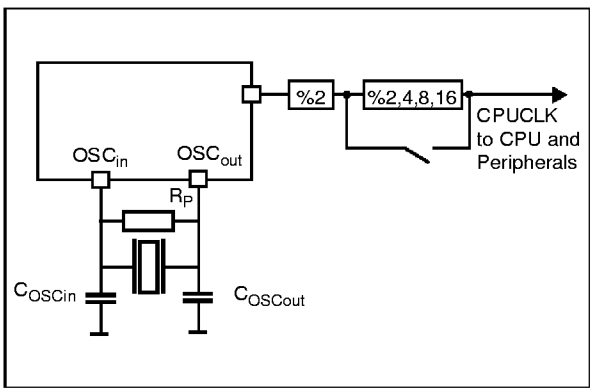


Figure 7. Equivalent Crystal Circuit



CLOCK SYSTEM (Cont'd)

3.1.3 Ceramic Resonator

A ceramic resonator may be used as an alternative to a crystal in low-cost applications. The circuit shown in Figure 6 is recommended when using a ceramic resonator. Table 3 lists the recommended feedback capacitance and resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

Table 2. Recommended Values for Crystal Resonator

	2MHz	4MHz	8MHz	Unit
R_{SMAX}	400	75	60	Ω
C_0	5	7	10	pF
C_1	8	12	15	nF
C_{OSCin}	15-40	15-30	15-25	pF
C_{OSCout}	15-30	15-25	15-20	pF
R_P	10	10	10	MΩ
Q	30	40	60	10^3

3.1.4 External Clock

An external clock may be applied to the OSCin input with the OSCout pin not connected, as shown on Figure 4. The t_{OXOV} and t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used instead of t_{OXOV} or t_{ILCH}.

See Section 6.5 CONTROL TIMING.

Table 3. Recommended Values for Ceramic Resonator

	2-8MHz	Unit
R_{SMAX}	10	Ω
C_0	40	pF
C_1	4.3	nF
C_{OSCin}	30	pF
C_{OSCout}	30	pF
R_P	1-10	MΩ
Q	1250	

3.2 MISCELLANEOUS REGISTER

MISCELLANEOUS REGISTER (MISCR)

Address: 003Fh — Read/Write

Reset Value: 0010 1010 (2Ah)

7							0
RXLAT	RXITE	1	TXEN	HVSEL	VSYNC	INT	WDGF

b7 = **RXLAT**: *Falling edge detector latch*

This bit is set when a falling edge occurs on the RX pin on Port C. It may be cleared by S/W. This bit can be used to monitor I^2C activity or implement RS232 RX S/W emulation.

b6 = **RXITE**: *Interrupt enable control bit*

Read/Write. If this bit is set, then an interrupt is generated when RXLAT is set. No other interrupt is generated.

b5 = **UNUSED**

Read as "1" when accessed.

b4 = **TXEN**

This bit (read/write) enables the OCMP1 Output to be connected to the TX pin. This function is enabled when the bit is set.

b3 = **HVSEL:** *Alternate Sync Input Select*

This bit selects between the two set of Horizontal and Vertical Sync inputs.

HVSEL= 0: HSYNCI2 (PC1) and VSYNCI2 (PD4) pins are selected as HSYNCI and VSYNCI inputs respectively.
HVSEL= 1: HSYNCI1 and VSYNCI1 pins are selected as HSYNCI and VSYNCI inputs respectively.

b2 = **VSYNC**: *Internal Vsync*

This bit (Read-Only) shows the state of the VSync input to the Sync Processor.

b1 = **INT**: *Interrupt Request*

This bit sets the interrupt configuration for the PORT B wake-up Interrupt Request:

INT = 0: selects the falling edge option only,
INT = 1: selects the falling edge or low-level option.

WARNING. *This bit can only be written ONCE after reset. Writing to INT is disabled after the first write to the Miscellaneous Register. Bit manipulation instructions should be used with extreme caution when writing to this register.*

b0 = **WDOGF**: *Watchdog flag*

Set by WDOG reset, cleared by S/W(a write of zero) or POR. This flag is useful to dinstinguish Power On Reset and Watchdog Reset.

3.3 RESETS

3.3.1 Introduction

There are three sources of Reset:

- External Reset (Reset pin)

- Power-On Reset (Internal source)

- Watchdog (Internal Source)

The starting address of the Reset Service Routine is located at address vector 7FFEh-7FFFh.

3.3.2 External Reset

The RESET pin is both an input and an open-drain output with integrated pull up resistor. When the Watchdog Reset is active, the Reset pin is driven low to reset the application.

3.3.3 Power-On Reset

Following power-up, or when exiting the HALT Mode, a delay period is initiated to allow for Reset State Recovery or oscillator stabilisation. This delay is 4096 CPU clock cycles. At the end of the Power-On Reset cycle, the MCU may be held in the Reset condition by an External Reset signal. The RESET pin may thus be used to ensure V_{DD} has risen to a point where the MCU can operate correctly before the User program is run.

During Power-on, the $\overline{\text{RESET}}$ pin is pulled low, thus permitting the MCU to reset other devices.

Power-On Reset is used exclusively for power-up and should not be used in order to attempt to detect any drop in the power supply voltage.

Table 4. Sections affected by Reset, WAIT and HALT.

Section	RESET	POR	WAIT	HALT
Timer Prescaler reset to zero	X	X		
Timer Counter set to FFFCh	X	X		
All Timer enable bit set to 0 (disable)	X	X		
Data Direction Registers set to 0 (as Inputs)	X	X		
Set Stack Pointer to 01FFh	X	X		
Force Internal Address Bus to restart vector 7FFEh,7FFFh	X	X		
Set Interrupt Mask Bit (I-Bit, CCR) to 1 (Interrupt Disable)	X	X		
Set Interrupt Mask Bit (I-Bit, CCR) to 0 (Interrupt Enable)			X	X
Reset HALT latch	X	X		
Reset INT latch	X	X		
Reset WAIT latch	X	X		
Disable Oscillator (for 4096 cycles)		X		X
Set Timer Clock to 0		X		X
Watchdog counter reset	X	X		X
Watchdog register reset	X	X		X
EEPROM control bits reset	X	X		
PWM/BRM registers reset	X	X		
EWPCC DAC register reset	X	X		
SYNC registers reset	X	X		
Port data registers				

RESETS (Cont'd)

Figure 8. Reset Timing

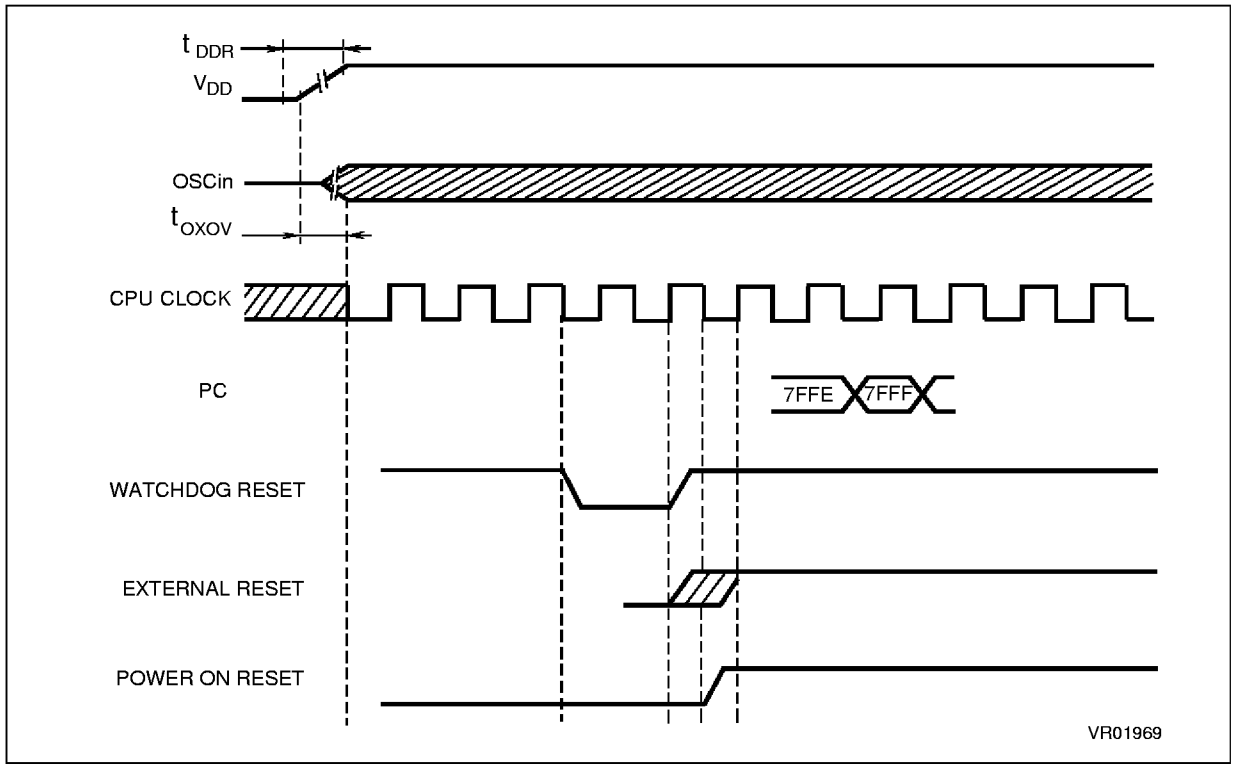
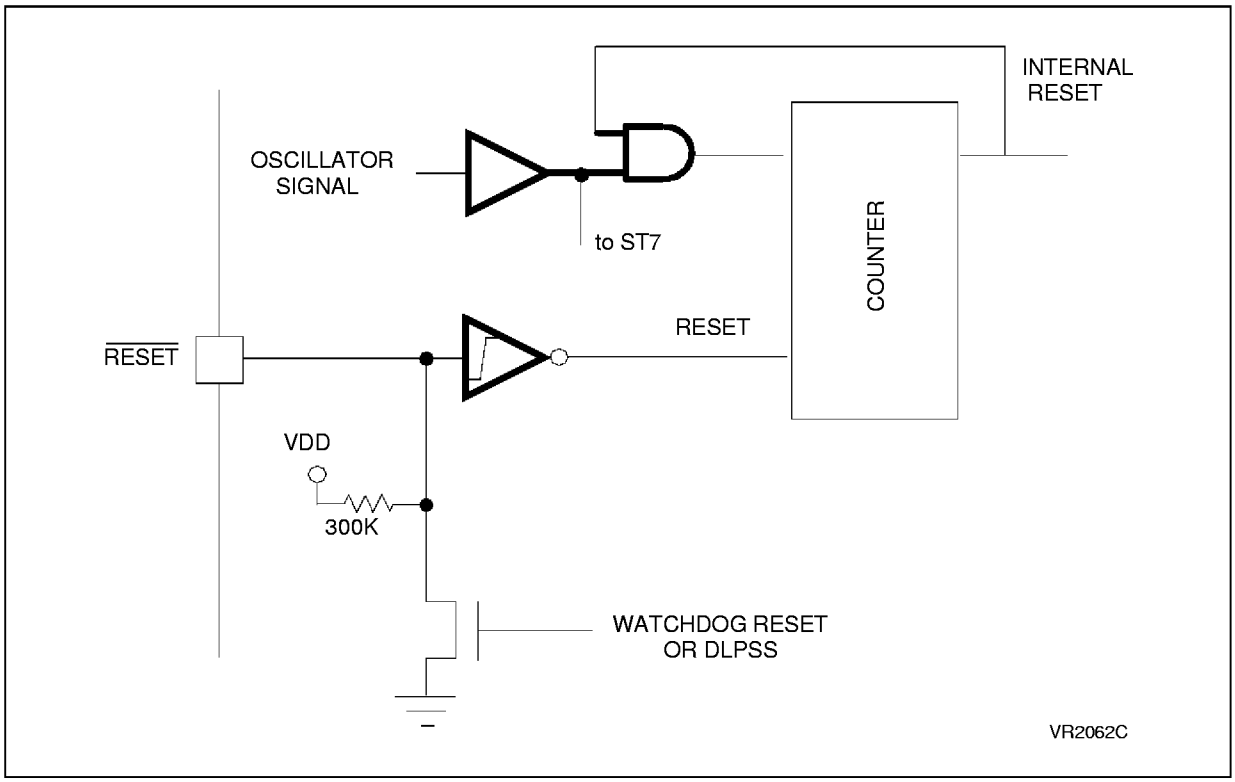


Figure 9. Reset Block Diagram



3.4 WATCHDOG TIMER SYSTEM (WDG)

3.4.1 Introduction

The Watchdog timer is used to detect the occurence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The Watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the counter's contents before it is decremented to zero.

3.4.2 Functional Description

The counter is decremented every 49,152 machine cycles, and the length of the timeout period can be programmed by the user in 64 increments, ranging from 12 msec to 784 msec at 8 MHz oscillator frequency, depending on the value loaded in bits 0-5 of the Watchdog register. The application program must be written so that the Watchdog register is reloaded at regular intervals during normal operation.

The Watchdog is not activated automatically on Reset, and must be activated by the user program if required. Once activated it cannot be disabled, except by a Reset.

Table 5. Watchdog Timing (f_{OSC} = 8 MHz)

WDG Register initial value	WDG timeout period (ms)
FF	784
C0	12

During the Watchdog initiated Reset cycle, the device Reset pin acts as an output that is pulsed low for 3 machine cycles (6 oscillator cycles). In its high state, an internal pull-up resistor of about 300KΩ is connected to the Reset pin. This resistor can be pulled low by external circuitry to reset the device.

The Watchdog delay time is defined by bits 5-0 of the Watchdog register; bit 6 must always be set in order to avoid generating an immediate reset. Conversely, this can be used to generate a software reset (bit 7 = 1, bit 6 = 0).

Once bit 7 is set, it cannot be cleared by software: i.e. the Watchdog cannot be disabled by software without generating a Reset. The Watchdog timer must be reloaded before bit 6 is decremented to "0" to avoid a Reset. Following a Reset, the Watchdog register will contain 7Fh (bits 0-6 = 1, bit 7 = 0).

If the Watchdog is activated, the HALT instruction will generate a Reset.

If the circuit is not used as a Watchdog (i.e. bit 7 is never set), bits 6 to 0 may be used as a simple 7-bit timer, for instance as a real time clock. Since no interrupt will be generated under these conditions, the Watchdog register must be monitored by software.

3.4.3 Watchdog Register

Register Address: 0024h — Read/Write

Reset Value: 0111 1111 (7Fh)

7							0
WDGA	T6	T5	T4	T3	T2	T1	T0

b7 = **WDGA:** Activation bit (is active if set)

b6-0 = **T6-T0**: 7 bit timer (Msb to Lsb)

3.5 INTERRUPTS

3.5.1 Introduction

The MCU may be interrupted by six maskable hardware interrupts (generated by PORT B, RX, DDC and TIMER) and a non-maskable software interrupt (TRAP). Reset also generates a non-maskable interrupt. These interrupt sources, together with their vector addresses and priorities are illustrated in Table 6 below. The Interrupt processing flowchart is shown in Figure 10.

Maskable interrupts must be enabled in order to be serviced, however disabled interrupts can be latched and processed when next enabled. When an interrupt needs servicing, the PC, as well as the X, A and CC registers are saved on the stack, and the Interrupt Mask (I bit of the Condition Code Register) is set to prevent further interrupts. The Y register is not automatically saved.

The PC is then loaded with the interrupt vector of the interrupt to be serviced and the interrupt service routine is executed. The interrupt service routine should end with an IRET instruction, which causes the contents of the registers to be recovered from the stack and normal processing to be resumed. The I bit is then cleared if, and only if, the corresponding bit stored in the stack is zero.

Though several interrupts may be simultaneously pending, a priority order is defined and they are dealt with in this order. The $\overline{\text{RESET}}$ pin has the highest priority. If the I bit is set, TRAP is the only enabled interrupt (Reset is, of course always enabled). All interrupts allow the processor to leave the Wait power saving mode. Only the external interrupt causes the processor to leave Halt mode.

3.5.2 Software Interrupt

The software interrupt is generated by the executable instruction TRAP. The interrupt is recognized when the TRAP instruction is executed, regardless of the state of the I bit, and the corresponding service routine will be executed.

3.5.3 Port B Interrupt

The PORTB Interrupt can be generated by a falling edge or by a low level on any pin of Port B, if it is defined as an interrupt source. When an enabled interrupt occurs, normal processing is suspended at the end of the current instruction execution and the corresponding interrupt service routine is executed.

If the interrupt is disabled (I high), the triggering edge of the wake-up interrupt source is internally latched and the interrupt remains pending to be processed as soon as the interrupt is next enabled. This internal latch is cleared in the first part of the service routine. Therefore, only one external interrupt can be latched and serviced at a time.

3.5.4 RX interrupt

The RX pin can generate an interrupt on a falling edge, if enabled via the RXITE bit in the Miscellaneous register and the I bit in the CCR. The RX service routine must reset the cause of this interrupt by clearing the RXLAT or RXITE bits in the Miscellaneous register. This function allows software implementation of a basic asynchronous serial communications interface with minimum processor overhead, by detecting a Start condition automatically.

3.5.5 Timer Interrupt

Five interrupt flags in the Timer Status Register can generate a timer interrupt if both the I bit of the CCR is reset and if the corresponding enable bit in the Timer Control Register is set, otherwise the interrupt is latched and remains pending.

The timer service routine must determine the source of the interrupt by examining the flags and status bits. The general sequence for clearing an interrupt is an access to the status register while the flag is set, followed by reading or writing an associated register.

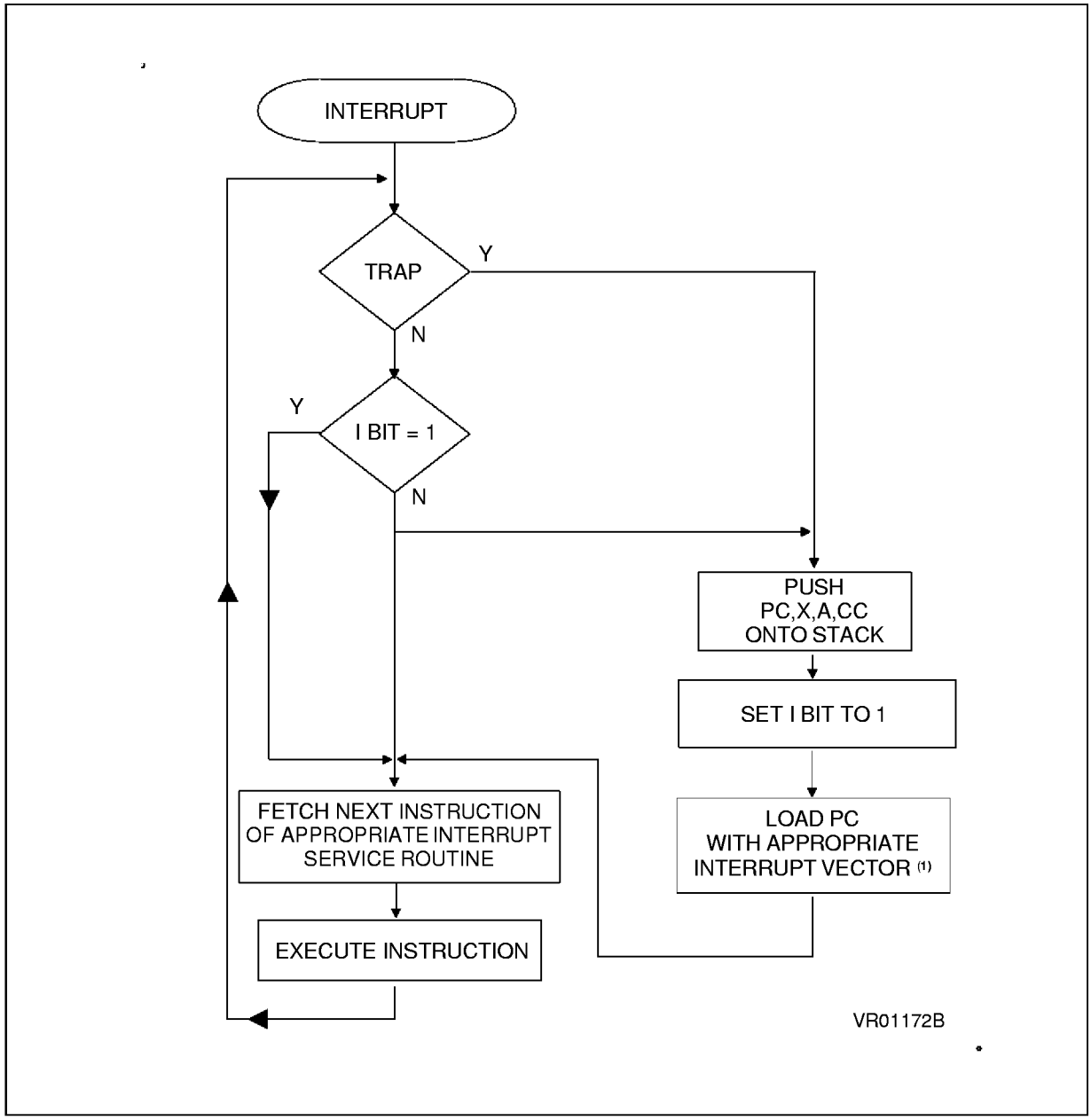
Note that the clearing sequence resets the internal latch. A pending interrupt will therefore be lost if the clearing sequence is executed.

Table 6. Interrupt Mapping and Priorities

Vector Address	Interrupt Source	Masked by	Priority
7FFE-7FFF h	RESET or POWER-ON (POR)	none	highest
7FFC-7FFD h	SOFTWARE interrupt (TRAP)	none	
7FFA-7FFB h	PORT B Wake up	I-Bit	
7FF8-7FF9 h	RX falling edge interrupt	I-Bit	
7FF6-7FF7 h	ICAP Input capture	I-Bit	
7FF4-7FF5 h	OCMP Output compare	I-Bit	
7FF2-7FF3 h	TOF Timer overflow	I-Bit	
7FF0-7FF1 h	DDC/DMA	I-Bit	Lowest

INTERRUPTS (Cont'd)

Figure 10. Interrupt Processing Flowchart



Note 1. See Table 6

3.6 POWER SAVING MODES

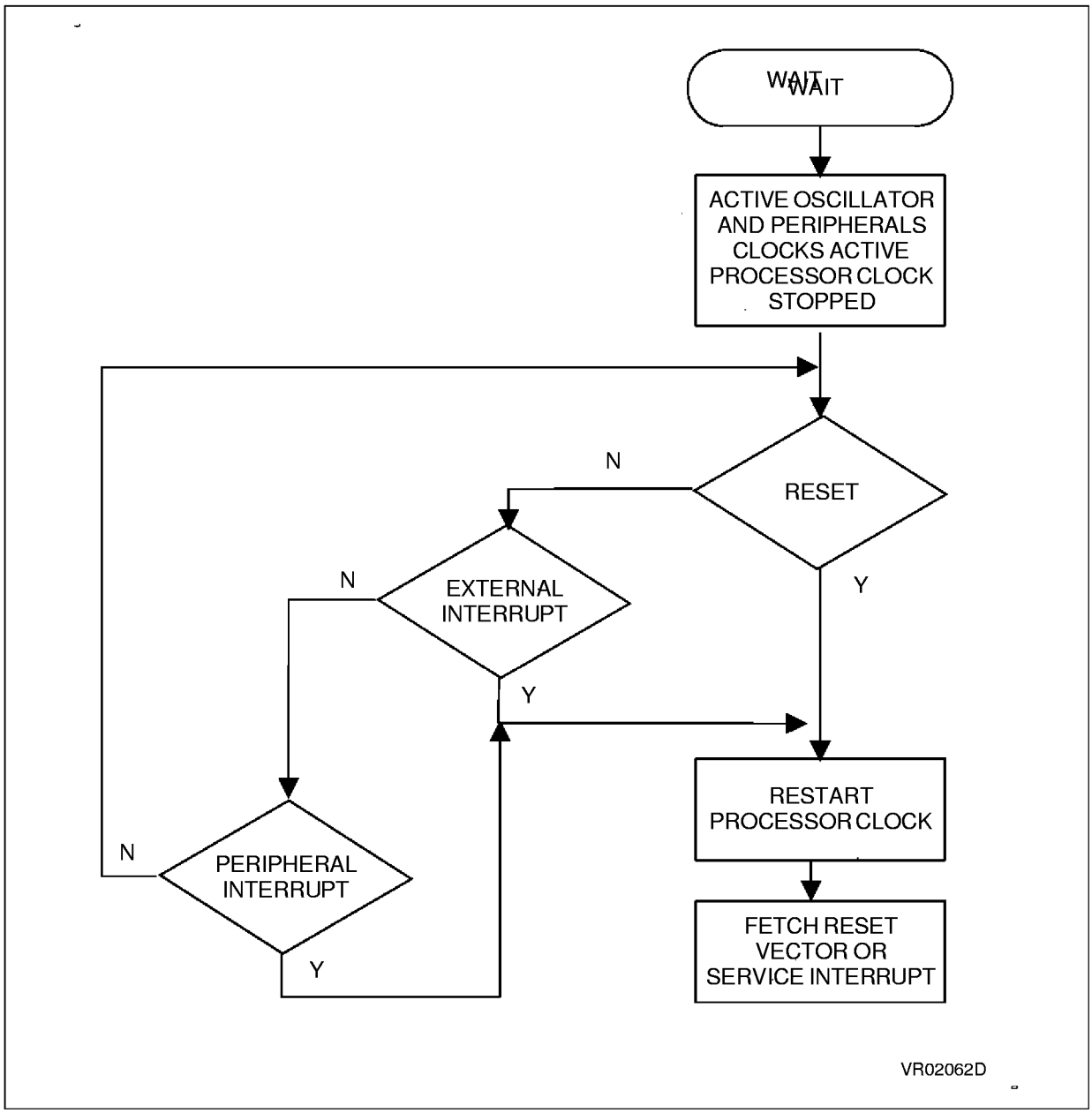
3.6.1 Introduction

Two special power saving operating modes are available: WAIT Mode and HALT Mode. These are described in the following paragraphs. Table 4 lists the various sections affected by the low power modes.

3.6.2 Wait Mode

The WAIT instruction places the MCU in a low power consumption mode by stopping the CPU. All peripherals remain active and the I bit (CC Register) is cleared, so as to enable all interrupts. All other registers and memory remain unchanged. The MCU will remain in WAIT mode until an Interrupt or Reset occurs, whereupon the Program Counter branches to the starting address of the Interrupt or Reset Service Routine. This is illustrated in Figure 11 below.

Figure 11. Wait Mode Flow Chart



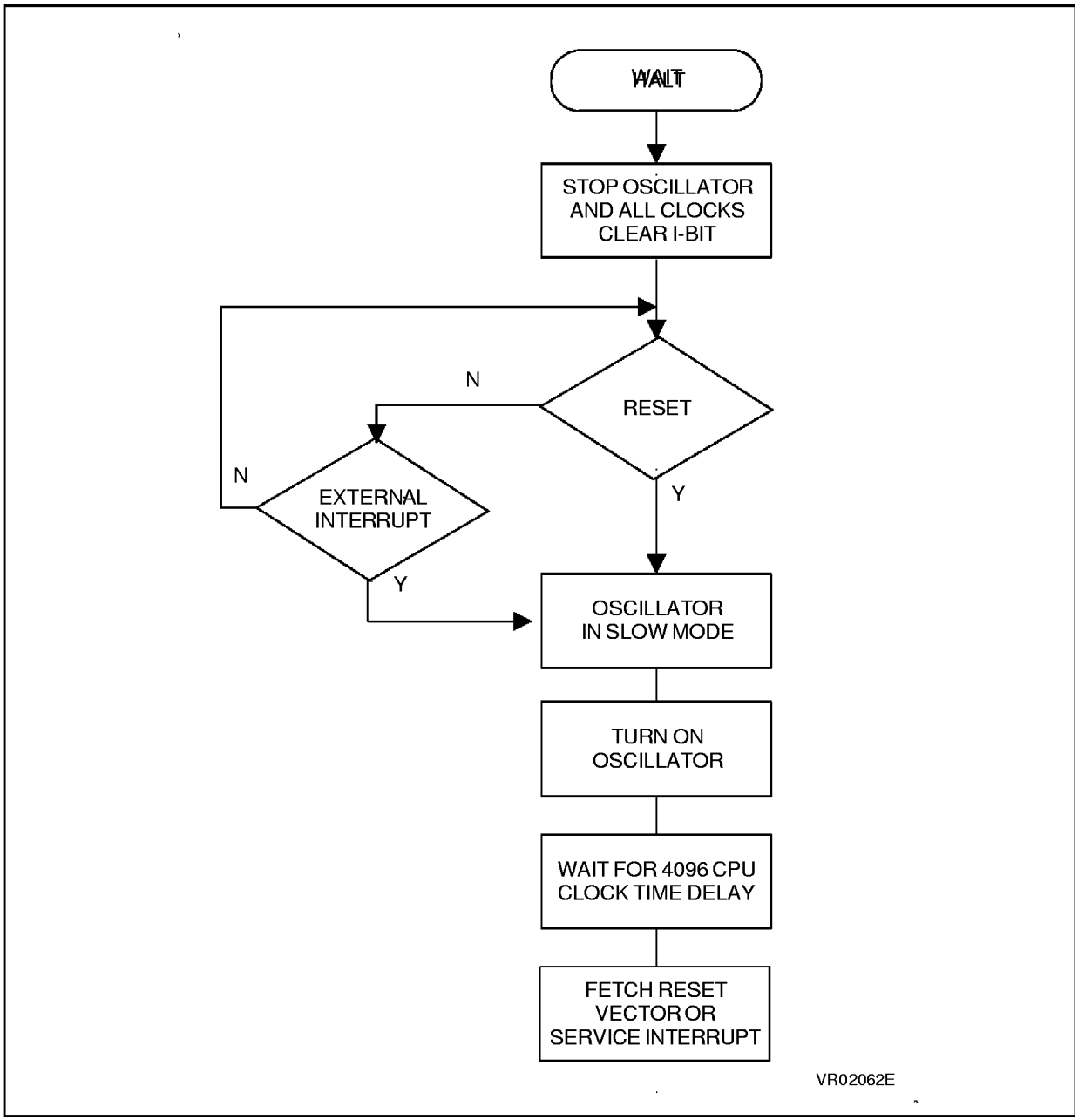
POWER SAVING MODES (Cont'd)

3.6.3 Halt Mode

The HALT instruction places the MCU in its lowest power consumption mode. In HALT mode the internal oscillator is turned off, causing all internal processing to be halted. During HALT mode, the I bit in the CC Register is cleared so as to enable External Interrupts.

All other registers and memory remain unaltered and all Input/Output lines remain unchanged. This state will endure until an External Interrupt or Reset is generated, whereupon the internal oscillator is turned on. A delay of 4096 CPU clock cycles is initiated prior to restarting, in order to allow the oscillator to stabilize. The External Interrupt or Reset causes the Program Counter to be set to the address of the corresponding Interrupt or Reset Service Routines.

Figure 12. Halt Mode Flow Chart



4 ON-CHIP PERIPHERALS

4.1 EEPROM (EEP)

4.1.1 Introduction

The on-chip EEPROM provides non-volatile storage for user data. It is read as a normal Read-Only memory location (user programs cannot however be run from EEPROM).

Programming and erasure are controlloed by means of the EEPROM control registers, and 8 data latches allow simultaneous erase or write operations to be carried out on up to 8 EEPROM memory bytes simultaneously. However, all addressed memory bytes must be on the same row of the EEPROM memory array, that is up to eight bytes with the address bits A7, A6, A5, A4 and A3 constant, and with A2, A1 and A0 selecting the address(es) to be written within the row.

The EEPROM cell includes an internal charge pump to avoid the need of an external high voltage supply for erasure and programming cycles.

The programming pulse duration is automatically controlled to achieve the shortest possible programming time.

4.1.2 Functional Description

As shown in See ". EEPROM Block Diagram" on page 26., the EEPROM is organised as an 8 column by 32 row array. The row is selected by the A7, A6, A5, A4, A3 bits. Each column is associated with an 8-bit data register.

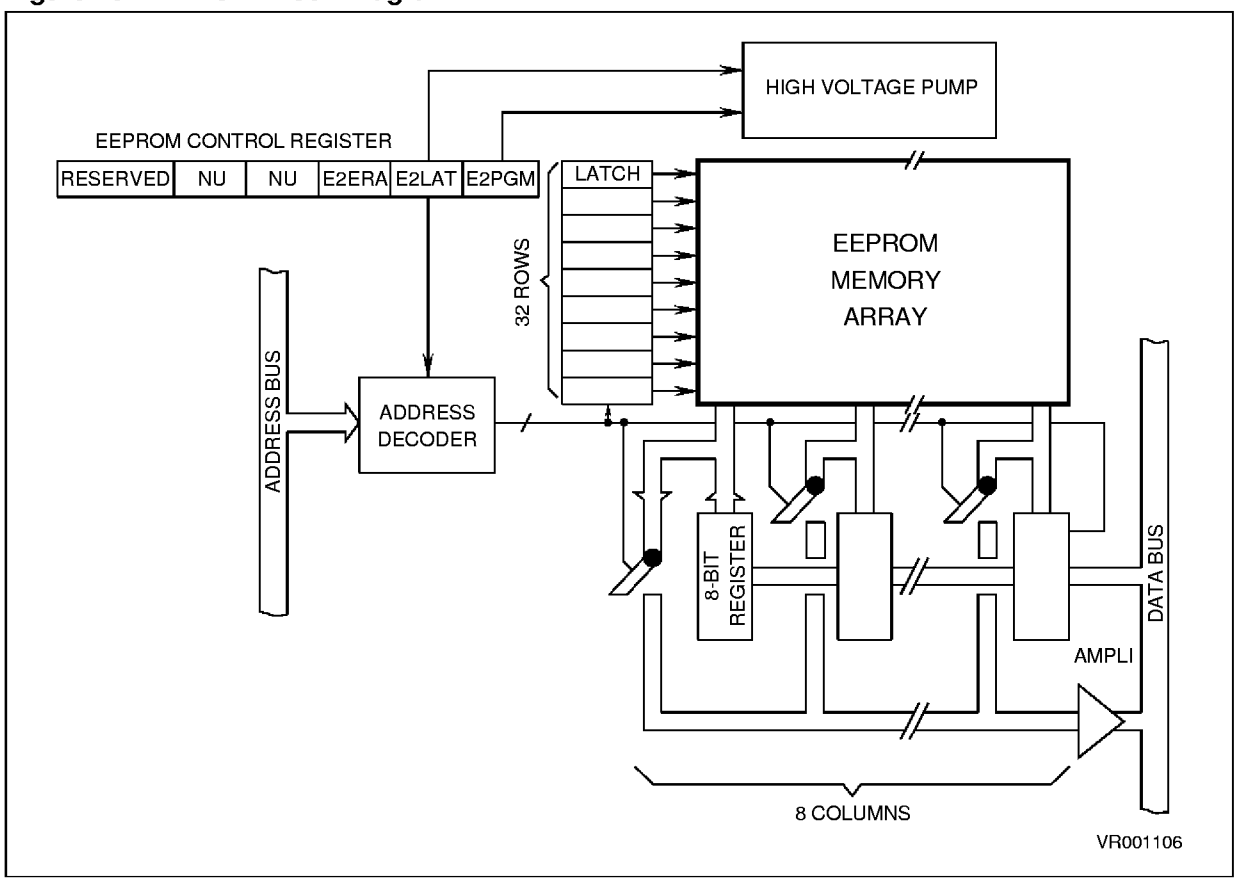
4.1.2.1 Read Operation

The EEPROM may be read as a normal ROM location when the E2LAT bit in the Control Register is cleared to "0". The E2PGM and E2ERA bits are also forced to "0" when E2LAT is at "0".

4.1.2.2 Write/Erase Operation

When E2LAT is set to "1", a write to an EEPROM location latches the data written in the 8-bit register corresponding to the decoded column and sets an internal flag for the decoded row. As there are 8 columns in each row, up to 8 locations (having the same A7, A6, A5, A4, A3 address bits) can be simultaneously written or erased.

Figure 13. EEPROM Block Diagram



EEPROM (Cont'd)

To **erase** bytes, the E2LAT and E2ERA bits are set, and the EEPROM addresses to be erased are written to (the data value is not significant). The E2PGM bit is set to turn the charge pump on.

To **write** bytes, the E2LAT bit is set, and data is written to the appropriate EEPROM address(es). The E2PGM bit is set to turn the charge pump on.

After a time T_{PROG}, the programming operation is automatically terminated. E2LAT, E2PGM and E2ERA bits are reset.

WARNING: *A minimum delay of T_{DIS} must be respected after a programming operation (the falling edge of E2LAT) before the next read or write of the EEPROM. This time is required to discharge the high voltage in the array.*

4.1.3 Application Notes

– Each EEPROM bank is controlled by an independent EEPROM Control Register. Please refer to the Memory Map for the four EEPROM memory block locations.

– It is mandatory to erase bytes before writing them.

– When E2LAT is high, access to the EEPROM array is not possible.

– It is possible to stop a programming sequence at any time by resetting the E2LAT bit. In this case, the programmed data value is not guaranteed. A minimum delay of T_{DIS} must be respected before the next read or program cycle.

4.1.4 Register Descriptions

DDC-EEP CONTROL REGISTER(CR0)

GP1-EEP CONTROL REGISTER(CR1)

GP2-EEP CONTROL REGISTER(CR2)

EWPCC EEP CONTROL REGISTER(CR3)

Read/Write

EEPROM Bank	EEPROM Address	Register Name	Register Address
DDC	0280-02FF	CR0	000Eh
GP1	0300-03FF	CR1	000Fh
GP2	0400-04FF	CR2	0010h
EWPCC	0500-05FF	CR3	0011h

Reset Value: 0000 0000 (00h)

7							0
Res.	Res.	Res.			E2ERA	E2LAT	E2PGM

These registers contain the bits required to read, erase and program the EEPROM memory banks. They are defined as follow:

b7-5 = **Reserved**, must be set to "0"

b4,3 = **Unused**, read as "0"

b2 = **E2ERA:** *EEPROM Erase*

E2ERA must be set for an erase operation. It must be set after or at the same time as E2LAT. It cannot be changed once an EEPROM address is selected. It is held low when E2LAT is low. It is therefore automatically reset when E2LAT is reset.

b1 = **E2LAT:** *EEPROM Latch Enable*

When E2LAT is reset, data can be read from the EEPROM. When it is set and E2PGM reset, a write into the EEPROM array causes the data to be latched, according to the address into one of 8 data registers. An additional internal flag is latched to select the row. The selected columns and row determine the locations involved in the next erase or programming operation. E2LAT is automatically cleared at the end of each programming operation. It can be reset by software, but in this case the programming result is not guaranteed. E2ERA and E2PGM are forced low when E2LAT is low

b0 = **E2PGM:** *EEPROM Program Mode*

This bit allows the internal charge pump to be switched on or off. When set, the charge pump generator is on and the high voltage is applied to the EEPROM array. When low, the charge pump generator is off. E2PGM can only be reset by resetting E2LAT.

EEPROM (Cont'd)

Figure 14. Basic EEPROM Programming Flow-chart

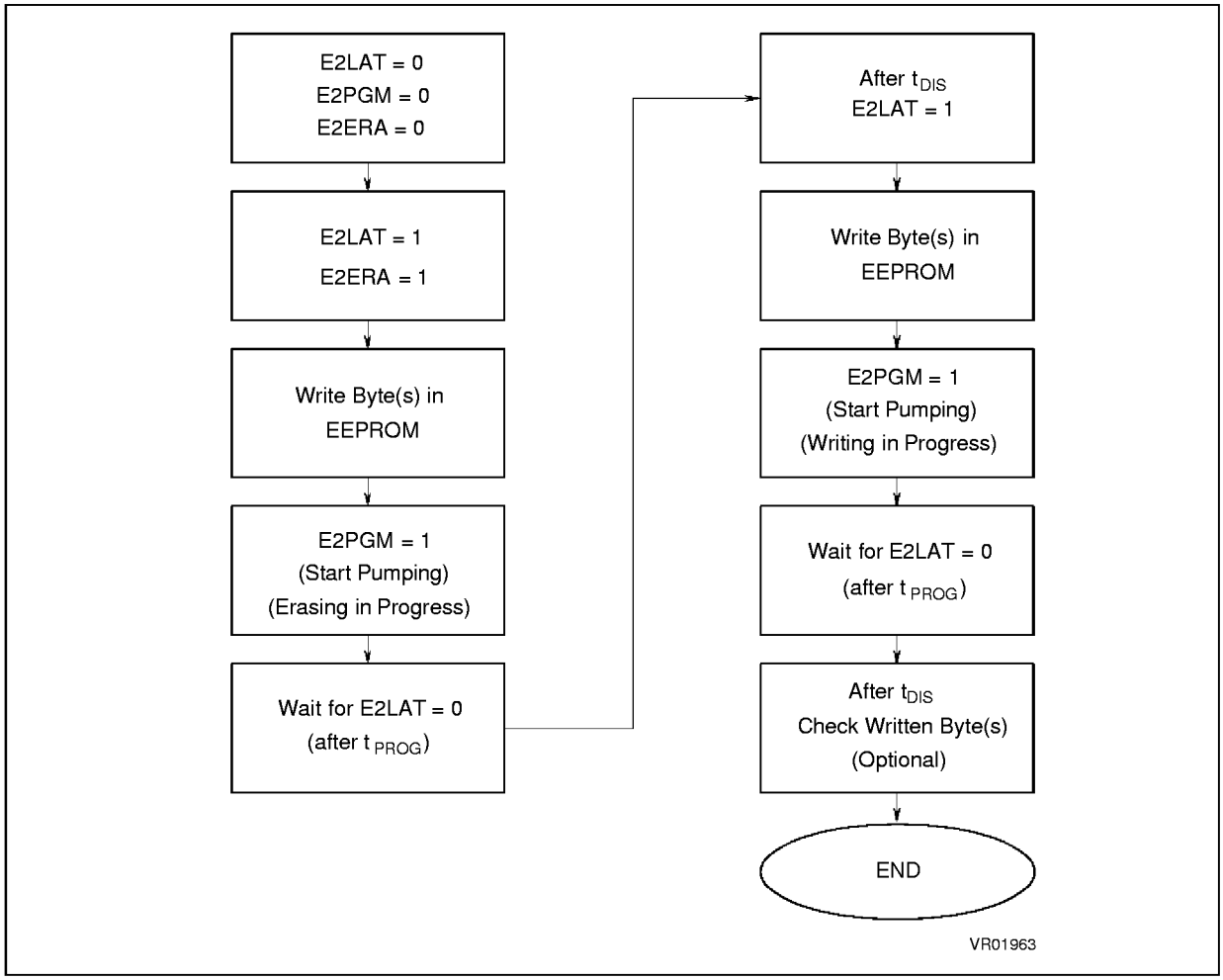
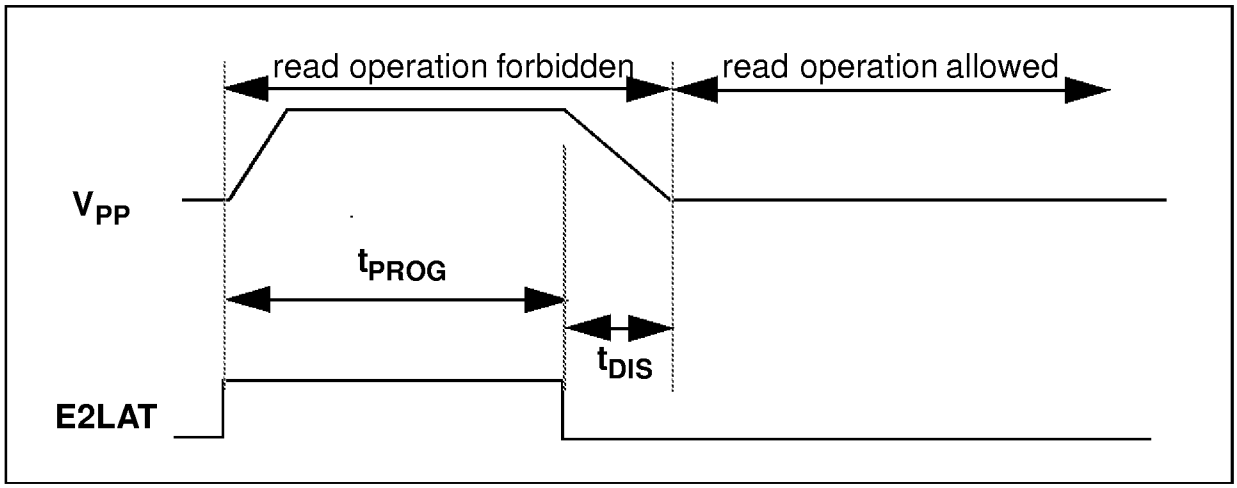


Figure 15. EEPROM Programming Timing Diagram



4.2 I/O PORTS

4.2.1 Introduction

The I/O ports allow data transfer by means of digital inputs and outputs and, for specific pins, input of analog signals or Input/Output of dedicated signals relating to the the on-chip peripherals (e.g. DDC, EWPCC, Timer, etc.).

4.2.2 Functional Description

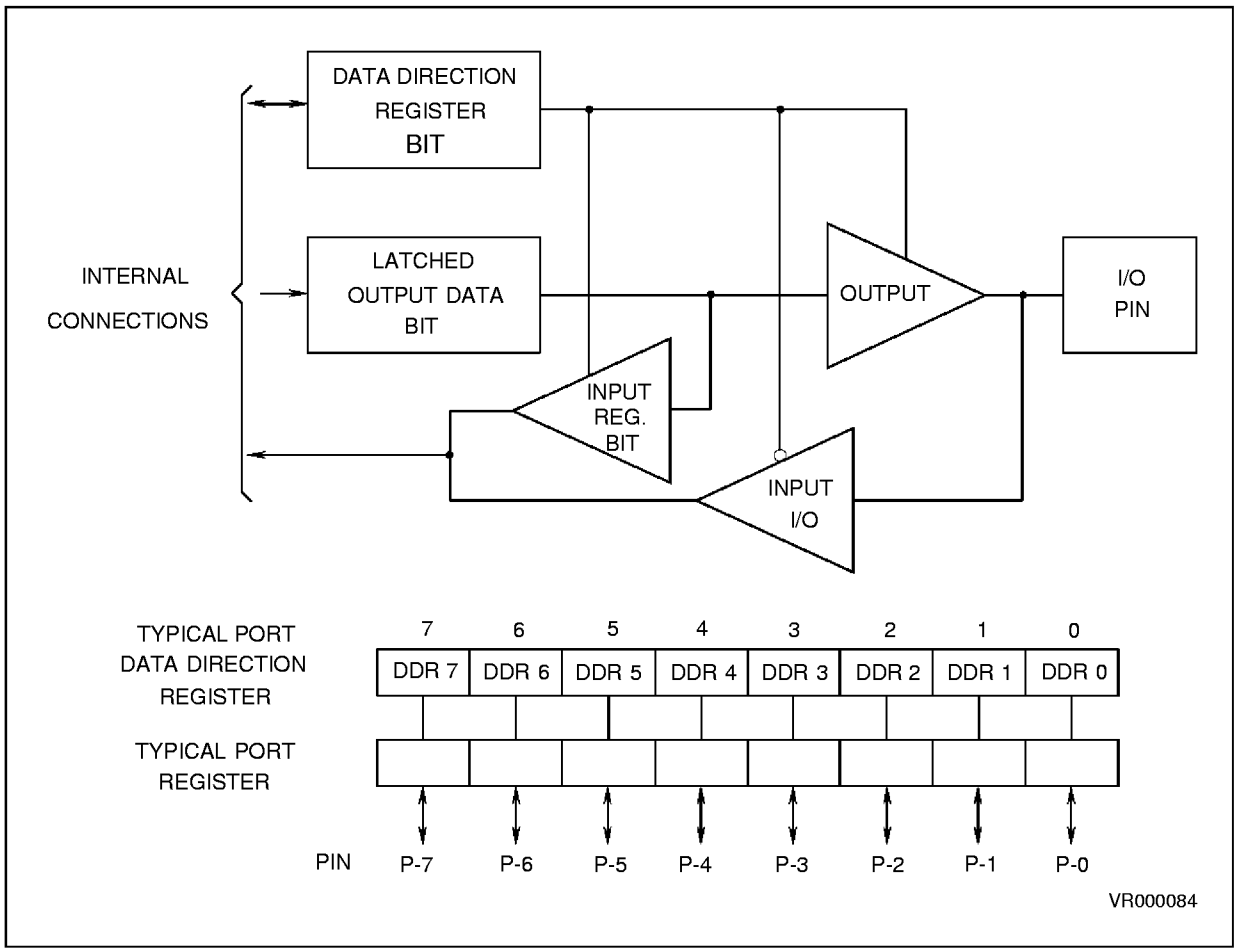
Each pin of the I/O Ports can be individually configured under software control as either input or output. Ports A and B are 8-bit ports, Port C is a 6-bit port and Port D is a 5-bit port.

Each bit of a Data Direction Register (DDR) relates to the corresponding I/O pin on the associated port. A bit must be set to configure its associated pin as an output, and must be cleared to configure the pin as an input. The Data Direction Registers may be read and written.

The typical I/O circuit is illustrated schematically in Figure 16. A write to an I/O port updates the port data register even if it is configured as an input. A read of an I/O port returns either the data latched in the port data register (pins configured as output) or the value at the I/O pin (pins configured as input).

At power-on or following an external reset, all DDR registers are cleared, which configures Ports B, C and D as inputs with pull-ups and Port A as inputs without pull-ups. The port data registers are not initialized. Thus, the I/O port should be written to before setting the DDR bit to avoid undefined output levels.

Figure 16. Typical I/O Circuit



I/O PORTS (Cont'd)

4.2.2.1 Port A

Each Port A bit can be defined as an Input line (no pull-up) or as an open-drain Output.

4.2.2.2 Port B

Any bit of Port B bit may be used as an Analog input to the Analog to Digital converter, by selecting each individual bit independently in the Port B Configuration Register.

When the Analog input function is selected, the pull-up on the respective pin of Port B is disconnected and both the Data and Direction (DR and DDR) registers of the respective pin are reset. Any further accesses to this particular DDR bit is blocked until the pin status is reset to normal I/O.

Port B bits can also be configured on a bit basis as a wake-up interrupt input with an internal pull-up resistor. This mode is enabled by setting the corresponding Port B bit as a digital input (its bit in DDR reset and its Analog function disabled) and the corresponding bit in the Port B Data Register must be set.

When this bit is subsequently forced low, an interrupt will be generated according to the status of the INT bit in the Miscellaneous Register.

Port B, bit 0 is only available for output if the East-West Pin-Cushion Correction circuit (EWPCC) is not used. If the EWPCC function is selected, Port B bit 0 MUST be set as input to enable the V_{FBACK} timing input.

All unused I/O lines should be tied to an appropriate logic level (either V_{DD} or V_{SS}).

4.2.2.3 Port C

The available Port C pins may be used as general purpose I/O, as the alternate HSYNCI2 Sync Input, HFBACK input or as I/O pins for the on-chip DDC and Timer Output Compare. When used as digital Input, pull-up resistors on PC 4,5 can be switched on by setting the PUPC bits of the Programmable Input/Output Configuration Register (PCR).

Port C, bit 0 is switched from the normal I/O functionality to the output of the Timer Output Compare signal by resetting the OCOP bit of the PCR. This pin is also the HFBACK input.

Port C, bit 1 is also the alternate HSYNCI2 input of the Sync Processor block.

Port C bits 2,3 are always open-drain outputs or inputs without pull-up resistors.

The default condition of open drain output allows software emulation of communication using the I^2C bus protocol on PC4,5.

4.2.2.4 Port D

The Port D I/O pins are normally used for input and output of video synchronization signals to the Sync Processor, but are set as I/O inputs with pull-ups on reset. The I/O mode can be set individually for each port bit to Input with pull-up or push-pull output through the Port D DDR.

The support the Sync Processor, the configuration requires that the SYNOP bit of the PCR be reset; this enables Port D bits 0, 1 and 2 as sync outputs.

Port D, bit 4 is switched to the alternate VSYNCI Input (VSYNCI2) by resetting the HVSEL bit of the Miscellaneous Register.

***Note** : Since these inputs are switched from normal I/O functionality, the video synchronization signals may also be monitored directly through the Port D Data Register for such tasks as checking for the presence of video signals or checking the polarity of Horizontal and Vertical synchronization signals (when the Sync Inputs are switched directly to the outputs using the Sync Processor multiplexers).*

Table 7. Port A Possible I/O Configuration.

PORT A	I / O		Alternate Function	
	Input	Output	Signal	Condition
PA0	without pull-up	open drain	-	-
PA1	without pull-up	open drain	-	-
PA2	without pull-up	open drain	-	-
PA3	without pull-up	open drain	-	-
PA4	without pull-up	open drain	-	-
PA5	without pull-up	open drain	-	-
PA6	without pull-up	open drain	-	-
PA7	without pull-up	open drain	BLK	BLKEN = 1

I/O PORTS (Cont'd)

Table 8. Port B Possible I/O Configurations.

PORT B	I / O		Alternate Function	
	Input	Output	signal	Condition
PB0	with pull-up	push-pull	analog input (ADC) (without pull-up)	AD0=1 (PBICFGR)
			wake up interrupt (input with pull-up)	PBDDR0=0 AD0=0 (PBICFGR) PBDR0=1
			VFBACK (input with schmitt trigger)	-
PB1	with pull-up	push-pull	analog input (ADC) (without pull-up)	AD1=1 (PBICFGR)
			wake up interrupt (input with pull-up)	PBDDR1=0 AD1=0 (PBICFGR) PBDR1=1
PB2	with pull-up	push-pull	analog input (ADC) (without pull-up)	AD2=1 (PBICFGR)
			wake up interrupt (input with pull-up)	PBDDR2=0 AD2=0 (PBICFGR) PBDR2=1
PB3	with pull-up	push-pull	analog input (ADC) (without pull-up)	AD3=1 (PBICFGR)
			wake up interrupt (input with pull-up)	PBDDR3=0 AD3=0 (PBICFGR) PBDR3=1
PB4	with pull-up	push-pull	analog input (ADC) (without pull-up)	AD4=1 (PBICFGR)
			wake up interrupt (input with pull-up)	PBDDR4=0 AD4=0 (PBICFGR) PBDR4=1
PB5	with pull-up	push-pull	analog input (ADC) (without pull-up)	AD5=1 (PBICFGR)
			wake up interrupt (input with pull-up)	PBDDR5=0 AD5=0 (PBICFGR) PBDR5=1
PB6	with pull-up	push-pull	analog input (ADC) (without pull-up)	AD6=1 (PBICFGR)
			wake up interrupt (input with pull-up)	PBDDR6=0 AD6=0 (PBICFGR) PBDR6=1
PB7	with pull-up	push-pull	analog input (ADC) (without pull-up)	AD7=1 (PBICFGR)
			wake up interrupt (input with pull-up)	PBDDR7=0 AD7=0 (PBICFGR) PBDR7=1

I/O PORTS (Cont'd)

Table 9. Port C Possible I/O Configurations

PORT C	I / O		Alternate Function	
	Input	Output	Signal	Condition
PC0	with pull-up	push-pull	OCMP (push-pull)	OCOP(PCR)=0
			HFBACK (input with schmitt trigger)	-
PC1	with pull-up	push-pull	HSYNCI2 (input with schmitt trigger)	-
PC2	input without pull-up	open-drain	SCL1 (input with schmitt trigger or open drain output)	DDC enable
			RX (input)	-
PC3	input without pull-up	open-drain	SDA1 (input with schmitt trigger or open drain output)	DDC enable
			TX (input)	TXEN
PC4	input with or without pull-up depending on PUPC (PCR)	open-drain	-	-
PC5	input with or without pull-up depending on PUPC (PCR)	open-drain	-	-

Table 10. Port D Possible I/O Configurations

PORT D	I / O		Alternate Function	
	Input	Output	Signal	Condition
PD0	with pull-up	push-pull	CSYNCI (input with pull-up)	-
PD1	with pull-up	push-pull	HSYNCO (push pull output)	SYNOP=0 (PCR)
PD2	with pull-up	push-pull	VSYNCO (push pull output)	SYNOP=0 (PCR)
PD3	with pull-up	push-pull	CLMPO (push pull output)	SYNOP=0 (PCR)
PD4	with pull-up	push-pull	VSYNCI2 (input with pull-up)	-

R/W	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the data latch
0	1	Data is written into the data latch and output to the I/O pin
1	0	The state of the I/O pin read.
1	1	The I/O pin is in an output mode.The data latch is read

I/O PORTS (Cont'd)

4.2.3 Register Descriptions

DATA REGISTERS

(PADR) Port A — Address: 0000 h
(PBDR) Port B — Address: 0001 h
(PCDR) Port C — Address: 0002 h
(PDDR) Port D — Address: 0003 h

Read/Write

Reset Value: Undefined

DATA DIRECTION REGISTERS

(PADDR) Port A — Address: 0004h
(PBDDR) Port B — Address: 0005h
(PCDDR) Port C — Address: 0006h
(PDDDR) Port D — Address: 0007h

Read/Write

Reset Value: 0000 0000 (00h) (as inputs)

PORT B CONFIGURATION REGISTER (PBICFGR)

Address: 003C h — Read/Write

Reset Value: 0000 0000 (00h)

7							0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

b7-0 = **AD7-AD0:** Port B Digital/Analog Input Configuration Bits. When AD#i is set (i = 7-0), the pull-up on the respective pin #i of Port B is disconnected and the pin is configured as analog input; otherwise the pull-up is connected and the pin configured as a digital input (RESET condition) with no power consumption in the A/D channel.

PROGRAMMABLE INPUT/OUTPUT CONFIGURATION REGISTER (PIOCFGR)

Address: 003D h — Read/Write

Reset Value: 1111 1000 (F8 h))

7							0
Res.	CLMOP	OCOP	SYNOP	PUPC	POC2	POC1	POC0

Bit-7= **Reserved**.

b6 = **CLMOP:** Clamping Signal Output Select. This bit selects either the PD3 I/O Pin Option or the output of the Clamping signal.
CLMOP = 0: Clamping Signal
CLMOP = 1: PD3 as Pull-up Input or Push-pull Output

b5 = **OCOP:** Timer Output Compare Select. This bit selects either the PC0 I/O Pin Option or the output of the Timer Output Compare.
OCOP = 0: Timer Output Compare
OCOP = 1: PC0 as pull-up Input or push-pull Output

b4 = **SYNOP:**SYNC Processor Function Select. This bit selects either the Sync Processor or PD0, PD1, PD2 I/O Pin Options.
SYNOP = 0: PD0 = CSYNCI, PD1 = HSYNCO and PD2 = VSYNCO
SYNOP = 1: PD0/PD1/PD2 as pull-up Inputs or push-pull Outputs

Note. HSYNCO and VSYNCO can be directly read as Port bits by configuring PD1 and PD2 as inputs.

b3 = **PUPC:** PORT C Input Configuration Bit. This bit selects the input configuration for present bits of I/O Port C (PC4:5).
PUPC = 1: Port C with Pull-up
PUPC = 0: Port C without Pull-up

b2-b0 = **POC2-POC0:** PWM/BRM Output Configuration Bits. These bits select the PWM/BRM output configuration.

Table 11. PWM Output Configurations.

PWM Group Channels		Value	
		0	1
A2 DA1.. D3-6	P0C0	push-pull	open drain
B1 DA7-11	P0C1	push-pull	open drain
B2 DA12-DA17	P0C2	push-pull	open drain

Note: In the case of incomplete ports (port C and port D),non-implemented bits are read as '0' whenever accessed

4.3 16-BIT TIMER

4.3.1 Introduction

The 16-bit programmable timer consists of a 16-bit free running counter complete with prescaler and the necessary control logic to handle two input capture and two output compare registers. The timer may be used for many purposes, amongst which period measurement of input signals and generation of output waveforms.

The two input capture functions are dedicated to the Sync Processor, and are internally connected to this source. They are thus not available for timing other external signals.

When used with an 8MHz oscillator frequency, the timer offers a resolution of 0.5 us.

4.3.2 Functional Description

Since the timer has a 16-bit architecture, each of its specific functional blocks comprises two registers. These registers contain the high order and low order byte of that function. However any access to the high order byte inhibits that specific timer capability until the low order byte is also accessed.

Note: correct software procedures should set the I bit of the Condition Code Register before accessing the high order byte to prevent an interrupt from occurring between the accesses to the high and low order bytes of any register.

4.3.3 Counter

The key element of the programmable timer is a 16-bit free running counter, preceded by a prescaler which divides the internal clock by two giving an operational frequency of 2MHz for an oscillator frequency of 8MHz.

Software can read the counter at any time without affecting its value. It can be read from two locations, the Counter Register (0018h, 0019h) and Alternate Counter Register (001Ah, 001Bh). The only difference between these two read-only registers is the way the overflow flag TOF is handled during a read sequence.

A read sequence containing only a read of the least significant byte of the free running counter (from either the Counter Register or the Alternate Counter Register) will receive the LSB of the count value at the time of the read. A read of the most significant byte (from either the Counter Register or the Alternate Counter Register) simultaneously returns the MSB of the count value and causes the LSB to be transferred into a buffer.

The buffered value remains unchanged until the 16-bit read sequence is completed, even if the user reads the MSB several times. The read sequence is completed by reading the free running counter LSB, which actually returns the buffered value.

The free running counter is configured to FFFCh during reset, after the RESET line goes high. During a power-on reset (POR), the counter is also configured to FFFCh and begins running after the oscillator start-up delay.

When the counter rolls over from FFFFh to 0000h, the Timer Overflow flag (TOF) of the Timer Status Register (SR) is set. A timer interrupt is then generated if the TOIE enable bit of the Timer Control Register (TCR) is set, provided the I bit of the CCR is cleared. If one of these conditions is false, the interrupt remains pending to be issued as soon as they are both true. The interrupt request is cleared by reading SR while TOF is set followed by an access (read or write) to the LSB of the Counter Register.

The TOF flag is not affected by accesses to the Alternate Counter Register. This feature allows simultaneous use of the overflow function and reads of the free running counter at random times (for instance, to measure elapsed time) without risking clearing the TOF flag unintentionally. Accesses to the timer without the intention of servicing the TOF flag should therefore be performed to the Alternate Counter Register while only the TOF service routine accesses the Counter Register.

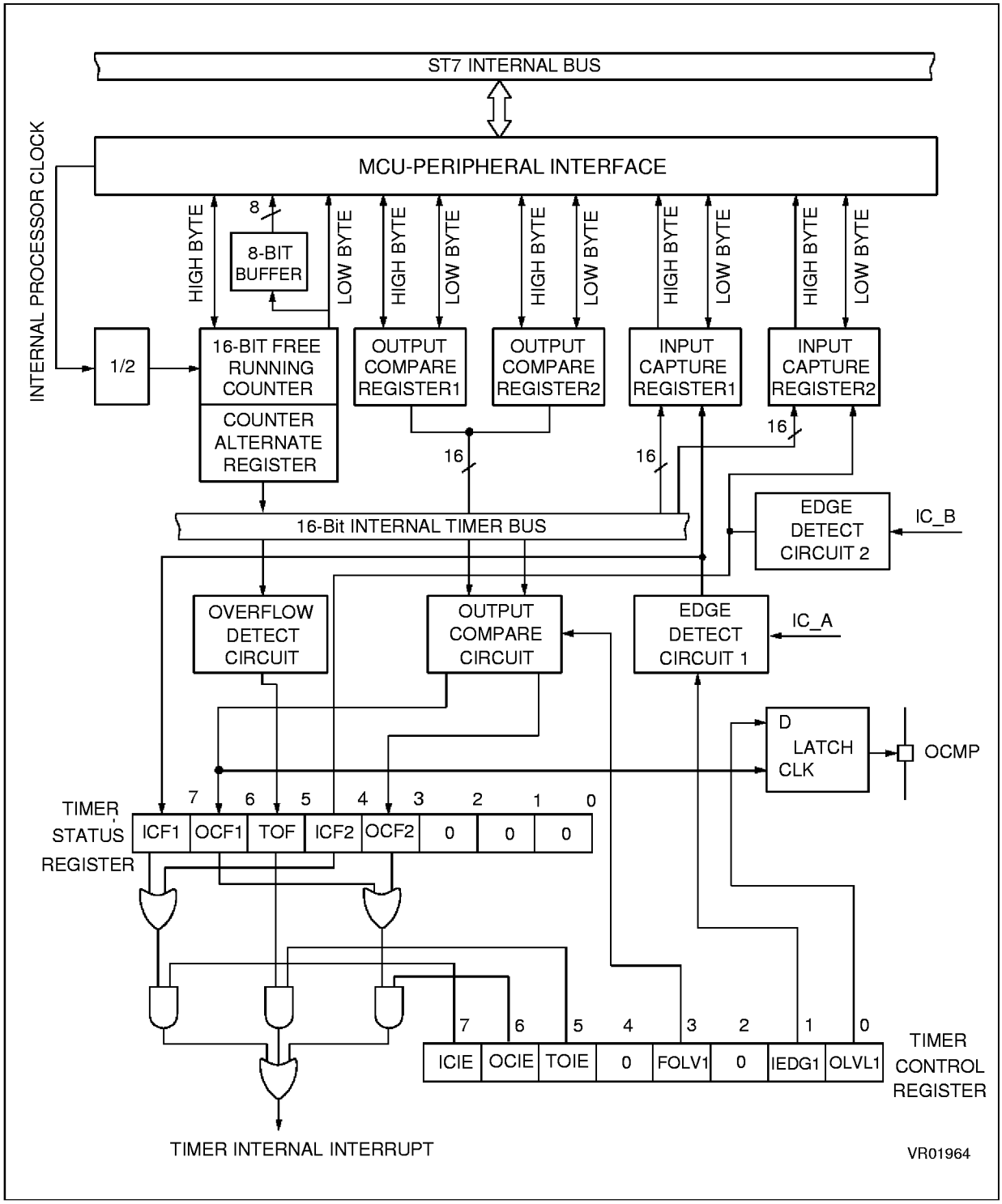
The free-running counter can be reset under software control. This is performed by writing to the LSB of either the Counter Register or the Alternate Counter Register. The counter and the prescaler are then configured to their reset conditions. This reset also completes any 16-bit access sequence. All flags and enable bits are unchanged.

The value in the counter registers repeats every 131,072 internal processor clock cycles (32 ms for f_{CPU} = 4 MHz). The counter increment is triggered by a falling edge of the CPU clock.

The timer is not affected by WAIT mode. In HALT mode, the counter stops counting until the mode is exited. Counting then resumes from the previous count (MCU woken by an interrupt) or from the reset count (MCU woken by a reset).

16-BIT TIMER (Cont'd)

Figure 17. Timer Block Diagram



16-BIT TIMER (Cont'd)

4.3.4 Input Capture.

The ST7272 features two input capture registers and one input capture interrupt enable bit. The input capture inputs IC_A and IC_B are connected through the VSYNCI and HSYNCI (OR CSYNCI) input pins respectively. When the SYNC processor is not being used, these pins may be used for the timer external input capture circuits. The input on HSYNCI may optionally be passed through a 256 prescaler before being passed to the IC_B input capture.

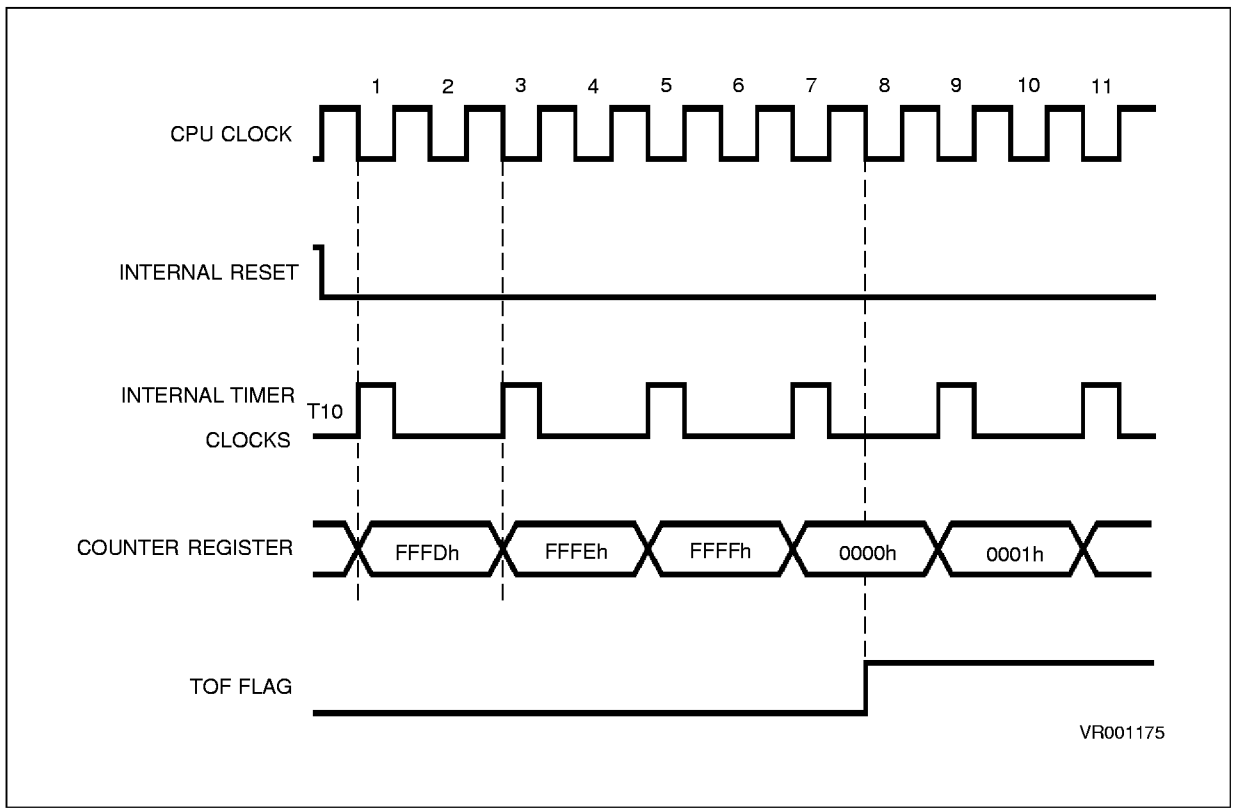
Input Capture Register 1 (ICR1) is a 16-bit register consisting of two 8-bit registers: the most significant byte register (ICHR1), located at 0014h, and the least significant byte register (ICLR1) located at 0015h.

ICR1 is a read-only register used to latch the value of the free running counter after a defined transition is sensed by the input capture edge detector IC_A. This transition is software programmable through the IEDG1 bit of the Timer Control Register (TCR). When IEDG1 is set, a rising edge triggers the capture; when IEDG1 is low, the capture is triggered by a falling edge. Care must be taken with the external circuitry to avoid unwanted interrupts when changing the interrupt edge.

When an input capture occurs, the ICF1flag in the Timer Status Register (SR) is set. An interrupt is requested if the interrupt enable bit ICIE of TCR is set, provided the I bit of the CCR is cleared. Otherwise, the interrupt remains pending until both conditions become true. It is cleared by reading the Timer Status Register SR followed by an access (read or write) to the LSB of ICR1.

The result stored in ICR1 is one more than the value of the free running counter on the rising edge of the internal processor clock preceding the active transition on IC_A. This delay is required for internal synchronization. Therefore, the timing resolution of the input capture system is one count of the free running counter, i.e. 2 internal clock cycles.

Figure 18. Timer Timing Diagram



16-BIT TIMER (Cont'd)

The free running counter is transferred to ICR1 on each proper signal transition, regardless of whether the Input Capture Flag ICF1 is set or cleared. The ICR1 always contains the free running counter value which corresponds to the most recent input capture.

After reading the MSB of ICR1 (ICHR1), counter transfer of input capture is inhibited until the LSB of ICR1 (ICLR1) is also read. This characteristic forces the minimum pulse period attainable to be determined by the time required to service the interrupt and to execute the interrupt routine.

Reading ICLR1 does not inhibit counter transfer. Again, minimum pulse periods are the ones which allow software to read the least significant byte and perform needed operations. There is no conflict between reading ICR1 and the running counter transfer since they occur on opposite edges of the internal processor clock.

The contents of ICR1 are undetermined at power-on and are not affected by an external reset. Hardware circuitrymust provide protection from generating a spurious input capture when changing the edge sensitivity option of the IC_A input through the IEDG1 bit.

During HALT mode, if at least one valid input capture edge occurs at the IC_A input, the input capture detect circuitry is armed. This action does not set any timer flags nor will it "wake-up" the MCU. If the MCU is woken up by an interrupt, there will be an active input capture flag and data from the first valid edge that occurred during HALT mode. If HALT mode is exited by a reset, the input capture detect circuitry is reset and thus any active edge that occurred during HALT mode will be lost.

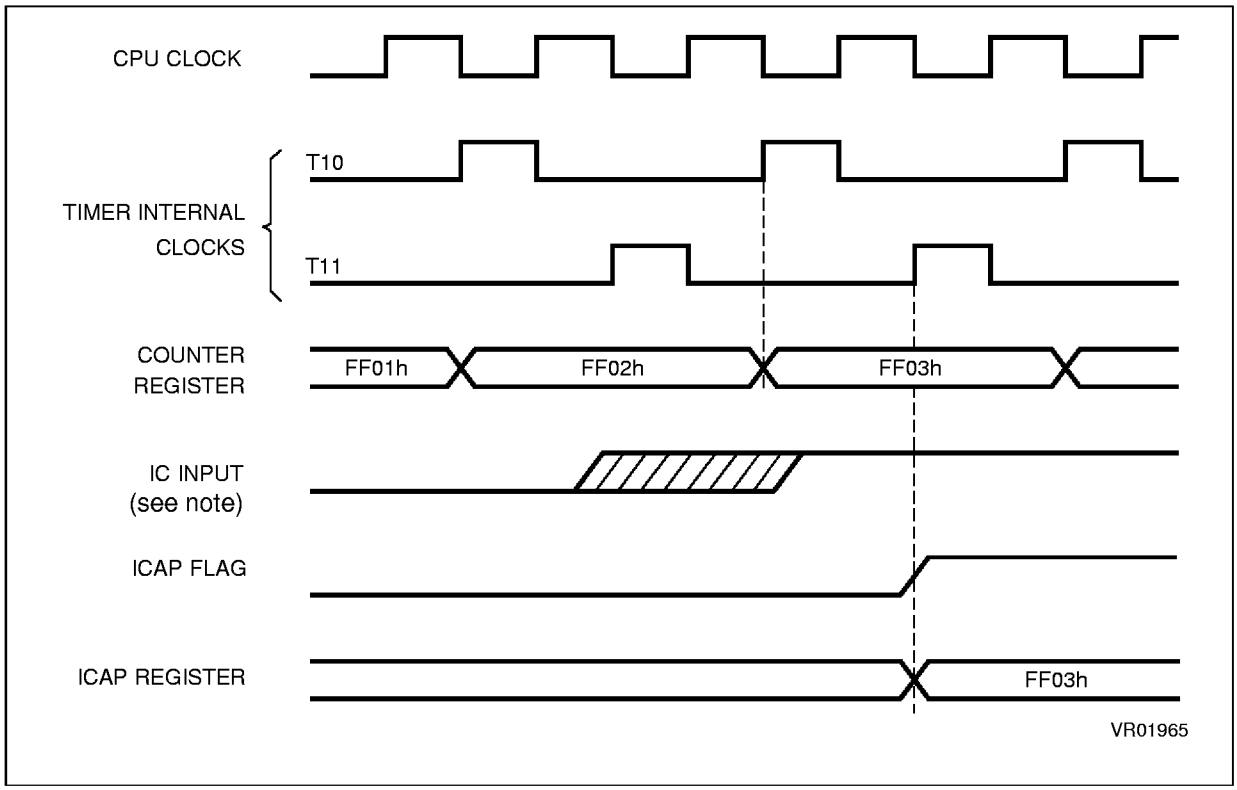
Input Capture Register 2 (ICR2) is a 16-bit register comprising two 8-bit registers: the most significant byte register (ICHR2), located at 001Ch, and the least significant byte register (ICLR2) located at 001Dh.

The previous description for Input Capture Register 1 is also applicable to Input Capture Register 2, with the exception that Input Capture Register 2 is triggered only on a negative edge on input IC_B (and with the substitution of the appropriate suffix in the bit and register names.

4.3.5 Output Compare

There are two output compare registers: Output Compare Register 1 and 2 (OCR1 and OCR2).

Figure 19. Input Capture Timing Diagram



16-BIT TIMER (Cont'd)

They can be used for several purposes, such as controlling an output waveform or indicating when a period of time has elapsed. The OCMP1 pin is associated with output compare 1; no pin is associated with Output Compare 2 which, however, may be usedto generate timer interrupts.

The Output Compare Registers are unique because all bits are readable and writable and are not affected by the timer hardware or reset. If a compare function is not used, the two bytes of the corresponding Output Compare Registers can be used as storage locations. Note that the same output compare interrupt enable bit is used for both output compares.

Output Compare Register 1. The Output Compare Register 1 (OCR1) is a 16-bit register, consisting of two 8-bit registers: the most significant byte register (OCHR1) at address 0016h and the least significant byte register (OCLR1) at address 0017h.

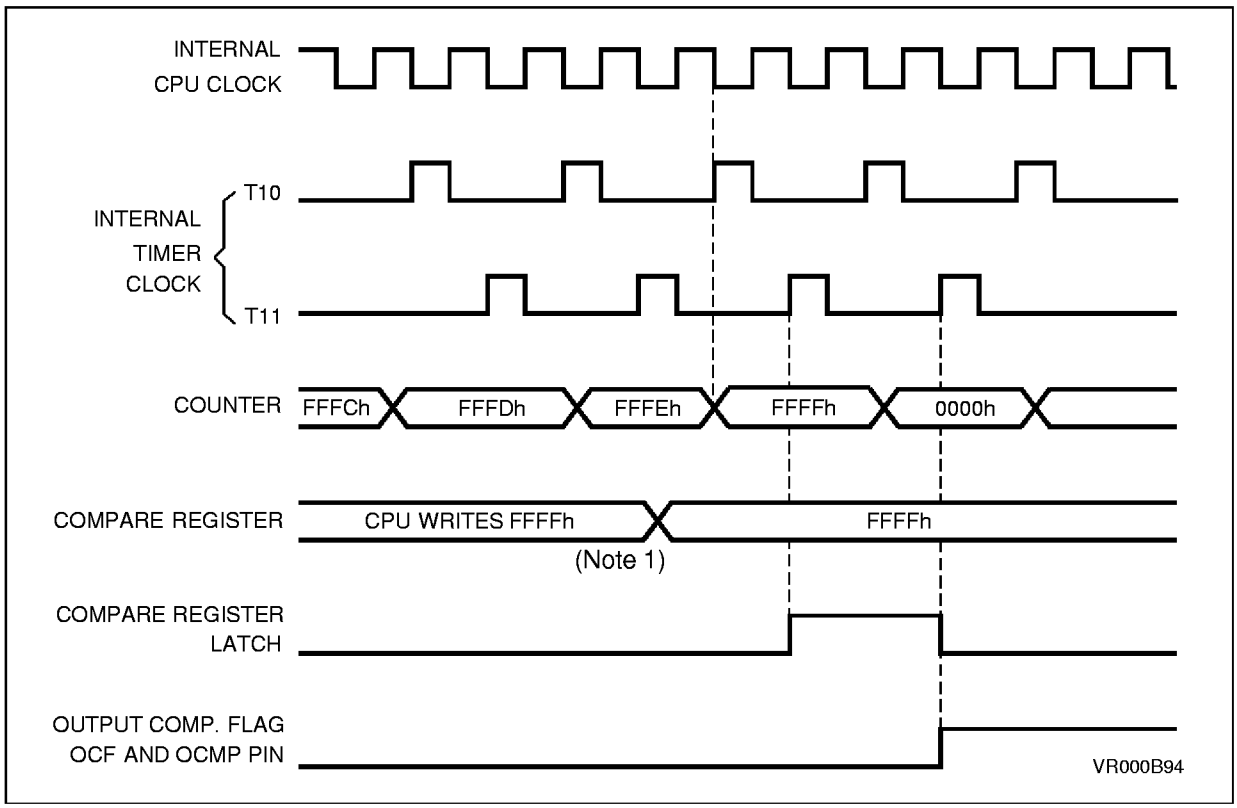
The content of OCR1 is compared with the content of the free running counter once during every timer clock cycle, i.e. every 2 internal processor clock periods. If a match is found, the Output Compare Flag OCF1 of the SR is set and the Output Level bit (OLVL1) of the TCR is clocked to the OCMP1 pin (see output compare timing diagram).

OLVL1 is copied to the corresponding output level latch and hence, to the OCMP1 pin regardless of whether the Output Compare Flag (OCF1) is set or not. The value in the OCR1 and the OLVL1 bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed time-out.

An interrupt follows a successful output compare if the corresponding interrupt enable bit OCIE of the TCR is set, provided the I-bit of the CCR is cleared. Otherwise, the interrupt remains pending until both conditions are true. It is cleared by reading the SR, followed by accessing the LSB of the OCR1.

After a processor write cycle to the OCHR1 register, the output compare function is inhibited until the OCLR1 is also written. Thus, the user must write both bytes if the MSB is written first. A write made only to the LSB will not inhibit the compare function. The minimum time between two successive edges on the OCMP1 pin is a function of the software program.

Figure 20. Output Compare Timing Diagram



16-BIT TIMER (Cont'd)

The OCMP1 output latch is forced low during reset and stays low until valid compares change it to a high level. Because the OCF1 flag and the OCR1 are undetermined at power-on and are not affected by an external reset, care must be exercised when initiating the output compare function by software. The following procedure is recommended to prevent the OCF1 flag from being set between the time it is read and the subsequent write to OCR1:

Write to OCHR1 (further compares are inhibited).

Read the SR (first step of the clearance of OCF1 [it may be already set]).

Write to OCLR1 (enables the output compare function and clears OCF1).

Output Compare Register 2 The Output Compare Register 2 (OCR2) is a 16-bit register, which consists of two 8-bit registers: the most significant byte register (OCHR2) at address 001Eh and the least significant byte register (OCLR2) at address 001Fh.

This register operates in a similar fashion to Output Compare Register 1. For a complete description, please refer to the latter and substitute the appropriate suffix in the bit and register names.

Software Forced Compare The main purpose of the forced compare function is to facilitate fixed frequency generation.

When the Force Output Level 1 bit (FOLV1) of TCR is written to 1, OLVL1 is copied to pin OCMP1 or TX pin (if TXEN control bit is set). To provide this function, internal logic allows a single instruction to change OLVL1 and causes a forced compare with the new value of OLVL1. OCF1 is not affected and thus, no interrupt request is generated.

4.3.6 Register Description

(CR) TIMER CONTROL REGISTER (0012 h)

Read/Write
Reset Value: 0000 00x0 (00h or 02h)

7							0
ICIE	OCIE	TOIE	RES	FOLV1	RES	IEDG1	OLVL1

b7 = **ICIE:** *Input Capture Interrupt Enable*
If ICIE is set, a timer interrupt is enabled whenever the ICF1/2 status flags of SR are set. If the ICIE bit is cleared, the interrupt is inhibited.

b6 = **OCIE:** *Output Compare Interrupt Enable*
If OCIE is set, a timer interrupt is enabled whenever the OCF1/2 status flags of SR are set. If the OCIE bit is cleared, the interrupt is inhibited.

b5 = **TOIE:** *Timer Overflow Interrupt Enable*
If TOIE is set, a timer interrupt is enable whenever the TOF status flag of SR is set. If the TOIE bit is cleared, the interrupt is inhibited.

b4 = **Reserved**, Read as '0'

b3 = **FOLV1:** *Force Output Compare 1.* When written to 1, FOLV1 forces OLVL1 to be copied to the OCMP pin.

b2 = **Reserved**, Read as '0'

b1 = **IEDG1:** *Input Edge 1*
The value of the IEDG1 bit determines which level transition on IC_A input will trigger a free running counter transfer to the ICR1. When IEDG1 is high, a rising edge triggers the capture and when low, a falling edge does.

b0 = **OLVL1**: Output Level 1
The OLVL1 bit is copied to the OCMP1 pin whenever a successful comparison occurs at OCR1.

(SR) TIMER STATUS REGISTER

(0013 h)

Read Only
Reset Value: Undefined

7							0
ICF1	OCF1	TOF	ICF2,	OCF2	0	0	0

b7 = **ICF1** *Input Capture Flag 1*
ICF1 is set when a proper edge has been sensed by the input capture edge detector at IC_A. The edge is selected by the IEDG1-bit in TCR. ICF1 is cleared by a processor access to the SR while ICF1 is set followed by an access (read or write) to the low byte of ICR1 (ICLR1).

b6 = **OCF1** *Output Compare Flag 1*
OCF1 is set when the content of the free running counter matches the content of OCR1. It is cleared by a processor access to SR while OCF1 is set followed by an access (read or write) to the low byte of OCR1.

b5 = **TOF** *Timer Overflow*
TOF is set by a transition of the free running counter from FFFFh to 0000h. It is cleared by a processor access to SR while TOF is set followed by an access (read or write) to the low byte of the counter low register. TOF is not affected by an access to the Alternate Counter Register.

16-BIT TIMER (Cont'd)

b4 = **ICF2** *Input Capture Flag 2*
ICF2 is set when a negative edge has been sensed by the input capture edge detector at IC_B. ICF2 is cleared by a processor access to the SR while ICF2 is set followed by an access (read or write) to the low byte of ICR2 (ICLR2).

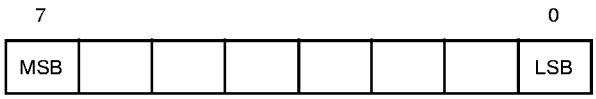
b3 = **OCF2** *Output Compare Flag 2*
OCF2 is set when the content of the free running counter matches the content of OCR2. It is cleared by a processor access to SR while OCF2 is set followed by an access (read or write) to the low byte of OCR2.

b2-0 = **Unused**, read as '0'.

INPUT CAPTURE REGISTER 1 (IC1HR)

High Byte address 0014 h — Read Only

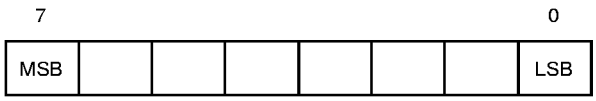
Reset Value: Undefined



INPUT CAPTURE REGISTER 1 (IC1LR)

Low byte address 0015 h — Read Only

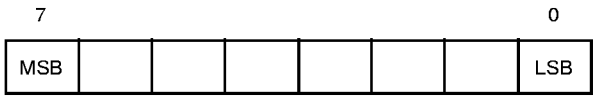
Reset Value: Undefined



OUTPUT COMPARE REGISTER 1 (OC1HR)

High byte address 0016 h — Read/Write

Reset Value: Undefined

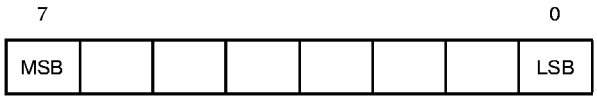


OUTPUT COMPARE REGISTER 1 (OC1LR)

Low byte address 0017 h — Read/Write

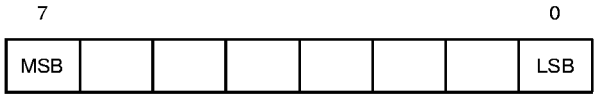
Reset Value: Undefined

COUNTER REGISTER (CNTHR)



High byte address 0018 h — Read Only

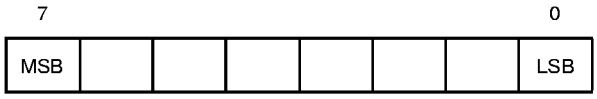
Reset Value: 1111 1111 (FF h)



COUNTER REGISTER (CNTLR)

Low byte address 0019 h — Read/Write

Reset Value: 1111 1100 (FC h)

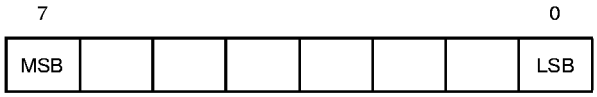


Writing to this Register will cause the counter to be reset to its reset value of FFFCh. Flags and enable bits remain unaltered by this operation.

ALTERNATE COUNTER REGISTER (ACNTHR)

High byte address 001A h — Read Only

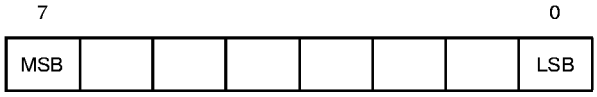
Reset Value: 1111 1111 (FF h)



ALTERNATE COUNTER REGISTER (ACNTLR)

Low byte address 001B h — Read/Write

Reset Value: 1111 1100 (FC h)



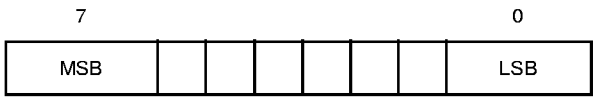
Writing to this Register will cause the counter to be reset to its reset value of FFFCh. Flags and enable bits remain unaltered by this operation.

16-BIT TIMER (Cont'd)

INPUT CAPTURE REGISTER 2 (IC2HR)

High byte address 001C h — Read Only

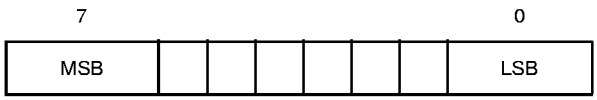
Reset Value: Undefined



OUTPUT COMPARE REGISTER 2(OC2HR)

High byte address 001E h — Read/Write

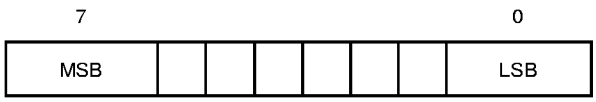
Reset Value: Undefined



INPUT CAPTURE REGISTER 2(IC2LR)

Low byte address 001D h — Read Only

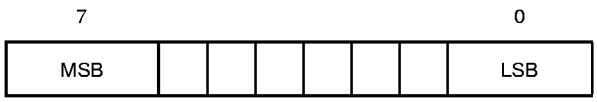
Reset Value: Undefined



OUTPUT COMPARE REGISTER 2 (OC2LR)

Low byte address 001F h — Read/Write

Reset Value: Undefined



4.4 SYNC PROCESSOR (SYNC)

4.4.1 Introduction

The Sync Processor manages the video synchronization signals, and is used in conjunction with the Timer to provide information and status on the video standard and timings. This Sync Processor is a superset of the ST7271 sync processor.

In order to be able to resolve all required timing information, the MCU must operate with an oscillator frequency of 8MHz.

Separate Horizontal and Vertical Synchronization pulses, provided on the (HSYNCI1, VSYNCI1) or (HSYNCI2, VSYNCI2) pins, are accepted, and polarity is detected by hardware. In this case HSYNCO = HSYNCI (with programmable polarity inversion, but without blanking).

Alternatively a composite sync signal (sync pulses only) may be input on CSYNCI (or HSYNCI pin), with automatic synchronization pulse extraction and hardware polarity detection.

Extraction of VSYNCO may be obtained from a composite signal (OR, XOR, or serration pulses).

Note: if the input is a composite signal both VSYNCO and HSYNCO will be extracted (the latter can be blanked during the VSYNCO pulse as far as potential serration pulses are concerned).

Processed sync pulses may be output to external parts of the circuit through the HSYNCO and VSYNCO pins, with programmable polarity. An independent programmable duration/polarity back-porch or pseudo front-porch (clamping) output signal (CLMPO) generator can be used as a Video clamp reference signal for the Video Preamplifier IC. Where HSYNCO and VSYNCO are extracted from CSYNCI, the signal is always suppressed during vertical blanking.

4.4.2 Features

- Determination H Sync In1 and V Sync In 1 signal levels
- Sync detection of H Sync In, V Sync In, C Sync In, H Fly In, V Fly In signals
- Detection of H Sync In polarity and presence of Composite Sync
- V Sync Out Polarity detection
- Programmable Clamp Out pulse polarity
- Built-in composite video blanking signal generator
- Internal programmable H Sync Out/V Sync Out frequency generator
- Acquisition of the number of scan lines during one frame
- Acquisition of the delay between two HSync pulses
- Detection of Pre-equalization pulses
- Programmable inhibition of Pre equalization/Post equalization pulses
- Programmable V Sync Out pulse width extension
- One shot programmable H sync edge generator
- Programmable V Sync Out pulse width extension during detection of post-equalization pulses
- VSYNCI1 Schmitt trigger sync signal is DDC1 clock reference for DDC/DMA cell.

4.4.3 Functional Description

The main function of the Sync Processor can be summarized as consisting of the following tasks:

- Checking the presence of input signals by H/W (VSYNCI, HSYNCI and CSYNCI)
- Polarity Detection by H/W (VSYNCI, HSYNCI or CSYNCI)
- HSYNCO, VSYNCO Extraction or Self Generation
- Video Standard Discrimination
- Composite Video Blanking Generator Stage

These tasks are performed by the Sync Processor in close conjunction with the Timer Input captures, and user software.

The block diagram of the Sync Processor is shown in Figure 22. This also shows the internal connections to the Timer Input Capture A (IC_A) and Input Capture B (IC_B). All quoted timings are for operation at 8MHz oscillator frequency.

4.4.3.1 Checking the presence of input signals

The Sync Processor offers two techniques for checking signal presence, a S/W regular check and an indirect check which is interrupt driven and uses the H/W of the Sync Processor.

Direct Check

Using the Latch Register (LATR), it is possible to detect the presence of HSYNCI, VSYNCI, CSYNCI, HFly and VFly signals. These latches are set upon falling edge detection, and cleared by S/W. With the Timer Overflow or Output Compare timebase, the Mode Recognition and Power Management tasks can be easily made.

SYNC PROCESSOR (Cont'd)

Indirect Check

To use the indirect check method, multiplexers are set to connect the VSYNCI input to Timer Input Capture A and HSYNCI or CSYNCI to the Input Capture B.

Step I - Checking VSYNCI. Any interrupt request coming from IC_A is monitored. (On detecting VSYNCI, the software may either detect the VSYNCI polarity or check for the presence of HSYNCI).

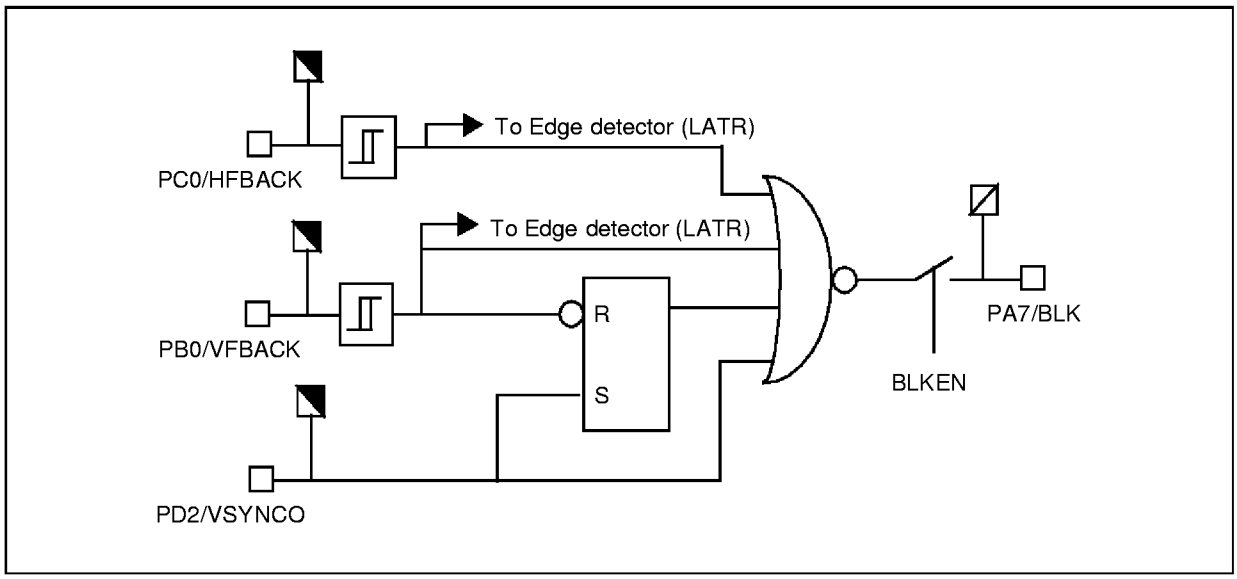
Step II - Checking HSYNCI. The HSYNCI input is connected directly to IC_B. An interrupt request is waited for (on detecting HSYNCI, the software may either detect the HSYNCI polarity or check the CSYNCI presence).

Step III - Checking CSYNCI. The CSYNCI input is connected directly to IC_B. An interrupt request is waited for.

Note. Input Capture A edge detection polarity can be selected to be positive or negative.
Input Capture B edge detection polarity is fixed for negative edges.

Steps I-III may be carried out in parallel.

Figure 21. Simplified Schematic of Video Blanking Stage



HFBACK, VFBACK and VSYNCO signals should have positive polarity

SYNC PROCESSOR (Cont'd)

4.4.3.2 Polarity Detection

The Sync Processor also offers two techniques for checking the polarity of signals: a regular software direct check and an indirect check which uses the Sync Processor hardware, thus avoiding CPU intensive S/W polling.

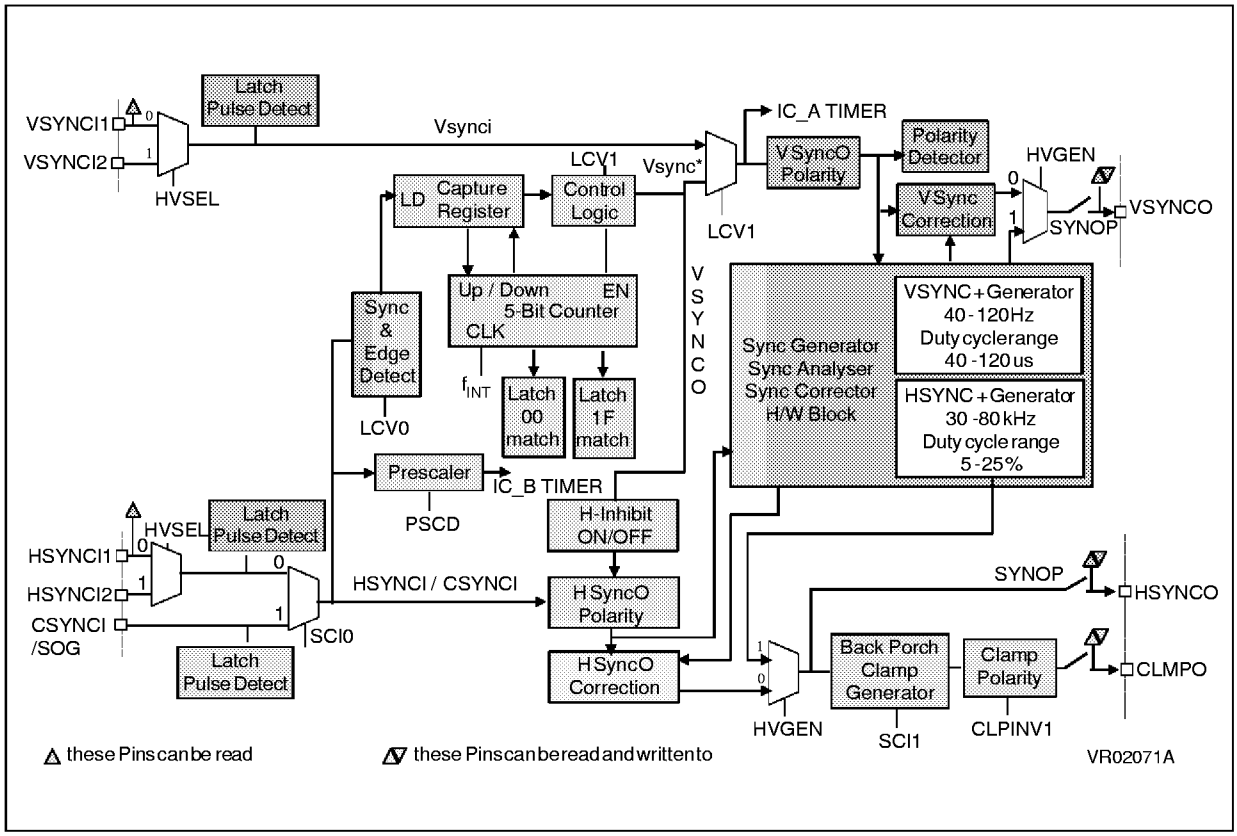
Indirect Polarity Detection

This method involves the internal 5-bit up/down counter. At the beginning of the detection phase, '11111' is written into the CCR register (CVM bits). These bits are refreshed by the 5-bit counter value at every detected edge on the signal considered. The counter increments when the signal is high; otherwise it decrements.

Software can thus check the SYNC Processor capture register after an interrupt (with the signal connected to IC_A or IC_B), or by polling. In the case of positive polarity the capture value will be '00000', since the counter stays at this value after underflowing. Otherwise, it will be non-zero (the value depending on the resolution of the counter) and thus indicate that the signal is of negative polarity.

This one-shot detection approach covers separate HSYNCI and VSYNCI signals only. For composite input signals, the software simply needs to check that the VSYNCO period and polarity are stable.

Figure 22. Sync Processor Block Diagram



SYNC PROCESSOR (Cont'd)

Direct Polarity detection

HSYNCI/CSYNCI polarity detection makes use of the UPLAT and DOWNLAT latches connected to the 5 bit Up/Down counter. This pair of latches in LATR indicates the nature of the HSYNCI Sync signal:

UPLAT	DWNLAT	H Sync In Nature
0	0	No Info
0	1	Negative Sync
1	0	Positive Sync
1	1	Composite Sync

The VSYNCI polarity detection is done by H/W and returned in the VPOL bit of the POLR register. The delay between VSYNC polarity changes and the VPOL bit typically toggles within 4 msec.

The polarity detector includes an integrator to filter possible incoming VSYNC glitches.

Figure 23. Horizontal Sync Input Timing

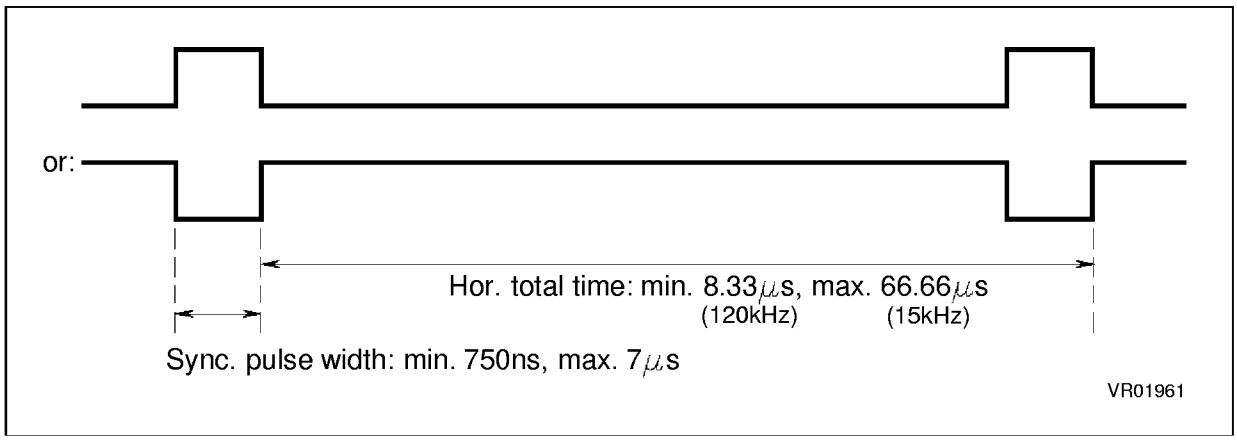
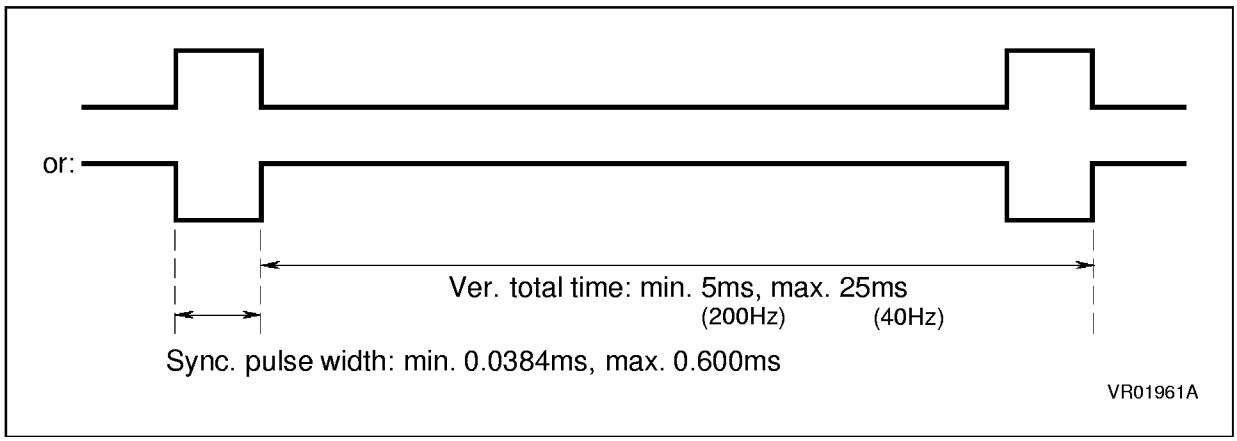


Figure 24. Vertical Sync Input Timing



SYNC PROCESSOR (Cont'd)

4.4.3.3 VSYNCO Extraction

VSYNCO is extracted from CSYNCI with the aid of the 5-bit up/down counter. Initially, the width of a Horizontal sync component pulse is determined automatically by hardware, which defines a threshold for the counter (which may be replaced with an optional user-defined value including a tolerance factor). The circuit then checks for any input period greater than this captured value. This is then processed as for the VSYNCO signal.

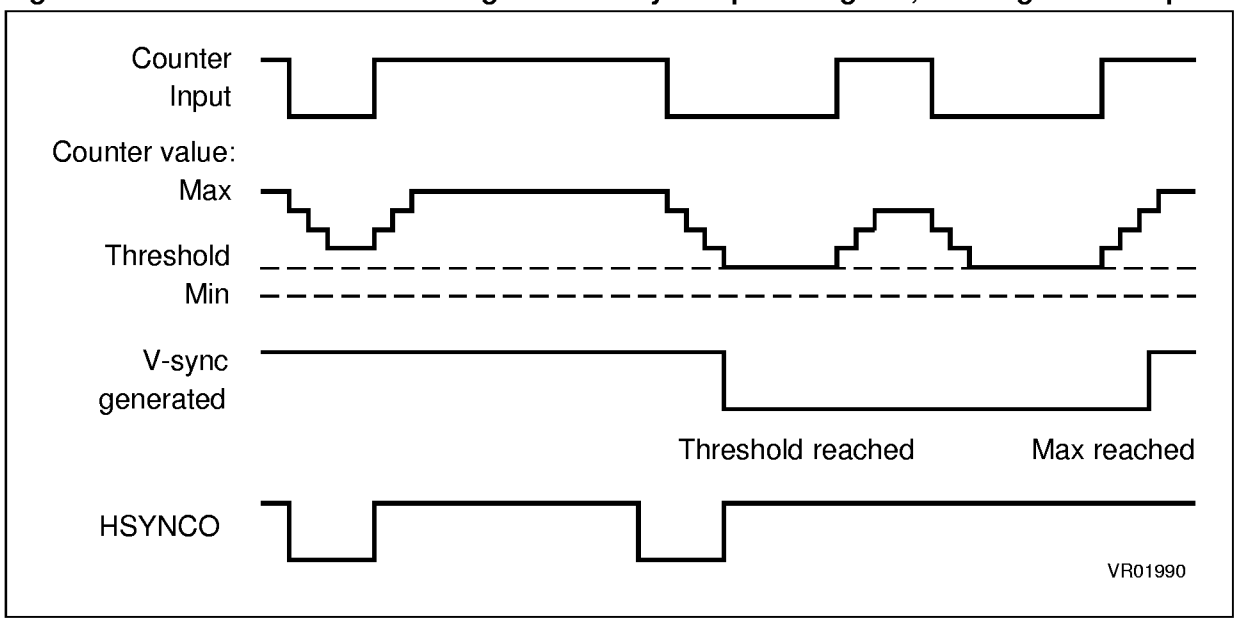
The S/W should first select the acquisition mode to measure the internal Horizontal sync component pulse width. The time-equivalent value is read after this value is captured in the CCR register. If a user-defined tolerance is to be added, an updated value can be re-written into the register.

Capture occurrence can be flagged by the timer Input Capture interrupt or by reading a new value in the Sync Processor Control Register. After this step, the S/W should set the extraction mode (LCV1 bit) to start the VSYNCO sync extraction by H/W as described in the following paragraph, for a negative polarity signal.

In extraction mode, the 5-bit comparator checks the counter value with respect to the threshold. When the counter reaches the threshold on a downcount, VSYNCO is asserted. During the vertical blanking period, the counter value is decreased down to a programmable minimum, i.e. it does not underflow. When the vertical period is over, the counter starts counting up, and when the maximum count is reached, VSYNCO is negated. The extracted signal may be validated by S/W since it is input to Timer IC_A.

The threshold is greater than the count for a HSYNCI pulse. Serration pulses during vertical blanking can be filtered. Similarly, positive CSYNCI signals are covered by properly selecting the edge sensitivity on the Hsync width measurement mode (LCV0 bit).

Figure 25. VSYNCO Generation for Negative Polarity Composite signals, showing Serration pulses



SYNC PROCESSOR (Cont'd)

4.4.3.4 Standard Discrimination

Discrimination of video standards is supported by use of the Timer peripheral in conjunction with the Sync Processor. For this purpose, either HSYNCI or CSYNCI is prescaled by 256.

Note: The prescaler can be bypassed for frequency synchronization signals lower than specified. The prescaler can be reset (disabled/enabled) to synchronize the H Sync period measurement with V Sync.

This function is carried out by using the Timer Input-Capture Channels:

a) VSYNCI is directly connected to IC_A (after synchronization; PV measured).

b) HSYNCI or CSYNCI is prescaled (or not) by a factor of 256 in the Sync Processor, and then sent to IC_B. (PHx256 measured).

Signal timing can be directly calculated using the time values between the appropriate interrupts generated by the Timer, and then used for comparison against existing pre-defined standards. An averaging method on Period measurement can yield more accurate timing for comparison, if serration pulses are present on CSYNCI.

Application Note:

Accuracy of period measurement

Basically, the substraction between two consecutive Input Captures (16-bit value) gives the period for 256xPH (horizontal period), and PV (vertical period). The period accuracy is one Timer clock (500ns), so that the tolerance is:

256xPH tolerance: 500ns (1.95 ns for PH itself)
PV tolerance: 500 ns

4.4.3.5 Video Blanking Signal Generator

This block involves VSYNCO, HFBACK and VFBACK as input signals and BLK Out as Video Blanking Output signal (active low).

The Video Blanking output (BLK) can be enabled/disabled by S/W. This pin is a 12V open-drain output and can be AND-wired with any external video blanking signa (coming, for example, from the TDA9103 Deflection processor).

Application Note:

To use the video blanking signal, the BLKEN bit must be set, PC0 and PB0 must be configured as digital inputs, and PA7/BLK as either a digital input or as a digital output set to a logic high level.

Forcing video blanking by S/W, by forcing the PA7 output low (Data Register bit) will do the job without any electrical conflicts, due to the open-drain feature of the PA7 I/O pin.

If the VFBACK signal disappears, the video blanking output signal will remain permanently low due to the RS flip/flop.

If PA7 is set as a digital input and the blanking output is enabled, the PA7 Data Register bit will indicate the BLK signal level.

If this block is not used, PC0 and PB0 can be used as falling edge signal detectors (LATR).

4.4.3.6 Inputs

The Sync Processor inputs consist of the Video Synchronization strobe pulses:

– VSYNCI1, VSYNCI2 (Vertical Sync input, TTL Level, Schmitt triggered).

– HSYNCI1, HSYNCI2 (Horizontal Sync input, TTL Level, Schmitt triggered).

– CSYNCI (Composite Sync input, TTL Level, Schmitt triggered).

Note: The Composite Sync signal may also be received on the HSYNCI input if this is supplied by the external circuit and the I/O function of the CYSYNCI I/O pin for is required.

Selection of the Sync input sources (HSYNCI1, VSYNCI1 or HSYNCI2 (PC1), VSYNCI2 (PD4)) is accomplished via the HVSEL bit of the MISCR.

Input Signal Waveforms.

The input signals must contain only synchronization pulses.
Timing characteristics of HSYNCI and VSYNCI:

– Where serration pulses are present on CSYNCI/HSYNCI, these pulses should be externally generated with a minimum of half a line delay from the VSYNCI edge.

– The HSYNCI or CSYNCI signal, optionally prescaled by 256, is connected to the IC_B input (Timer Input Capture B) of the Timer.

– The Timer resolution is 500ns for an external oscillator frequency of 8MHz.

4.4.3.7 Outputs

HSYNCO: HSYNC Output, (CMOS Level). This programmable polarity signal can be blanked by S/W during the vertical period (if the input is a composite signal). Its internal propagation delay has been optimized to its lowest possible delay.

SYNC PROCESSOR (Cont'd)

If separate HSYNCI and VSYNCI signals are provided, no blanking is generated on HSYNCO.
VSYNCO: VSYNC Output, (CMOS Level) with programmable polarity.
VSYNCO is connected to IC_A, input to Timer Input Capture A.
CLMPO: (CMOS level) back-porch clamp signal with programmable polarity.

If VSYNCO is extracted from a composite signal, the minimum delay is 500ns + HSYNCO pulse width. The maximum delay is software defined (the threshold value in extraction mode) and corresponds to 8750 ns.

Notes:

– If separated HSYNCI and VSYNCI are provided, no blanking is generated on HSYNCO.

– No direct interrupt request is used by the Sync Processor, although the optional interrupt in the timer can be used by the software since VSYNCO and HSYNCI/CSYNCI signals are connected to Input Capture (IC_A and IC_B, respectively).

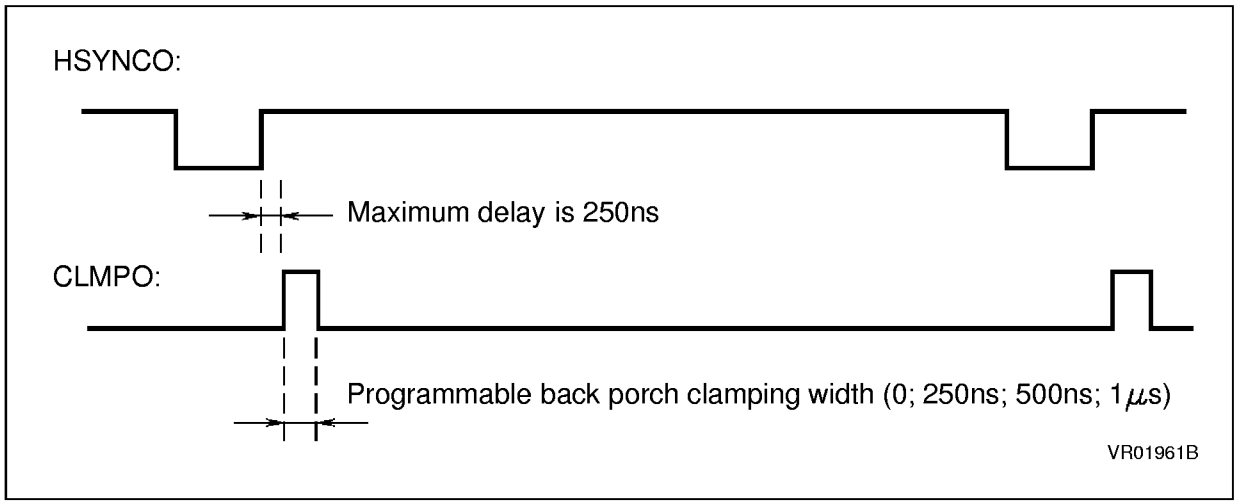
– The Timer Interrupt Request should be masked during a write access to the SYNC Control Registers.

Application note:

The clamping pulse generator can also be configured as a pseudo front-porch pulse generator instead of back-porch signal by sensing the leading edge of the H Sync O signal.

If the clamping pulse generator block is not used (e.g. when the TDA920X Video Preamplifier with internal clamping pulse generator is used), the output pin can be used as normal I/O.

Figure 26. Back Porch (CLMPO) Delay



Note: The Clamping pulse generator can generate both back porch and pseudo front porch signals and polarity can be programmed as positive or negative. The illustration above shows the maximum delay between the trailing edge of HSYNCO and the leading edge of CLMPO for a back porch signal; the delay (250 ns max) will be the same in the case of a pseudo front porch signal, but in this case the delay will be between the leading edge of HSYNCO and the leading edge of CLMPO. Note that the clamping signal pulse width can be programmed as 0, 250ns, 500ns or 1µs via bits BP0 and BP1 of the MCR register.

SYNC PROCESSOR (Cont'd)

4.4.4 Register Description

(CCR) COUNTER CONTROL REGISTER (0042 h)

Read/Write
Reset Value 0000 0000 (00 h)

7							0
PSCD	LCV1	LCV0	CV4	CV3	CV2	CV1	CV0

b7 = **PSCD:** Prescaler Enable bit

PSCD	Enable/Disable the 256 Prescaler
0	Prescaler enabled
1	Prescaler disabled and preset to FEh

Application note: For a Composite Sync signal, the horizontal period measurement can be synchronized on VSYNC pulse by doing a Set/Reset of PSCD bit by S/W during VICAP interrupt.

b6-5 = **LCV1,LCV0:** VSYNCO Extraction Control Bits

b4-0 = **CV4-0:** Counter Captured Value.

These bits correspond to the counter captured value in different modes. Upon VSYNCO extraction, it corresponds to a HSYNCI pulse-width measurement, which may be changed by software before extraction.

LCV1	LCV0	VSYNC0 Control Bits
0	0	Acquisition mode Counter capture on input signal falling edge
0	1	Acquisition mode Counter capture on input signal rising edge
1	0	Extraction mode CSYNCI/HSYNCI Negative polarity CV4-0 = counter minimum threshold
1	1	Extraction mode CSYNCI/HSYNCI Positive polarity CV4-0 = counter maximum threshold

(MCR) MUX CONTROL REGISTER (0041 h)

Read/Write
Reset Value: 0000 0000 (00 h)

7							0
BP1	BP0	SCI1	SCI0	HS1	HS0	VOP	VIP

b7-6 = **BP1, BP0**: Back Porch Pulse Width control

BP1	BP0	Back Porch pulse width
0	0	No Back Porch
0	1	250ns
1	0	500ns
1	1	1000ns

b5 = **SCI1**: Horizontal/Vertical Signal Path Selection Bit. This bit selects the path for the incoming signals towards IC_A, IC_B, VSYNCO and HSYNCO:

SCI1	5 bit Up/Down Counter Mode Selection
0	VSYNCI Polarity Detection IC_B connected to HSYNCI/CSYNCI w/o prescaling
1	HSYNCI/CSYNCI Polarity detection / VSYNCO Extraction IC_B connected to Prescaled HSYNCI/CSYNCI

Application Note: This bit should be always set

b4 = **SCI0:** HSYNCI/CSYNCI Selection

SCI0	HSYNCI/CSYNCI Sync Processor Input selection
0	HSYNCI selected
1	CSYNCI selected

SYNC PROCESSOR (Cont'd)

b3-2 = **HS1, HS0:** Horizontal Signal Selection Bits. These bits allow inversion of the HSYNCI/CSYNCI polarity, output as HSYNCO, as well as the generation of CLMPO as follows:

HS1	HS0	HSYNC Selection Mode
0	0	CLMPO after HSYNCO rising edge HSYNC0 <- (HSYNCI, CSYNCI)
0	1	CLMPO after HSYNCOI rising edge HSYNC0 <- ($\overline{\text{HSYNCI}}$, $\overline{\text{CSYNCI}}$)
1	0	CLMPO after HSYNCOI falling edge HSYNC0 <- ($\overline{\text{HSYNCI}}$, $\overline{\text{CSYNCI}}$)
1	1	CLMPO after HSYNCOI falling edge HSYNC0 <- (HSYNCI,CSYNCI)

b1-0 = **VOP,VIP:** Vertical Signal Polarity Selection Bits. These bits are only S/W controlled and are related to the polarity of the outgoing vertical signal.

VOP	VIP	VSYNC Selection Mode
0	0	ICAP_A <- VSYNCI VSYNCO <- VSYNCI
0	1	ICAP_A <- $\overline{\text{VSYNCI}}$ VSYNCO <- $\overline{\text{VSYNCI}}$
1	0	ICAP_A <- VSYNCI VSYNCO <- $\overline{\text{VSYNCI}}$
1	1	ICAP_A <- $\overline{\text{VSYNCI}}$ VSYNCO <- VSYNCI

Application Note:

VIP bit should be always fixed to "0".

VOP bit is used to negate or not the VSYNCO sync signal. In composite sync extraction mode (LCV1=1), the internal extracted VSYNC is ALWAYS negative polarity.

If each vertical input capture the VPOL bit is copied by S/W on VOP bit, the
VSYNCO sync signal will have constant positive polarity.

(CFGR) CONFIGURATION REGISTER (0040 h)

Read Write
Reset Value: 0000 0000 (00 h)

7							0
HACQ	VACQ	XTRAH	2FHINH	VEXT	Q'2	Q'1	Q'0

bit 7: **HACQ**uisition (set by S/W, cleared by H/W when the acquisition is over)

HACQ	Horizontal Sync Acquisition Mode (HVGEN=0)
0	Acquisition is over, and the result can be read in HGENR
1	Measurement of Low level period of HSYNC activated

bit 6: **VACQ**uisition (Set by S/W, cleared by H/W when the acquisition is over)

VACQ	Vertical Sync Acquisition Mode (HVGEN=0)
0	Acquisition is over, and the result can be read in VGENR
1	Measurement of the number of scan lines during VSYNCO low level period is activated

bit 5: **XTRAH** (HVGEN=0, HACQ=0) HSYNC edge generation enable. This function can correct HSYNC especially in composite sync where a HSYNC pulse is missing just before VSYNC pulse. This function generates an HSYNC raising edge when the monostable reaches 00, once per frame.
1 = Function enabled/ 0 = Function disabled.

bit 4: **2FHINH** (HVGEN=0, HACQ=0) Inhibition of Pre/Post equalization pulses. This function can remove pre/post equalization pulses on HSyncO signal. The duration of the inhibition is done between the falling edge of H Sync O up to the monostable reaches 8 value. (HGENR-2us)
1 = Function enabled / 0 = Function disabled.

bit 3: **VEXT** (HVGEN=0, VACQ=0, HACQ=0) V Sync Out pulse width extension. This function allows a VSYNCO pulse width extension in case of post-equalization pulse presence (2FHDET signal), up to 7 scan lines.
1 = Function enabled (extension done after the VGENR extension)
0 = Function disabled
Note: If VGENR=00, this function is disabled.

bit 2.0: **Q'2..Q'0** These are the read/write less significant bits of the VGENR 11-bit counter.

SYNC PROCESSOR (Cont'd)

(LATR) LATCH REGISTER (0044 h)

Read/Write
Reset Value: 0000 0000 (00 h)

7							0
CSYN	HSYN	VSYN	HFLY	VFLY	UPLAT	DWNLAT	2FHLAT

b0= **2FHLAT** - Set when Pre/Post equalization pulses are detected cleared by S/W (write of zero) (valid if HVGEN=0, HACQ=0)

b1= **DWNLAT** - Set when the 5 bit up-down counter reaches its minimum value (00 or Threshold) Cleared by S/W.

b2= **UPLAT** - Set when the 5 bit up-down counter reaches its maximum value (1F or Threshold) Cleared by S/W.

b3 = **VFLY** - Set on falling edge of VFLY/PB0 input. Cleared by S/W.

b4 = **HFLY** - Set on falling edge of HFLY/PC0 input Cleared by S/W.

b5 = **VSYN** - Set on falling edge of VSyncIn. Cleared by S/W.

b6 = **HSYN** - Same for HSync In (after HVSEL mux). Cleared by S/W.

b7 = **CSYN** - Set on falling edge of CSyncIn. Cleared by S/W.

Application Note:

DWNLAT and UPLAT may be used for HSYNC polarity detection and Composite
Sync detection.

CSYN/HSYN/VSYN may simplify the mode recognition and Power Management features.

HFLY/VFLY may be used for the DDC/Access Bus Self-Test command.

2FHLAT may be used to detect pre/post-equalization pulses or an excessively high Horizontal Frequency.

(POLR) POLARITY REGISTER (0043 h)

Read only 4 MSB bits
Read/Write 4 LSB bits
Reset Value: 0000 0000 (00 h)

7							0
----	0	VPOL	2FHDet	0	0	CLPINV	0

bit 0: **0** - Not used

bit 1: **CLPINV** - Programmable Clamp Out pulse polarity (0: Positive, 1: Negative)

bits 2,3: **0** - RESERVED

bit 4: **2FHDet** - Detection of Pre/Post equalization pulses (Read Only)
(HVGEN = 0, HACQ = 0)

bit 5: **VPOL** - Vertical sync polarity (Read Only) (0: Positive, 1: Negative)
VSYNC: [40..200] Hz, Pulse width [10..700] us

bit 6: **0** - RESERVED

bit 7: X - UNDEFINED

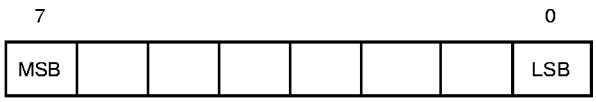
Application Note:

If the Vertical Sync polarity is changing, the VPOL bit should be updated after a typical delay of 4 msec.

SYNC PROCESSOR (Cont'd)

(HGENR) HORIZONTAL SYNC GENERATOR REGISTER (0045 h)

Read/Write
Reset Value: 0000 0000 (00 h)



Case HVGEN = 1: Generation mode

This register programs the H Sync generated frequency when HVGEN=1

The generated signal (Positive polarity) is as follows:
Pulse width: 2 us.
Period: (HGENR/4) us.
Note: HGENR value must be in [8..255] range.

Case HVGEN = 0: Acquisition/Correction Mode (HSYNCO/VSYNCO must be positive sync signals)

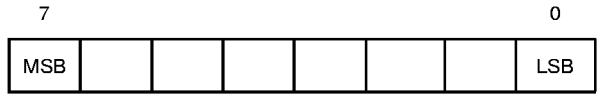
Sub-case HACQ = 1: Acquisition Mode
By setting HACQ bit by S/W the acquisition mode starts
When HACQ is cleared by H/W, HGENR returns the duration of HSYNCO low level. The acquisition should be done before the correction mode.

Sub-case HACQ = 0: Correction Mode
In this mode, the final HSYNCO signal on the pin can be corrected in order to detect and inhibit pre/post equalization pulses, etc... See dedicated control bits for more information

HGENR (hex value)	H Period (µs)	H Freq (KHz)	Pulse width (µs)	Duty Cycle
1F	8	125	2	25%
3F	16	62.5	2	12.5%
7F	32	31.25	2	6.2%
FF	64	15.6	2	3.1%

(VGENR) VERTICAL SYNC GENERATOR REGISTER (0046 h)

Read/Write
Reset Value: 0000 0000 (00 h)



Case HVGEN = 1: Generation mode

This register programs the V Sync Generated signal frequency (11 bit value)
Pulse width: 4 HGEN periods
Period: (HGENR*8) scan lines. VGENR value must be in [5..255] range.
This block works as an 11 bit Horizontal line counter (2047 scan lines per frame max)
Note that the 3 less significant bit are accessible in CFGR register. If you want to have a vertical period multiple of 8*HGENR, the 3 LSB (in CFGR) must be freeze to 000.

Case HVGEN = 0: Acquisition/Correction Mode (HSYNCO and VSYNCO must be positive sync signal)

Sub-case VACQ = 1: Acquisition Mode
By setting VACQ bit by S/W the acquisition mode starts
When VACQ is cleared by H/W, VGENR returns the number of scan lines during VSYNCO low level period

Sub-case VACQ = 0: Correction Mode
VSYNCO pulse width is extended of VGENR scan lines.
If VGENR = 0, all VSYNCO corrections are disabled.
(except 2FHEN test control bit)

HGENR (hex value)	HPeriod (µs)	H Freq (KHz)	VGENR (hex value)	V Period (ms)	V Freq (Hz)	Pulse width (µs)
1F	8	125	7FF (2047)	16.3	61	32
1F	8	125	400 (1024)	8.2	122	32
3F	16	62.5	7FF (2047)	32.6	30.6	64
3F	16	62.5	400 (1024)	16.4	60.9	64
7F	32	31.25	7FF (2047)	130.5	15	128
7F	32	31.25	400 (1024)	32.8	30	128

SYNC PROCESSOR (Cont'd)

(ENR) ENABLE REGISTER (0047 h)

Read/Write
Reset Value: 0000 0000 (00 h)

7							0
0	0	BLKEN	HVGEN	2FHEN	HINH	HSyncIn 1	VSyncIn 1

bit 0 = **VSYNCIN1** (Read Only): Returns the VSYNCIN1 pin level

bit 1 = **HSYNCIN1** (Read Only): Returns the HSYNCIN1 pin level

bit 2: **HINH** - HSYNCO Blanking

HINH	H SYNCO blanked by extracted VSYNCO
0	HSYNCO blanked
1	HSYNCO not blanked (=HSYNCI)

bit 3 = **2FHEN** - VSYNCO expansion (HVGEN=0, HACQ=0, VACQ=0)

2FHEN	VSYNCO Forced high when detection of 2FH pulses
0	Function disabled (Normal Application configuration)
1	Function enabled: VSYNCO = VSYNCO + 2FHDET

bit 4 = **HVGEN** enable the Sync Generation function)

HVGEN	Generation/Acquisition/Correction mode Selection
0	Acquisition/Correction Mode
1	H/V Sync Generation

bit 5 = **BLKEN** - Blanking Output Enable

BLKEN	Enable/Disable Video Blanking Signal Generation
0	Function disabled
1	Function enabled

bit 6..7: **0** - Reserved

Application Note: HSYNCIN1 and VSYNCIN1 may simplify the Power Management Algorithm.

After the ST7271 compatible Sync Processor Block, a new H/W cell has been pipelined in order to improve the functionality with optimized H/W. This block works in 3 different modes which are: Generation of Sync Signals, Analysis of the Sync Processor Output signals, and correction of sync signals if necessary.

Overview of generation/acquisition/correction H/W block functionality:

SYNC PROCESSOR (Cont'd)

Table 12. Summary of most important Sync Processor Modes

Sync Processor Mode	SYNOP	HVSEL	HVGEN	HACQ	VACQ
DSUB Selected as Inputs (HSYNCI1/VSYNCI1)	---	0	---	---	---
BNC Selected as Inputs (HSYNCI2/VSYNCI2)	---	1	---	---	---
Don't drive the monitor with any sync signals	0	---	---	---	---
Generate Sync Signals to drive the Monitor H/W	1	---	1	0	0
Use the Sync Processor to drive the monitor H/W by incoming sync signals	1	---	0	---	---
Analyse the number of Scan Lines during one vertical frame	---	--	0	---	1
Analyse the HSYNC delay between two pulses	---	---	0	1	---

Table 13. Sync Generator/Analyzer/Corrector H/W Block Description

Function	Applications
Sync Generation	Drive the monitor H/W when no or bad sync signals are received Allow stabilised OSD screen when monitor is unlocked Smooth frequency transitions Faster auto alignment system for Factory or Service Purpose
Sync Acquisition	Fast estimation of the incoming H Sync Input period Estimation of the number of scan lines per frame Simplify the OSD vertical centring algorithm
Sync Correction	Detection of pre/post equalisation pulses Detection of H SYNC reaches too high frequency Inhibition of Pre/Post equalisation pulses Programmable VSYNCO pulse width extension (PLL Inhibit) Possible VSYNCO extra pulse width extension during post-equalisation pulses detection up to XX lines) Possible generation of VSYNCO sync upon detection of high frequency H Sync Pulses Possible generation of missing H Sync Edge in composite sync

4.5 DIGITAL TO ANALOG CONVERTER

4.5.1 Introduction

The ST7272 offers two types of Digital to Analog Converter, with differing step resolutions based on the Pulse-Width Modulator (PWM) and Binary Rate Multiplier (BRM) Generator technique. These may act as digital potentiometers, when used with external, filtering to control brightness, saturation/contrast and other analog variables.

A 10-Bit PWM/BRM with a repetition rate of 64KHz, 250ns resolution and a step of 5mV (0/5V, excepting DA2). 16 channels are provided with this configuration (channels PWM2-PWM17 with outputs DA2-DA17 respectively). DA2 has a fixed open-drain output, with an external V_{DD} capability up to 12V, while DA3-DA17 are programmable to open-drain or push-pull output configuration, with a 0-V_{DD} (+5V) range.

A 12-bit PWM/BRM generator (2 Channels: PWM0 and PWM1) with a repetition rate of 64KHz, 250ns resolution and a step of 1.25mV (0/5V excepting DA0). The channels PWM0 and PWM1 correspond with outputs DA0 and DA1 respectively. DA0 has a fixed open-drain output, with an external V_{DD} capability up to 12V, while DA1 is programmable to open-drain or push-pull output configuration, with a 0-V_{DD} (+5V) range.

4.5.2 Functional Description

4.5.2.1 10-bit PWM/BRM

The 10-Bits of the 10 bit PWM/BRM are distributed as 6 PWM bits and 4 BRM bits. The generator consists of a 10-bit counter (common for all channels), a comparator and the PWM/BRM generation logic.

PWM Generation

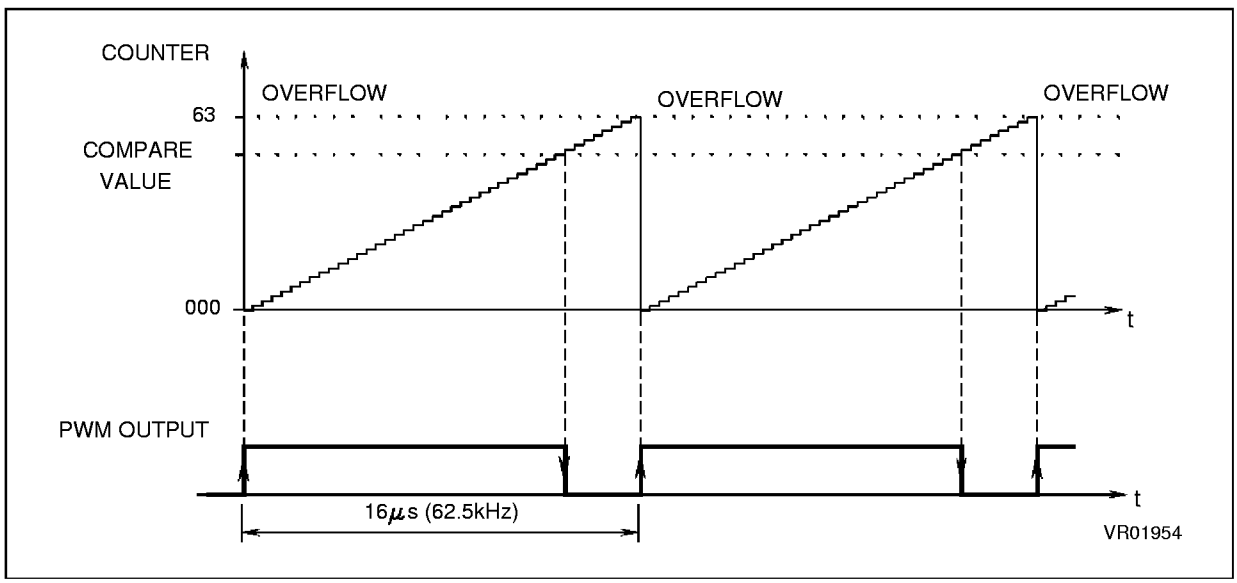
The counter increments continuously, clocked at the main oscillator frequency divided by 2 (with a period $t_{CLK} = 1/f_{CLK} = 250ns$). Whenever the 6 least significant bits of the counter (defined as the PWM counter) overflow, the output level for all active channels is set.

The state of the PWM counter is continuously compared to the PWM binary weight for each channel, as defined in the relevant PWM register, and when a match occurs the output level for that channel is reset.

This Pulse Width modulated signal must be filtered, using an external RC network placed as close as possible to the associated pin. This provides an analog voltage proportional to the average charge passed to the external capacitor. Thus for a higher mark/space ratio (High time much greater than Low time) the average output voltage is higher. The external components of the RC network should be selected for the filtering level required for control of the system variable.

Each output may individually have its polarity inverted by software, and can also be used as a logical output.

Figure 27. PWM Generation



DIGITAL TO ANALOG CONVERTER (Cont'd)

Figure 28. Typical PWM Output Filter

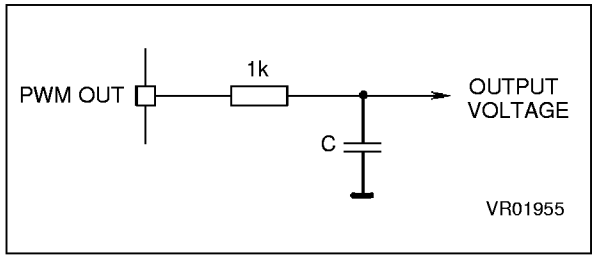
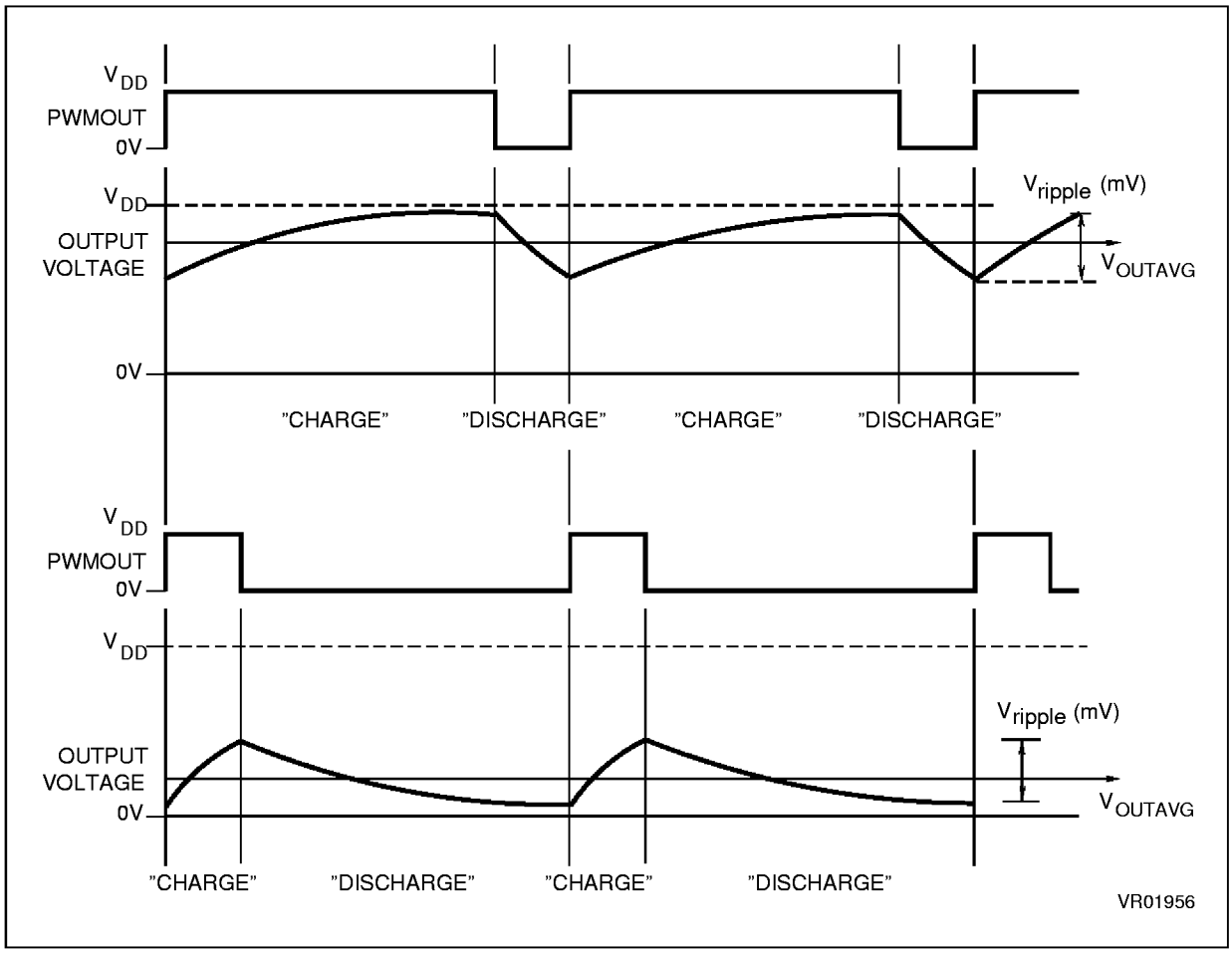


Table 14. 6-Bit PWM Ripple After Filtering

C (mF)	V RIPPLE (mV)	t (ms)
0.256	78	0.256
2.56	7.8	2.56
25.6	0.78	25.6

Assuming RC filter (R=1kW) and V_{DD} = 5V
PWM Duty Cycle 50%
Step = 5V/64 = 78mV which requires a minimum T (filter time constant) of 250ns x 64 x 64 / 4 = 256 µS to ensure integral linearity of+ / _0.5 LSB.

Figure 29. PWM Simplified Voltage Output After Filtering



DIGITAL TO ANALOG CONVERTER (Cont'd)

BRM Generation

The BRM bits allow the addition of a 250ns-pulse to widen a standard PWM pulse for specific PWM cycles. This has the effect of "fine-tuning" the PWM Duty cycle (without modifying the base duty cycle), thus, with the external filtering, providing additional fine voltage steps.

The incremental pulses (with duration of t_{CLK} = $1/f_{CLK}$ = 250ns) are added to the beginning of the original PWM pulse. The PWM intervals which are added to are specified in the 4-bit BRM register and are encoded as shown in the following table. The BRM values shown may be combined together to provide a summation of the incremental pulse intervals specified.

The pulse increment corresponds to the PWM resolution. For example, if data 18h is written to the PWM register and data 06h (00000110b) to the BRM register, for a 4 MHz internal clock (250ns resolution), a 6.0 ms-long pulse will be output at 64ms intervals, except for cycles numbered #2,4,6,10,12,14, where the pulse is broadened to 6.25ms.

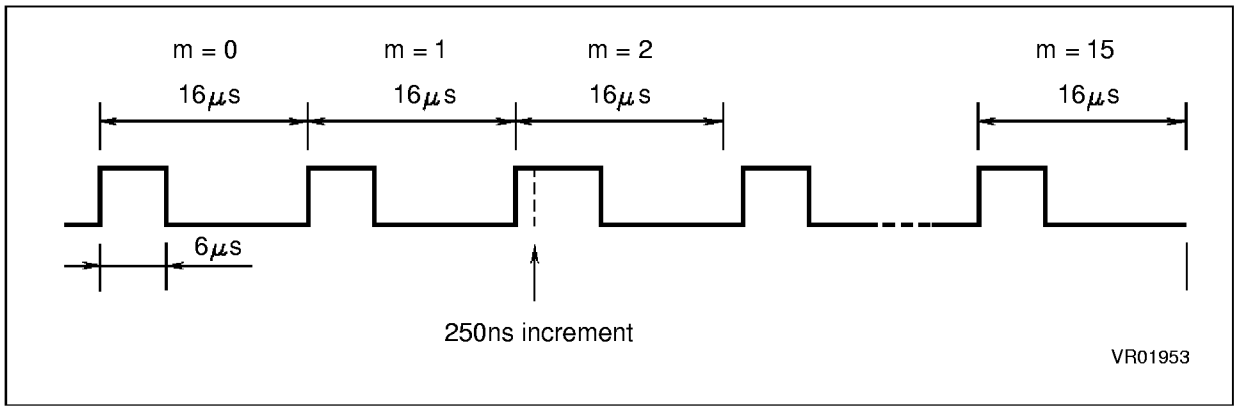
Note. If 00h is written to both PWM and BRM registers, the generator output will remain at "0". Conversely, if both registers hold data 3Fh and 0Fh, respectively, the output will remain at "1" for all intervals #1 i #15, but it will return to zero at interval #0 for an amount of time corresponding to the PWM resolution (250ns).

An output can be set to a continuous "1" level by clearing the PWM and BRM values and setting POL = "1" (inverted polarity) in the PWM register. This allows a PWM/BRM channel to be used as an additional I/O pin if the DAC function is not required.

Table 15. Bit BRM Added Pulse Intervals (interval #0 not selected).

BRM 4 - Bit Data	Incremental Pulse Intervals
0000	none
0001	i = 8
0010	i = 4,12
0100	i = 2,6,10,14
1000	i = 1,3,5,7,9,11,13,15

Figure 30. BRM pulse addition (PWM > 0)



DIGITAL TO ANALOG CONVERTER (Cont'd)

Figure 31. Simplified Filtered Voltage Output Schematic with BRM added

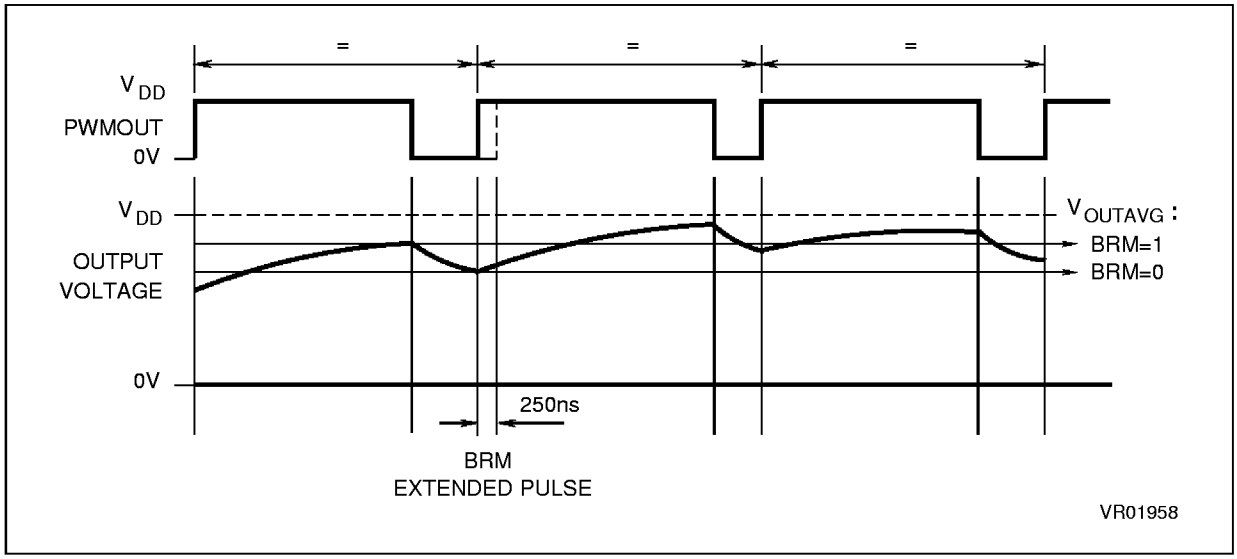
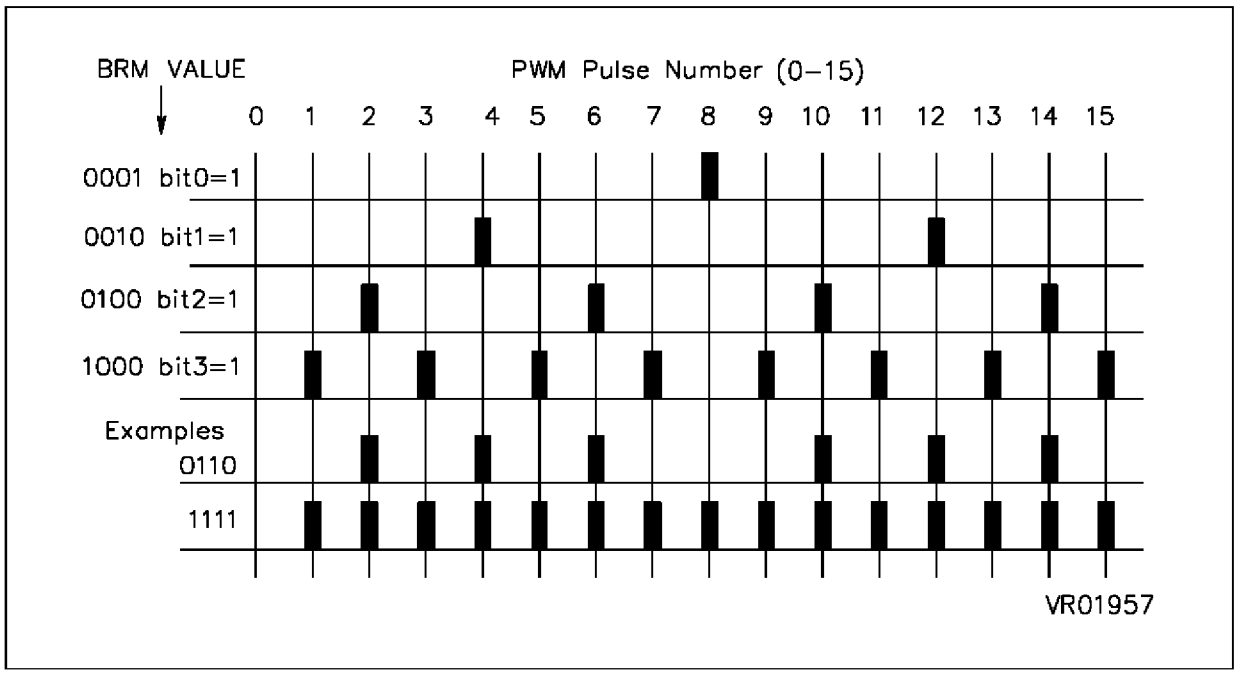


Figure 32. Graphical Representation of 4-Bit BRM added pulse Positions



DIGITAL TO ANALOG CONVERTER (Cont'd)

4.5.2.2 12-Bit PWM/BRM

The 12 Bits of the two channels of the 12-bit PWM/BRM generator are distributed as 6 PWM bits and 6 BRM bits. The two 12-bit channels correspond to PWM0 and PWM1, and outputs DA0 and DA1 respectively.

PWM Generation

The functionality of the PWM generation is equivalent to the PWM generation of the 10-bit PWM/BRM described in the previous paragraph and so will not be repeated here. Please refer to the previous paragraph for functionality, to be used in conjunction with the following Register description.

BRM Generation

A 6-bit BRM register defining the intervals where an incremental pulse (with duration of t_{CLK} = $1/f_{CLK}$=250ns) is added to the beginning of the original PWM pulse.

BRM 6 - Bit Data	Incremental Pulse Intervals
000000	none
000001	i = 32
000010	i = 16,48
000100	i = 8,24,40,56
001000	i = 4,12,20,28,36,44.52,60
010000	i = 2,6,10,...50,54,58,62
100000	i = 1,3,5,7,9,...55,59,61,63

4.5.3 Register Description

4.5.3.1 10-bit PWM/BRM REGISTERS

On a channel basis, the 10 bits are separated into two data registers:

A 6-bit PWM register corresponding to the binary weight of the PWM pulse.

A 4-bit BRM register defining the intervals where an incremental pulse is added to the beginning of the original PWM pulse. Two BRM channel values share the same register.

(PWM 2:17) PULSE BINARY WEIGHT REGISTER (see register map)

Read / Write
Reset Value 1000 0000 (80 h)

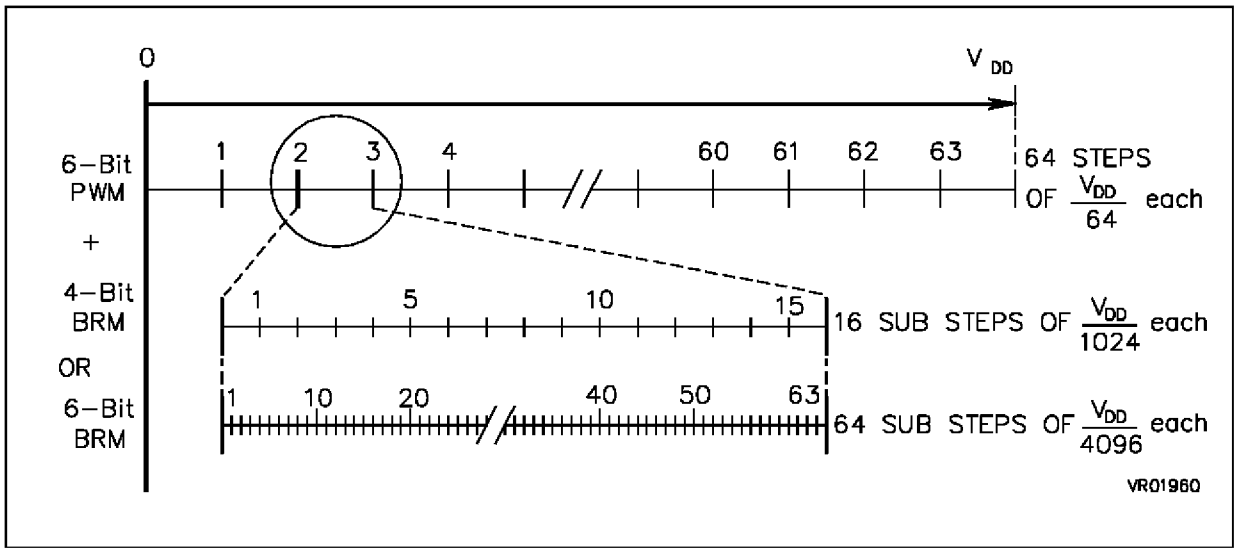
7							0
1	POL	P5	P4	P3	P2	P1	P0

b7 = **Reserved** (read as a "1")

b6 = **POL** Polarity Bit. When POL is set, output signal polarity is inverse; otherwise, no change occurs.

b5-0 = **P5-P0** PWM Pulse Binary Weight for channel i

Figure 33. Precision for PWM/BRM Tuning for VOUTEFF (After filtering)



DIGITAL TO ANALOG CONVERTER (Cont'd)

(BRM 2:17) BRM REGISTER (see register map)

Read / Write
Reset Value: 0000 0000 (00 h)

7							0
B7	B6	B5	B4	B3	B2	B1	B0

b7-4 = **B7-B4** BRM Bits (channel i+1)

b3-0 = **B3-B0** BRM Bits (channel i)

12-bit PWM/BRM REGISTERS

For each of the two channels, the 12 bits are separated into two data registers:

A 6-bit PWM register corresponding to the binary weight of the PWM pulse.

A 6-bit BRM register defining the intervals where incremental pulses are added to the beginning of the original PWM pulse.

(PWM 0:1) PULSE BINARY WEIGHT REGISTER (see register map)

Read / Write
Reset Value: 1000 0000 (80 h)

7							0
1	POL	P5	P4	P3	P2	P1	P0

b7 = **Reserved** (read as a "1")

b6 = **POL** Polarity Bit. When POL is set, output signal polarity is inverse; otherwise, no change occurs.

b5-0 = **P5-P0** PWM Pulse Binary Weight for channel i

(BWM 0:1) BRM REGISTER

Register BRMi, i=0,1
Reset Value: 1100 0000 (00 h)

7							0
1	1	B5	B4	B3	B2	B1	B0

b7-6 = **Unused**

b5-0 = **B5-B0** BRM Bits (channel i)

Note: From the programmer's point of view, the PWM and BRM registers can be regarded as being combined to give one data value.

PWM/BRM OUTPUTS

The PWM/BRM outputs are assigned to the following pins (unless otherwise stated, they are 10-Bit PWM/BRM, push-pull/open-drain output (0-V_{DD}) configuration):

PWM/BRM	Pin	PWM/BRM	Pin
0 (1.2)	DA.0	9	DA.9
0 (1)	DA.1	10	DA.10
2 (2)	DA.2	11	DA.11
3	DA.3	12	DA.12
4	DA.4	13	DA.13
5	DA.5	14	DA.14
6	DA.6	15	DA.15
7	DA.7	16	DA.16
8	DA.8	17	DA.17

For example

0	Pol	P	P	P	P	P	P	+	B	B	B	B

Effective (with external RC filtering) DAC value

0	Pol	P	P	P	P	P	P	B	B	B	B

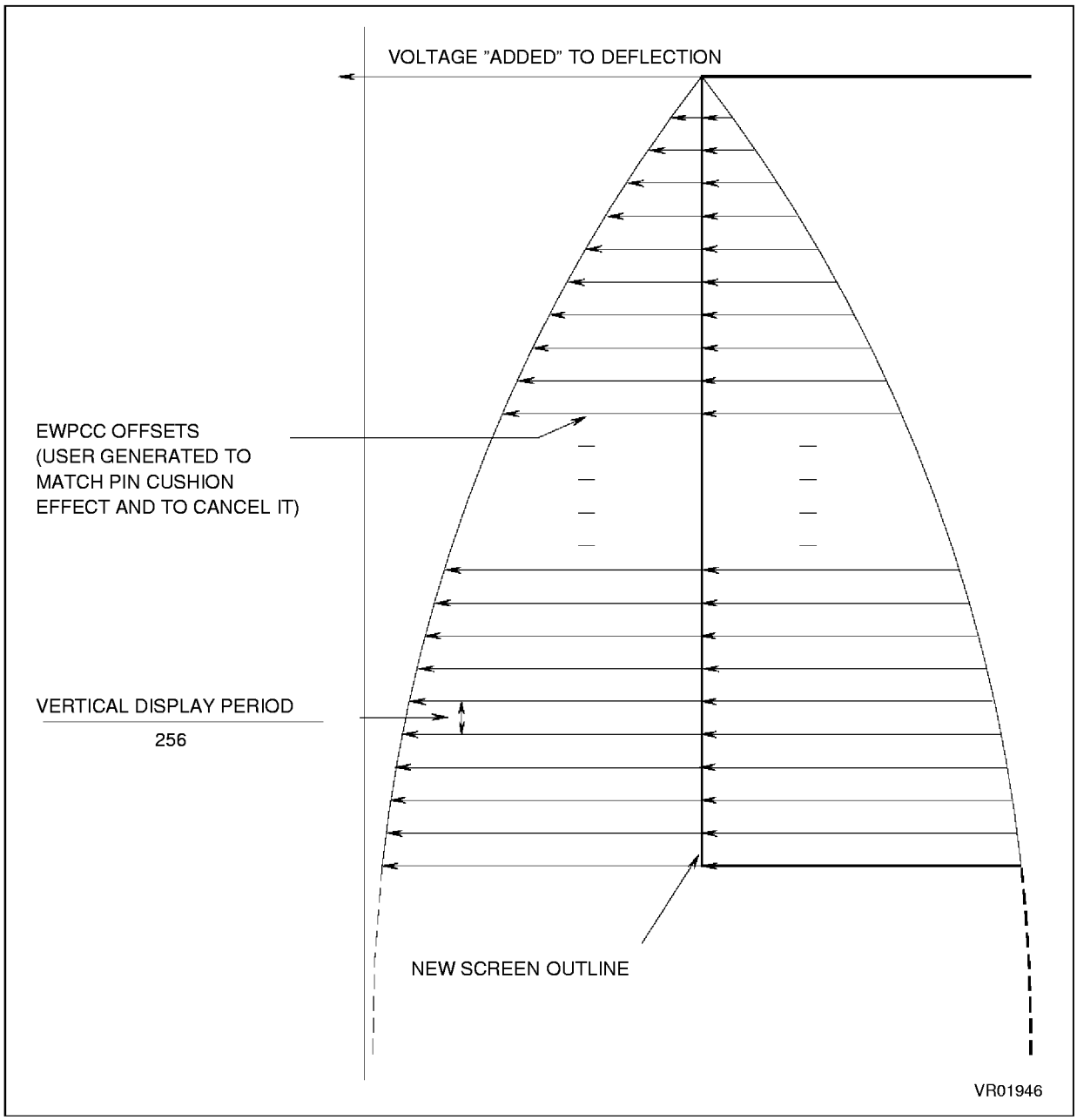
4.6 EAST-WEST PIN CUSHION CORRECTION

4.6.1 Introduction

The function of the East-West Pin Cushion Correction circuit (EWPCC) is to correct the horizontal synchronization timing signals to compensate for pin-cushion distortion on the display screen, normally caused by the magnetic display components.The EWPCC operates by storing, during monitor manufacrture, 256 coefficients related to the pin-cushion effect in a dedicated memory (EEPROM) and then implementing real-time correction by sending the stored coefficients out through the dedicated D/A Converter (DAC). The analog output is added (off-chip) to the deflection voltage that determines the starting point for the next line on the screen.

These coefficients are uniformly distributed over the effective vertical refresh field of the screen.

Figure 34. EWPC Coefficient Working on Pin-Cushion



EWPCC (Cont'd)

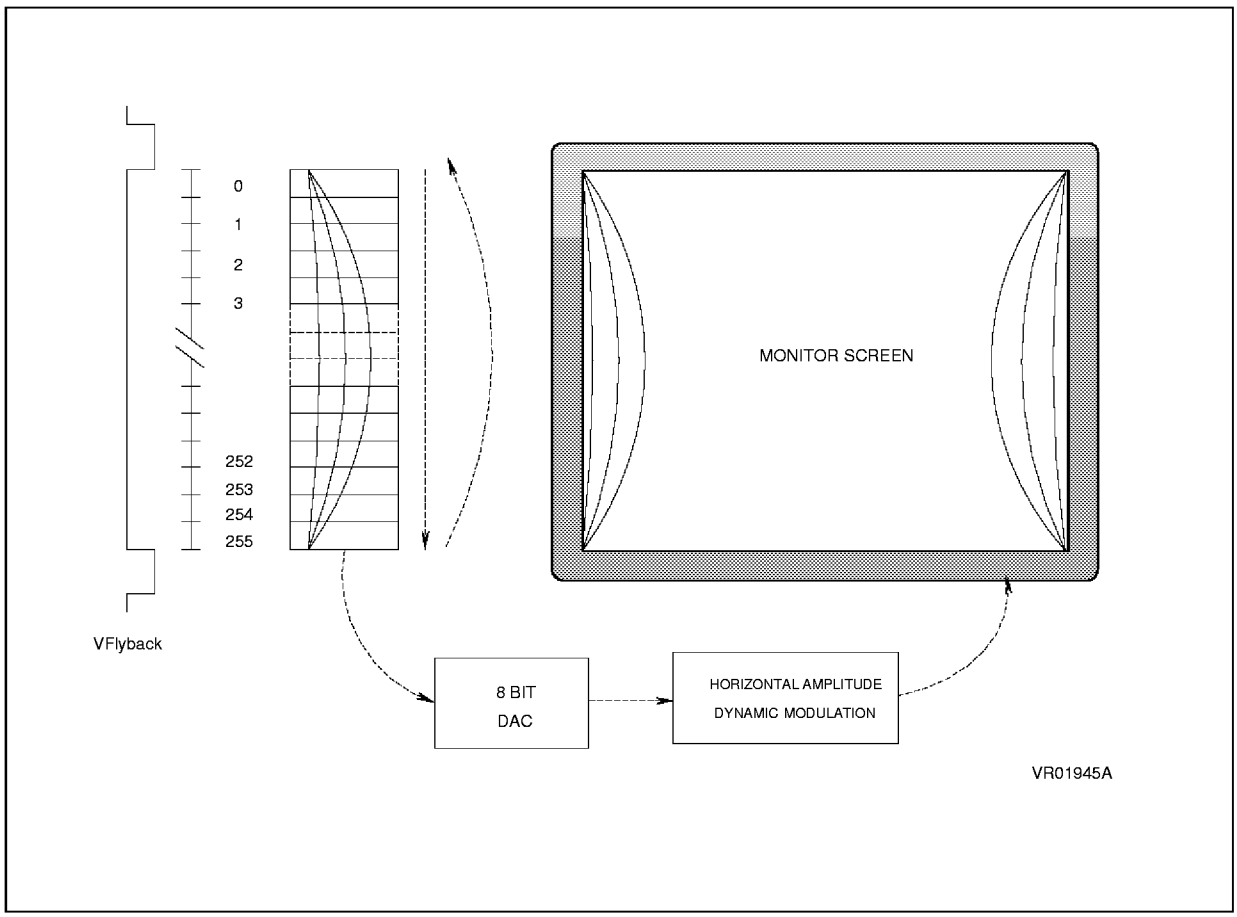
4.6.2 Functional Description

The EWPCC output is based on the signal present on the VFBACK input pin. The input signal is required to be asserted during the Vertical Fly-Back period (with a fixed positive polarity assumed).

Warning: when the EWPCC is used, this I/O pin must be set to input mode; if the EWPCC is not used, the pin is available for normal I/O functions.

For correct operation the MCU internal clock frequency must be 1024 times greater than the fly-back frequency.

Figure 35. EWPC Effective Action



EWPCC (Cont'd)

In normal operation (after initialization), the EWPCC EEPROM is sequentially scanned by the address generator during the time interval that VFBACK is negated, that is during the active vertical display period. When VFBACK is asserted (flyback period) the address generator is reset, so that the address points to the first EEPROM position and the DAC register is loaded with the first coefficient.

The address generator consists of a 17-bit processor (8-bit up-counter + 9-bit up/down-counter), data/control registers and logic to minimize rounding-up effect.

Figure 36. VFBACK Input Timing

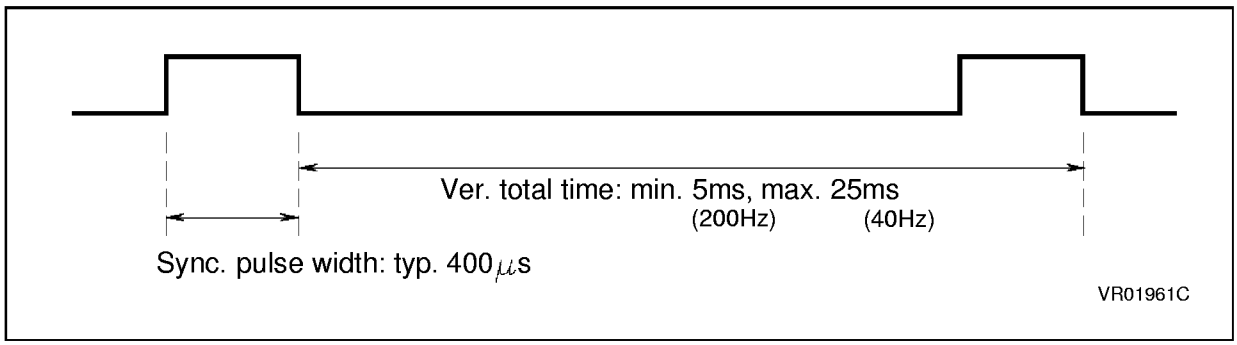
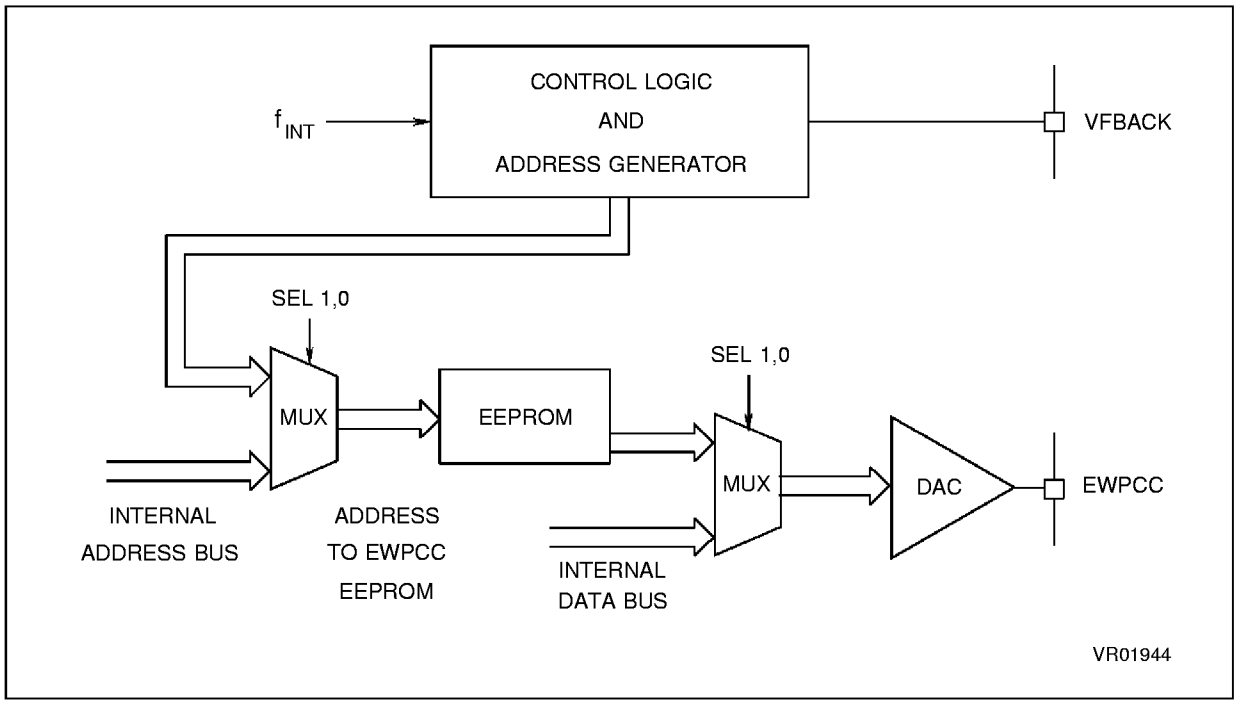


Figure 37. EWPCC Block Diagram



EWPCC (Cont'd)

When the EWPCC function is disabled (SEL1,0 = [0,0]), the CPU may fill the EEPROM memory with the EWPCC coefficients calculated or measured during production test or transferred from a preset table within memory.

In normal operation, when enabled, 256 analog levels on the EWPCC output (DAC analog output) are generated in evenly-spaced time/space intervals during the time that VFBACK is negated.

To do so, the EWPCC performs two operating modes that are automatically chained once the sequence is triggered by writing a "1" to the INI control bit in the EWPCC1 register:

a) Acquisition Mode:

The output of the 8-bit prescaler, fed by the CPU clock (f_{CPU}), is counted up by a 9-bit counter during the time that VFback is negated. The rising edge of VFback captures the 9-bit counter value and the 8-bit prescaler MSB into the data registers, as follows:

8-Bit Prescaler MSB ->> EWPCC0.0

9-Bit Counter 7 LSB's ->> EWPCC0.7,1

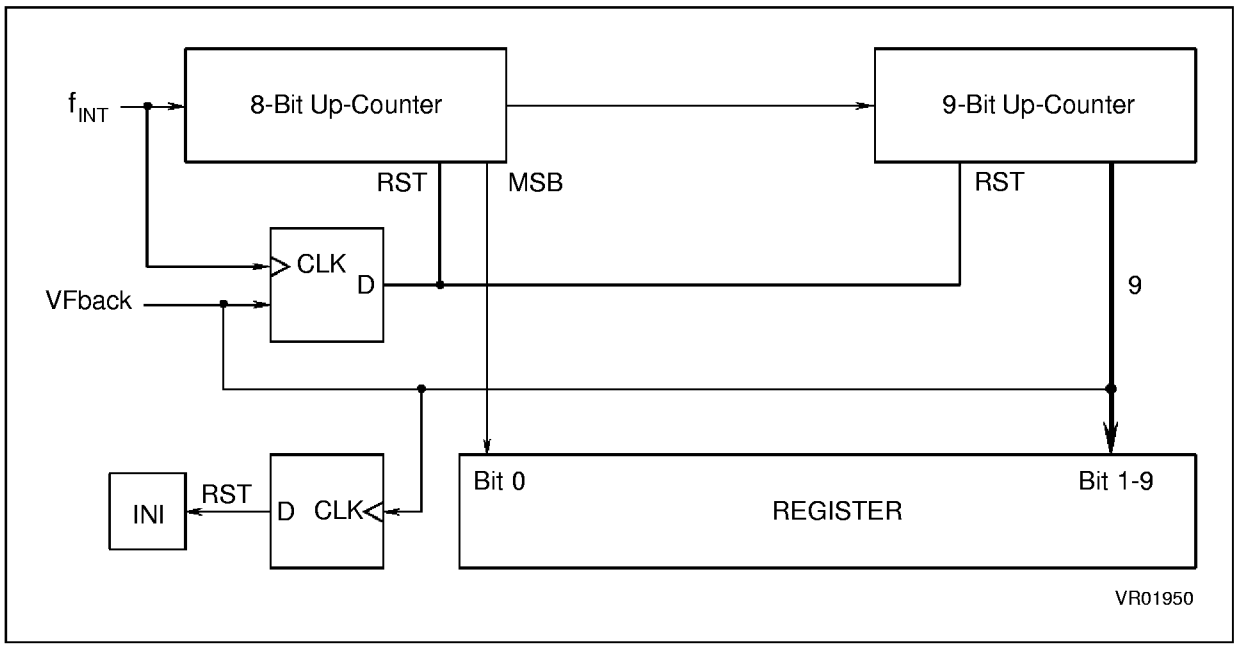
9-Bit Counter 2 MSB's ->> EWPCC1.1,0

Thus the 9-bit counter contains a value proportional to the duration of the "VFback low" condition. Since the lower 7 bits of the prescaler are not passed through to the next stage, there is an effective division by 256, thus the value in the counter may be considered as the number of f_{INT} cycles required to give the time of the complete non-retrace period equally divided by 256.

The counter and the INI control bit (EWPCC1,2) are then automatically reset and the hardware is switched to the address generation mode.

In order to minimize the truncation effect on the captured value accuracy, the overall 17-bit counter (8-bit prescaler + 9-bit counter) is preset to 00040h during assertion of VFBACK.

Figure 38. Acquisition Mode Block Diagram



EWPCC (Cont'd)

Figure 39. Acquisition Mode Timing

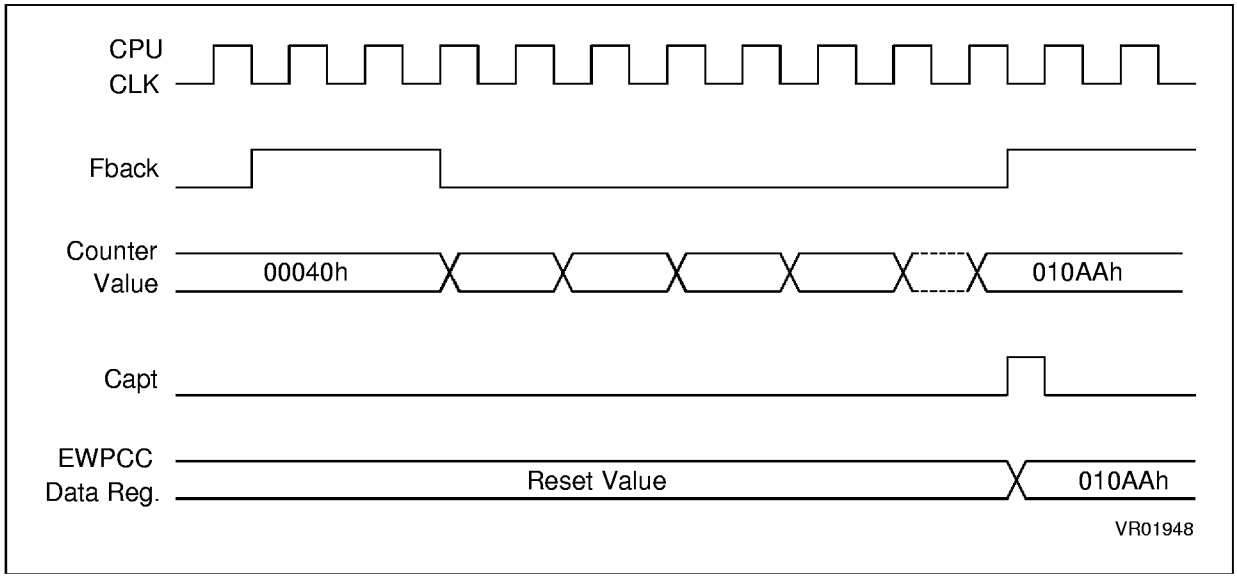
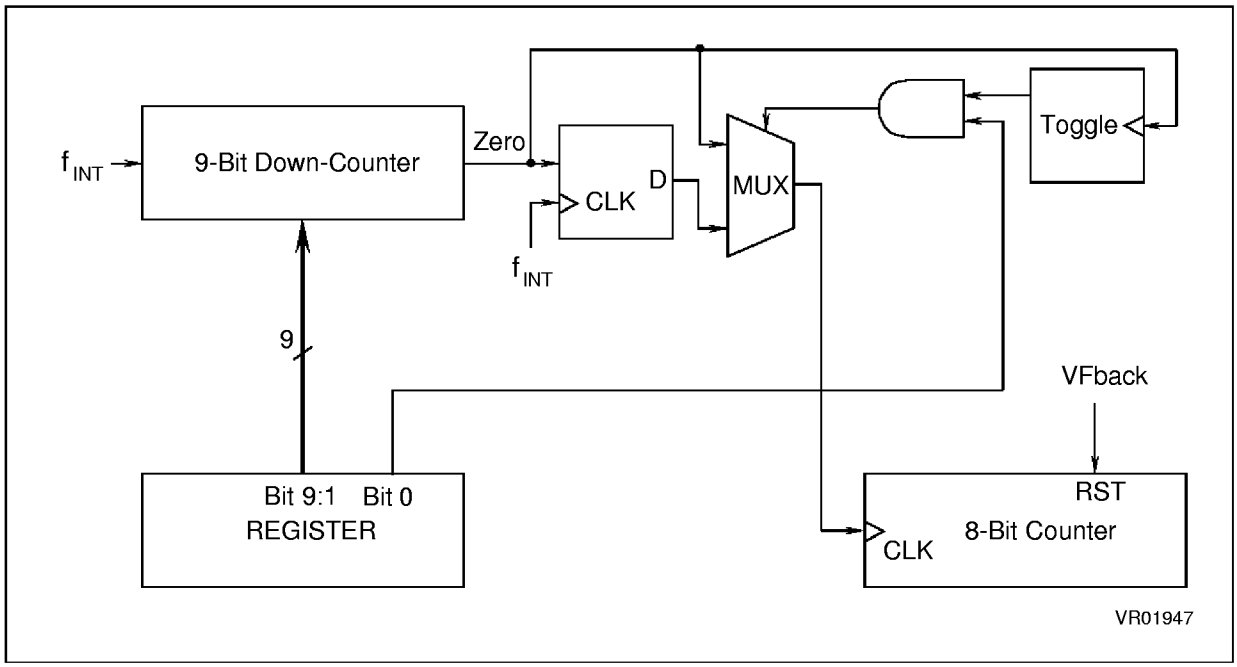


Figure 40. Address Generation Mode Block Diagram



EWPCC (Cont'd)

Figure 41. Address Clock Generation Mode (Division by N)

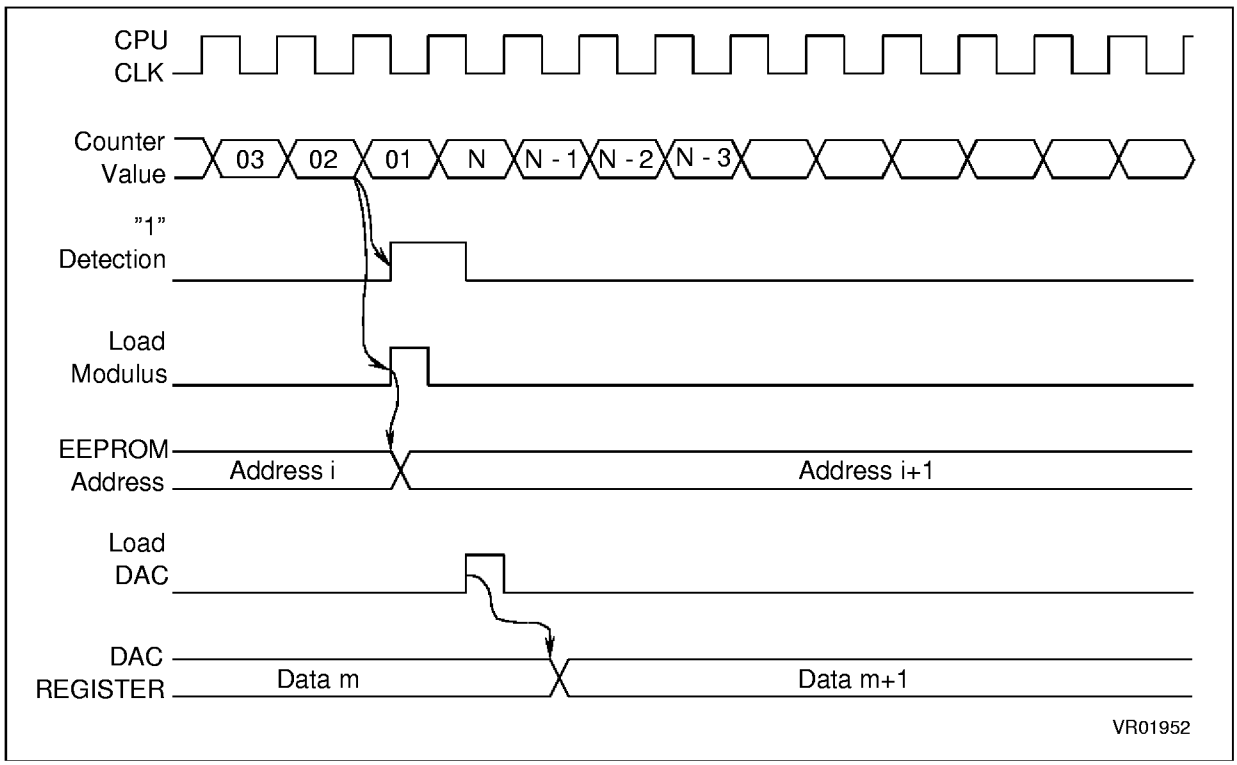
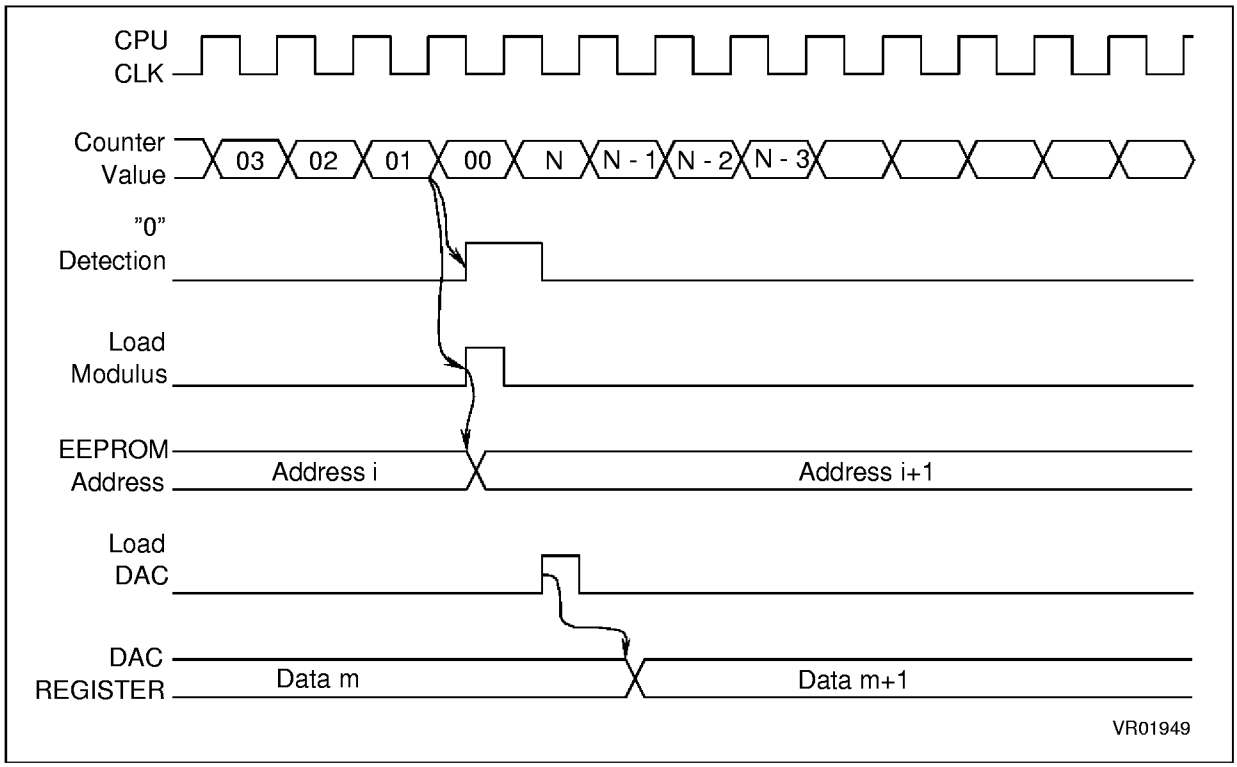


Figure 42. Address Clock Generation Mode (Division by N + 1)



EWPCC (Cont'd)

b) Address Generation Mode:

Once the acquisition phase is complete, addresses are continuously issued to the EEPROM. The 17-bit processor is reconfigured as:

– A 9-bit modulus (divide-by-N/N+1) down-counter, clocked by the CPU clock (f_{INT}), and reloaded on zero detection with the value captured in the acquisition mode.

– An 8-bit up-counter, clocked by zero detection in the 9-bit counter, which generates the EEPROM addresses.

The division ratio N corresponds to the 9 MSB's of the value captured in the acquisition mode (EWPCC1,0 + EWPCC07,1) which is equivalent to the original number of f_{INT} cycles to achieve the display time of VFBACK low divided by 256. The effect of this is then to divide the VFBACK time evenly by 256 and to increment the address to the EEPROM at each interval.

The choice of N or N+1 is controlled by EWPCC0.0. If this bit is "0", the counter modulus is always N, otherwise an extra step is introduced into the counter to give N+1 and the counter divides by N and N+1 alternately. This algorithm performs a division by (N + 0.5).

Note. After reset, the EWPCC function is disabled and the INI bit is cleared. By writing SEL1,0 = [1,1] and INI=1, the EWPCC function is enabled and the acquisition mode starts.

4.6.2.1 EWPCC Operation Modes

The EEPROM content addressed by the address counter is loaded into the Digital to Analog converter (DAC) 8-bit data register through a multiplexer and then sent to the D/A Converter. The other input to the multiplexer is the internal Data Bus.
This architecture allows the user the alternative of different configurations, selected by the control bits SEL1, 0.

- SEL1, 0 = [1,1]:

EWPCC Function Enabled (Normal Operation): EEPROM is addressed by the EWPCC Address Sequencer and its values directly sent to the DAC register through a dedicated bus.

- SEL1,0 = [0,1]:

EWPCC Function Disabled and Direct Loading (by a Single Instruction) to the DAC Register from the EEPROM through the dedicated bus. This direct transfer is synchronized with a dummy read instruction of the EEPROM with the addresses generated by the CPU. In this dummy operation, EEPROM data is not loaded onto the main data bus, but can be accessed by reading the DAC register.

- SEL1,0 = [0,0]

EWPCC Function Disabled. EEPROM and DAC in Stand-Alone Mode.

Whenever the dedicated path between the EEPROM and the Digital to Analog Converter is enabled, after accessing the EEPROM, the byte read is sent to the DAC data register. If the DAC is configured as stand-alone, its data register is directly loaded by the CPU through the internal data bus.

The architecture of the EWPCC circuit also gives the user the possibility (if necessary) of adjusting by software the captured value on the generation mode by writing into the EWPCC registers the new modulus that will be transferred to the counter upon the following underflow condition.

The EWPCC function may also be used for the generation of other waveforms by suitable programming of the EWPCC EEPROM.

Tolerance

The truncation error on the acquired value corresponds to -0.25 < Error < 0.25 (with the algorithm used) which can be related to a maximum shift of 32ms on the vertical axis of the screen, at the 256th address (or a maximum 16ms at the 128th) with respect to the ideal case of zero truncation error when generating evenly-spaced intervals by dividing the time interval in which VFBACK is negated by 256.

EWPCC (Cont'd)

4.6.3 Register Description

(PCC0) EAST-WEST CONTROL REGISTER (000C h)

Read/Write
Reset Value: 0000 0000 (00h)

7							0
M7	M6	M5	M4	M3	M2	M1	M0

b7-1 = **M7-M1**: 9-Bit Counter 7 LSBs. These bits correspond to the 7 least-significant bits of the captured value from the 9-bit counter when in acquisition mode.

b0 = **M0:** 8-Bit Prescaler MSB. This bit corresponds to the most significant bit of the 8-bit prescaler, captured during acquisition mode.

(PCC1) EAST-WEST CONTROL REGISTER (000D h)

Read / Write
Reset Value: 1100 0000 (C0 h)

7							0
1	1	0	SEL1	SEL0	INI	M1	M0

b7-6 = **Reserved (**read as "1")

b5 = **Reserved** MUST BE PROGRAMMED AS "0"

b4-3 = **SEL1,SEL0:** Mode Selection Bits. These read/write bits allow selection of configuration, as follows:

SEL1	SEL0	
0	0	EWPCC Function Disabled EEPROM and DAC Stand Alone
0	1	EWPCC Function Disabled EEPROM addressed by CPU and its data sent directly to
1	0	Reserved
1	1	EWPCC Function Enabled EEPROM addressed by EWPCC block Data sent to DAC Register

b2 = **INI:** Acquisition Mode Initialization/Status Bit. Writing a "1" to INI triggers the acquisition mode, after detection of VFback rising edge. During this mode, INI is read as a "1". Once acquisition is completed, this bit is cleared by hardware and address generation mode is chained.

b1-0 = **M1-M0:** 9-bit Counter Value MSB's. These bits correspond to the two most-significant bits of the captured value from the 9-bit counter on acquisition mode.

Notes. When EWPCC mode is selected (SEL1,0 = [1,1]), any writing operation into the EEPROM control register is blocked by hardware.

– When SEL0 = "1", the EEPROM value is not transferred onto the databus.

– During acquisition mode, re-writing the INI control/status bit as "1" will not have any effect - the acquisition procedure already in progress will not be reset.

(DACR) EWPCC DAC REGISTER (000B h)

Read/Write
Reset Value: 0000 0000 (00h)

7							0
D7	D6	D5	D4	D3	D2	D1	D0

b7-0 = **D7-D0:** DAC Input Binary Byte. This byte corresponds to the binary value to be converted onto an analog signal.

(CR3) EWPCC EEPROM CONTROL REGISTER (0011 h)

This register contains the bits required to read, erase and program the EWPCC EEPROM.

Please refer to the EEPROM chapter for details on using this register and for programming the EWPCC EEPROM.

4.7 A/D CONVERTER (ADC)

4.7.1 Introduction

The Analog to Digital converter is a single 8-bit successive approximation converter. Analog voltages from external sources are input to the converter through up to 6 pins (PB0 to PB7). The result of the conversion is stored in the 8-bit Result Data Register. The A/D converter is controlled through the A/D Converter Control/Status Register.

4.7.2 Functional Description

The A/D converter is enabled by setting the A/D Converter ON bit (ADON) of the A/D Converter Control/Status Register. A delay time is then required for the converter to stabilize (see characterization section).

When the A/D function is active, pins PB0 to PB7 can be used as analog inputs. The inputs must first be enabled for analog input by setting the corresponding bit(s) of the Port B Configuration Register as described in the Section on I/O Ports. Bits CH2 to CH0 of the A/D Converter Control/Status Register then select the channel to be converted. The high and low level reference voltages are connected to pins V_{DD} and V_{SS}.

When enabled, the A/D converter performs a continuous conversion of the selected channel. When a conversion is completed (16 µs for f_{CPU} = 4 MHz), the result is loaded into the read only Result Data Register and the COCO (Conversion Complete) flag is set. No interrupt is generated. Any write to the A/D Converter Control/Status Register aborts the current conversion, resets the COCO flag and starts a new conversion.

The A/D converter is ratiometric. An input voltage equal to, or greater than V_{DD}, converts to FFh (full scale) without overflow indication if greater. An input voltage equal to, or lower than V_{SS} converts to 00h. The conversion is monotonic: the results never decrease if the analog input does not and never increase if the analog input does not. Each step of conversion is equal to V_{DD} divided by 256: thus the conversion result is expressed as 8 bits, with a maximum error corresponding to three conversion steps.

Using a pin, or pins, as analog inputs does not affect the ability to read port B as logic inputs.

The minimal conversion time is 32 ADC clock cycles (16us if A/D clock frequency at 2 MHz). The A/D converter clock is generated from the CPU clock divided by 2.

The A/D converter can be disabled by resetting the ADON bit. This feature allows the reduction of power consumption when no conversion is in progress. The A/D converter is disabled after Power-On and external resets.

The A/D converter is not affected by WAIT mode but, in power sensitive applications, it can be switched off before entering this mode. When the MCU enters the HALT mode with the A/D converter enabled, the A/D clocks are stopped and the converter is disabled until the HALT mode is exited and the start-up delay has elapsed. A stabilisation time is also required before accurate conversions can be performed.

The converter uses the power supply lines as voltage refernces, consequently conversion accuracy may be degraded by voltage drops in the event of heavily loaded power supply lines.

A/D CONVERTER (Cont'd)

4.7.3 Register Description

A/D CONTROL/STATUS REGISTER (CSR)

Address: 0071h — Read/Write

Reset condition: 00 h

7							0
COCO	0	ADON	-	0	CH2	CH1	CH0

Bit-7: **COCO** *Conversion Complete.* COCO is set as soon as a new conversion can be read from the Result Data Register. COCO is cleared by reading the result or writing to the A/D Converter Control/Status Register.

Bit-6: **Reserved,** must be programmed to 0

Bit-5: **ADON** *A/D converter On.* ADON allows the A/D converter to be switched on and off in order to reduce consumption when needed. When turned on (ADON = 1), a delay time (typically 10us) is necessary for the current to stabilize. Conversions can be inaccurate during this time.

Bit-4: **Not used**

Bit-3: **Reserved,** must be programmed to 0

Bits 2-0: **CH2-CH0** *Channel Selection*

These bits select the analog input to convert.

CH2-CH0	Pin	Channel
000	PC0	AIN0
001	PC1	AIN1
010	PC2	AIN2
011	PC3	AIN3
100	PC4	AIN4
101	PC5	AIN5

A/D DATA REGISTER (DR)

Address: 0070h — Read Only

Reset condition: (undefined)

7							0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Bits 7-0: **AD7-AD0** *Analog Converted Value.*

4.8 DDC BUS INTERFACE (DDC)

4.8.1 Introduction

The DDC Bus Interface is an extension of the I²C Bus Interface. In addition to the Multiple Master/Slave I²C DDC2A modes, both DDC1 and DDC2B modes can be handled. Thanks to the presence of a Direct Memory Access channel, the interface can transfer data bytes with the minimum CPU overhead at all DDC levels.

4.8.1.1 DDC Features:

– I²C, DDC1 and DDC2B modes.
– Programmable automatic switchover from DDC1 to I²C mode.
– DMA transfer/1 byte transfer.
– Interrupt generation for error conditions.
– Interrupt generation for transfer request.

4.8.1.2 I²C Features:

– Parallel-bus to I²C protocol conversion.
– Multi-master capability.
– 7-bit Addressing.
– Transmitter/Receiver flag.
– End of Byte transmission flag.

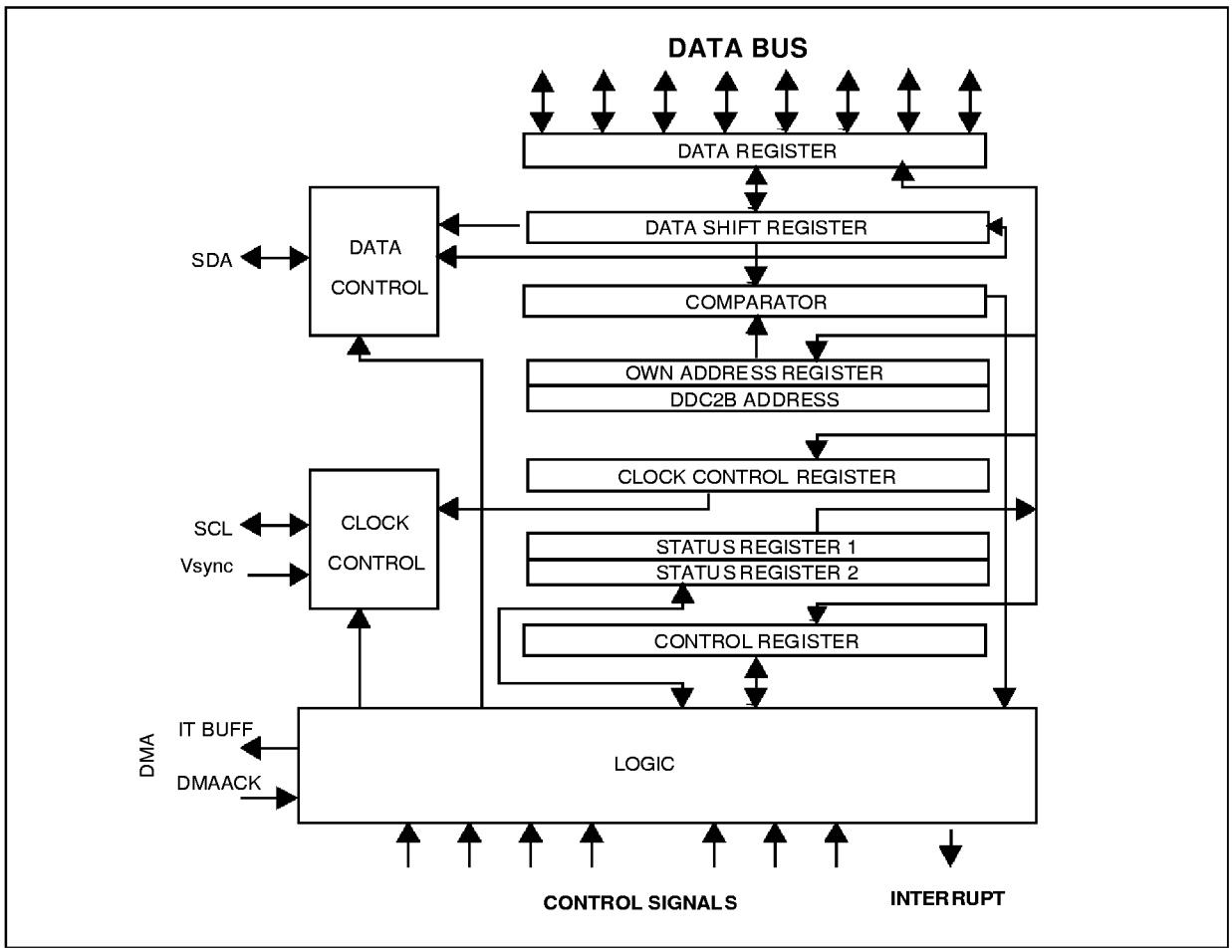
4.8.1.3 I²C Master Features:

– Clock generation
– Flag indicating when the I²C bus is in use
– Flag indicating the loss of arbitration

4.8.1.4 I²C Slave Features:

– Start bit detection flag
– Detection of a misplaced Start or Stop condition
– Detection of a problem during the transfer
– I²C Address Matched detection
– DDC2B Address Matched Detection

Figure 43. I²C Block Diagram



DDC BUS INTERFACE (Cont'd)

4.8.2 Functional Description

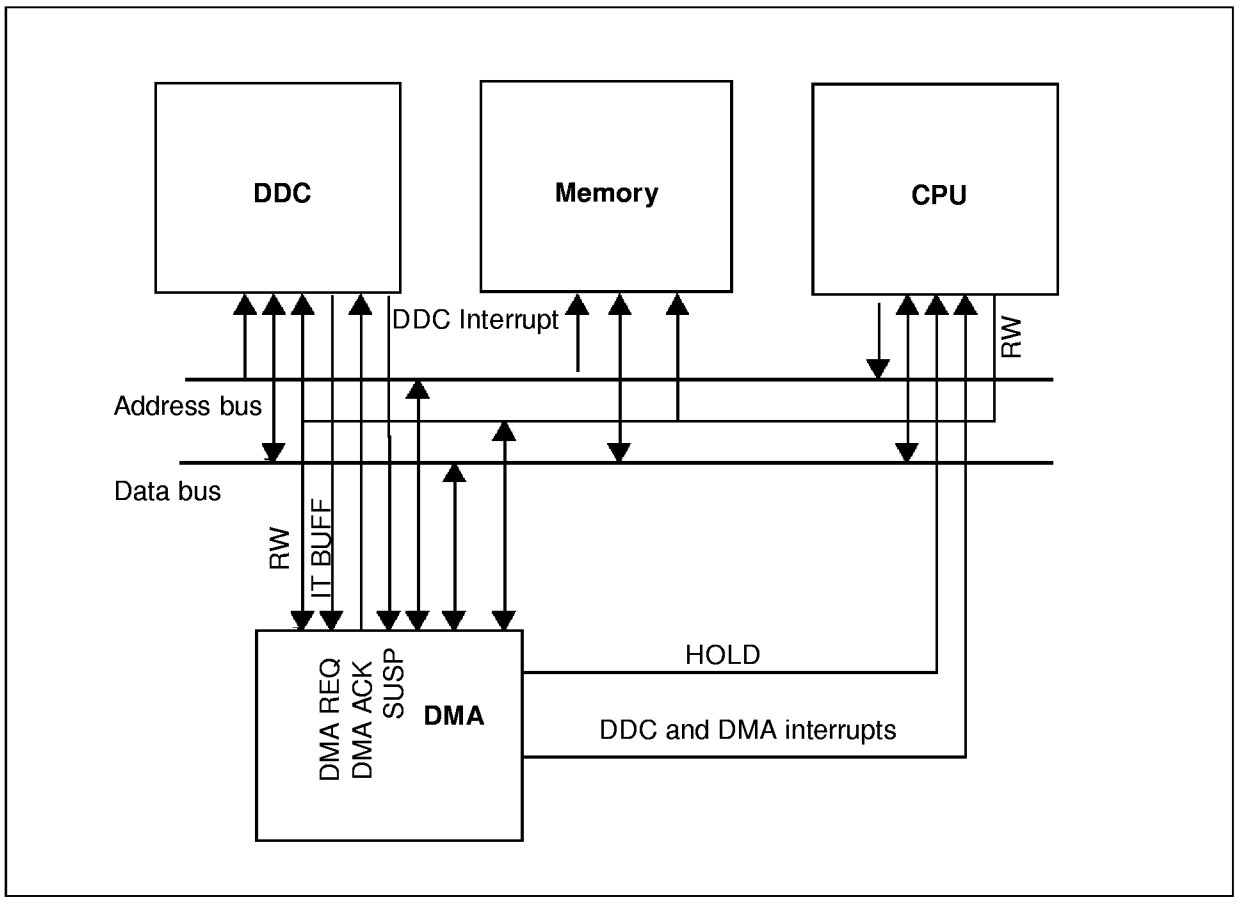
The DDC Interface serves as an I/O interface between the MCU and the Display Data Channel protocol. In addition to receiving and transmitting data, the interface converts data from serial to parallel format and vice versa, using an interrupt or polled handshake. The interface is able to operate in two different modes: DDC1 and I^2C, with a special DDC2B dedicated function. It can transfer a data byte in as little as two CPU clock cycles, using Direct Memory Access (DMA).

The DDC Interface is externally connected by a data line (SDA) and by two clock lines (SCL and V_{SYNC}); the SDA and the SCL lines are connected to an I^2C bus. The interface is connected to the CPU by an interrupt (IT ERR), and to the DMAREQ input of the DMA by an output signal (IT BUFF), as well as to the DMAACK output of the DMA by an input (DMAACK).

In the DDC protocol, there are two types of communication protocols which are called DDC1 and DDC2.

In DDC2B communication protocol, the interface operates in Multimaster/Slave I2C mode. So, the selection of these protocols can be made by software, by using the I2C mode (see I2C mode)

Figure 44. DDC/DMA Cell Block Diagram



DDC BUS INTERFACE (Cont'd)

The DDC Interface makes use of seven internal register locations. Three of these are used for interface initialization (Own Address Registers and Clock Control Register), while the remaining four are used during data transmission/reception (Data Register, Control Register and Status Registers).

The SCL frequency (F_{SCL}) is controlled by a programmable clock divider which depends on the I^2C bus mode. The interface address is stored by software in the OAR1 register .

For DDC1 operation, DMA must be used to handle data transfer automatically, without placing an extra burden on the CPU. Following a Reset, the interface is disabled. DDC1 mode is selected by software. In DDC1 mode, I^2C mode selection is made by software or by the detecting a "high" to "low" transition on the SCL line.

4.8.2.1 DDC1 mode

In DDC1 mode, the interface reads data bytes from memory using DMA, which it then transmits as 8-bit bytes, MSB first. Data bits are clocked on the rising edge of V_{SYNC}, which is received by the interface at a maximum frequency of 25 KHz. A ninth clock pulse, during which the interface expects to receive an acknowledge, follows the eight clock cycles of the byte transfer. Prior to each transfer, the interface sets the IT BUFF interrupt to signal a DMA transfer request, then waits for the DMA to issue the DMAACK signal. Data transfer between the DDC cell and memory will then begin on the subsequent rising edge of V_{SYNC}.

4.8.2.2 DDC2B mode

In DDC2 mode, the interface actually operates in I^2C Mode, but the extra A0/A1 I^2C address is enabled in addition to the standard programmable address (6E). To enable the DDC2B A0/A1 I^2C address comparator, DDC2BEN must be set. In DDC2A mode, the A0/A1 address should be disabled by clearing the same bit.

4.8.2.3 I^2C Mode

In I^2C mode, the interface can operate in the following four modes:

– Master Transmitter

– Master Receiver

– Slave Transmitter

– Slave Receiver

When it is inactive, it operates in Slave mode.

Table 16. DDC Levels.

DDC Level	Cell Mode	Comments
1	DDC1	Possible Automatic DDC1 H/W mode w/o Int Possible Automatic DDC1->2B H/W switch VSyncI1 is used as clock. (up to 25 kHz)
2B	I^2C Slave	Enable DDC2B A0/A1 I^2C decoding address Set the I^2C address at 6E DMA allows automatic EDID & extEDID transfer
2AB	I^2C Multi-Master/Slave	CPU Load minimized with DMA data block transfer DDC/DMA cell maximizes speed transmission and take minimum Access Bus bandwidth

DDC Level	DDC1	DDC2B	I^2C Master Transmitter	I^2C Master Receiver	I^2C Slave Transmitter	I^2C Slave Receiver
1	Yes	Yes	No	No	No*	No*
2B	No	Yes	No	No	Yes	Yes
2AB (A.Bus)	No	No	Yes	No**	No**	Yes

(*): Programmable automatic H/W DDC1 -> DDC2B transition

(**): Slave Transmitter and Master Receiver modes are not used by Access Bus I^2C protocol.

DDC BUS INTERFACE (Cont'd)

The DDC interface allows Multimaster operation, thanks to automatic switching between Master and Slave mode in the event of a loss of arbitration. The slave process is therefore always active when a Start condition is detected on the SDA line.

When acting as Master, a data transfer is initiated and the clock signal is generated. A serial data transfer always begins with a Start condition and ends with a Stop condition. Both Start and Stop conditions are generated by software in Master mode.

In Slave mode, the Own Address, or the DDC2B address are recognised. DDC2B mode is enabled and disabled by software.

Data and addresses are transferred as 8-bit bytes, MSB first. The first byte following the Start condition is the address byte; it is always transmitted in Master mode. A 9th clock pulse follows the 8 clock cycles of a byte transfer, during which the receiver must send an acknowledge bit to the transmitter. Acknowledge is enabled and disabled by software.

In Slave transmitter mode, the interface is able to convert data formats between the micro-controller and the I^2C bus directly or by using DMA. In the first case, it waits for the MCU to write in the Data Register before transmission of a data byte, or to read the Data Register following reception of of a data byte, by holding the SCL line low. In the latter case, the interface sets the IT BUFF interrupt to signal a request for DMA transfer, then waits for the DMA to set the DMAACK signal. Transfer between the interface and the I^2C bus will begin on the next rising edge of V_{SYNC}.

For further information relating to practical implementation, consult the relevant Application Notes for I^2C, Access Bus, DDC1/2B and DDC1/2AB management.

4.8.3 Register Descriptions

DDC CLOCK CONTROL REGISTER (CCR)

Address: 0053h — Read/Write

Reset condition: 0000 0000 (00 h)

7							0
0	D6	D5	D4	D3	D2	D1	D0

bit 7: Must be set to "0" for correct operation.

D6-D0: *7-bit divider programming*

In I^2C mode:

$$F_{SCL} = PHI1/(2x([D6..D0]+2))$$

DDC DATA REGISTER (DR)

Address: 0056h — Read / Write

Reset condition: 0000 0000 (00 h)

7							0
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

In transmit mode, DR contains the next byte of data which is to be loaded into the shift register. Transmission of the byte begins after the MCU has written to DR, or on the subsequent rising edge of V_{SYNC}, if DMAACK is set.

In receive mode, DR contains the last byte of data received from the shift register. Reception of the next byte begins after the MCU has read DR, or on the subsequent rising edge of V_{SYNC} if DMAACK is set.

DDC OWN ADDRESS REGISTER1 (OAR1)

Address: 0054h — Read/Write

Reset condition: 0000 0000 (00 h)

7							0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

ADD7-ADD1 represent the peripheral address in I^2C mode

ADD0 is the Data Direction bit.

DDC BUS INTERFACE (Cont'd)

DDC CONTROL REGISTER (CR)

Address: 0050h — Read/Write

Reset condition: 0000 0000 (00 h)

7							0
DDC1	TRANS	PE	DDC 2BEN	Start	Ack	Stop	ITE

ITE: *Interrupt Enable*

When the Interrupt Enable bit is set, the DDC interface interrupts (IT ERR and IT BUFF) are generated after anyone of these following conditions:

– A Start condition is generated in I^2C Master Mode (IT ERR).

– The address is matched in I^2C slave mode while the ACK flag is at a logic high (IT ERR).

– A data byte has been received or is to be transmitted (IT BUFF).

– A loss of arbitration of the bus to another master in I^2C master mode (IT ERR).

– A misplaced Start or Stop condition is detected (IT ERR).

– There is no acknowledge in I^2C transmitter mode (IT ERR).

– A Stop condition has been detected in I^2C slave mode (IT ERR).

– A high to low transition on SCL line has been detected in DDC1 mode if the TRANS flag is set (IT ERR).

If the ITE flag is set, an interrupt is generated, SCL is hold low and the transfer is suspended except when a loss of arbitration or a detection of a Stop condition have been detected. ITE is reset by software, when the peripheral is disabled (PE=0) or by reset.

STOP: *Generation of Stop condition (I^2C mode)*

If the Stop bit is set in master mode, then a Stop condition is generated after the transfer of the current byte, or after the current Start condition is sent. If it is set in slave mode, then both SCL and SDA lines are released at the end of the current byte in order to recover from an error condition, and the peripheral waits for the detection of a Start or Stop condition. This bit can be cleared by software. It is automatically cleared after the Stop condition is sent on the SCL line in master mode or by Reset. This bit is not cleared by hardware in slave mode.

ACK: *Acknowledge level*

When this bit is set, an acknowledge is returned after an address byte is received or after a data byte is received.When it is cleared, no acknowledge is returned.It is set by software and it is cleared by software, when the peripheral is disabled (PE=0) or by reset.

START: *Generation of Start condition (I^2C mode)*

When the Start bit is set in slave mode, the interface generates a Start condition as soon as the bus is free. In master mode, it generates a repeated Start condition. Then an interrupt is generated if ITE is set.This bit is set by software and is cleared by software, when the peripheral is disabled (PE=0) or by reset. It is automatically cleared after the start condition is sent.

DDC2EN: *Enable DDC2B model*

When this bit is set, the peripheral acknowledges the A0/A1 call address.DDC2BEN bit is set or cleared by software. It is cleared when the peripheral is disabled (PE=0) or by reset.

PE: *Peripheral Enable*

1: Master/Slave capability.
0: Peripheral disabled (all outputs will be released after the end of the current byte transmission). When this bit is reset, all the bits of the control register and the status register except the Stop bit are reset. PE selects the alternate function on the corresponding I/O. This bit is set by software and cleared by software.

TRANS: *Automatic transition mode*(DDC1EN set)

1: A falling edge on SCL line will automatically switch from DDC1 to I^2C modes (SCLFAL is set).
0: No automatic transition.

DDC1EN: *DDC1/I^2C mode selection*

When the DDC1EN bit is set then the interface operates in DDC1 mode else it operates in I^2C mode.The DDC1EN bit is set by software. It is cleared by software, when both the SCLFAL flag and the TRANS flag are set, when the peripheral is disabled (PE=0) or by a reset.

DDC BUS INTERFACE (Cont'd)

DDC FIRST STATUS REGISTER (SR1)

Address: 0051 h — Read Only

Reset condition: 0000 0000 (00 h)

7							0
ITFLAG	0	TRA	BUSY	BTF	ADSL	M/SL	SB

SB: *Start Bit (I^2C master mode)*

In master mode, SB bit is set when the hardware has generated a Start condition. When this bit is set, an interrupt (IT ERR) is sent to the micro-controller if ITE is set. Then the micro-controller must write the address byte in the data register.This bit is cleared by a read of the status register (when SB is set), followed by a write in the data register. It is also cleared when the peripheral is disabled (PE=0) or by reset.

M/SL: *Master/Slave (I^2C mode)*

The M/SL bit is set when the interface generates a Start condition. When it is set, the interface operates in master mode.It is cleared by the generation of a Stop condition, by a loss of arbitration, by reset or when the peripheral is disabled (PE=0).

ADSL: *Addressed as Slave (I^2C mode)*

ADSL bit is set when the address comparator recognizes either its own slave address or the DDC2B address. When this bit is set, an interrupt (IT ERR) is sent to the micro-controller if ITE is set. This bit is cleared by reading the status register (when ADSL is set). It is also cleared when the peripheral is disabled (PE=0) or by reset.

BTF: *Byte Transmission Finished*

In transmit mode, the BTF bit is set after the transmission of a data byte and an acknowledge clock pulse. It is cleared by reading the Status Register (with BTF set), followed by writing to the Data Register, or when DMAACK is set.

In receive mode, the BTF bit is set following reception of a byte acknowledge. It is cleared by reading the Status Register (with BTF set), followed by reading the Data Register, or when DMAACK is set.

While the DDC1 flag is set, BTF is the only source of the IT BUFF interrupt (if ITE is set).

It is also cleared when the peripheral is disabled (PE=0) or on Reset.

When BTF is set, the DDC interrupt (IT BUFF) occurs if ITE is set. The MCU must then access the Data Register, or the DMA must set the DMAACK signal.

BUSY: *Bus Busy (I^2C mode)*

The BUSY bit is active when there is a communication in progress. Detection of communications is always active (even if the peripheral is disabled). This bit is set on detection of a Start condition, and it is cleared on detection of a Stop condition.

It is also cleared when the peripheral is disabled (PE=0) or on Reset.

TRA: *Transmission mode*

The TRA bit is set when the interface is in data transmission mode.

TRA is cleared on detection of a Stop condition or in the event of a loss of bus arbitration (ARLO set).

It is also cleared when the peripheral is disabled (PE=0) or on Reset.

In DDC1 mode, TRA is always set.

ITFLAG: *Interrupt Flag*

The ITFLAG bit is set after any of the following conditions:

– A Start condition is generated in I^2C Master Mode.

– The address is matched (in I^2C Slave mode) while the ACK flag is set to "1".

– A data byte has been received or is to be transmitted.

– In the event of the loss of bus arbitration to another master, while in I^2C master mode.

– On detection of a misplaced Start or Stop condition.

– When there is no acknowledge in I^2C transmitter mode.

– A Stop condition has been detected in I^2C slave mode.

– A high to low transition has been detected on the SCL line in DDC1 mode, while the TRANS flag is set.

This bit is cleared when SR2 is read, when the peripheral is disabled (PE=0) or by reset.

DDC BUS INTERFACE (Cont'd)

DC SECOND STATUS REGISTER (SR2)

Address: 0052h — Read Only

Reset condition: 0000 0000 (00 h)

7							0
SCLFAL	0	0	AF	STOPF	ARLO	BERR	DDC2BF

DDC2BF:

If DDC2BEN is set, DDC2BF is set on detection of the DDC2B A0/A1 address. It is cleared on detection of a Stop condition, on Reset, or when the peripheral is disabled (PE=0).

BERR: *Bus Error (I^2C mode)*

The BERR bit is set on detection of a misplaced Start or Stop condition. If this bit is set, an interrupt (IT ERR) is sent to the MCU, providing ITE is set. During this interrupt, the SCL line is not held low. The Bus Error flag bit is cleared by reading the Status Register (while BERR is set).

A bus error is not internally considered as a Stop or a Start.

The bit is also cleared when the peripheral is disabled (PE=0), or on Reset.

ARLO: *Arbitration Lost (I^2C master mode)*

The ARLO bit is set when the I^2C interface loses arbitration of the bus in favour of another Master. Once ARLO has been set, the interface will operate in Slave mode (M/SL at a logic low) and an interrupt (IT ERR) is generated, providing ITE is set. During this interrupt, the SCL line is not held low. The ARLO bit is cleared by reading the Status Register.

It is also cleared when the peripheral is disabled (PE=0) or on Reset.

STOPF: *Stop Detection (I^2C Slave mode)*

The STOPF bit is set when a Stop condition is detected on the SCL line after an acknowledge of byte.When this bit is set, an interrupt (IT ERR) is sent to the micro-controller if ITE is set. During this interrupt, the SCL line is not hold low.This bit is cleared by a read of the status register (when StopF is set). It is also cleared when the peripheral is disabled (PE=0) or by reset.

AF: *Acknowledge Failure (I^2C mode)*

The Acknowledge Failure bit is set when there is a problem during the transfer. If this bit is set, then an interrupt (IT ERR) is sent to the micro-controller if ITE is set. During this interrupt, the SCL line is not hold low. The Acknowledge Failure bit is cleared by a reading of the Status Register or by a reset.

SCLFAL: *SCL Falling Edge (DDC1 mode)*

This bit is set on detecting an SCL falling edge while the DDC1EN flag is set. While the DDC1 flag is set, SCLFAL is the only source of the IT ERR interrupt, providing ITE is set. All other flags in SR2 are disabled. During this interrupt the SCL line is not held low.

The SCLFAL bit is cleared by reading the Status Register.

Table 17. DDC Register Map

A2	A1	A0	Register
1	1	0	DR
1	0	1	Reserved
1	0	0	OAR1
0	1	1	CCR
0	1	0	SR2
0	0	1	SR1
0	0	0	CR

4.8.4 DDC1 Mode

In order to enter DDC1 mode, the PE flag and the DDC1EN flag must be set. Bytes are sent on the rising edge of V_{SYNC} on the SDA line, MSB first. A ninth clock pulse follows the 8 clock cycles of a byte transfer. During this ninth clock pulse an acknowledge bit is sent, providing the ACK bit is set. The DDC1EN bit is then cleared and an interrupt (IT ERR) is generated. This interrupt is cleared by reading the Status Register.

4.8.5 I^2C Mode

Following a Reset, the DDC interface operates in I^2C mode. When the interface is operating in DDC1 mode, it will automatically switch to I^2C mode on detecting a falling edge on the SCL line. In order to enter I^2C mode, the PE bit must be set and the DDC1EN bit must be cleared.

4.8.6 I^2C State Machine

In I^2C mode, the DDC interface always operates in Slave mode (M/SL "low"), except when it initiates a transmission or a receive sequence.

Multimaster mode is implemented by automatically switching from Master mode to Slave mode when the interface loses arbitration of the I^2C bus.

DDC BUS INTERFACE (Cont'd)

4.8.7 Slave Mode

As soon as a Start condition is detected, the address word is received on the SDA line and transferred to the shift register; it is then compared with the interface address, whereupon one of the following two conditions are possible:

– **Address does not match**: the state machine is reset and awaits another Start bit.

– **Address matches**: the "Addressed As Slave" bit (ADSL) is set and an Acknowledge bit is sent to the Master, providing ACK is set. An interrupt is thus sent to the MCU if ITE is set. The interface then waits for the MCU to read Status Register 1, by holding the SCL line low. Next, depending on the state of the Data Direction bit (LSB), and after issuing an acknowledge, the Slave must enter transmit or in a receive mode.

4.8.7.1 Slave Sending

The Slave device waits for the MCU to write to the Data Register, or waits for the DMA controller to set DMAACK by holding the SCL line low. Data is then moved into the Shift Register and transmitted on the SDA line.

– When the acknowledge bit is received, the BTF flag is set and an interrupt (IT BUFF) is generated if ITE is set.

– On detection of a Stop or Start condition during a byte transfer, the BERR flag is set, and an interrupt (IT ERR) is generated.

– On detection of a Start condition after the expiry of an acknowledge time-slot, the state machine is reset and begins a new process. The ADSL flag is set and an interrupt (IT ERR) is generated if ITE is set.

– On detection of a Stop condition after the expiry of an acknowledge time-slot, the state machine is reset. The STOPF flag is set and an interrupt (IT ERR) is generated if ITE is set.

4.8.7.2 Slave Receiving

The Slave receives words on the SDA line which are transferred to the shift register, these are then forwarded to the Data Register. After each word, an acknowledge bit is issued, providing the Enable Acknowledge flag is set. When the acknowledge bit is sent, the BTF flag is set and an interrupt (IT BUFF) is generated if ITE is set.The interface then waits for the MCU to read the Data Register, or for the DMA to set DMAACK by holding the SCL line low. The following conditions are possible:

– On detecting a Stop or Start condition during byte reception, the BERR flag is set and an interrupt (IT ERR) is generated.

– On detecting a Start condition after expiry of an acknowledge time-slot, the state machine is reset and begins a new process.

– On detecting a Stop condition after the expiry of an acknowledge time-slot, the Slave state machine is reset. The STOPF flag is then set and an interrupt (IT ERR) is generated if ITE is set.

– The Stop bit in the Control register is set: the State machine is reset after transfering the current byte.

DDC BUS INTERFACE (Cont'd)

4.8.8 Master Mode

The interface operates in Master mode after generating a Start condition. Therefore the Start flag must be set in the Control register and the I^2C bus must be free (Busy bit "low"). Once the Start condition is generated, the M/SL and SB flags are set and an interrupt (IT ERR) is generated if ITE is set. The interface waits for the micro-controller to write the slave address to the Data Register, by holding the SCL line low. Then the address byte is sent on the SDA line, an acknowledge clock pulse is sent on the SCL line, and an interrupt (IT ERR) is generated if ITE is set. The interface waits for the MCU to write to the Control Register by holding the SCL line low. If there is no acknowledge, the AF flag is set and the master must write Start or Stop in the Control Register.

The state machine then enters a send or receive process, depending on the status of the Data Direction bit (LSB); an interrupt (IT BUFF) is generated if ITE is set.

If the master loses bus arbitration, or if there is no acknowledge, the AF flag is set and the master must write a Start or a Stop in the Control register.

The ARLO flag is set, the M/SL flag is cleared and the process is reset. An interrupt (IT ERR) is generated if ITE is set.

4.8.8.1 Master Sending

The Master waits for the MCU to write to the Data Register or for the DMA controller to set DMAACK by holding the SCL line low. The byte is loaded into the shift register and sent on the SDA line. The BTF flag is set and an interrupt (IT BUFF) is generated if ITE is set.

– On detection of a Stop or a Start condition during a byte transfer, the BERR flag is set and an interrupt is generated if ITE is set.

– If the Stop bit is set in the Control Register, a Stop condition is generated after the current byte has been transferred, the M/SL flag is cleared and the state machine is reset. Then an interrupt is generated if ITE is set.

– If the Start bit is set in the Control Register, the state machine is reset and begins a new process. The SB flag is set and an interrupt (IT ERR) is generated if ITE is set.

– If there is no acknowledge, the AF flag is set and an interrupt is generated if ITE is set.

4.8.8.2 Master Receiving

The Master receives a byte from the SDA line into the shift register and then transfers it to the Data Register. An acknowledge bit is genertated if the ACK bit is set and an interrupt is generated (IT BUFF) if ITE is set. The interface then waits for the MCU to read the Data Register or for the DMA controller to set DMAACK by holding the SCL line low.

On detection of a Stop or Start condition during reception of a byte, the BERR flag is set and an interrupt (IT ERR) is generated if ITE is set.

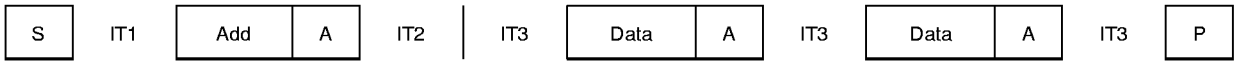
If the Stop bit is set in the Control Register, a Stop condition is generated following transfer of the current byte; the M/SL flag is cleared and the state machine is reset. Then an interrupt (IT ERR) is generated if ITE is set.

If the Start bit is set in the Control Register, the state machine is reset and begins a new process. The SB flag is set and an interrupt (IT ERR) is generated if ITE is set.

DDC BUS INTERFACE (Cont'd)

4.8.9 Transfer sequencing

Master Transmitter (I^2C mode):

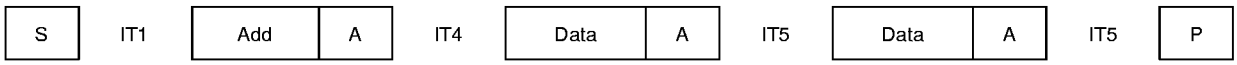


IT1: SB =1. Cleared by a read of SR1 followed by a write to the DR (IT ERR).

IT2: Cleared by a read of SR1 followed by a write to the CR.

IT3: BTF=1; TRA=1. Cleared by reading SR1 followed by writing to the DR, or cleared when DMAACK is set (IT BUFF).

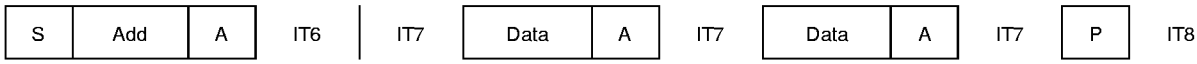
Master Receiver (I^2C mode):



IT4: Cleared by reading SR1 followed by writing to the CR.

IT5: BTF=1; TRA=1. Cleared by reading SR1 followed by reading the DR, or cleared when DMAACK is set.

Slave Transmitter (I^2C mode):

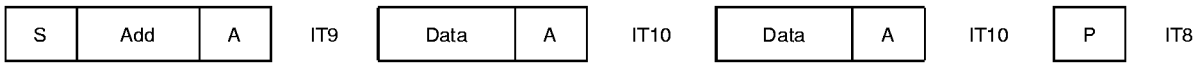


IT6: ADSL =1. Cleared by reading SR1.

IT7: BTF=1. Cleared by reading SR1, followed by writing to the DR, or cleared when DMAACK is set.

IT8: STOPF=1. Cleared by reading SR2.

Slave Receiver (I^2C mode):



IT9: ADSL =1. Cleared by reading SR1.

IT10: BTF=1. Cleared by reading SR1 followed by reading the DR, or cleared when DMAACK is set.

Slave Transmitter (DDC1 mode):



IT12: BTF=1; TRA=1. Cleared by reading SR1 followed by writing to the DR, or cleared when DMAACK is set.

S: Start; P: Stop; A: Acknowledge; IT: interrupt

Detailed timing information is available inSection 6 ELECTRICAL CHARACTERISTICS.

4.9 DDC DMA CHANNEL (DDC-DMA)

4.9.1 Introduction

The DMA channel is associated with the DDC peripheral interface and handles direct accesses to RAM memory as required by the peripheral.

When a DMA access is performed the CPU must not be in WAIT mode: before executing a WAIT instruction, the DMA must therefore be disabled, if necessary.

4.9.2 Main Features

– Single DMA channel for management of direct memory access by the DDC peripheral.

– 16-bit Initial Address Register (IADHR, IADLR)

– 16-bit Current Address Register (CADHR, CADLR)

– 8-bit Initial Counter Register (ICTR)

– 8-bit Current Counter Register (CCTR)

– 8-bit Control Register (CTLR)

– Address incrementing and decrementing following each transfer.

– Counter decrementing following each transfer.

– Auto reload and linear modes.

– Daisy-chained DMA capability.

– DMA transfer performed in only 2 CPU cycles.

4.9.3 Functional Description

The DDC-DMA channel allows direct transfer between the DDC peripheral and memory. The transfer can be from DDC cell to memory or vice versa, depending on the state of the RW bit in the DMA Control Register.

The DMAREQ signal causes the DMA cell to stop the CPU clock for 2 cycles on the subsequent op-code fetch or immediately if the CPU is in WAIT state (by setting HOLD signal). During these two cycles, the CPU releases the address bus and the control signal lines used to synchronize bus accesses.

During DMA operations, memory is accessed in exactly the same way as it normally is by the CPU. The contents of the CADHR and CADLR registers is output to the address bus, and the RW signal is driven in accordance with the RW bit setting.

If DMA is disabled when a peripheral requests it, the DMA cell simply transmits the request to the CPU using an interrupt line. The DMA request will then be serviced as an interrupt request.

4.9.4 DMA Control Signals

DMAREQ: *DMA REQuest (input from the peripheral).*

The peripheral associated with the DMA channel generates this input signal in order to request a DMA transfer. The transfer will occur on the subsequent op-code fetch, or immediately, if the CPU is in WAIT mode. The DMA cell knows when the op-code fetch occurred, by monitoring the LI signal from the CPU.

HOLD: *HOLD CPU (output to the CPU).*

This output is generated during DMA transfer, in order to put the CPU in Hold. The CPU releases the RW signal line and the address bus. The CPU clock is stopped.

DMAACK: *DMA ACKnowledge (output to the peripheral).*

This output is generated during a DMA transfer, when the peripheral can read (RW bit = 1) or write (RW bit = 0) the data present on the data bus.

RW: *Read/Write (input/output)*

During a DMA transfer, the RW signal is defined as an output signal and its value correspond to RW-bit. In the others cases, RW is an input coming from the CPU (RW=1:read; RW=0 write)

A0-15: *Address bus (input/output)*

During a DMA transfer, Address bus bits A0-15 are defined as outputs and their value corresponds to the value of the CADR. In all other cases, A0-15 are inputs coming from the CPU.

DDC-DMA (Cont'd)

4.9.5 DDC DMA Channel (DDC-DMA)

Register Descriptions

DMA INITIAL ADDRESS REGISTER (IADHR & IADLR)

Addresses:0048 & 0049h — Read / Write

Reset condition: XXXX XXXX (XX h)

This 16-bit register pair contains the initial address for the DMA transfer. It is not affected by Reset or by disabling the DMA. Read accesses are always allowed. Write accesses are allowed only in Suspend Mode (SUSP bit "high").

DMA CURRENT ADDRESS REGISTER(CADHR & CADLR)

Addresses: 004A & 004B h — Read / Write

Reset condition: XXXX XXXX (XX h)

This 16-bit register pair contains the address of the next DMA transfer. It is not affected by Reset or by disabling the DMA.

DMA INITIAL COUNTER REGISTER(ICTR)

Address: 004C h — Read / Write

Reset condition: XXXX XXXX (XX h)

This 8-bit register contains the initial number of bytes to be transmitted before an autoreload occurs, or before an interrupt request is to be sent to the CPU. It is not affected by Reset or by disabling the DMA. Read accesses are always allowed. Write accesses are allowed only in SUSPEND MODE (SUSP bit "high").

DMA CURRENT COUNTER REGISTER(CCTR)

Address: 004D h) — Read / Write

Reset condition: XXXX XXXX (XX h)

This 8-bit register contains the number of byte to be transmitted before an autoreload occurs or before send an interrupt request to the CPU. It is not affected by RESET or when the DMA is disabled.The CCTR is a read/write register.

DMA CONTROL REGISTER(CTLR)

Address: 004E h — Read / Write

Reset condition: 0000 0000 (00 h)

7							0
MATCH	0	EN	ITE	RW	DECR	AUTOR	SUSP

MATCH: *Match to 00h*

– Set by hardware when CCTR reaches 00h (end of a block transmission). If the ITE bit is set, an interrupt request is sent to the CPU.

– Reset by Reset or by software.

***Note**: As MATCH is set by the DMA when the CPU is activity is stopped, there is no risk of resetting it in error when bit manipulation instructions are used.*

EN: *Enable / Disable*.

0 = DMA cell disabled.

The value of IADR, CADR, ICTR and CCTR are not affected when EN is reset. If the DMA is disabled when the DDC peripheral requests a DMA access, the DMA cell will simply transmit the request to the CPU using an interrupt line. The DMA request will then be serviced as an interrupt request.

1 = DMA cell enabled.

Set and reset by software.

ITE: *Interrupt Enable*

0 = Interrupt request disabled

1 = Interrupt request enabled.

An interrupt is sent to the CPU when CCTR reaches 00 (MATCH-bit high). Set and reset by software.

RW: *Transfer Direction*.

0 = From the DDC cell to memory.

1 = From memory to the DDC cell.

Set and reset by software.

DDC-DMA (Cont'd)

DECR: *Decrementing / Incrementing*

1 = CADR will be decremented after each DMA transfer.

0 = CADR will be incremented after each DMA transfer.

In both cases, CCTR is decremented after each DMA transfer, Set and reset by software.

AUTOR: *Auto Reload / Non Auto Reload*

0 = At the end of a block transfer, when the CCTR reaches 00h, the DMA cell goes into Suspend mode (SUSP bit high), and if the ITE bit is set an interrupt is sent to the CPU just after the DMA transfer (MATCH bit high). It allows the received block to be procesed, or the preparation of the next block before initiating a new block transfer. Transfer is inhibited until the SUSP bit is reset by software.

1 = At the end of a block transfer, when the CCTR reaches 00h, the CADR is automatically reloaded with the IADR value, and the CCTR is reloaded with the ICTR value. The MATCH bit is set, but the transfer is not suspended (the SUSP bit remains "low"). Set and reset by software.

SUSP: *Suspend Mode*

0 = The DMA cell is active.

1 = The DMA cell is in Suspend Mode. If a DMA request occurs when the DMA is in Suspend Mode, the request remains pending. It will be serviced as soon as SUSP goes "low". SUSP is set by software or when the CCTR reaches 00 in non-autoreload mode. SUSP is reset by software.

Note: *As the SUSP bit is set by the DMA when the CPU activity is stopped, there is no risk of reseting it in error when bit manipulation instructions are used. When IT-ERR is generated by the DDC peripheral, SUSP is set by hardware.*

5 SOFTWARE

5.1 ST7 ARCHITECTURE

The 8-bit ST7 Core is designed for high code efficiency. It contains 6 internal registers, 17 main addressing modes and 63 instructions. The 6 internal registers include 2 index registers, an accumulator, a 16-bit Program Counter, a stack pointer and a condition code register. The two Index registers X and Y enable Indexed Addressing modes with or without offset, along with read-modify-write type data manipulations. These registers simplify branching routines and data modifications.

The 16-bit Program Counter is able to address up to 64K of ROM/EPROM memory. The 6-bit Stack Pointer provides access to a 64-level Stack and an upgrade to an 8-bit Stack Pointer is foreseen in order to be able to manage a 256-level Stack. The Core also includes a Condition Code Register providing 5 Condition Flags that indicate the result of the last instruction executed.

The 17 main Addressing modes, including Indirect Relative and Indexed addressing, allow sophisticated branching routines or CASE-type functions. The Indexed Indirect Addressing mode, for instance, permits look-up tables to be located anywhere in the address space, thus enabling very flexible programming and compact C-based code.

The 63-instruction Instruction Set is 8-bit oriented with a 2-byte average instruction size. This Instruction Set offers, in addition to standard data movement and logic/arithmetic functions, byte multiplication, bit manipulation, data transfer between Stack and Accumulator (Push/Pop) with direct stack access, as well as data transfer using the X and Y registers.

5.2 ST7 ADDRESSING MODES

The ST7 Core features 17 different addressing modes which can be classified in 7 main groups:

Addressing Mode	Example
Inherent	nop
Immediate	ld A,#$55
Direct	ld A,$55
Indexed	ld A,($55,X)
Indirect	ld A,([$55],X)
Relative	jrne loop
Bit operation	bset byte,#5

The ST7 Instruction set is designed to minimize the number of bytes required per instruction: To do so, most of the addressing modes may be subdivided in two sub-modes called long and short:

– The long addressing mode is the most powerful because it can reach any byte in the 64kb addressing space, but the instruction is bigger and slower than the short addressing mode.

– The short addressing mode is less powerful because it can generally only access page zero (0000 - 00FFh range), but the instruction size is more compact, and faster. All memory to memory instructions are only working with short addressing modes (CLR, CPL, NEG, BSET, BRES, BTJT, BTJF, INC, DEC, RLC, RRC, SLL, SRL, SRA, SWAP)

Both modes have pros and cons, but the programmer does not need to choose which one is the best: the ST7 Assembler will always choose the best one.

ST7 ADDRESSING MODES(Cont'd)

Table 18. ST7 Addressing Mode Overview:

Mode			Syntax	Destination	Ptr addr	Ptr size	Lngth
Inherent			nop				+ 0
Immediate			ld A,#$55				+ 1
Short	Direct		ld A,$10	00..FF			+ 1
Long	Direct		ld A,$1000	0000..FFFF			+ 2
No Offset	Direct	Indexed	ld A,(X)	00..FF			+ 0
Short	Direct	Indexed	ld A,($10,X)	00..1FE			+ 1
Long	Direct	Indexed	ld A,($1000,X)	0000..FFFF			+ 2
Short	Indirect		ld A,[$10]	00..FF	00..FF	byte	+ 2
Long	Indirect		ld A,[$10.w]	0000..FFFF	00..FF	word	+ 3
Short	Indirect	Indexed	ld A,([$10],X)	00..1FE	00..FF	byte	+ 2
Long	Indirect	Indexed	ld A,([$10.w],X)	0000..FFFF	00..FF	word	+ 3
Relative	Direct		jrne loop	PC+/-127			+ 1
Relative	Indirect		jrne [$10]	PC+/-127	00..FF	byte	+ 2
Bit	Direct		bset $10,#7	00..FF			+ 1
Bit	Indirect		bset [$10],#7	00..FF	00..FF	byte	+ 2
Bit	Direct	Relative	btjt $10,#7,skip	00..FF			+ 2
Bit	Indirect	Relative	btjt [$10],#7,skip	00..FF	00..FF	byte	+ 3

ST7 ADDRESSING MODES(Cont'd)

Inherent:

All related instructions are single byte ones. The op-code fully specify all required information for the CPU to process the operation. These instructions are single byte ones.:

Inherent Instruction	Function
NOP	No operation
TRAP	S/W Interrupt
WFI	Wait For Interrupt (Low Power Mode)
HALT	Halt Oscillator (Lowest Power Mode)
RET	Sub-routine Return
IRET	Interrupt Sub-routine Return
SIM	Set Interrupt Mask
RIM	Reset Interrupt Mask
SCF	Set Carry Flag
RCF	Reset Carry Flag
RSP	Reset Stack Pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
MUL	Byte Multiplication
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles

Immediate:

The required data byte to do the operation is following the op-code. These are two byte instructions, one for the op-code and the other one for the immediate data byte.

Immediate Instruction	Function
LD	Load
CP	Compare
BCP	Bit Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Operations

Direct (short, long):

The data byte required to carry out the operation is found by its memory address, which follows the op-code.

Available Long and Short Direct Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substractions operations
BCP	Bit Compare

Short Direct Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The direct addressing mode consists of two submodes:

Direct (short):

The address is a byte, thus require only one byte after the op-code, but only allow 00..FF addressing space.

Direct (long):

The address is a word, thus allowing 64Kb addressing space, but requires 2 bytes after the op-code.

ST7 ADDRESSING MODES(Cont'd)

Indexed (no offset, short, long)

The required data byte to do the operation is found by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset which follows the op-code.

No Offset, Long and Short Indexed Instruc.	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substractions operations
BCP	Bit Compare

No Offset and Short Indexed Inst. Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The indirect addressing mode consists of three sub-modes:

Indexed (no offset):

There is no offset, (no extra byte after the op-code), but only allows 00.FF addressing space.

Indexed (short):

The offset is a byte, thus require only one byte after the op-code, but only allow 00..1FE addressing space.

Indexed (long):

The offset is a word, thus allowing 64Kb addressing space, but requires 2 bytes after the op-code.

Indirect (short, long):

The required data byte to do the operation is found by its memory address, located in memory (pointer).

Available Long and Short Indirect Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substractions operations
BCP	Bit Compare

Short Indirect Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The pointer address follows the op-code. The indirect addressing mode consists of two sub-modes:

Indirect (short):

The pointer address is a byte, the pointer size is a byte, thus allowing 00..FF addressing space, and requires 1 byte after the op-code.

Indirect (long):

The pointer address is a byte, the pointer size is a word, thus allowing 64Kb addressing space, and requires 1 byte after the op-code.

ST7 ADDRESSING MODES(Cont'd)

Indirect Indexed (short, long):

This is a combination of indirect and short indexed addressing mode. The required data byte to do the operation is found by its memory address, which is defined by the unsigned addition of an index register value (X or Y) with a pointer value located in memory. The pointer address follows the op-code.

Long and Short Indirect Indexed Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substractions operations
BCP	Bit Compare

Short Indirect Indexed Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The indirect indexed addressing mode consists of two sub-modes:

Indirect Indexed (short):

The pointer address is a byte, the pointer size is a byte, thus allowing 00..1FE addressing space, and requires 1 byte after the op-code.

Indirect Indexed (long):

The pointer address is a byte, the pointer size is a word, thus allowing 64Kb addressing space, and requires 1 byte after the op-code.

Relative mode (direct, indirect):

This addressing mode is used to modify the PC register value, by adding an 8 bit signed offset to it.

Available Relative Direct/Indirect Instructions	Function
JRxx	Conditional Jump
CALLR	Call Relative

The relative addressing mode consists of two sub-modes:

Relative (direct):

The offset is following the op-code.

Relative (indirect):

The offset is defined in memory, which address follows the op-code.

5.3 ST7 INSTRUCTION SET

The ST7 family devices use an Instruction Set consisting of 63 instructions. The instructions may be subdivided into 13 main groups as illustrated in the following table:

Load and Transfer	LD	CLR						
Stack operation	PUSH	POP	RSP					
Increment/Decrement	INC	DEC						
Compare and Tests	CP	TNZ	BCP					
Logical operations	AND	OR	XOR	CPL	NEG			
Bit Operation	BSET	BRES						
Conditional Bit Test and Branch	BTJT	BTJF						
Arithmetic operations	ADC	ADD	SUB	SBC	MUL			
Shift and Rotates	SLL	SRL	SRA	RLC	RRC	SWAP	SLA	
Unconditional Jump or Call	JRA	JRT	JRF	JP	CALL	CALLR	NOP	RET
Conditional Branch	JRxx							
Interruption management	TRAP	WFI	HALT	IRET				
Code Condition Flag modification	SIM	RIM	SCF	RCF				

Using a pre-byte

The instructions are described with one to four op-codes.

In order to extend the number of available op-codes for an 8-bit CPU (256 op-codes), three different prebyte opcodes are defined. These prebytes modify the meaning of the instruction they precede.

The whole instruction becomes:

PC-2 End of previous instruction

PC-1 Prebyte

PC Op-code

PC+1 Additional word (0 to 2) according to the number of bytes required to compute the effective address

These prebytes enable instruction in Y as well as indirect addressing modes to be implemented. They precede the opcode of the instruction in X or the instruction using direct addressing mode. The prebytes are:

PDY 90 Replace an X based instruction using immediate, direct, indexed, or inherent addressing mode by a Y one.

PIX 92 Replace an instruction using direct, direct bit, or direct relative addressing mode to an instruction using the corresponding indirect addressing mode.
It also changes an instruction using X indexed addressing mode to an instruction using indirect X indexed addressing mode.

PIY 91 Replace an instruction using X indirect indexed addressing mode by a Y one.

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
ADC	Add with Carry	A = A + M + C	A	M	H		N	Z	C
ADD	Addition	A = A + M	A	M	H		N	Z	C
AND	Logical And	A = A . M	A	M			N	Z	
BCP	Bit compare A, Memory	tst (A . M)	A	M			N	Z	
BRES	Bit Reset	bres Byte, #3	M						
BSET	Bit Set	bset Byte, #3	M						
BTJF	Jump if bit is false (0)	btjf Byte, #3, Jmp1	M						C
BTJT	Jump if bit is true (1)	btjt Byte, #3, Jmp1	M						C
CALL	Call subroutine								
CALLR	Call subroutine relative								
CLR	Clear		reg, M				0	1	
CP	Arithmetic Compare	tst(Reg - M)	reg	M			N	Z	C
CPL	One Complement	A = FFH-A	reg, M				N	Z	1
DEC	Decrement	dec Y	reg, M				N	Z	
HALT	Halt					0			
IRET	Interrupt routine return	Pop CC, A, X, PC			H	I	N	Z	C
INC	Increment	inc X	reg, M				N	Z	
JP	Absolute Jump	jp [TBL.w]							
JRA	Jump relative always								
JRT	Jump relative								
JRF	Never jump	jrf *							
JRIH	Jump if Port B INT pin = 1	(no Port B Interrupts)							
JRIL	Jump if Port B INT pin = 0	(Port B interrupt)							
JRH	Jump if H = 1	H = 1 ?							
JRNH	Jump if H = 0	H = 0 ?							
JRM	Jump if I = 1	I = 1 ?							
JRNM	Jump if I = 0	I = 0 ?							
JRMI	Jump if N = 1 (minus)	N = 1 ?							
JRPL	Jump if N = 0 (plus)	N = 0 ?							
JREQ	Jump if Z = 1 (equal)	Z = 1 ?							
JRNE	Jump if Z = 0 (not equal)	Z = 0 ?							
JRC	Jump if C = 1	C = 1 ?							
JRNC	Jump if C = 0	C = 0 ?							
JRULT	Jump if C = 1	Unsigned <							
JRUGE	Jump if C = 0	Jmp if unsigned >=							
JRUGT	Jump if (C + Z = 0)	Unsigned >							
JRULE	Jump if (C + Z = 1)	Unsigned <=							

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
LD	Load	dst <= src	reg, M	M, reg			N	Z	
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A	0				0
NEG	Negate (2's compl)	neg $10	reg, M				N	Z	C
NOP	No Operation								
OR	OR operation	A = A + M	A	M			N	Z	
POP	Pop from the Stack	pop reg pop CC	reg CC	M M	H	I	N	Z	C
PUSH	Push onto the Stack	push Y	M	reg, CC					
RCF	Reset carry flag	C = 0							0
RET	Subroutine Return								
RIM	Enable Interrupts	I = 0				0			
RLC	Rotate left true C	C <= A <= C	reg, M				N	Z	C
RRC	Rotate right true C	C => A => C	reg, M				N	Z	C
RSP	Reset Stack Pointer	S = Max allowed							
SBC	Substract with Carry	A = A - M - C	A	M			N	Z	C
SCF	Set carry flag	C = 1							1
SIM	Disable Interrupts	I = 1				1			
SLA	Shift left Arithmetic	C <= A <= 0	reg, M				N	Z	C
SLL	Shift left Logic	C <= A <= 0	reg, M				N	Z	C
SRL	Shift right Logic	0 => A => C	reg, M				0	Z	C
SRA	Shift right Arithmetic	A7 => A => C	reg, M				N	Z	C
SUB	Substraction	A = A - M	A	M			N	Z	C
SWAP	SWAP nibbles	A7-A4 <=> A3-A0	reg, M				N	Z	
TNZ	Test for Neg & Zero	tnz lbl1					N	Z	
TRAP	S/W trap	S/W interrupt				1			
WFI	Wait for Interrupt					0			
XOR	Exclusive OR	A = A XOR M	A	M			N	Z	

6 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Devices of the ST72 family contain circuitry to protect the inputs against damage due to high static voltage or electric fields. Nevertheless, it is recommended that normal precautions be observed in order to avoid subjecting this high-impedance circuit to voltages above those quoted in the Absolute Maximum Ratings. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained within the range:

$$V_{SS} \leq V_{IN} \text{ and } V_{OUT} \leq V_{DD}$$

To enhance reliability of operation, it is recommended to configure unused I/Os as inputs and to connect them to an appropriate logic voltage level such as V_{SS} or V_{DD}.

All the voltage in the following tables are referenced to V_{SS}.

Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Absolute Maximum Ratings (Voltage Referenced to V_{SS}).

Symbol	Ratings	Value	Unit
V_{DD}	Recommended Supply Voltage	-0.3 to +6.0	V
V_{DDA}	Analog Reference Voltage	-0.3 to +9.0	V
V_{IN}	Input Voltage	V_{SS} -0.3 to VDD + 0.3	V
V_{OUT}	Output Voltage	V_{SS} -0.3 to VDD + 0.3	V
I_{IN}	Input Current	-10.....+10	mA
I_{OUT}	Output Current	-10.....+10	mA
T_A	Operating Temperature Range	0 to +70	^{O}C
T_{STG}	Storage Temperature Range	-65 to +150	^{O}C
PD	Power Dissipation	TBA	mW
ESD	ESD susceptibility	2000	V

Note: The maximum accumulated current off all I/O pins should not exceed 40 mA for V_{DD} and 40 mA for V_{SS}.

6.2 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \theta J_A) \quad (1)$$

Where:

– T_A is the Ambient Temperature in°C,

– θJ_A is the Package Junction-to-Ambient Thermal Resistance, in °C/W,

– P_D is the sum of P_{INT} and $P_{I/O}$,

– P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power

– $P_{I/O}$ represents the Power Dissipation on Input and Output Pins; User Determined.

For most applications $P_{I/O} < P_{INT}$ and may be neglected. $P_{I/O}$ may be significant if the device is configured to drive Darlington bases or sink LED Loads.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Therefore:

$$K = P_D \times (T_A + 273°C) + \theta J_A \times P_D^2 \quad (3)$$

Where:

– K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 20. Thermal Characteristics

Symbol	Package	Value	Unit
θJ_A	PSDIP56	60	°C/W

6.3 DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to +70°C unless otherwise specified

Symbol	Parameter	Test Conditions	Value			Unit
			min	typ	max	
V_{DD}	Supply Voltage		4.5		5.5	V
V_{OL}	Output Voltage Low Port A (Open drain)	I_{OL}=1.6 mA			0.4	V
V_{OL}	Output Voltage Low Port B (0-7), Port D(0:7) Push-pull	I_{OL}=1.6 mA			0.4	V
V_{OL}	Output Voltage Low Port C (PC2,PC3,PC4) Push-pull	I_{OL}=1.6 mA			0.4	V
V_{OL}	Output Voltage Low Port C (PC0,PC1,PC5) Open drain	I_{OL}=1.6 mA			0.4	V
V_{OL}	during Power ON Reset and Watch-dog Reset				0.4	V
V_{OH}	Output Voltage High Push-pull	I_{OH}=1.6 mA	V_{DD}-0.8			V
V_{IH}	Input High Voltage PA(0-7), PB(0-7), PC(0-5), PD(0-4), $\overline{\text{RESET}}$	Leading Edge	0.7xV_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage PA(0-7), PB(0-7), PC(0-5), PD(0-4), $\overline{\text{RESET}}$	Trailing Edge	V_{SS}		0.3xV_{DD}	V
I_{IL}	I/O Ports Hi-Z Leakage Current PA(0-7), PB(0-7), PC(0-5), PD(0-4), $\overline{\text{RESET}}$	V_{SS} V_{DD}			10	uA uA
C_{OUT} C_{IN}	Capacitance: Ports (as Input or Output), RESET				12 8	pF pF
R_{ON}	DA1,D(A3-17)(PWM/BRM) Serial Resistor			700	1000	Ohms
I_{RPU}	Pull-up resistor current	V_{DD}=5v V_{IN}=V_{SS}		20		uA

DC ELECTRICAL CHARACTERISTICS(Cont'd)

DDC Bus (I^2C INTERFACE)				
Symbol	**Parameter**	**Min**	**Max**	**Unit**
V_{HYS}	Hysteress of Shmitt trigger inputs fixed input levels V_{DD}-related input levels	 na na	 na na	V
T_{SP}	Pulse width of spikes which must be suppressed by the input filter	na	na	ns
T_{OF}	Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400pF with up 3mA sink current at VOL1		 250	ns
I	Input current each I/O pin with an input voltage between 0.4v and 0.9 V_{DD} max	-10	10	µA
C	Capacitive load for each I/O pin		10	pF

A/D CONVERTER						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Val	Resolution	F_{OSC} = 8 MHz		8		bit
Terr	Total Error	F_{OSC} = 8 MHz			± 3	LSB
Tcon	Conversion Time	F_{OSC} = 8 MHz	16			µs
Rva	Analog Source Impedance			30		KΩ

6.4 AC ELECTRICAL CHARACTERISTICS

(T_A = 0 to +70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ.	Max	
V_{DD}	Operating Supply Voltage	4 MHz Internal	4.5		5.5	V
I_{DD}	Supply Current	RUN Mode F_{ext} = 8MHz V_{DD} = 5.0V		7.5	10	mA
		WAIT Mode f_{ext} = 8MHz V_{DD} = 5.5V		3.5	5	mA

6.5 CONTROL TIMING

(Operating conditions T_A 0 to +70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ.	Max	
f_{OSC}	Frequency of Operation	V_{DD} = 4.5V f external f internal			8 4	MHz
t_{ILCH}	Halt Mode Recovery Startup Time				20	ms
t_{RL}	External RESET Input pulse Width		1.5			t_{CYC}
t_{PORL}	Power Reset Duration		4096			t_{CYC}
T_{DOGL}	Watchdog RESET Output Pulse Width		2		2	t_{CYC}
t_{DOG}	Watchdog Time-out		49,152		3,145,728	t_{CYC}
t_{ILIL}	Interrupt Pulse Period		(1)			t_{CYC}
t_{OXOV}	Crystal Oscillator Start-up Time				50	ms
t_{DDR}	Power up rise time	V_{DD} min			100	ms

Notes :
1. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 cycles.

AC ELECTRICAL CHARACTERISTICS(Cont'd)

6.5.1 DDC (I^2C BUS) Interface

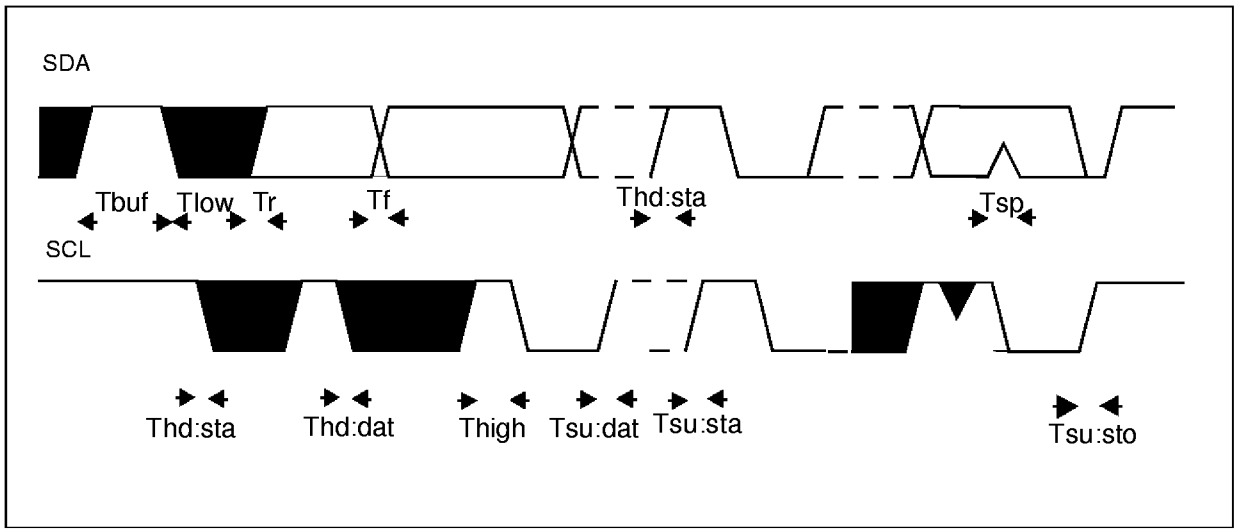
6.5.1.1 Timing

Parameter	Min	Max	Symbol	Unit
Bus free time between a STOP and START condition	4.7		Tubs	ms
Hold time START condition. After this period, the first clock pulse is generated	4.0		Thd:sta	µs
LOW period of the SCL clock	4.7		Tlow	µs
HIGH period of the SCL clock	4.0		Thigh	µs
Set-up time for a repeated START condition	4.7		Tsu:sta	µs
Data hold time	250 (1)		Thd:dat	ns
Data set-up time	250		Tsu:dat	ns
Rise time of both SDA and SCL signals		1000	Tr	ns
Fall time of both SDA and SCL signals		300	Tf	ns
Set-up time for STOP condition	4.0		Tsu:sto	ns
Capacitive load for each bus line		400	Cb	pF

1. The device provides a hold time of at least 250ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Cb = total capacitance of one bus line in pF

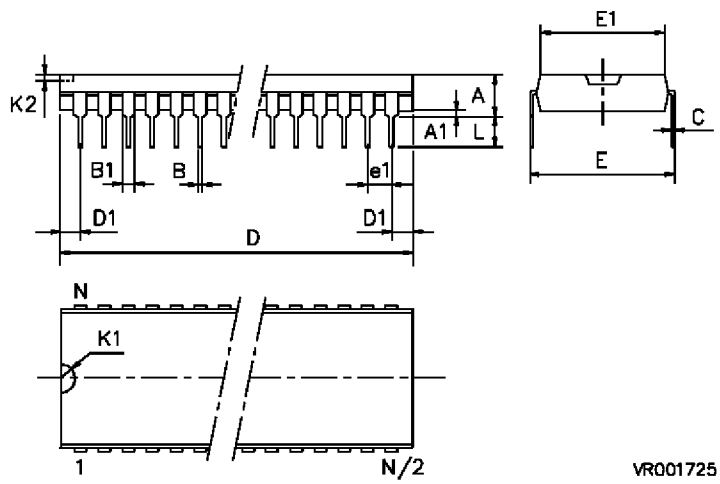
Figure 45. Definition of Timing Terminology



7 GENERAL INFORMATION

7.1 PACKAGE MECHANICAL DATA

Figure 46. 56 Shrink Plastic Dual In Line Package, 600-mil Width



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
B	0.35		0.59	0.014		0.023
B1	0.75		1.42	0.030		0.056
C	0.20		0.36	0.008		0.014
D		52.12			2.052	
D1	-	-	-	-	-	-
E			18.54			0.730
E1		13.72				0.540
K1	-	-	-	-	-	-
K2	-	-	-	-	-	-
L	2.54		3.81	0.100		0.150
e1		1.78			0.070	
Number of Pins						
N	56					

7.2 ORDERING INFORMATION

7.2.1 Introduction

The following section describes the approved procedure for transfer of User Program/Data ROM Code to SGS-THOMSON Microelectronics as well as the basis for contractual agreement with respect to mask programmed devices.

7.2.2 Communication of the User ROM Code

To formally communicate the desired Program/Data ROM contents to SGS-THOMSON Microelectronics, the following must be supplied:

– a file in MOTOROLA S19 FORMAT (on diskette, via electronic mail or by BBS);

– a correctly completed and signed Option List form as shown overleaf.

The User Code must respect the ROM Memory Map for the selected device option.

The User Code must be generated using an approved ST7 assembler. All unused memory locations shall be set to FFh.

7.2.3 Verification and Formal Approval

When SGS-THOMSON Microelectronics receives the User Code file, it will return a copy of the processed file to the Customer. The Customer will then send formal notification to SGS-THOMSON Microelectronics, approving the file contents. This statement and the file copies to which it refers will then form the basis of the contractual agreement between the Customer and SGS-THOMSON Microelectronics and the agreed file will be used to produce the mask for the programmed MCU device.

The SGS-THOMSON Sales Organization will be pleased to provide detailed information relating to the above technical and contractual points.

Table 21. Ordering Information

Sales Types	ROM Size	RAM Size	Temperature Range	Package
ST7272N5B1	24K	384	0 to +70°C	PSDIP56

ST7272 MICROCONTROLLER OPTION LIST

Customer . . . . . .

Address . . . . . .

. . . . . .

Contact . . . . . .

Phone No . . . . . .

Reference . . . . . .

SGS-THOMSON Microelectronics references

Device: [ ] ST7272 24K ROM

Package: [ ] SDIP56

Temperature Range: [ ] 0°C to + 70°C

Special Marking: [ ] No

[ ] Yes "_ _ _ _ _ _ _ _ _ _ _ _"

Clamping Output Option: [ ] Maximum delay 250ns
Programmable back porch clamping width (0, 250ns, 500ns, 1 us)

[ ] Maximum delay 125ns
Programmable back porch clamping width (0, 125ns, 250ns, 500 us)

All options must be defined before acceptance

Signature

Date

Notes:

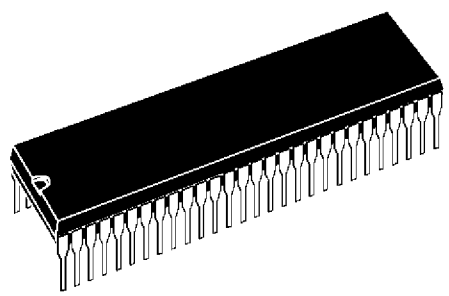
SGS-THOMSON MICROELECTRONICS

ST72E72
ST72T72

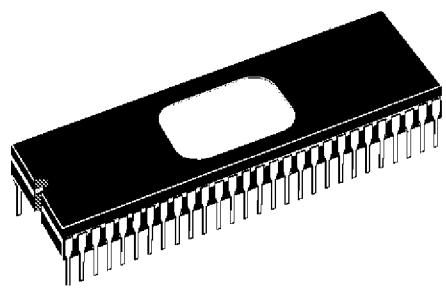
8-BIT MCU WITH 24K EPROM, EEPROM, ADC, PWM/BRM DACs, SYNC PROCESSOR, EWPCC, TIMER AND DDC I/F

PRELIMINARY DATA

- 4.5V to 5.5V Supply Operating Range
- 8MHz Maximum Oscillator Frequency
- Fully Static operation
- 0°C to + 70°C Operating Temperature Range
- Run, Wait, Halt, and RAM Retention modes
- User EPROM/OTP: 24Kbytes
- Data RAM: 384 bytes
- EEPROM: 640 + 256 bytes
- 56 pin Shrink Dual-in-Line package
- 27 multifunctional bidirectional I/O lines:
  - 8 lines with 12V open-drain drive capability
  - 8 Programmable Interrupt inputs
  - 8 Analog inputs
- 16-bit Timer, featuring:
  - 2 Input Captures
  - 2 Output Compares (1 output pin)
- 8-bit Analog-to-Digital converter
- Programmable Watchdog Timer
- 16 10-bit PWM/BRM Digital to Analog outputs
- 2 12-bit PWM/BRM Digital to Analog outputs
- EWPCC circuit with on-chip EEPROM
- New upgraded Sync processor for Mode Recognition, Power Management and Composite Video Blanking Generator
- DDC 1/2/AB interface with built-in DMA and I^2C Master/Slave Modes
- Master Reset and Power-On Reset
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS Real-Time Emulator
- Full Software Package (C-Compiler, Cross-Assembler, Debugger)



PSDIP56



CSDIP56

This is advance information from SGS-THOMSON. Details are subject to change without notice.

1 GENERAL DESCRIPTION

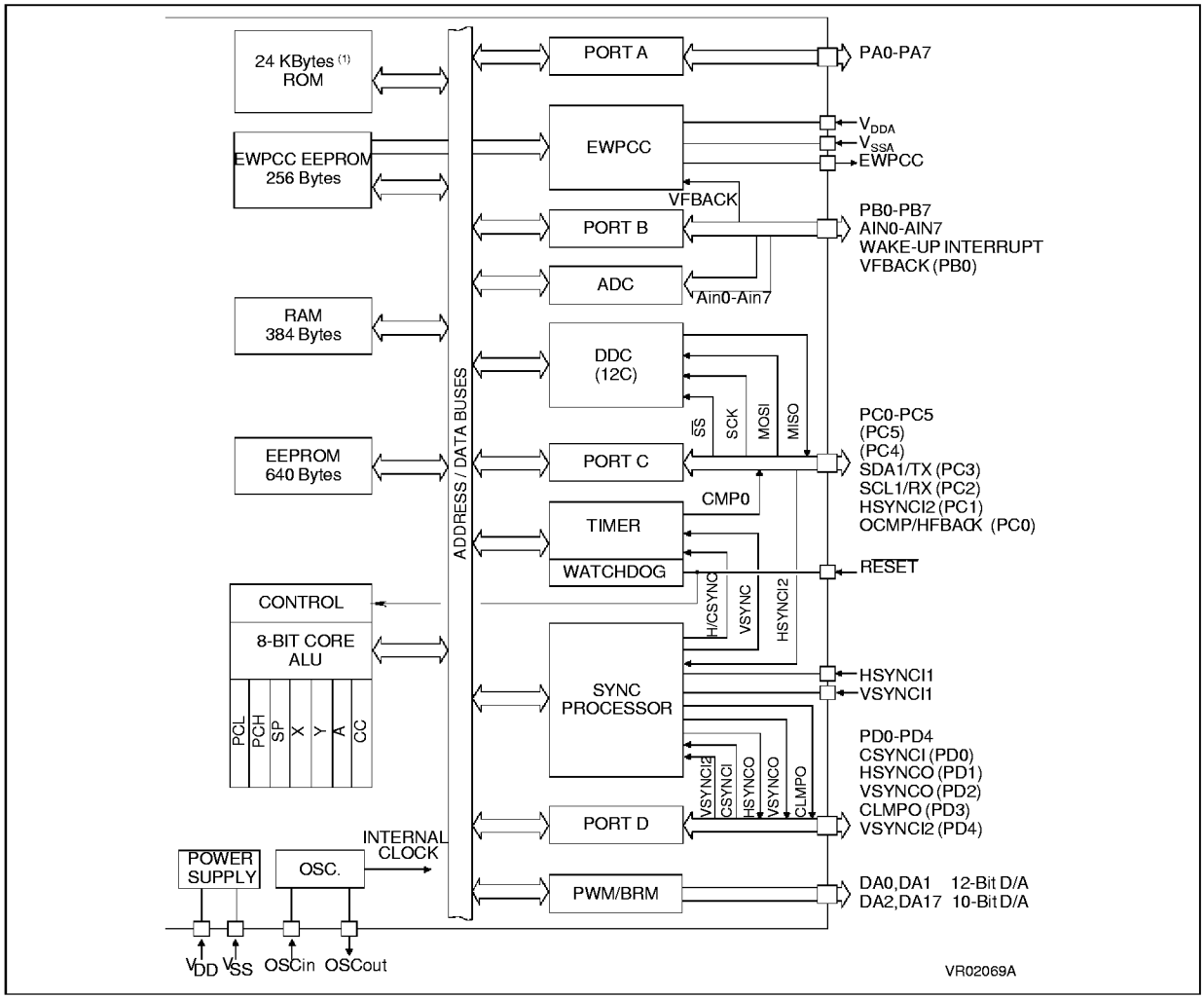
1.1 INTRODUCTION

The ST72T72 and the ST72E72 devices are OTP and EPROM versions respectively of the ST7272 ROM based HCMOS Microcontroller Unit. Please refer to the ST7272 ROM device Datasheet for further details.

From the user's point of view, both the OTP and EPROM devices are functionally identical to the ROM device and possess the same software and hardware features. An additional mode is available to allow programming of the EPROM user memory array. This is set by a specific voltage applied to the V_{PP}/Test pin.

The EPROM and OTP devices feature 24K of user programmable EPROM memory; the EPROM device features a windowed ceramic package which allows the contents of the memory array to be erased by exposure to UV light.

Figure 1. ST72E72/T72 Block Diagram



Note1: EPROM/OTP

1.2 PIN DESCRIPTION

V_{DD} Power supply

V_{SS} Digital Ground

V_{DDA} Analog V_{DD} and reference for EWPCC Digital to Analog Converter (typically 8 Volts).

V_{SSA} Analog V_{SS} for EWPCC DAC.

OSCin, OSCout Oscillator input and output pins; usually connected to a parallel resonant crystal or ceramic resonator. Altenatively an external clock source may also be input via OSCin.

EWPCC Analog correction signal output from East-West Pin Cushion Correction circuit.

SCL1/RX DDC Serial Clock or RX (Falling edge detector with interrupt).

SDA1/TX DDC Serial Data or TX.

OCMP / HFBACK Output compare signal from the Timer.

HSYNCI1 Horizontal Synchronization Input 1.

VSYNCI1 Vertical Synchronization Input 1.

HSYNCI2 Sync Processor Horizontal or complete Synchronization Input 2.

VSYNCI2 Vertical Synchronization Input 2.

CSYNCI Composite Synchronization Input. This pin accepts the composite synchronization input when the Sync Processor I/O functions are enabled.

VFBACK Vertical Flyback signal used for timing correlation for the East-West Pin Cushion correction.

HFBACK Horizontal Flyback Input.

BLANK OUT Video Blanking Output.

HSYNCO Horizontal Synchronization Output from the Sync Processor.

VSYNCO Vertical Synchronization Output from the Sync Processor.

CLMPO Clamp Output. This pin outputs the clamping (back porch) output signal from the Sync Processor .

DA0, DA1 12-bit PWM/BRM outputs (for Analog Controls, after external filtering).

DA2-DA17 10-bit PWM/BRM outputs (for Analog controls, after external filtering).

PORT A 8 I/O lines, bit programmable, accessed through PADDR and PADR Registers. Each bit can be defined as a standard input port bit without pull-up resistor or as an open drain output port (up to 12V).

PORT B 8 Standard bit-programmable I/O lines accessed through the PBDDR and PBDR Registers. Each bit can be programmed as an analog input (by control bits in the PORT B Configuration register), digital input (with internal pull-up resistor), push-pull digital output or as interrupt wake-up (with pull-up). These negative edge or low-level sensitive interrupt lines can wake-up the MCU from WAIT or HALT mode. PB0 is used for the East-West Pin cushion controller VFBACK input when the EWPCC is used.

PORT C 6 Standard bit-programmable I/O lines accessed through the PCDDR and PCDR Registers. PC 0,1 are Inputs with Pull-Up or Push-Pull Outputs, PC 2,3 are Open Drain outputs or Inputs without Pull-Up, PC 4,5 are Open Drain outputs or Digital Inputs with or without Pull-Up internal resistor. The pull-up resistor is enabled for all bits by one control bit in the Programmable Input/Output Configuration Register. PC0 can also be configured as Timer Output Compare pin or Horizontal Flyback Input. PC1 can be programmed as HSYNCI2 sync input for the Sync Processor. PC2/SCL1 and PC3/SDA1 are alternate functions with the DDC cell.

PORT D 5 Standard bit-programmable I/O lines accessed through PDDDR and PDDR Registers. Each bit can be programmed as an input (with internal pull-up resistor), push-pull output or Synchronization inputs and outputs to/from the Sync Processor. When programmed as inputs, Video Synchronization signals can be directly inspected. The inputs may also be passed through the Sync Processor to the Timer Input Captures.

$\overline{\text{RESET}}$ An active-low signal on this pin forces initialization of the MCU. This is the top priority non maskable interrupt. This pin is driven low if the Watchdog Timer has been triggered. The resulting pulse can be used to reset external peripherals.

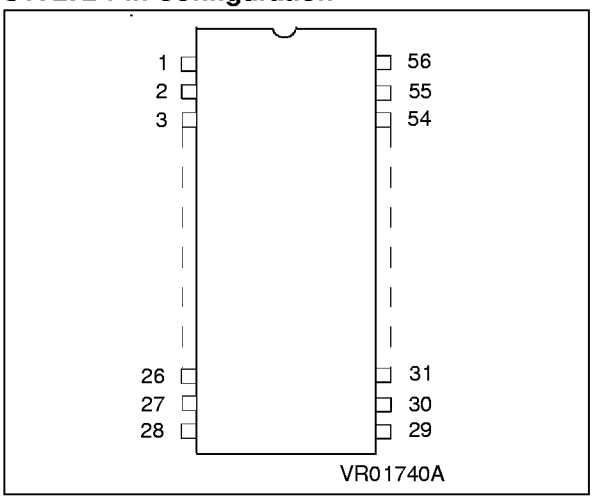
V_{PP}/TEST This pin must be held low for normal operation. In programing mode, this pin is connected to V_{PP}.

CAUTION: *The V_{PP}/TEST pin MUST be connected directly to the V_{SS} pin on the device in order to ensure correct operation.*

PIN DESCRIPTION (Cont'd)

The following table describes basic and alternate functions for each pin. Relevant ancillary information is given in the Remarks column. The pin configuration is illustrated for convenience.

ST7272 Pin Configuration

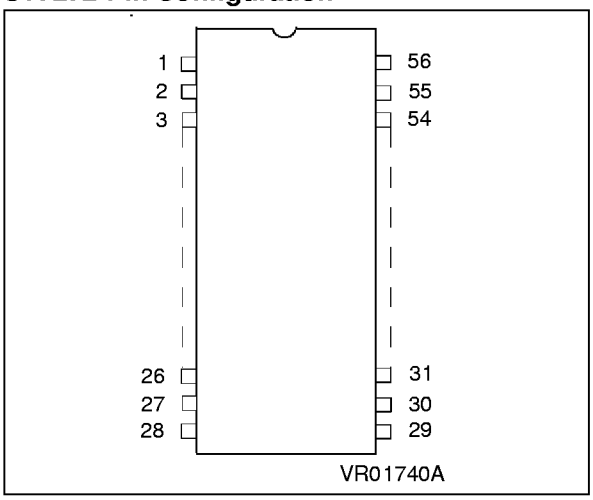


Pin Name(s)	Basic Function	Alternate Function	Pin	Remarks
V_{DDA}	Analog power supply	-	1	Typically +8V
EWPCC	EWPCC circuit analog output	-	2	2 - 6V
DA0	12-bit DAC PWM outputs	--	3	Generated by PWM/BRM circuitry, need external filtering.
DA1			4	
DA2	10-bit DAC PWM outputs	--	5	
DA3			6	
DA4			7	
DA5			8	
DA6			9	
DA7			10	
DA8			11	
DA9			12	
PB7	Port B I/Os	Analog input	13	Standard I/O or alternate function. The I/O configuration is software programmable as input with pull-ups, wake-up interrupt input, or push-pull output.
PB6			14	
PB5			15	
PB4			16	
PB3			17	
PB2			18	
PB1			19	
PB0 / VFBACK		Analog input or VFBACK	20	As above, or input for EWPCC circuit, when active.
PD4 / VSYNCI2	Port D I/O	VSYNCI2	21	Vertical Sync input 2 (TTL with pull-up).
PD3 / CLMPO	Port D I/O	CLMPO	22	Clamp output from Sync circuit.
DA10	10-bit DAC PWM outputs	-	23	Generated by PWM/BRM circuitry, need external filtering.
DA11			24	

PIN DESCRIPTION (Cont'd)

The following table describes basic and alternate functions for each pin. Relevant ancillary information is given in the Remarks column. The pin configuration is illustrated for convenience.

ST7272 Pin Configuration

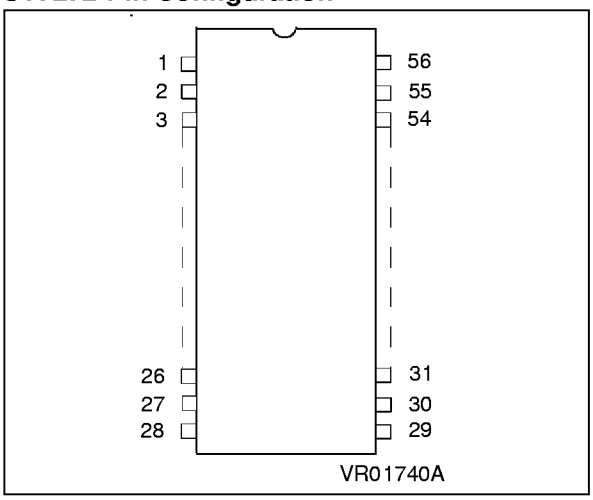


Pin Name(s)	Basic Function	Alternate Function	Pin	Remarks
$\overline{\text{RESET}}$	General reset input and output	-	25	As an input, a Reset is generated by an active low signal; when the Watchdog has triggered this pin will be driven low to reset external peripherals.
PD2 / VSYNCO	Port D I/O	VSYNCO	26	Vertical Sync output from Sync processor.
VSYNCI1	VSYNCI1		27	Vertical Sync input to Sync processor (TTL with pull-up).
V_{DD}	Power supply to digital circuits.	-	28	4.5 - 5.5V
HSYNCI1	HSYNCI1		29	Horizontal Sync input to Sync processor (TTL with pull-up).
PD1 / HSYNCO	Port D I/Os	HSYNCO	30	Horizontal Sync output from Sync processor.
PD0 / CSYNCI		CSYNCI	31	Composite Sync input (TTL with pull-up).
OSCOUT	Oscillator output	-	32	These pins may be connected to a parallel resonant crystal or ceramic resonator; alternatively an external clock source may be connected to OSCIN.
OSCIN	Oscillator input		33	
DA12	10-bit DAC PWM outputs	-	34	Generated by PWM/BRM circuitry, need external filtering.
DA13			35	
PA7 / BLANKOUT	Port A I/Os	BLANKOUT	36	Video blanking output from Sync processor.
PA6		-	37	Standard I/Os, bit programmable via PADDR and PADR registers as inputs without pull-ups or as open-drain outputs (up to 12V).
PA5			38	
PA4			39	
PA3			40	
PA2			41	
PA1			42	
PA0			43	

PIN DESCRIPTION (Cont'd)

The following table describes basic and alternate functions for each pin. Relevant ancillary information is given in the Remarks column. The pin configuration is illustrated for convenience.

ST7272 Pin Configuration



Pin Name(s)	Basic Function	Alternate Function	Pin	Remarks
DA14	10-bit DAC PWM outputs	-	44	Generated by PWM/BRM circuitry, need external filtering.
DA15			45	
DA16			46	
DA17			47	
V_{PP}/TEST	TEST	V_{PP}	48	This pin is for SGS-THOMSON internal use only and **MUST** be tied directly to V_{SS} for normal operation. In programing mode this pin is connected to V_{PP}.
PC0 / OCMP / HFBACK	Port C I/Os	OCMP or HFBACK	49	Output compare from Timer peripheral. or Horizontal flyback input (TTL with pull-up).
PC1 / HSYNCI2		HSYNCI2	50	Horizontal Sync input to Sync processor (TTL with pull-up).
PC2 / SCL1 / RX		SCL1 RX	51	DDC serial clock. Can generate interrupt on falling edge for RX Start detection for software SCI.
PC3 / SDA1 / TX		SDA1 TX	52	DDC serial data. OCMP can generate interrupt for TX bit timing for software SCI.
PC4		-	53	
PC5			54	
V_{SS}	Digital Ground	-	55	
V_{SSA}	Analog Ground	-	56	

1.3 MEMORY MAP

Table 1. ST7272 Memory Map

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0000h		PADR	Port A Data Register	XXh	R/W Register
0001h		PBDR	Port B Data Register	XXh	R/W Register
0002h		PCDR	Port C Data Register	XXh	R/W Register
0003h		PDDR	Port D Data Register	XXh	R/W Register
0004h		PADDR	Port A Data Direction Register	00h	R/W Register
0005h		PBDDR	Port B Data Direction Register	00h	R/W Register
0006h		PCDDR	Port C Data Direction Register	00h	R/W Register
0007h		PDDDR	Port D Data Direction Register	00h	R/W Register
0008h	ADC	DR	ADC Data Register	XX	Read Only Register
0009h		CR	ADC control/Status register	00h	R/W Register
000Ah	Reserved				
000Bh		DACR	East/West DAC Register	00h	R/W Register
000Ch	EW	PCC0	East/West Control 0	00h	R/W Register
000Dh		PCC1	East/West Control 1	C0h	R/W Register
000Eh		CR0	DDC EEPROM Control register	00h	R/W Register
000Fh	EEP	CR1	GP1 EEPROM Control register	00h	R/W Register
0010h		CR2	GP2 EEPROM Control register	00h	R/W Register
0011h		CR3	E/W EEPROM Control register	00h	R/W Register
0012h		CR	TIMER Control Register	00h	R/W Register
0013h		SR	TIMER Status Register	XXh	Read Only Register
0014h		IC1HR	TIMER Input Capture High Register 1	XXh	Read only
0015h		IC1LR	TIMER Input Capture Low Register 1	XXh	Read only
0016h		OC1HR	TIMER Output Compare High Register 1	XXh	R/W Register
0017h		OC1LR	TIMER Output Compare Low Register 1	XXh	R/W Register
0018h	TIM	CNTHR	TIMER Counter High Register	FFh	Read only
0019h		CNTLR	TIMER Counter Low Register	FCh	R/W Register
001Ah		ACNTHR	TIMER Alternate Counter High Register	FFh	Read only
001Bh		ACNTLR	TIMER Alternate Counter Low Register	FCh	R/W Register
001Ch		IC2HR	TIMER Input Capture High Register 2	XXh	Read only
001Dh		IC2LR	TIMER Input Capture Low Register 2	XXh	Read only
001Eh		OC2HR	TIMER Output Compare High Register 2	XXh	R/W Register
001Fh		OC2LR	TIMER Output Compare Low Register 2	XXh	R/W Register
0020h		PWM0	(12-BIT PWM) Register	80h	R/W Register
0021h	PWM/BRM	BRM0	(12-BIT BRM) Register	C0h	R/W Register
0022h		PWM1	(12-BIT PWM) Register	80h	R/W Register
0023h		BRM1	(12-BIT BRM) Register	C0h	R/W Register

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0024h	PWM/BRM	PWM2	10-BIT PWM/BRM Registers	80h	R/W Registers
0025h		BRM3 + BRM2		00h	
0026h		PWM3		80h	
0027h		PWM4		80h	
0028h		BRM5+ BRM4		00h	
0029h		PWM5		80h	
002Ah		PWM6		80h	
002Bh		BRM7 + BRM6		00h	
002Ch		PWM7		80h	
002Dh		PWM8		80h	
002Eh		BRM9+ BRM8		00h	
002Fh		PWM9		80h	
0030h		PWM10		80h	
0031h		BRM11 + BRM10		00h	
0032h		PWM11		80h	
0033h		PWM12		80h	
0034h		BRM13+ BRM12		00h	
0035h		PWM13		80h	
0036h		PWM14		80h	
0037h		BRM15 + BRM14		00h	
0038h		PWM15		80h	
0039h		PWM16		80h	
003Ah		BRM17+ BRM16		00h	
003Bh		PWM17		80h	
003Ch		PBICFGR	Port B Input Pull-Up Configuration Register	00h	R/W Register
003Dh		PIOCFGR	Programmable I/O Configuration Register	F8h	R/W Register
003Eh		WDOGR	Watchdog Register	7Fh	R/W Register
003Fh		MISCR	Miscellaneous Register	2Ah	R/W Register
0040h	SYNC	CFGR	SYNCHRO Configuration Register	00h	R/W Register
0041h		MCR	SYNCHRO Multiplexer Register	00h	R/W Register
0042h		CCR	SYNCHRO Counter Register	00h	R/W Register
0043h		POLR	SYNCHRO Polarity Register	00h	R/W Register
0044h		LATR	SYNCHRO Latch Register	00h	R/W Register
0045h		HGENR	SYNCHRO H Sync Generator Register	00h	R/W Register
0046h		VGENR	SYNCHRO V Sync Generator Register	00h	R/W Register
0047h		ENR	SYNCHRO Processor Enable Register	00h	R/W Register

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0048h	DMA	IADHR	DMA Initial High Address Register	XXh	R/W Register
0049h		IADLR	DMA Initial Low Address Register	XXh	R/W Register
004Ah		CADHR	DMA current High Address Register	XXh	R/W Register
004Bh		CADLR	DMA current Low Address Register	XXh	R/W Register
004Ch		ICTR	DMA Initial Counter Register	XXh	R/W Register
004Dh		CCTR	DMA current Counter Register	XXh	R/W Register
004Eh		CTLR	DMA Control Register	00h	R/W Register
004Fh	Reserved				
0050h	DDC	CR	DDC Control Register	00h	R/W Register
0051h		SR1	DDC 1st Status Register	00h	Read only
0052h		SR2	DDC 2nd Status Register	00h	Read only
0053h		CCR	DDC Clock Control Register	00h	R/W Register
0054h		OAR1	DDC 7 Bits Slave address Register	00h	R/W Register
0055h			Reserved		
0056h		DR	DDC Data Register	00h	R/W Register
0057h			Reserved		
0058h	CRC	CRCL	CRC Low register / Reserved	ST INTERNAL USE ONLY	
0059to		CRCH	CRC High register/ Reserved		
005Ah to 007Fh	Reserved				
0080h to 01BFh			User RAM 384 bytes, including stack		
01C0h to 01FFh			Stack 64bytes		
0200h to 027Fh	Reserved				
0280h to 02FFh		DDC-EEPROM	128 bytes dedicated for DDC EEPROM		EEPROM 896 bytes in 4 banks
0300h to 03FFh		GP1-EEPROM	256 bytes for Data GP1 EEPROM		
0400h to 04FFh		GP2-EEPROM	256 bytes for Data GP2 EEPROM		
0500h to 05FFh		EWPCC-EEP-ROM	256 bytes for either EWPCC or Data GP3 EEPROM		

Add	Block name	Block Register mnemonic	Register name	Reset Status	Remarks
0600h to 07FFh	Unused				
0800h to 08FFh	Reserved				
0900h to 13FFh	Unused				
1400h to 1FFFh	Reserved				
2000h to 7EFFh			24K bytes program EPROM/OTP		
7F00h to 7FEFh	Reserved				
7FF0h to 7FFFh		7FF0-7FF1	DDC/DMA (OR wiring)		Internal Interrupts
		7FF2-7FF3	TIMER Overflow TOF		"
		7FF4-7FF5	TIMER Output compare OCMP		"
		7FF6-7FF7	TIMER Input capture ICAP		"
		7FF8-7FF9	RX falling edge		"
		7FFA-7FFB	Keyboard (PORT B)		External Interrupts
		7FFC-7FFD	TRAP (software)		"
		7FFE-7FFF7	RESET vector		CPU Interrupt

1.4 EPROM ERASURE

The EPROM memory on the ST72E72 device is erased by exposure to high intensity UV light admitted through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current.

It is recommended that the device be kept out of direct sunlight, since the UV content of sunlight can be sufficient to cause functional failure. Extended exposure to room level fluorescent lighting may also cause erasure. An opaque coating (paint, tape, label, etc...) should be placed over the package window if the product is to be operated under these lighting conditions. Covering the window also reduces I_{DD} in power-saving modes due to photo-diode leakage currents.

An Ultraviolet source of wave length 2537 Å yielding a total integrated dosage of 15 Watt-sec/cm is required to erase the device. The device will be erased in 15 to 20 minutes if such a UV lamp with a 12mW/cm power rating is placed 1 inch from the device window without any interposed filters.

2 ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS

Devices of the ST72 family contain circuitry to protect the inputs against damage due to high static voltage or electric fields. Nevertheless, it is recommended that normal precautions be observed in order to avoid subjecting this high-impedance circuit to voltages above those quoted in the Absolute Maximum Ratings. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained within the range:

$$V_{SS} \leq V_{IN} \text{ and } V_{OUT} \leq V_{DD}$$

To enhance reliability of operation, it is recommended to configure unused I/Os as inputs and to connect them to an appropriate logic voltage level such as V_{SS} or V_{DD}.

All the voltage in the following tables are referenced to V_{SS}.

Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings (Voltage Referenced to V_{SS}).

Symbol	Ratings	Value	Unit
V_{DD}	Recommended Supply Voltage	-0.3 to +6.0	V
V_{DDA}	Analog Reference Voltage	-0.3 to +9.0	V
V_{IN}	Input Voltage	V_{SS} -0.3 to VDD + 0.3	V
V_{OUT}	Output Voltage	V_{SS} -0.3 to VDD + 0.3	V
I_{IN}	Input Current	-10.....+10	mA
I_{OUT}	Output Current	-10.....+10	mA
T_A	Operating Temperature Range	0 to +70	^{O}C
T_{STG}	Storage Temperature Range	-65 to +150	^{O}C
PD	Power Dissipation	TBA	mW
ESD	ESD susceptibility	2000	V

Note: The maximum accumulated current off all I/O pins should not exceed 40 mA for V_{DD} and 40 mA for V_{SS}.

2.2 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \theta J_A) \quad (1)$$

Where:

– T_A is the Ambient Temperature in°C,

– θJ_A is the Package Junction-to-Ambient Thermal Resistance, in °C/W,

– P_D is the sum of P_{INT} and $P_{I/O}$,

– P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power

– $P_{I/O}$ represents the Power Dissipation on Input and Output Pins; User Determined.

For most applications $P_{I/O} < P_{INT}$ and may be neglected. $P_{I/O}$ may be significant if the device is configured to drive Darlington bases or sink LED Loads.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Therefore:

$$K = P_D \times (T_A + 273°C) + \theta J_A \times P_D^2 \quad (3)$$

Where:

– K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 3. Thermal Characteristics

Symbol	Package	Value	Unit
θJ_A	PSDIP56/CSDIP56W	60	°C/W

2.3 DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to +70°C unless otherwise specified

Symbol	Parameter	Test Conditions	Value			Unit
			min	typ	max	
V_{DD}	Supply Voltage		4.5		5.5	V
V_{OL}	Output Voltage Low Port A (Open drain)	I_{OL}=1.6 mA			0.4	V
V_{OL}	Output Voltage Low Port B (0-7), Port D(0:7) Push-pull	I_{OL}=1.6 mA			0.4	V
V_{OL}	Output Voltage Low Port C (PC2,PC3,PC4) Push-pull	I_{OL}=1.6 mA			0.4	V
V_{OL}	Output Voltage Low Port C (PC0,PC1,PC5) Open drain	I_{OL}=1.6 mA			0.4	V
V_{OL}	during Power ON Reset and Watch-dog Reset				0.4	V
V_{OH}	Output Voltage High Push-pull	I_{OH}=1.6 mA	V_{DD}-0.8			V
V_{IH}	Input High Voltage PA(0-7), PB(0-7), PC(0-5), PD(0-4), $\overline{\text{RESET}}$	Leading Edge	0.7xV_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage PA(0-7), PB(0-7), PC(0-5), PD(0-4), $\overline{\text{RESET}}$	Trailing Edge	V_{SS}		0.3xV_{DD}	V
I_{IL}	I/O Ports Hi-Z Leakage Current PA(0-7), PB(0-7), PC(0-5), PD(0-4), $\overline{\text{RESET}}$	V_{SS} V_{DD}			10	uA uA
C_{OUT} C_{IN}	Capacitance: Ports (as Input or Output), RESET				12 8	pF pF
R_{ON}	DA1,D(A3-17)(PWM/BRM) Serial Resistor			700	1000	Ohms
I_{RPU}	Pull-up resistor current	V_{DD}=5v V_{IN}=V_{SS}		20		uA

DC ELECTRICAL CHARACTERISTICS(Cont'd)

DDC Bus (I^2C INTERFACE)				
Symbol	**Parameter**	**Min**	**Max**	**Unit**
V_{HYS}	Hysteress of Shmitt trigger inputs fixed input levels V_{DD}-related input levels	 na na	 na na	V
T_{SP}	Pulse width of spikes which must be suppressed by the input filter	na	na	ns
T_{OF}	Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400pF with up 3mA sink current at VOL1		 250	ns
I	Input current each I/O pin with an input voltage between 0.4v and 0.9 V_{DD} max	-10	10	µA
C	Capacitive load for each I/O pin		10	pF

A/D CONVERTER						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Val	Resolution	F_{OSC} = 8 MHz		8		bit
Terr	Total Error	F_{OSC} = 8 MHz			± 3	LSB
Tcon	Conversion Time	F_{OSC} = 8 MHz	16			µs
Rva	Analog Source Impedance			30		KΩ

2.4 AC ELECTRICAL CHARACTERISTICS

(T_A = 0 to +70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ.	Max	
V_{DD}	Operating Supply Voltage	4 MHz Internal	4.5		5.5	V
I_{DD}	Supply Current	RUN Mode F_{ext} = 8MHz V_{DD} = 5.0V		7.5	10	mA
		WAIT Mode f_{ext} = 8MHz V_{DD} = 5.5V		3.5	5	mA

2.5 CONTROL TIMING

(Operating conditions T_A 0 to +70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ.	Max	
f_{OSC}	Frequency of Operation	V_{DD} = 4.5V f external f internal			8 4	MHz
t_{ILCH}	Halt Mode Recovery Startup Time				20	ms
t_{RL}	External RESET Input pulse Width		1.5			t_{CYC}
t_{PORL}	Power Reset Duration		4096			t_{CYC}
T_{DOGL}	Watchdog RESET Output Pulse Width		2		2	t_{CYC}
t_{DOG}	Watchdog Time-out		49,152		3,145,728	t_{CYC}
t_{ILIL}	Interrupt Pulse Period		(1)			t_{CYC}
t_{OXOV}	Crystal Oscillator Start-up Time				50	ms
t_{DDR}	Power up rise time	V_{DD} min			100	ms

Notes :
1. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 cycles.

AC ELECTRICAL CHARACTERISTICS(Cont'd)

2.5.1 DDC (I^2C BUS) INTERFACE

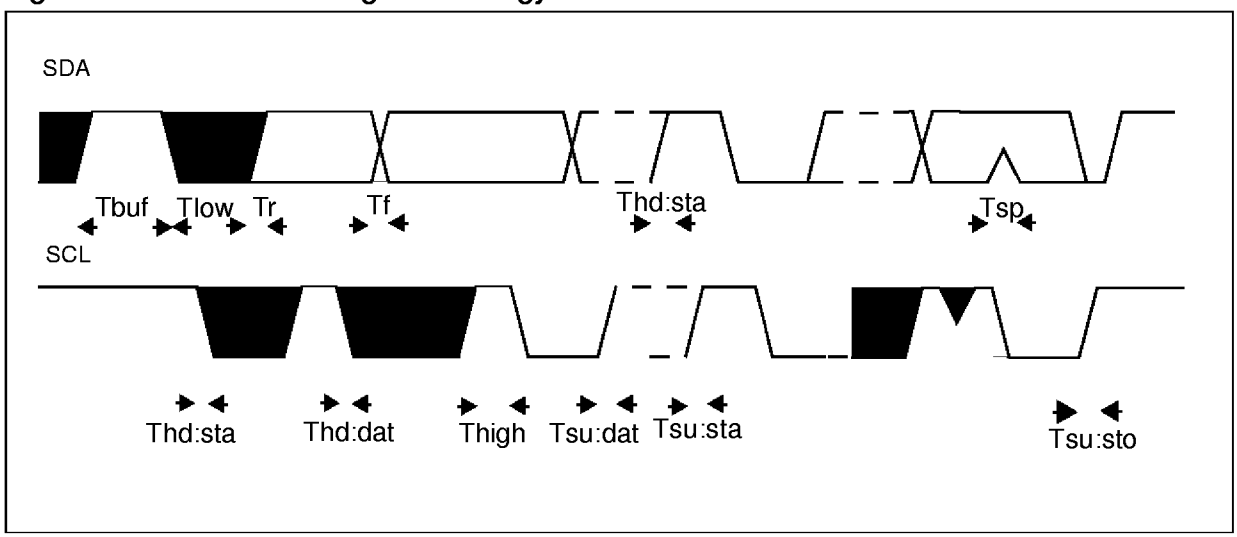
2.5.1.1 Timing

Parameter	Min	Max	Symbol	Unit
Bus free time between a STOP and START condition	4.7		Tubs	ms
Hold time START condition. After this period, the first clock pulse is generated	4.0		Thd:sta	µs
LOW period of the SCL clock	4.7		Tlow	µs
HIGH period of the SCL clock	4.0		Thigh	µs
Set-up time for a repeated START condition	4.7		Tsu:sta	µs
Data hold time	250 (1)		Thd:dat	ns
Data set-up time	250		Tsu:dat	ns
Rise time of both SDA and SCL signals		1000	Tr	ns
Fall time of both SDA and SCL signals		300	Tf	ns
Set-up time for STOP condition	4.0		Tsu:sto	ns
Capacitive load for each bus line		400	Cb	pF

1. The device provides a hold time of at least 250ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Cb = total capacitance of one bus line in pF

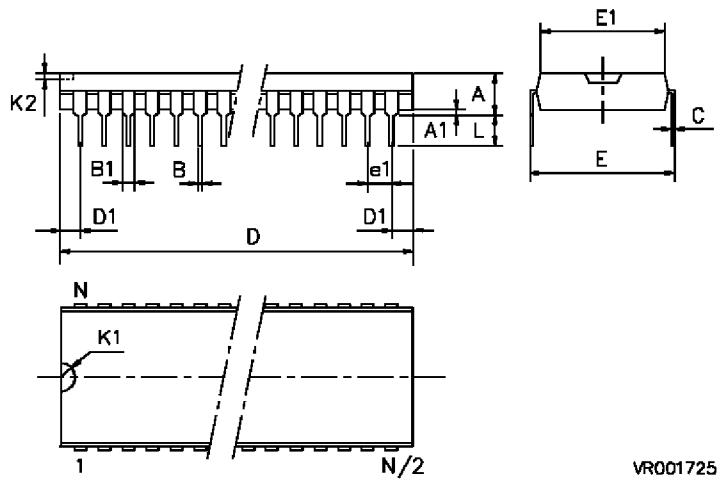
Figure 2. Definition of Timing Terminology



3 GENERAL INFORMATION

3.1 PACKAGE MECHANICAL DATA

Figure 3. 56 Shrink Plastic Dual In Line Package, 600-mil Width



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
B	0.35		0.59	0.014		0.023
B1	0.75		1.42	0.030		0.056
C	0.20		0.36	0.008		0.014
D		52.12			2.052	
D1	-	-	-	-	-	-
E			18.54			0.730
E1		13.72				0.540
K1	-	-	-	-	-	-
K2	-	-	-	-	-	-
L	2.54		3.81	0.100		0.150
e1		1.78			0.070	
Number of Pins						
N	56					

3.2 ORDERING INFORMATION

Sales Types	EPROM/OTP Size	RAM Size	Temperature Range	Package
ST72E72N5D1	24K	384	25°C	CSDIP56
ST72T72N5B1	24K	384	0 to +70°C	PSDIP56

ST72T72 MICROCONTROLLER OPTION LIST

Customer . . . . . .

Address . . . . . .

. . . . . .

Contact . . . . . .

Phone No . . . . . .

Reference . . . . . .

SGS-THOMSON Microelectronics references

Device:

[ ] ST72T72N5B1
24K OTP

CLPOUT OPTION:
Maximum delay 250ns
Programmable back porch clamping width
(0, 250ns, 500ns, 1 us)

Package: PSDIP56

[ ] ST72E72N5B1
24K EPROM

CLPOUT OPTION:
Maximum delay 250ns
Programmable back porch clamping width
(0, 250ns, 500ns, 1 us)

Package: CSDIP56

[ ] ST72T72M5B1
24K OTP

CLPOUT OPTION:
Maximum delay 125ns
Programmable back porch clamping width
(0, 125ns, 250ns, 500 us)

Package: PSDIP56

[ ] ST72E72M5B1
24K EPROM

CLPOUT OPTION:
Maximum delay 125ns
Programmable back porch clamping width
(0, 125ns, 250ns, 500 us)

Package: CSDIP56

Temperature Range: [ ] 0°C to + 70°C

Signature

Date

Notes:

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