ST3004

Speech Decoder/Encoder

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1. FEATURES

- **DSP based voice/audio processor**
- **Operation voltage**
  – Core logic: 2.25V~2.7V
  – I/O pads: 3.0V~3.6V
- **Voltage regulator for core logic**
- **Low Voltage Reset (LVR)**
  _ 2.5V low voltage reset
- **One PLL to generate high system frequency from a 4MHz source**
  _ 12M~28MHz PLL output
- **Tow clock sources**
  _ Crystal.....4MHz
  _ External input.....4MHz
- **Low power down current**
  _Typical current: 3uA
- **One 16-bit programmable Timer**
- **One clocking output**
- **One external interrupt**
  _ Edge/level trigger supported
- **One 14-bit direct-drive DAC**
  – Maximum current: 145mA
- **MCU interfaces**
  _ Serial mode
  _ Parallel mode
- **Two Serial PORT interfaces(SP)**
  _ Programmable data length from 8-bit to 16-bit
  _ I2S, Left/Right Justified interfaces to external DAC/ADC
- **Speech playback/recorder**
  _ Low Bit Rate Compression (LBRC)
    _ 1.2K/1.6K/2.4Kbps@8KHz playback
    _ 1.6K/2.2K/3.3Kbps@11.025KHz playback
  _ High Bit Rate Compression (HBRC)
    _ 12K/16K/24Kbps@8KHz playback
    _ 16.5K/22K/33Kbps@11.025KHz playback
    _ 24K/32K/48Kbps@16KHz playback
    _ 12k/16k/24kbps@8KHz encoder
  _ PCM playback
  _ TTS
  _ LPC
  _ RS-Word
  _ RS-PY
  _ Time stretch (half~double speed)

2. GENERAL DESCRIPTION

The ST3004 is a highly integrated and cost-effective DSP based audio processor for various consumer applications. It consists of one powerful DSP for advanced voice decoder and encoder algorithms of natural speech with less memory. It provides low bit rate compression (LBRC) for voice playback and high bit rate compression (HBRC) for audio or better voice quality. Both LBRC and HBRC can playback simultaneously. For encoder, it has capability to compress PCM raw data from MCU and send back encoded data to MCU. TTS, LPC, RS-Word, and RS_PY algorithms are also available for various voice applications. ST3004 can adjust playback frequency (half~double speed) without pitch shifting.

System clock comes from 4MHz crystal or external input.

ST3004 has 32 I/Os and these can be either GPIO or functional pins. Each pin can be programmed to input or output. One external interrupt pin can be requested by external devices.

One internal 14bit DAC can provide significant volume equipping with internal amplifier. For particular application or recorder, two general audio interfaces are supported to interface with external DAC/ADC. Audio interface can be configured to I2S or Left/Right Justified compatible mode.

There are serial and parallel interfaces for various connections with different MCUs.

2.1 Block Diagram

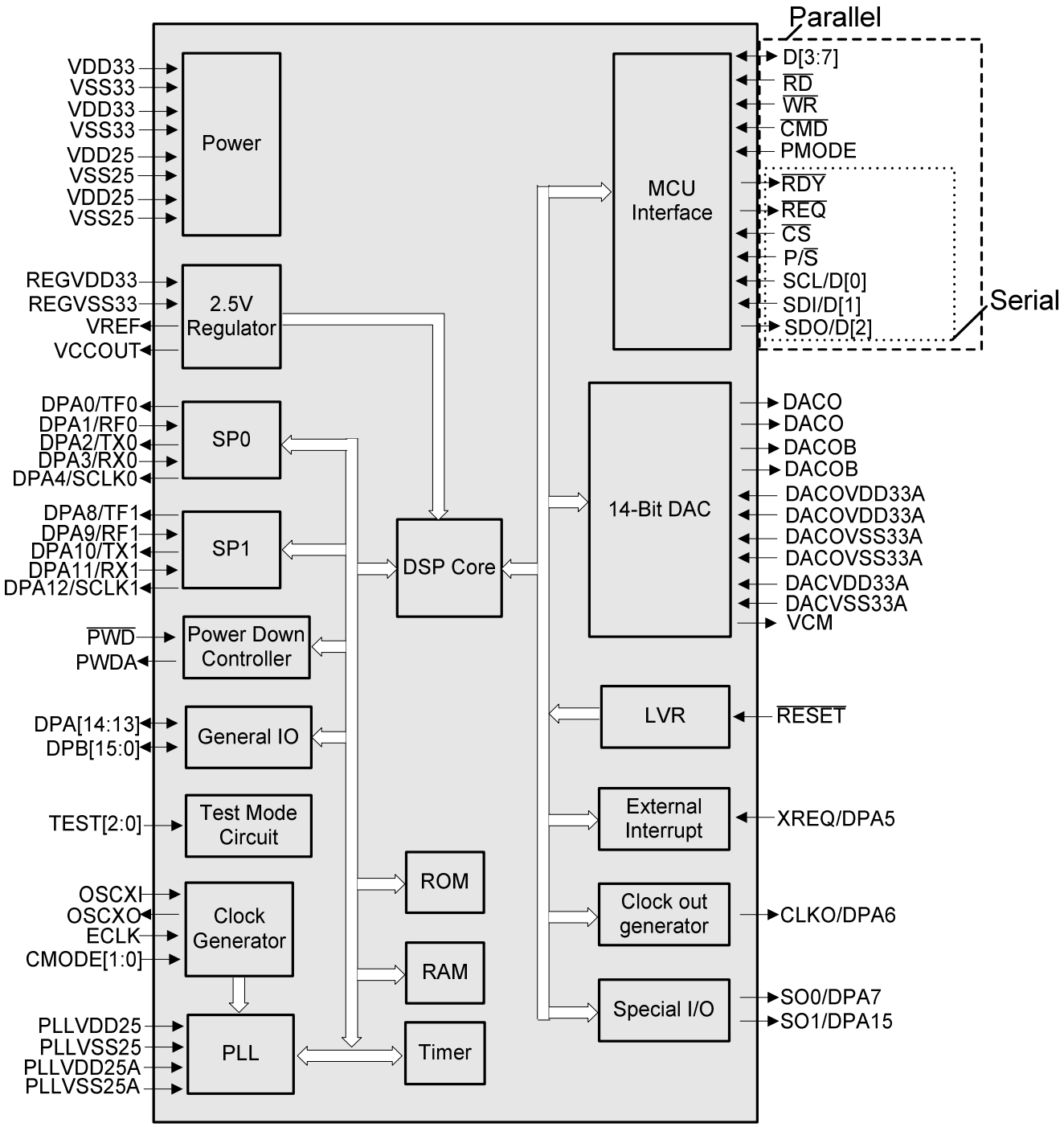


Figure 2-1 ST3004 Block Diagram

3. SIGNAL DESCRIPTIONS

Table 3-1 Signal Function Description

Function Group	Pin Name	Pin #	I/O	Description
System control	RESET	1	I	System reset, low active
	PWD	1	I	Power down, low active
	PWDA	1	O	Power down acknowledge, high active
	OSCXI	1	I	Crystal input or R-oscillator input. If not used, it connects to GND
	OSXO	1	O	Crystal output. If not used, it connects to GND
	ECLK	1	I	External clock input. If not used, it connects to GND
	CMODE[1:0]	2	I	Clock source select 01=Crystal. ECLK connects to GND 1X=ECLK. OSCXI and OSXO connect to GND
	TEST[2:0]	3	I	Test mode. TEST[2:0] connect to GND
Special I/O	SO[1:0]/ DPA[7,15]	2	O	SO0/DPA[7], SO1/DPA[15]
	CLKO/ DPA[6]	1	O	Clock output/DPA[6]
GPIO	DAP[13,14], DPB[0:15]	18	I/O	General I/O
External Interrupt	XREQ/DPA[5]	1	I	External interrupt/DPA[5]
Serial Port0/ DPA[4:0]	TF0/DPA[0]	1	O	Transmit frame synchronization/DPA[0]
	RF0/DPA[1]	1	I	Receive frame synchronization/DPA[1]
	TX0/DPA[2]	1	O	Serial data transmit/DPA[2]
	RX0/DPA[3]	1	I	Serial data receive/DPA[3]
	SCLK0/DPA[4]	1	O	Serial clock/DPA[4]
Serial Port1/ DPA[12:8]	TF1/DPA[8]	1	O	Transmit frame synchronization/DPA[8]
	RF1/DPA[9]	1	I	Receive frame synchronization/DPA[9]
	TX1/DPA[10]	1	O	Serial data transmit/DPA[10]
	RX1/DPA[11]	1	I	Serial data receive/DPA[11]
	SCLK1/DPA[12]	1	O	Serial clock/DPA[12]
MCU Interface	D[0]/SCL	1	I/O	Parallel : Data bus Serial : Serial clock
	D[1]/SDI	1	I/O	Parallel : Data bus Serial : Serial data input
	D[2]/SDO	1	I/O	Parallel : Data bus Serial : Serial data output
	D[3:7]	5	I/O	Parallel : Data bus Serial : Not used
	WR	1	I	Parallel : Write enable, low active Serial : Not used
	RD	1	I	Parallel : Read enable, low active Serial : Not used
	CS	1	I	Parallel : Chip select, low active Serial : Chip select
	CMD	1	I	Parallel : Command/data select “H”: Data “L”: Command Serial : Not used

	REQ	1	O	DSP wants to sent command to MCU, low active
	RDY	1	O	DSP permit MCU access data, low active
	PMODE	1	I	Parallel interface select 0: Parallel (default). Connecting to GND 1: Not used
	P/S	1	I	Parallel/serial interface select 0: Serial 1: Parallel
Power	VDD25	2	I	2.5V power
	VSS25	2	I	2.5V power ground
	VDD33	2	I	3.3V power
	VSS33	2	I	3.3V power ground
	REGVDD33	1	I	Digital power input of regulator
	REGVSS33	1	I	Digital power ground of regulator
	PLLVDD25	1	I	Digital power input of PLL
	PLLVSS25	1	I	Digital power ground of PLL
	PLLVDD25A	1	I	Analog power input of PLL
	PLLVSS25A	1	I	Analog power ground of PLL
	DACVDD33A	1	I	Analog power input of DAC
	DACVSS33A	1	I	Analog power ground of DAC
	DACOVDD33A	2	I	Analog power input of DAC output stage
	DACOVSS33A	2	I	Analog power ground of DAC output stage
Regulator	VCCOUT	1	O	2.5V output of regulator
	VREF	1	O	Voltage reference
DAC	DACO	2	O	DAC direct drive pin(+)
	DACOB	2	O	DAC direct drive pin(-)
	VCM	1	O	Common mode voltage reference

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Rations

DC Supply Voltage: VDD33 ---------- -0.3V to +4.5V
Operating Ambient Temperature --------- -10°C to +60°C
Storage Temperature ---------- -10°C to +125°C

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. All the ranges are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC Electrical Characteristics

Standard operation conditions: VDD33 = 3.3V, GND = 0V, T_A = 25°C, unless otherwise specified

Table 4-1 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	VDD33	3.0		3.6	V	
Operating Voltage	VDD25	2.25	2.5	2.7	V	
Operating Current	I_{OP1}		30		mA	Run at 24MHz without speaker
Power Down Current	I_{PD}		3	4.5	μA	
Output driving	I_{od}		16		mA	
Output sinking	I_{os}		26		mA	
Input low voltage	V_{IL}		0.6		V	
Input high voltage	V_{IH}		1.3		V	
Pull-up resistor	R_{PU}		54		KΩ	
Pull-down resistor	R_{PD}		50		KΩ	
Low Voltage Reset Level	V_{LVR}	2.4	2.5	2.6	V	

4.3 AC Electrical Characteristics

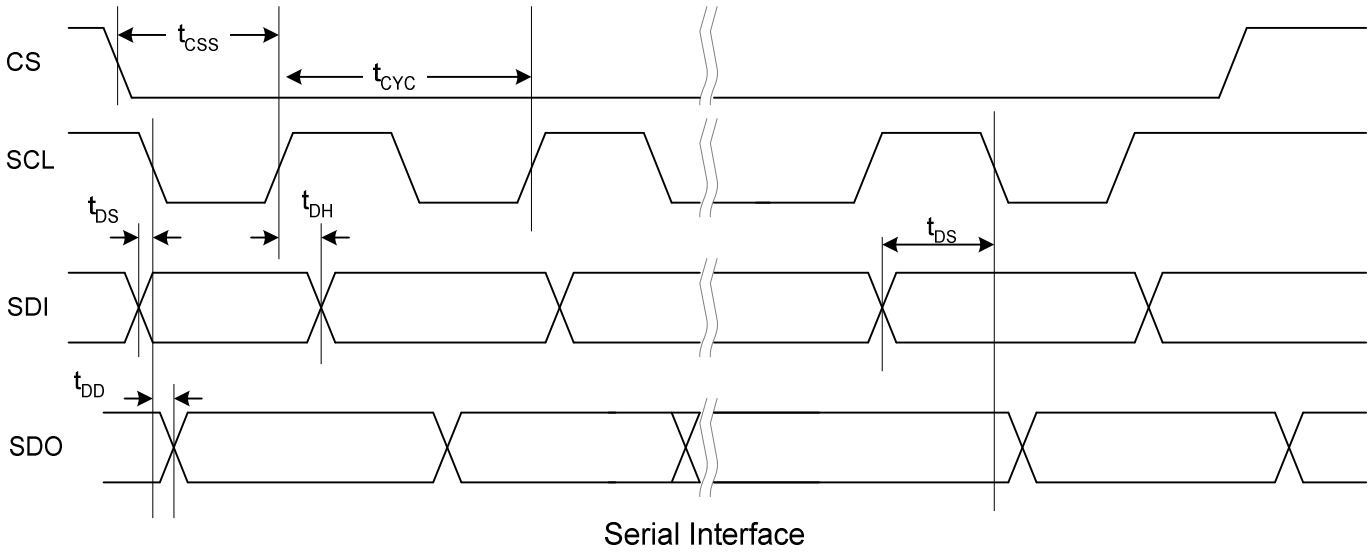


Figure 4-1 Serial Interface Timing Diagram

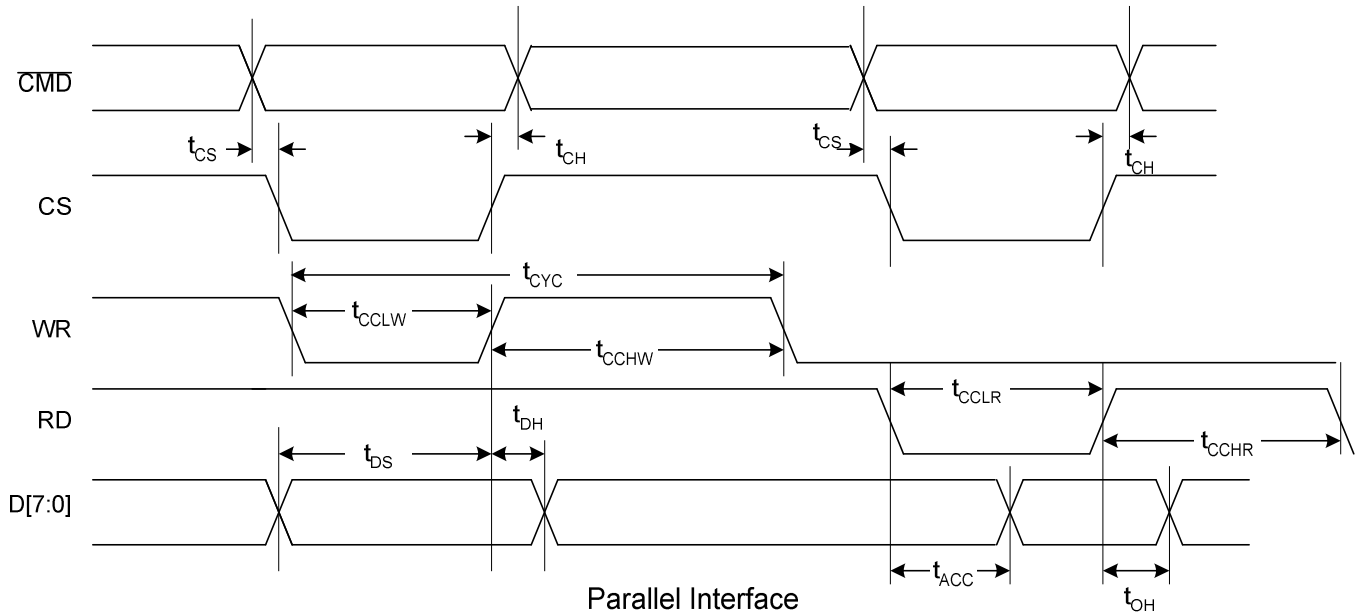


Figure 4-2 Parallel Interface Timing Diagram

Table 4-2 Timing parameters for 0

Standard operation conditions: VDD33 = 3.3V, GND = 0V, T_A = 25°C

Symbol	Characteristic	Rating			Unit
		Min.	Typ.	Max.	
t_{CSS}	CS low to 1st SCL rising	100			nS
t_{CYC}	SCL cycle time	200			nS
t_{DS}	Data valid prior SCL falling	0			nS
t_{DH}	Data Hold time after SCL rising	10			nS
t_{DD}	SDO output delay from SCL falling			10	nS

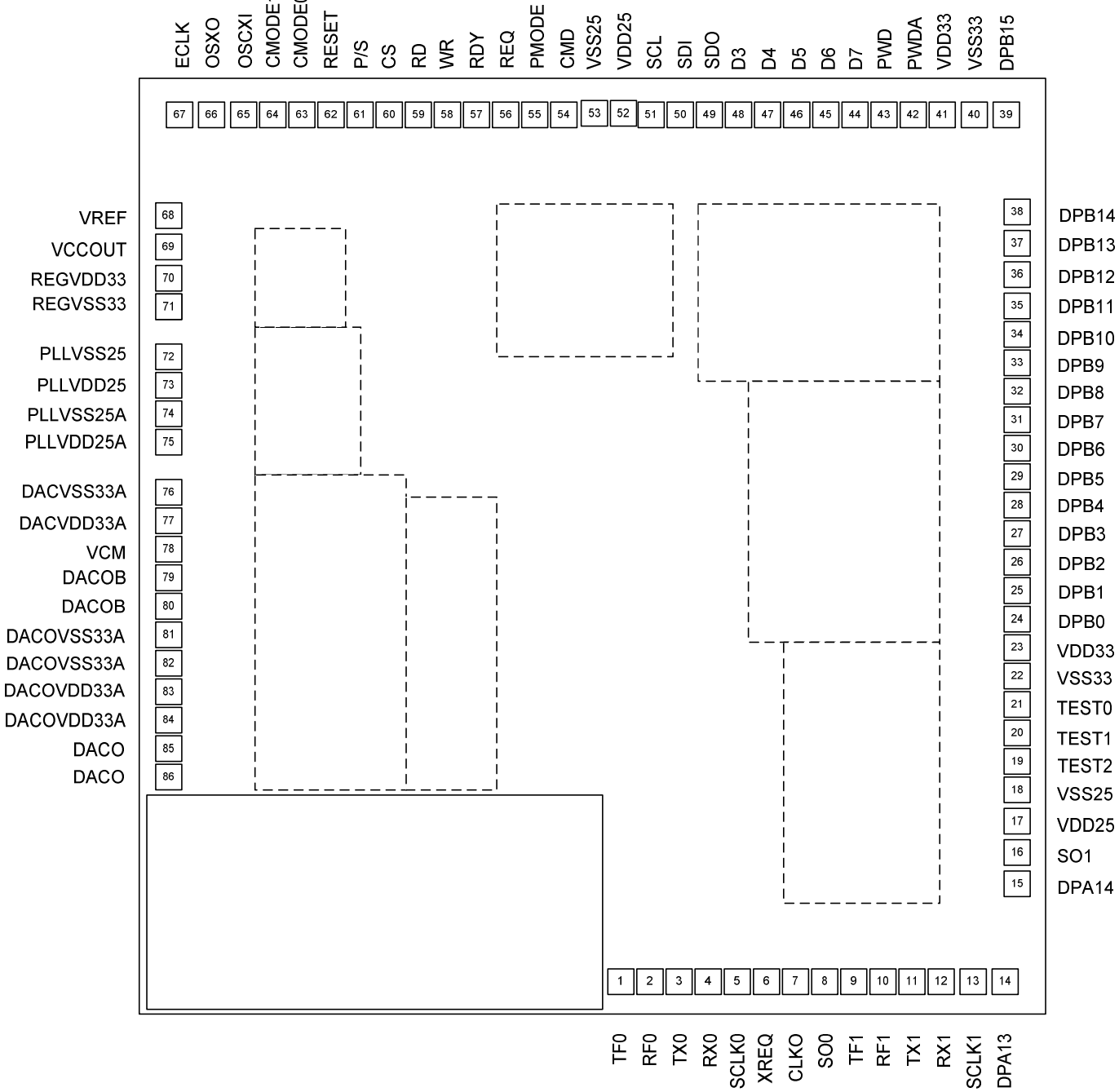
Table 4-3 Timing parameters for 0

Standard operation conditions: VDD33 = 3.3V, GND = 0V, T_A = 25°C

Symbol	Characteristic	Rating			Unit
		Min.	Typ.	Max.	
t_{CH}	Cmd pin hold time	5			nS
t_{CS}	Cmd pin setup time	5			nS
t_{CYC}	System cycle time	3.5D			nS
t_{CCLW}	Write pulse width	0.5D			nS
t_{CCHW}	Enable H write width	3D			nS
t_{CCLR}	Read pulse width	0.5D			nS
t_{CCHR}	Enable H read width	3D			nS
t_{DS}	Write data setup time	0.5D			nS
t_{DH}	Write data hold time	5			nS
t_{ACC}	Read access time			25	nS
t_{OH}	Read data disable time	4			nS

Remark: D = time of one DSP system clock

5. PAD DIAGRAM



6. DEVICE INFORMATION

1. **Substrate: GND**

PAD No.	Symbol	X	Y
1	TF0	1616.23	62.5
2	RF0	1716.23	62.5
3	TX0	1816.23	62.5
4	RX0	1916.23	62.5
5	SCLK0	2016.23	62.5
6	XREQ	2116.23	62.5
7	CLKO	2216.23	62.5
8	SO0	2316.23	62.5
9	TF1	2416.23	62.5
10	RF1	2516.23	62.5
11	TX1	2616.23	62.5
12	RX1	2716.23	62.5
13	SCLK1	2826.23	62.5
14	DPA13	2936.23	62.5
15	DPA14	2977.5	406.55
16	SO1	2977.5	516.55
17	VDD25	2977.5	626.55
18	VSS25	2977.5	736.55
19	TEST2	2977.5	836.55
20	TEST1	2977.5	936.55
21	TEST0	2977.5	1036.55
22	VSS33	2977.5	1136.55
23	VDD33	2977.5	1236.55
24	DPB0	2977.5	1336.55
25	DPB1	2977.5	1436.55
26	DPB2	2977.5	1536.55
27	DPB3	2977.5	1636.55
28	DPB4	2977.5	1736.55
29	DPB5	2977.5	1836.55
30	DPB6	2977.5	1936.55

PAD No.	Symbol	X	Y
31	DPB7	2977.5	2036.55
32	DPB8	2977.5	2136.55
33	DPB9	2977.5	2236.55
34	DPB10	2977.5	2336.55
35	DPB11	2977.5	2436.55
36	DPB12	2977.5	2546.55
37	DPB13	2977.5	2656.55
38	DPB14	2977.5	2766.55
39	DPB15	2940	3107.5
40	VSS33	2830	3107.5
41	VDD33	2720	3107.5
42	PWDA	2620	3107.5
43	PWD	2520	3107.5
44	D7	2420	3107.5
45	D6	2320	3107.5
46	D5	2220	3107.5
47	D4	2120	3107.5
48	D3	2020	3107.5
49	SDO	1920	3107.5
50	SDI	1820	3107.5
51	SCL	1720	3107.5
52	VDD25	1620	3107.5
53	VSS25	1520	3107.5
54	CMD	1420	3107.5
55	PMODE	1320	3107.5
56	REQ	1220	3107.5
57	RDY	1120	3107.5
58	WR	1020	3107.5
59	RD	920	3107.5
60	CS	820	3107.5

PAD No.	Symbol	X	Y
61	P/S	720	3107.5
62	RESET	620	3107.5
63	CMODE0	520	3107.5
64	CMODE1	420	3107.5
65	OSCXI	320	3107.5
66	OSXO	210	3107.5
67	ECLK	100	3107.5
68	VREF	62.5	2753.04
69	VCCOUT	62.5	2643.04
70	REGVDD33	62.5	2533.04
71	REGVSS33	62.5	2433.04
72	PLLVSS25	62.5	2257.04
73	PLLVDD25	62.5	2157.04
74	PLLVSS25A	62.5	2057.04
75	PLLVDD25A	62.5	1957.04
76	DACVSS33A	62.5	1781.04
77	DACVDD33A	62.5	1681.04
78	VCM	62.5	1581.04
79	DACOB	62.5	1481.04
80	DACOB	62.5	1381.04
81	DACOVSS33A	62.5	1281.04
82	DACOVSS33A	62.51	1181.04
83	DACOVDD33A	62.5	1081.04
84	DACOVDD33A	62.5	981.04
85	DACO	62.5	881.04
86	DACO	62.5	781.04

7. APPLICATION CIRCUIT

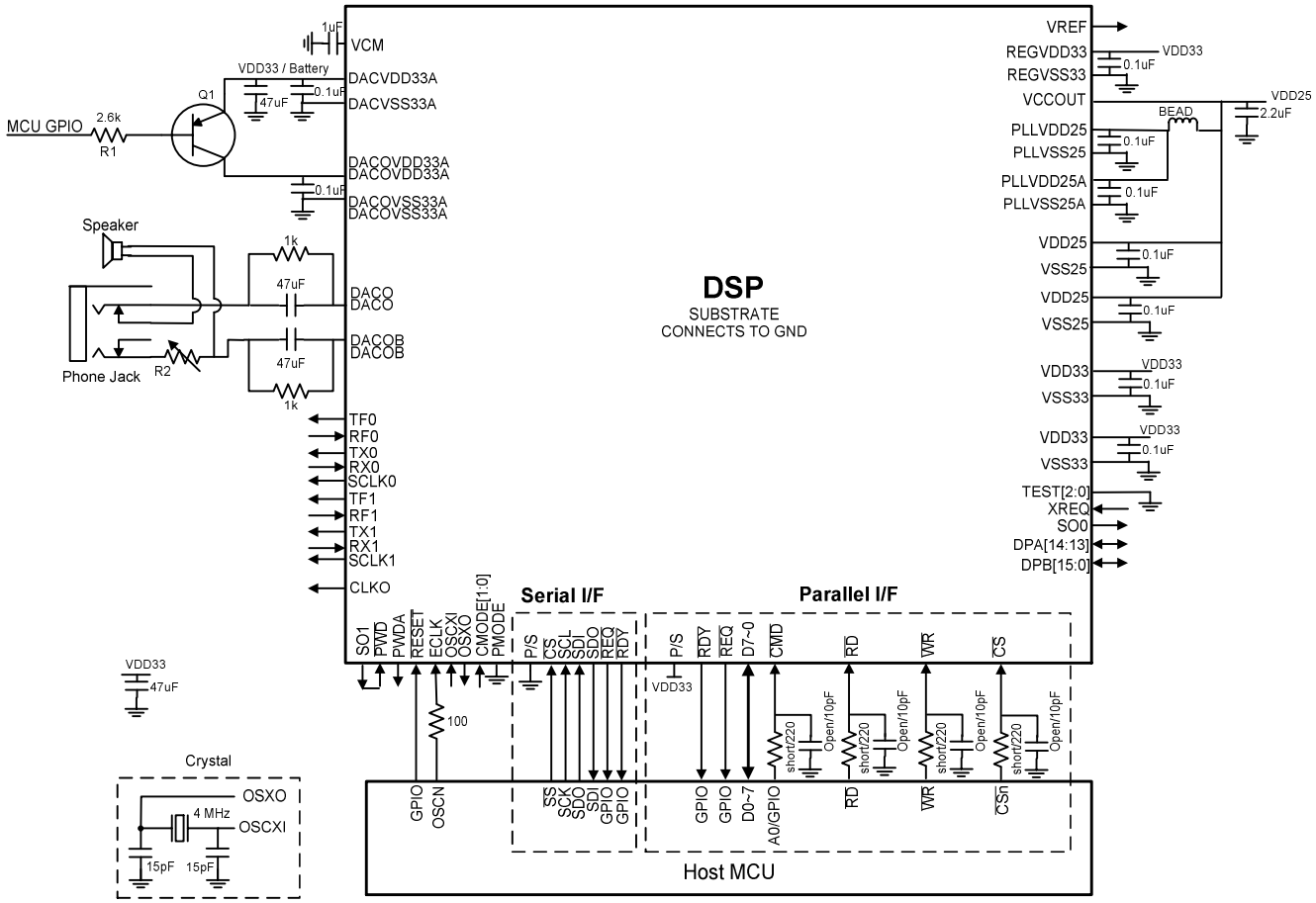


Figure 7-1 Application Circuit Diagram

Note:

1. 47uF capacitor must be close to DACOVDD33A and DACOVSS33A.
2. If any of OSCXI, OSXO, and ECLK is not used, it needs to connect to GND.
3. The cascade resistor and parallel capacitor on CMD, RD, WR, and CS pins can reduce noise interference. In general, resistor is short and capacitor is open. Please preserve the options on PCB.
4. R2 resistor can adjust headphone volume.

8. REVISION

REVISION	DESCRIPTION	PAGE	DATE
0.2	First release		2005/05/12
0.3	1. Modify DAC driving capacity 2. Change IREF to DACVDD33A, change CLICK to DACVSS33A 3. Rename DACVDD33A to DACOVDD33A, rename DACVSS33A to DACOVSS33A	1 2,4,8,9,10 2,4,8,9,10	2005/06/27
0.4	1. TEST[2:0] wire to GND 2. WR, RD cascade 120 Ohm and parallel 10p capacitor 3. ECLK cascade 100 Ohm to low noise 4. Remove R-Oscillator function	1 10 10 1,3,10	2005/0705
0.5	1. System low voltage changes from 2.7V to 3.0V 2. The resistor in RD/WR changes from 120Ohm to 220Ohm	1 10	2005/08/02
0.6	1. Change PLL output frequency from 32MH to 28MHz 2. Add inductor and capacitor before power input, revise regulator output capacitor, DACVDD33A and DACOVDD33A power come from battery, add 4MHz crystal label	1 10	2005/09/05
0.7	1. Add CMODE, ECLK, TEST pins descriptions 2. Revise PMODE pin parallel interface select description 3. Revise output driving/sinking, input low/high, and input pull-up/pull-down resistor DC electrical characteristics 4. Revise Read access time from 10ns to 25ns 5. Remove external DAC/ADC block, DC2DC block. Add headphone jack and CMD pin cascade resistor and parallel capacitor. Revise DAC power circuit. Add note item 2 to 4	3 4 5 7 10	2006/02/22
0.8	1. Revise parallel interface timing diagram(CWD pin change to CMD Pin) 2. Application circuit diagram Add parallel capacitor and cascade resistor circuit on CS pin	6 10	2006/04/25

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