ST16C550

UART WITH 16-BYTE FIFO's

April 2005

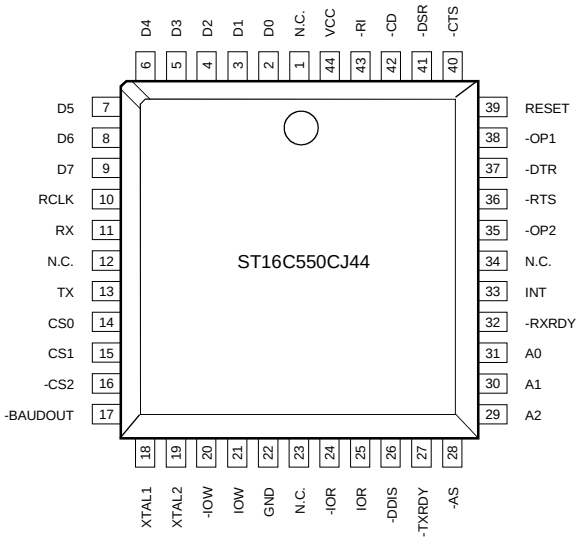
GENERAL DESCRIPTION

The ST16C550 (550) is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. It operates at 2.97 to 5.5 volts. A programmable baud rate generator can select transmit and receive clock rates from 50 bps to 1.5 Mbps.

The ST16C550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C550 provides internal loopback capability for on board diagnostic testing.

The ST16C550 is available in 40 pin PDIP, 44 pin PLCC, and 48 pin TQFP packages. It is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Pin to pin and functionally compatible to the Industry Standard 16C550
- 2.97 to 5.5 volt operation
- 24MHz clock operation at 5V
- 16MHz clock operation at 3.3V
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Full duplex operation
- Transmit and receive control
- Four selectable receive FIFO interrupt trigger levels
- Standard modem interface
- Compatible with ST16C450
- Low operating current (1.2mA typ.)

ORDERING INFORMATION

Part number	Package	Operating temperature	Device Status
ST16C550CP40	40-Lead PDIP	0° C to + 70° C	Active. See the ST16C550CQ48 for new designs.
ST16C550CJ44	44-Lead PLCC	0° C to + 70° C	Active
ST16C550CQ48	48-Lead TQFP	0° C to + 70° C	Active
ST16C550IP40	40-Lead PDIP	-40° C to + 85° C	Active. See the ST16C550IQ48 for new designs.
ST16C550IJ44	44-Lead PLCC	-40° C to + 85° C	Active
ST16C550IQ48	48-Lead TQFP	-40° C to + 85° C	Active

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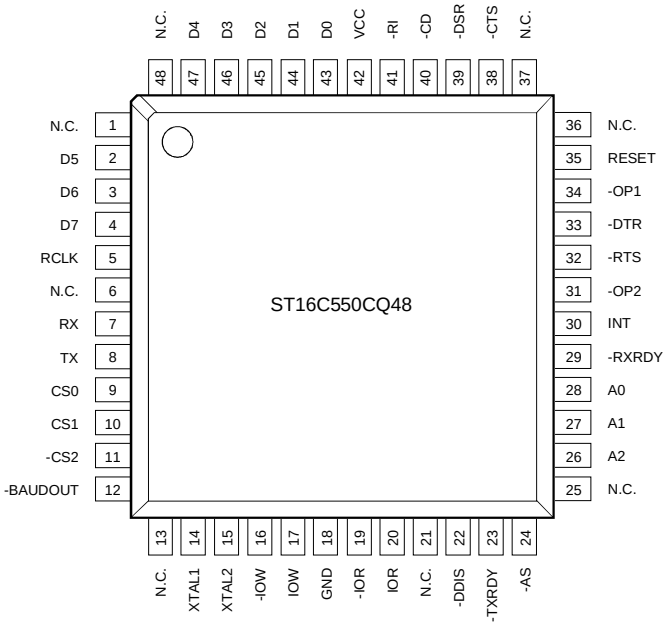
Figure 1, PACKAGE DESCRIPTION, ST16C550

48 Pin TQFP Package



40 Pin DIP Package

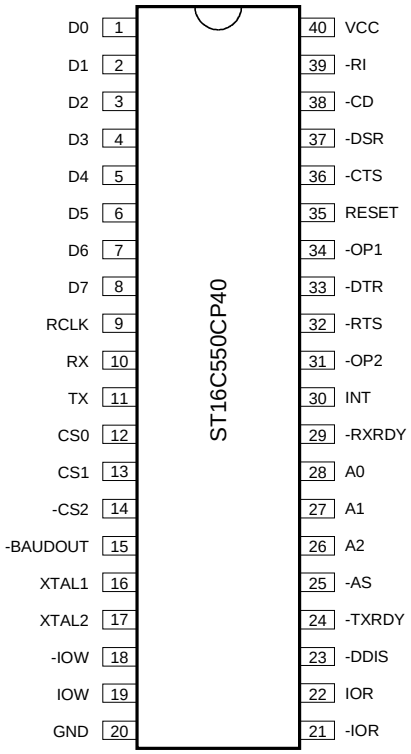
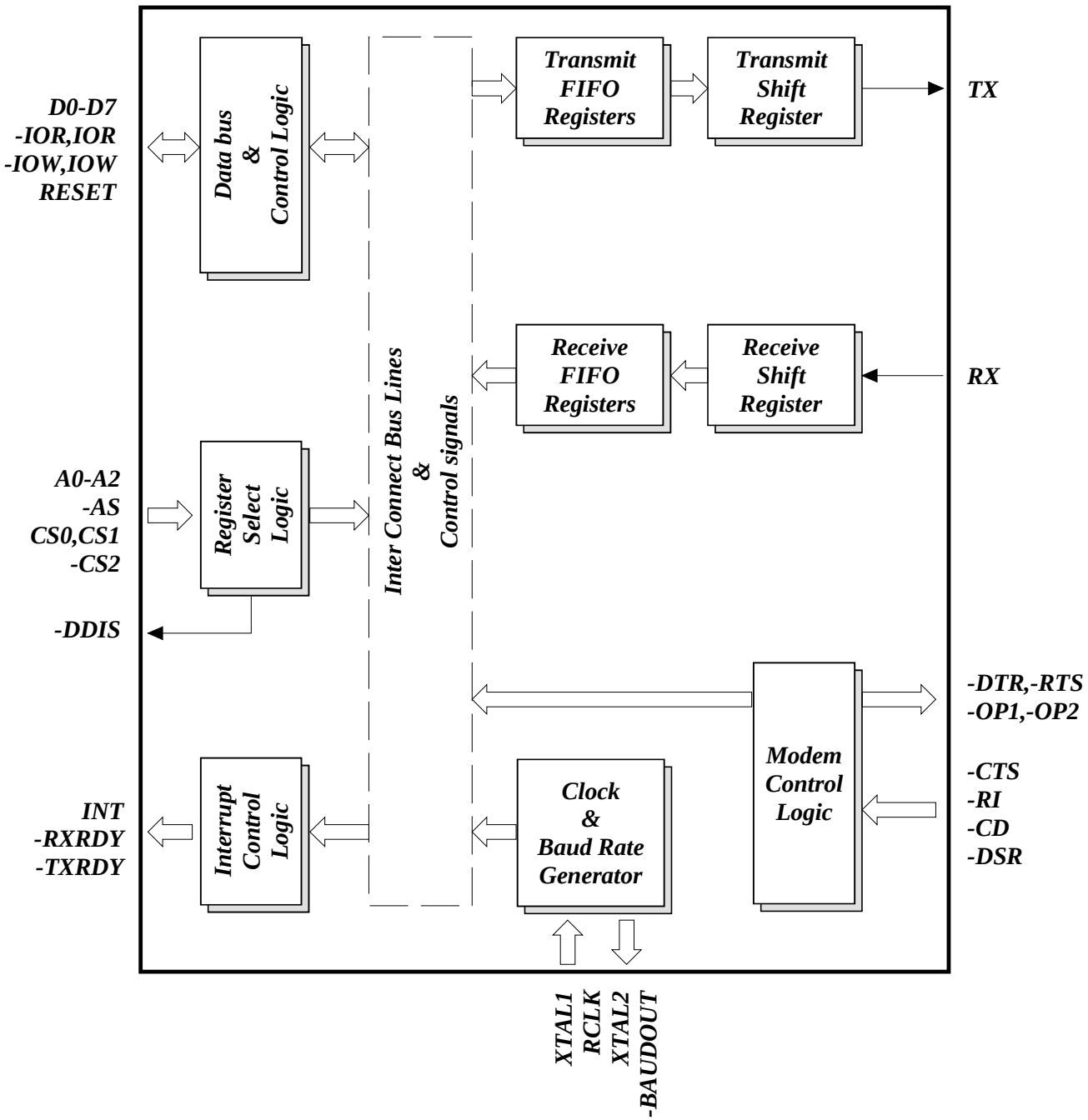


Figure 2, BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Pin 48	Signal type	Pin Description
A0	28	31	28	I	Address-0 Select Bit Internal registers address selection.
A1	27	30	27	I	Address-1 Select Bit Internal registers address selection.
A2	26	29	26	I	Address-2 Select Bit Internal registers address selection.
IOR	22	25	20	I	Read data strobe. Its function is the same as -IOR (see -IOR), except it is active high. Either an active -IOR or IOR is required to transfer data from 16C550 to CPU during a read operation. Connect to logic 0 when using -IOR.
CS0	12	14	9	I	Chip Select-0. Logical 1 on this pin provides the chip select-0 function. Connect CS0 to logic 1 if using CS1 or -CS2.
CS1	13	15	10	I	Chip Select-1. Logical 1 on this pin provides the chip select-1 function. Connect CS1 to logic 1 if using CS0 or -CS2.
-CS2	14	16	11	I	Chip Select -2. Logical 0 on this pin provides the chip select-2 function. Connect to logic 0 if using CS0 or CS1.
IOW	19	21	17	I	Write data strobe. Its function is the same as -IOW (see -IOW), but it acts as an active high input signal. Either -IOW or IOW is required to transfer data from the CPU to ST16C550 during a write operation. Connect to logic 0 when using -IOW.
-AS	25	28	24	I	Address Strobe. A logic 1 transition on -AS latches the state of the chip selects and the register select bits, A0-A2. This input is used when address and chip selects are not stable for the duration of a read or write operation, i.e., a microprocessor that needs to de-multiplex the address and data bits. If not required, the -AS input can be permanently tied to a logic 0.
D0-D7	1-8	2-9	43-47 2-4	I/O	Data Bus (Bi-directional) - These pins are the eight bit, tri-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
GND	20	22	18	Pwr	Signal and Power Ground.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Pin 48	Signal type	Pin Description
-IOR	21	24	19	I	Read data strobe (active low strobe). A logic 0 on this pin transfers the contents of the ST16C550 data bus to the CPU. Connect to logic 1 when using IOR.
-IOW	18	20	16	I	Write data strobe (active low strobe). A logic 0 on this pin transfers the contents of the CPU data bus to the addressed internal register. Connect to logic 1 when using IOW.
INT	30	33	30	O	Interrupt Request (active high). Interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected.
-RXRDY	29	32	29	O	Receive Ready. When operating in the FIFO mode, one of two types of DMA signaling can be selected using the FIFO control register bit-3. When operating in the ST16C450 mode, only DMA mode “0” is allowed. Mode “0” supports single transfer DMA in which a transfer is made between CPU bus cycles. Mode “1” supports multi-transfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode “0” -RXRDY is low, when there is at least one character in the receiver FIFO or receive holding register. In DMA mode “1”, -RXRDY is low, when the trigger level or the time-out has been reached.
-TXRDY	24	27	23	O	Transmit Ready. When operating in the FIFO mode, one of two types of DMA signaling can be selected using the FIFO control register bit-3. When operating in the ST16C450 mode, only DMA mode “0” is allowed. Mode “0” supports single transfer DMA in which a transfer is made between CPU bus cycles. Mode “1” supports multi-transfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
-BAUDOUT	15	17	12	O	Baud Rate Generator Output. This pin provides the 16X clock of the selected data rate from the baud rate generator. The RCLK pin must be connected externally to -BAUDOUT when the receiver is operating at the same data rate.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Pin 48	Signal type	Pin Description
-DDIS	23	26	22	O	Drive Disable. This pin goes to a logic 0 when the external CPU is reading data from the ST16C550. This signal can be used to disable external transceivers or other logic functions.
-OP1	34	38	34	O	Output-1 (User Defined) - See bit-2 of modem control register (MCR bit-2).
RESET	35	39	35	I	Reset. (active high) - A logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See ST16C550 External Reset Conditions for initialization details.)
RCLK	9	10	5	I	Receive Clock Input. This pin is used as external 16X clock input to the receiver section. External connection to - Baudout pin is required in order to utilize the internal baud rate generator.
-OP2	31	35	31	O	Output-2 (User Defined). This pin provides the user a general purpose output. See bit-3 modem control register (MCR bit-3).
VCC	40	44	42	Pwr	Power Supply Input.
XTAL1	16	18	14	I	Crystal or External Clock Input - Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. An external 1 MΩ resistor is required between the XTAL1 and XTAL2 pins (see figure 3). Alternatively, an external clock can be connected to this pin to provide custom data rates (Programming Baud Rate Generator section).
XTAL2	17	19	15	O	Output of the Crystal Oscillator or Buffered Clock - (See also XTAL1). Crystal oscillator output or buffered clock output.
-CD	38	42	40	I	Carrier Detect (active low) - A logic 0 on this pin indicates that a carrier has been detected by the modem.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Pin 48	Signal type	Pin Description
-CTS	36	40	38	I	Clear to Send (active low) - A logic 0 on the -CTS pin indicates the modem or data set is ready to accept transmit data from the ST16C550. Status can be tested by reading MSR bit-4. This pin has no effect on the UART's transmit or receive operation.
-DSR	37	41	39	I	Data Set Ready (active low) - A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.
-DTR	33	37	33	O	Data Terminal Ready (active low) - A logic 0 on this pin indicates that the ST16C550 is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR bit-0 will set the -DTR output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR bit-0, or after a reset. This pin has no effect on the UART's transmit or receive operation.
-RI	39	43	41	I	Ring Indicator (active low) - A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
-RTS	32	36	32	O	Request to Send (active low) - A logic 0 on the -RTS pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register (MCR bit-1) will set this pin to a logic 0 indicating data is available. After a reset this pin will be set to a logic 1. This pin has no effect on the UART's transmit or receive operation.
RX	10	11	7	I	Receive Data - This pin provides the serial receive data input to the ST16C550. A logic 1 indicates no data or an idle channel. During the local loop-back mode, the RX input pin is disabled and TX data is internally connected to the UART RX Input, internally, see figure 12.
TX	11	13	8	O	Transmit Data - This pin provides the serial transmit data from the ST16C550, the TX signal will be a logic 1 during reset, idle (no data). During the local loop-back mode, the TX pin is set to a logic 1 and TX data is internally connected to the UART RX Input, see figure 12.

GENERAL DESCRIPTION

The ST16C550 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The ST16C550 represents such an integration with greatly enhanced features. The ST16C550 is fabricated with an advanced CMOS process.

The ST16C550 is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of 1 byte provided in the 16C450. The ST16C550 is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the ST16C550 by the larger transmit and receive FIFO's. This allows the external processor to handle more networking tasks within a given time. The 4 selectable levels of FIFO trigger provided for maximum data throughput performance especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The ST16C550 is capable of operation to 1.5Mbps with a 24 MHz crystal or external clock input.
With a crystal of 14.7464 MHz and through a software option, the user can select data rates up to 460.8Kbps or 921.6Kbps.

FUNCTIONAL DESCRIPTIONS

Internal Registers

The ST16C550 provides 12 internal registers for monitoring and control. These registers are shown in Table 3 below. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers, (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user assessable scratchpad register (SPR).

Table 2, INTERNAL REGISTER DECODE

A2	A1	A0	READ MODE	WRITE MODE
General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR):				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	Reserved
1	1	0	Modem Status Register	Reserved
1	1	1	Scratchpad Register	Scratchpad Register
Baud Rate Generator Registers (DLL/DLM). Accessible only when LCR bit-7 is set to 1.				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

FIFO Operation

The 16 byte transmit and receive data FIFO's are enabled by the FIFO Control Register (FCR) bit-0. With 16C550 devices, the user can set the receive trigger level but not the transmit trigger level. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Time-out Interrupts

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER bit-0). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case the ST16C550 FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should recheck LSR bit-0 for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read (see Figure 10, Receive Time-out Interrupt). The actual time out value is T (**T**ime out length in bits) = 4 X P (**P**rogrammed word length) + 12. To convert the time out value to a character value, the user has to consider the complete word length, including data information length, start bit, parity bit, and the size of stop bit, i.e., 1X, 1.5X, or 2X bit times.

Example -A: If the user programs a word length of 7, with no parity and one stop bit, the time out will be: T = 4 X 7(programmed word length) +12 = 40 bit times. The character time will be equal to 40 / 9 = 4.4 characters, or as shown in the fully worked out ex-

ample: T = [(programmed word length = 7) + (stop bit = 1) + (start bit = 1) = 9]. 40 (bit times divided by 9) = 4.4 characters.

Example -B: If the user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bit times.
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

Programmable Baud Rate Generator

The ST16C550 supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example a 33.6Kbps modem that employs data compression may require a 115.2Kbps input data rate. A 128.0Kbps ISDN modem that supports data compression may need an input data rate of 460.8Kbps. The ST16C550 can support a standard data rate of 921.6Kbps.

The programmable Baud Rate Generator is capable of accepting an input clock up to 24 MHz, as required for supporting a 1.5Mbps data rate. The ST16C550 can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/ 22 pF load) is connected externally between the XTAL1 and XTAL2 pins, with an external 1 MΩ resistor across it. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. See figure 3 for crystal oscillator connection.

The generator divides the input 16X clock by any divisor from 1 to 2^{16} -1. The ST16C550 divides the basic crystal or external clock by 16. The frequency of the -BAUDOUT output pin is exactly 16X (16 times) of the selected baud rate (-BAUDOUT =16 x Baud Rate). Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 3 below shows selectable baud rates when using a 1.8432 MHz crystal.

For custom baud rates, the divisor value can be calculated using the following equation:

Divisor (in decimal) = (XTAL1 clock frequency) / (serial data rate x 16)

Table 3, BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

Output Baud Rate	User 16 x Clock Divisor (Decimal)	User 16 x Clock Divisor (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)
50	2304	900	09	00
75	1536	600	06	00
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1200	96	60	00	60
2400	48	30	00	30
4800	24	18	00	18
7200	16	10	00	10
9600	12	0C	00	0C
19.2k	6	06	00	06
38.4k	3	03	00	03
57.6k	2	02	00	02
115.2k	1	01	00	01

DMA Operation

The ST16C550 FIFO trigger level provides additional flexibility to the user for block mode operation. The user can optionally operate the transmit and receive FIFO's in the DMA mode (FCR bit-3). The DMA mode affects the state of the -RXRDY and -TXRDY output pins. The following tables show this:

-RXRDY pin:

Non-DMA mode	DMA mode
1 = FIFO empty	0 to 1 transition when FIFO empties
0 = at least 1 byte in FIFO	1 to 0 transition when FIFO reaches trigger level, or timeout occurs

-TXRDY pin:

Non-DMA mode	DMA mode
1 = at least 1 byte in FIFO	1 = FIFO is full
0 = FIFO empty	0 = FIFO has at least 1 empty location

Loop-back Mode

The internal loop-back capability allows onboard diagnostics. In the loop-back mode the normal modem interface pins are disconnected and reconfigured for loop-back internally. In this mode MSR bits 4-7 are also disconnected. However, MCR register bits 0-3 can be used for controlling loop-back diagnostic testing. In the loop-back mode -OP1 and -OP2 in the MCR register (bits 0-1) control the modem -RI and -CD inputs respectively. MCR signals -DTR and -RTS (bits 0-1) are used to control the modem -CTS and -DSR inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (See Figure 4). The -CTS, -DSR, -CD, and -RI are disconnected from their normal modem control inputs pins, and instead are connected internally to -DTR, -RTS, -OP1 and -OP2. Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits.

In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. The interrupts are still controlled by the IER.

Figure 3, TYPICAL EXTERNAL CRYSTAL OSCILLATOR CONNECTION

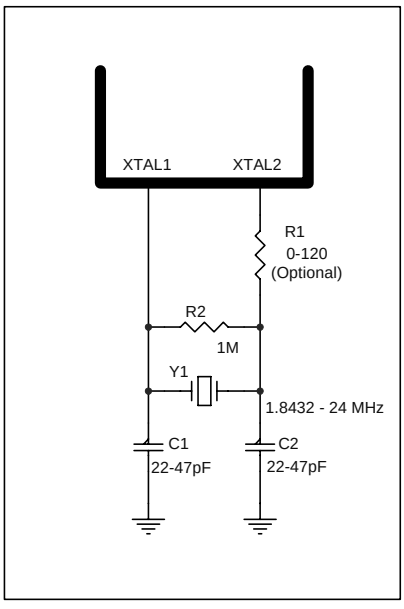
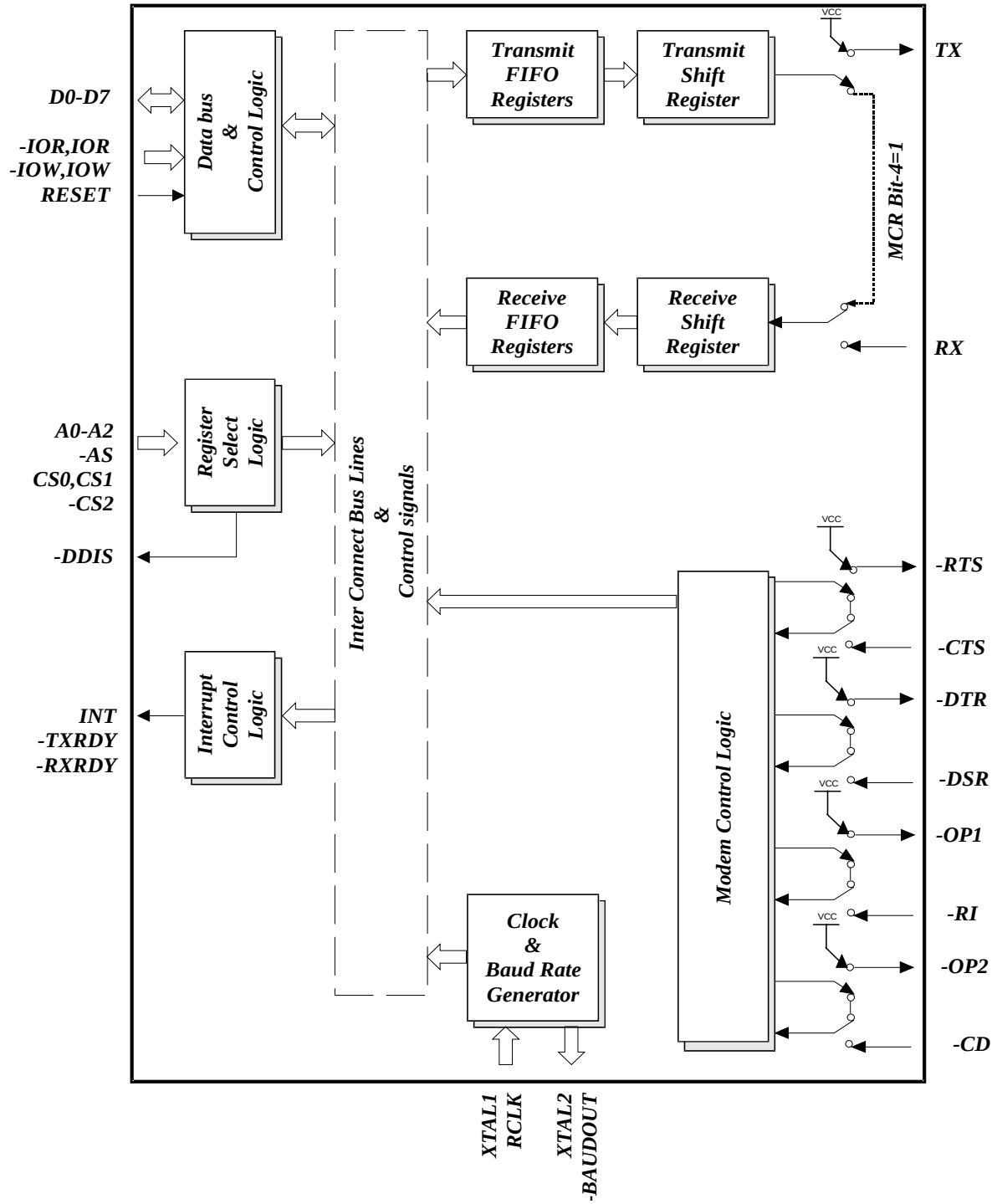


Figure 4, INTERNAL LOOP-BACK MODE DIAGRAM



REGISTER FUNCTIONAL DESCRIPTIONS

The following table delineates the assigned bit functions for the twelve ST16C550 internal registers. The assigned bit functions are more fully defined in the following paragraphs.

Table 4, ST16C550 INTERNAL REGISTERS

A2 A1 A0	Register [Default] Note *2	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
General Register Set									
0 0 0	RHR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER [00]	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR [00]	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR [01]	FIFO's enabled	FIFO's enabled	0	0	INT priority bit-2	INT priority bit-1	INT priority bit-0	INT status
0 1 1	LCR [00]	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR [00]	0	0	0	loopback enable	-OP2	-OP1	-RTS	-DTR
1 0 1	LSR [60]	FIFO data error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR [X0]	CD	RI	DSR	CTS	delta -CD	delta -RI	delta -DSR	delta -CTS
1 1 1	SPR [FF]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Baud Rate Generator Divisor Registers. Accessible when LCR bit-7 is set to logic 1. Note 1*									
0 0 0	DLL [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM [XX]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

Note *1: The BRG registers are accessible only when LCR bit-7 is set to a logic 1.
Note *2: The value represents the register's initialized HEX value. An "X" signifies a 4-bit un-initialized nibble.

Transmit and Receive Holding Register

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the transmit holding register empty flag is set (logic 0 = at least one byte in FIFO / THR, logic 1= FIFO/THR empty).

The serial receive section also contains an 8-bit Receive Holding Register, RHR. Receive data is removed from the ST16C550 and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at 16x clock rate. After 7 1/2 clocks the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the ST16C550 INT output pin.

IER Vs Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the receive interrupts and register status will reflect the following:

A) The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B) FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

IER Vs Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1; resetting IER bits 0-3 enables the ST16C550 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A) LSR BIT-0 will be a logic 1 as long as there is one byte in the receive FIFO.

B) LSR BIT 1-4 will indicate if an overrun error occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both the transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate any FIFO data errors.

IER BIT-0:
Logic 0 = Disable the receiver ready interrupt. (normal default condition)
Logic 1 = Enable the receiver ready interrupt.

IER BIT-1:
Logic 0 = Disable the transmitter empty interrupt. (normal default condition)
Logic 1 = Enable the transmitter empty interrupt.

IER BIT-2:
Logic 0 = Disable the receiver line status interrupt. (normal default condition)
Logic 1 = Enable the receiver line status interrupt.

IER BIT-3:
Logic 0 = Disable the modem status register interrupt. (normal default condition)
Logic 1 = Enable the modem status register interrupt.

IER BIT 4-7: Not used and set to "0".

FIFO Control Register (FCR)

This register is used to enable the FIFO's, clear the FIFO's, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

DMA MODE:
See description and DMA tables on page 11.

FCR BIT-0:
Logic 0 = Disable the transmit and receive FIFO. (normal default condition)
Logic 1 = Enable the transmit and receive FIFO. This bit must be a "1" when other FCR bits are written to or they will not be programmed.

FCR BIT-1:
Logic 0 = No FIFO receive reset. (normal default condition)
Logic 1 = Clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-2:
Logic 0 = No FIFO transmit reset. (normal default condition)
Logic 1 = Clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-3:
Logic 0 = Set DMA mode "0". (normal default condition)
Logic 1 = Set DMA mode "1."

Transmit operation in mode "0":
When the ST16C550 is in the ST16C450 mode (FIFO's disabled, FCR bit-0 = logic 0) or in the FIFO mode (FIFO's enabled, FCR bit-0 = logic 1, FCR bit-3 = logic 0) and when there are no characters in the transmit FIFO or transmit holding register, the -TXRDY pin will be a logic 0. Once active the -TXRDY pin will go to a logic 1 after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When the ST16C550 is in mode "0" (FCR bit-0 = logic 0) or in the FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 0) and there is at least one character in the receive FIFO, the -RXRDY pin will be a logic 0. Once active the -RXRDY pin will go to a logic 1 when there are no more characters in the receiver.

Transmit operation in mode "1":
When the ST16C550 is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1), the -TXRDY pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty.

Receive operation in mode "1":
When the ST16C550 is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1) and the trigger level has been reached, or a Receive Time Out has occurred, the -RXRDY pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.

FCR BIT 4-5: Not used.

FCR BIT 6-7: These bits are used to set the trigger level for the receive FIFO interrupt.

An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However the FIFO will continue to be loaded until it is full.

BIT-7	BIT-6	RX FIFO trigger level
0	0	1
0	1	4
1	0	8
1	1	14

Interrupt Status Register (ISR)

The ST16C550 provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after rereading the interrupt status bits. The Interrupt Source Table 5 (below) shows the data values (bit 0-3) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels:

Table 5, INTERRUPT SOURCE TABLE

Priority Level	[ISR] Bit-3	Bit-2	Bit-1	Bit-0	Source of the interrupt
X	0	0	0	1	No interrupt pending
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
Logic 1 = No interrupt pending. (normal default condition)

ISR BIT 1-3: (logic 0 or cleared is the default condition)
These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (See Interrupt Source Table).

ISR BIT 4-5: Not used and set to "0".

ISR BIT 6-7: (logic 0 or cleared is the default condition)
These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFO's are enabled

Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR BIT 0-1: (logic 0 or cleared is the default condition)
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2: (logic 0 or cleared is the default condition)
The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	Word length	Stop bit length (Bit time(s))
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
Logic 0 = No parity (normal default condition)
Logic 1 = A parity bit is generated during the transmission, receiver checks the data and parity for transmission errors.

LCR BIT-4:
If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.
Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted data. The receiver must be programmed to check the same format. (normal default condition)
Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted. The receiver must be programmed to check the same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = logic 0, parity is not forced (normal default condition)
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

LCR Bit-5	LCR Bit-4	LCR Bit-3	Parity selection
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity "1"
1	1	1	Forced "0"

LCR BIT-6:
When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR bit-6 to a logic 0.
Logic 0 = No TX break condition. (normal default condition)
Logic 1 = Forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.

LCR BIT-7:
The internal baud rate counter latch and Enhance Feature mode enable.
Logic 0 = Divisor latch disabled. (normal default condition)
Logic 1 = Divisor latch and enhanced feature register enabled.

Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

MCR BIT-0:
Logic 0 = Force -DTR output to a logic 1. (normal default condition)
Logic 1 = Force -DTR output to a logic 0.

MCR BIT-1:
Logic 0 = Force -RTS output to a logic 1. (normal default condition)
Logic 1 = Force -RTS output to a logic 0.

MCR BIT-2:
Logic 0 = Set -OP1 output to a logic 1. (normal default condition)
Logic 1 = Set -OP1 output to a logic 0.

MCR BIT-3:
Logic 0 = Set -OP2 output to a logic 1. (normal default condition)
Logic 1 = Set -OP2 output to a logic 0.

MCR BIT-4:
Logic 0 = Disable loop-back mode. (normal default condition)
Logic 1 = Enable local loop-back mode (diagnostics).

MCR BIT 5-7: Not used and set to “0”.

Line Status Register (LSR)

This register provides the status of data transfers between. the ST16C550 and the CPU.

LSR BIT-0:
Logic 0 = No data in receive holding register or FIFO. (normal default condition)
Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR BIT-1:
Logic 0 = No overrun error. (normal default condition)
Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transfer into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR BIT-2:
Logic 0 = No parity error (normal default condition)
Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.

LSR BIT-3:
Logic 0 = No framing error (normal default condition).
Logic 1 = Framing error. The receive character did not have a valid stop bit(s). In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
Logic 0 = No break condition (normal default condition)
Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.

LSR BIT-5:
This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition,

this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

LSR BIT-6:
This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

LSR BIT-7:
Logic 0 = No Error (normal default condition)
Logic 1 = At least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when there are no remaining LSR errors in the RX FIFO.

Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device that the ST16C550 is connected to. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

MSR BIT-0:
Logic 0 = No -CTS Change (normal default condition)
Logic 1 = The -CTS input to the ST16C550 has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-1:
Logic 0 = No -DSR Change (normal default condition)
Logic 1 = The -DSR input to the ST16C550 has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-2:
Logic 0 = No -RI Change (normal default condition)
Logic 1 = The -RI input to the ST16C550 has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.

MSR BIT-3:
Logic 0 = No -CD Change (normal default condition)
Logic 1 = Indicates that the -CD input to the has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-4:
CTS (active high, logical 1). Normally this bit is the compliment of the -CTS input. In the loop-back mode, this bit is equivalent to the RTS bit in the MCR register.

MSR BIT-5:
DSR (active high, logical 1). Normally this bit is the compliment of the -DSR input. In the loop-back mode, this bit is equivalent to the DTR bit in the MCR register.

MSR BIT-6:
RI (active high, logical 1). Normally this bit is the compliment of the -RI input. In the loop-back mode this bit is equivalent to the OP1 bit in the MCR register.

MSR BIT-7:
CD (active high, logical 1). Normally this bit is the compliment of the -CD input. In the loop-back mode this bit is equivalent to the OP2 bit in the MCR register.

Scratchpad Register (SPR)

The ST16C550 provides a temporary data register to store 8 bits of user information.

ST16C550 EXTERNAL RESET CONDITIONS

REGISTERS	RESET STATE
IER	IER BITS 0-7 = logic 0
ISR	ISR BIT-0=1, ISR BITS 1-7 = logic 0
LCR, MCR	BITS 0-7 = logic 0
LSR	LSR BITS 0-4 = logic 0, LSR BITS 5-6 = logic 1 LSR, BIT 7 = logic 0
MSR	MSR BITS 0-3 = logic 0, MSR BITS 4-7 = logic levels of the input signals
FCR	BITS 0-7 = logic 0

SIGNALS	RESET STATE
TX	Logic 1
-OP1	Logic 1
-OP2	Logic 1
-RTS	Logic 1
-DTR	Logic 1
-RXRDY	Logic 1
-TXRDY	Logic 0
INT	Logic 0

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T_{1w},T_{2w}	Clock pulse duration	17		17		ns	
T_{3w}	Oscillator/Clock frequency		16		24	MHz	
T_{4w}	Address strobe width	35		25		ns	
T_{5s}	Address setup time	5		0		ns	
T_{5h}	Address hold time	5		5		ns	
T_{6s}	Chip select setup time	5		0		ns	
T_{6h}	Chip select hold time	0		0		ns	
$T_{6s'}$	Address setup time	10		5		ns	see Note 1
T_{7d}	-IOR delay from chip select	10		10		ns	
T_{7w}	-IOR strobe width	77		38		ns	
$T_{7w'}$	Chip select width	77		38		ns	
T_{7h}	Chip select hold time from -IOR	0		0		ns	
$T_{7h'}$	Address hold time	5		5		ns	see Note 1
T_{8d}	-IOR delay from address	10		10		ns	
T_{9d}	Read cycle delay	77		38		ns	
T_{11d}	-IOR to -DDIS delay		15		10	ns	100 pF load
T_{12d}	Delay from -IOR to data		35		25	ns	
T_{12h}	Data disable time		25		15	ns	
T_{13d}	-IOW delay from chip select	10		10		ns	
T_{13w}	-IOW strobe width	27		15		ns	
$T_{13w'}$	Chip select width	77		38		ns	
T_{13h}	Chip select hold time from -IOW	0		0		ns	
T_{14d}	-IOW delay from address	10		10		ns	
T_{15d}	Write cycle delay	77		38		ns	
T_{16s}	Data setup time	20		15		ns	
T_{16h}	Data hold time	5		5		ns	
T_{17d}	Delay from -IOW to output		50		40	ns	100 pF load
T_{18d}	Delay to set interrupt from MODEM input		40		35	ns	100 pF load
T_{19d}	Delay to reset interrupt from -IOR		40		35	ns	100 pF load
T_{20d}	Delay from stop to set interrupt		1		1	Rclk	
T_{21d}	Delay from -IOR to reset interrupt		45		40	ns	100 pF load
T_{22d}	Delay from stop to interrupt		45		40	ns	
T_{23d}	Delay from initial INT reset to transmit start	8	24	8	24	Rclk	
T_{24d}	Delay from -IOW to reset interrupt		45		40	ns	
T_{25d}	Delay from stop to set -RxRdy		1		1	Rclk	
T_{26d}	Delay from -IOR to reset -RxRdy		45		40	ns	
T_{27d}	Delay from -IOW to set -TxRdy		45		40	ns	
T_{28d}	Delay from start to reset -TxRdy		8		8	Rclk	
T_R	Reset pulse width	40		40		ns	
N	Baud rate divisor	1	2^{16}-1	1	2^{16}-1	Rclk	

Note 1: Applicable only when -AS is tied low.

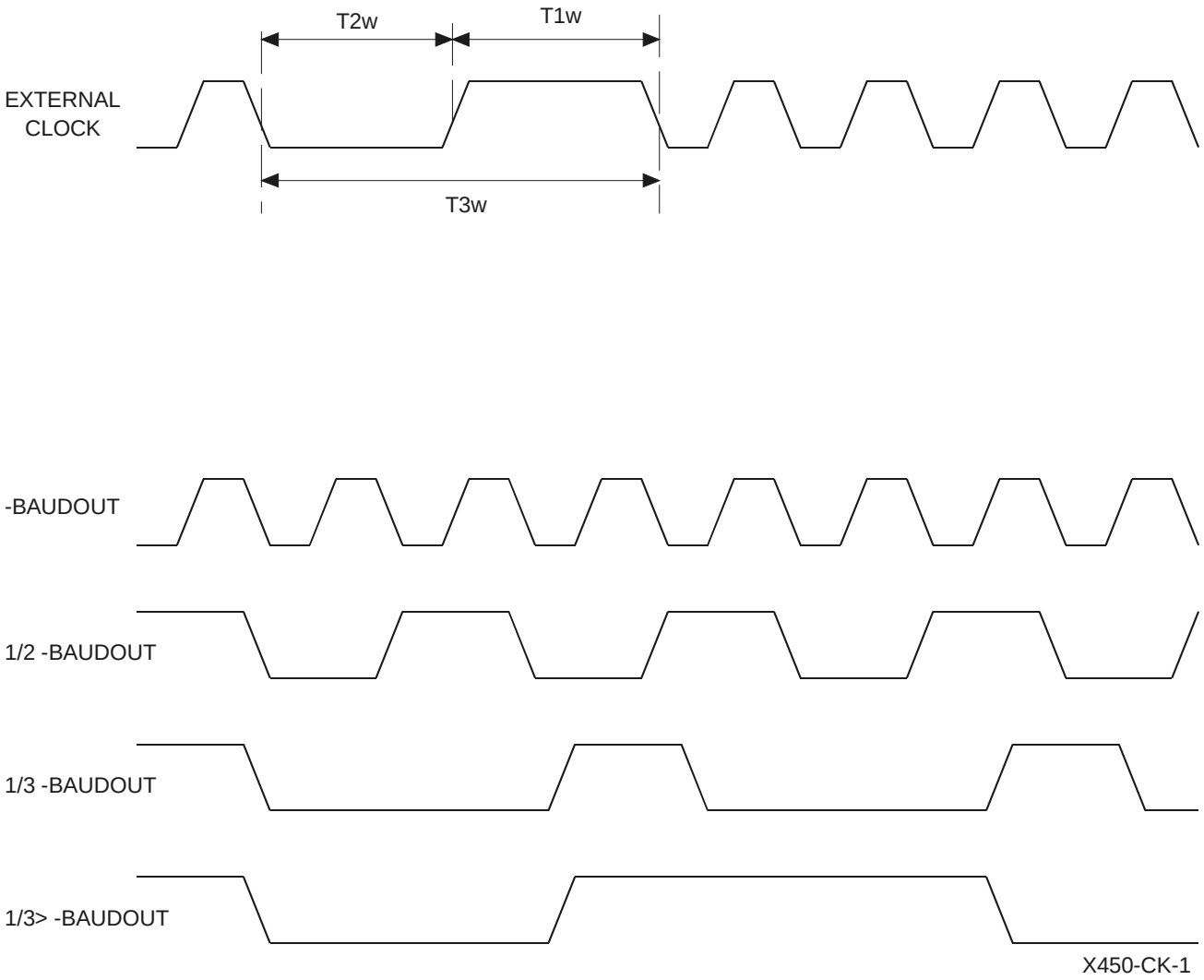
ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND - 0.3 V to VCC +0.3 V
Operating temperature	-40° C to +85° C
Storage temperature	-65° C to 150° C
Package dissipation	500 mW

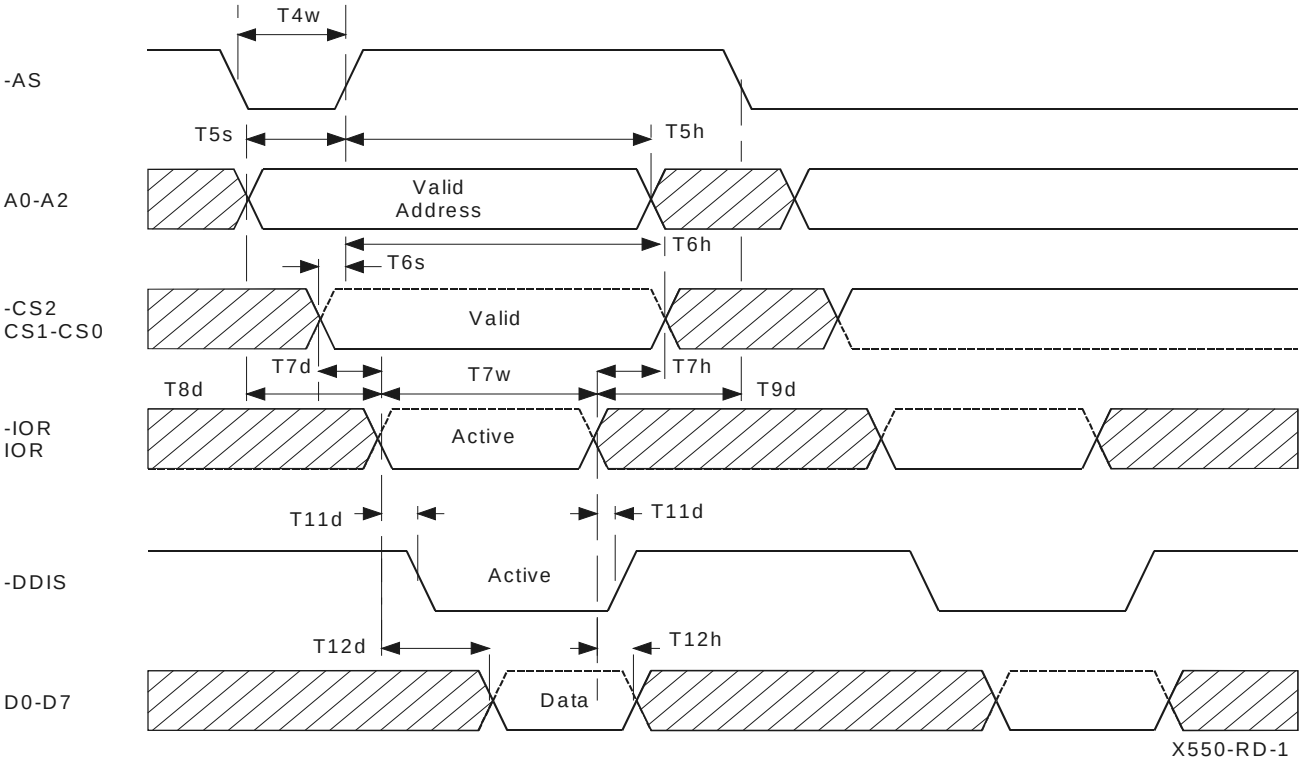
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

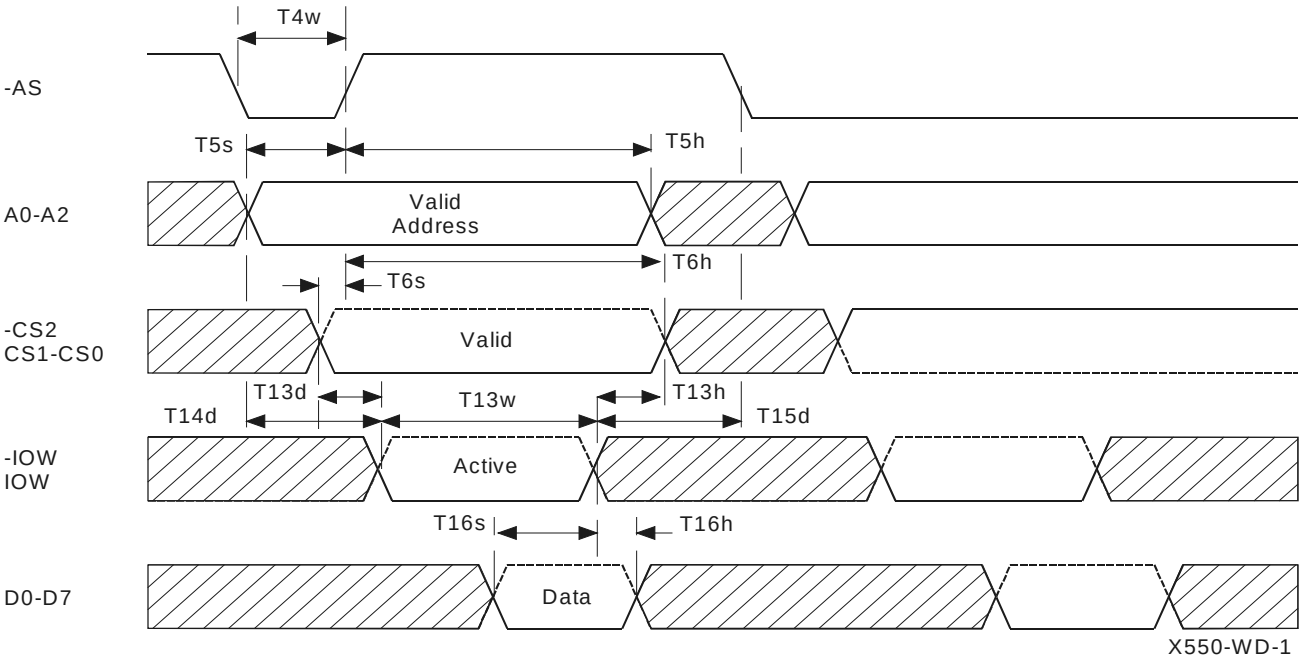
Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
V_{ILCK}	Clock input low level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock input high level	2.4	VCC	3.0	VCC	V	
V_{IL}	Input low level	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input high level	2.0	VCC	2.2	VCC	V	
V_{OL}	Output low level on all outputs				0.4	V	I_{OL}= 5 mA
V_{OL}	Output low level on all outputs		0.4			V	I_{OL}= 4 mA
V_{OH}	Output high level			2.4		V	I_{OH}= -5 mA
V_{OH}	Output high level	2.0				V	I_{OH}= -1 mA
I_{IL}	Input leakage		±10		±10	µA	
I_{CL}	Clock leakage		±10		±10	µA	
I_{CC}	Avg power supply current		1.3		3	mA	
C_P	Input capacitance		5		5	pF	



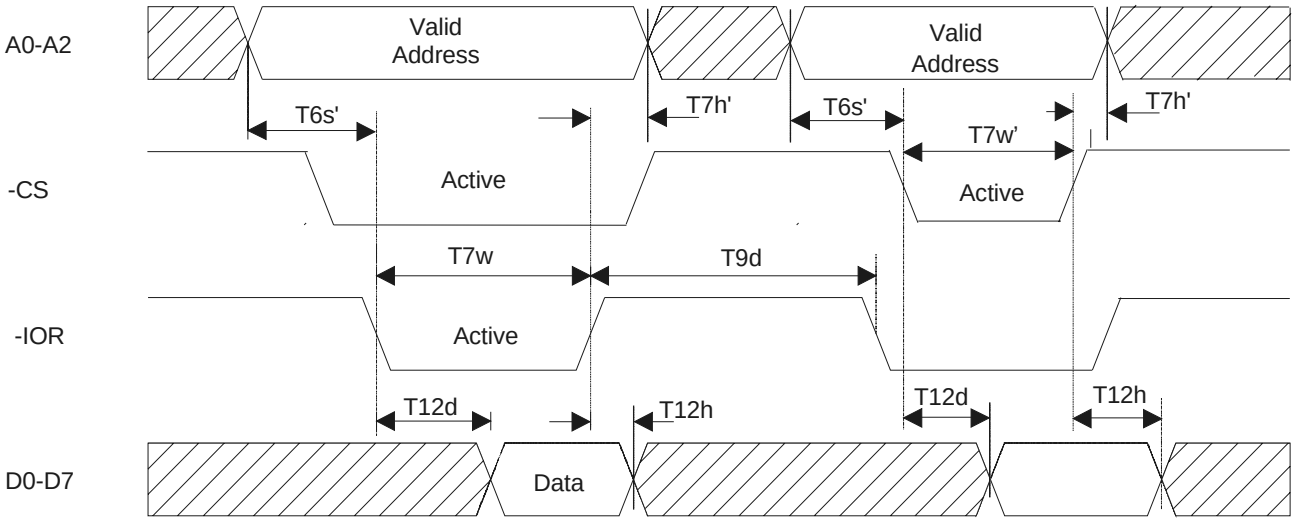
Clock timing



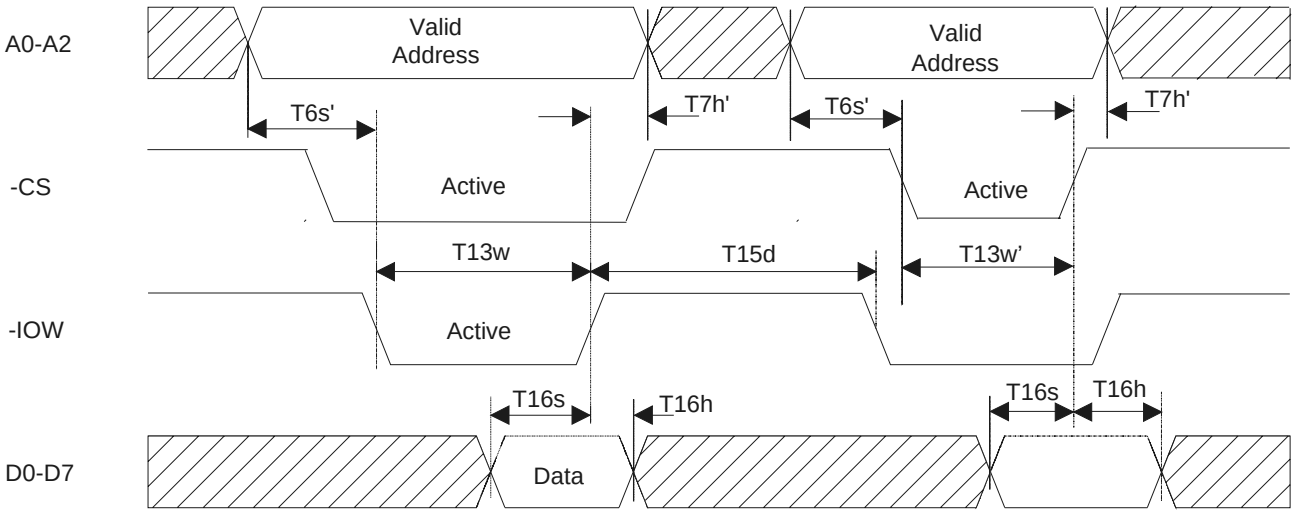
General Read Timing when using -AS signal



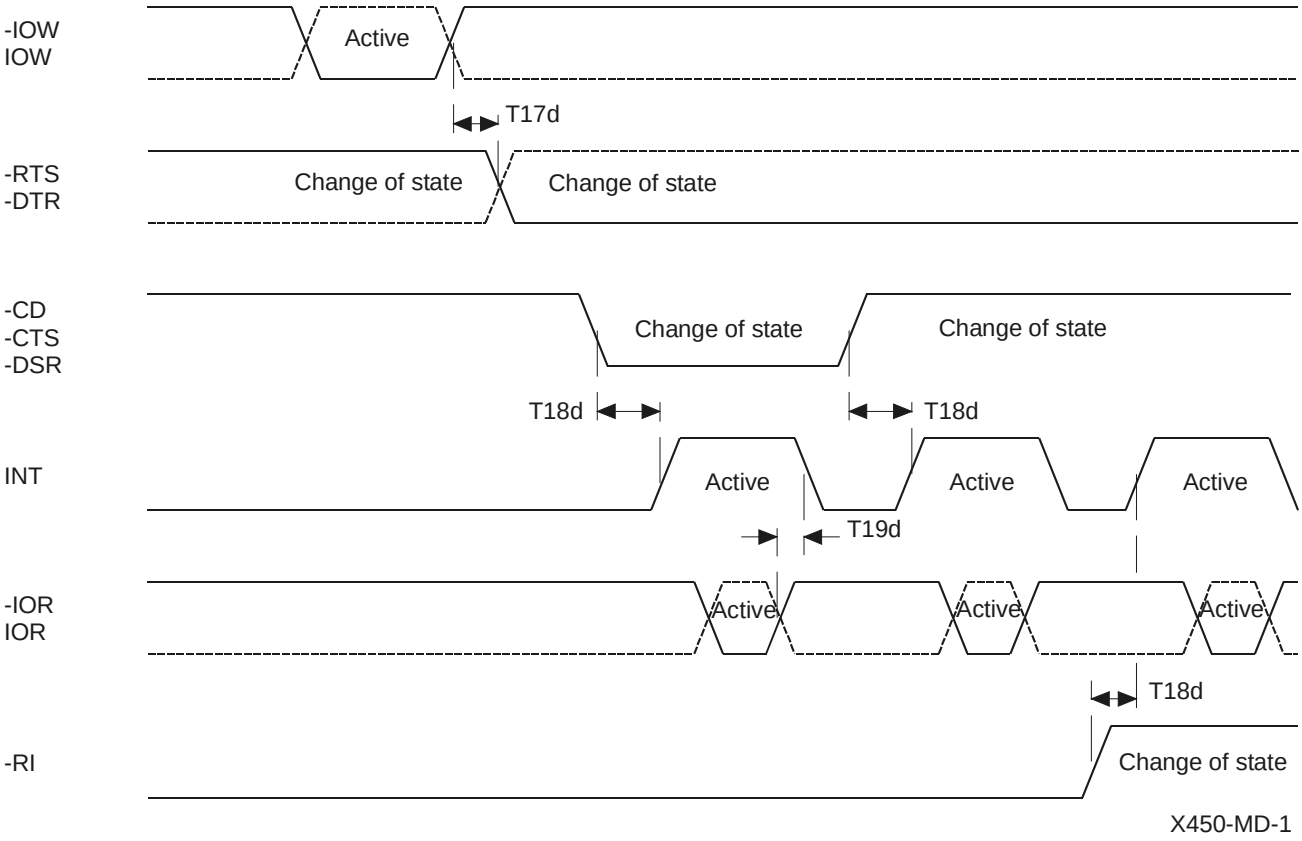
General Write Timing when using -AS signal.



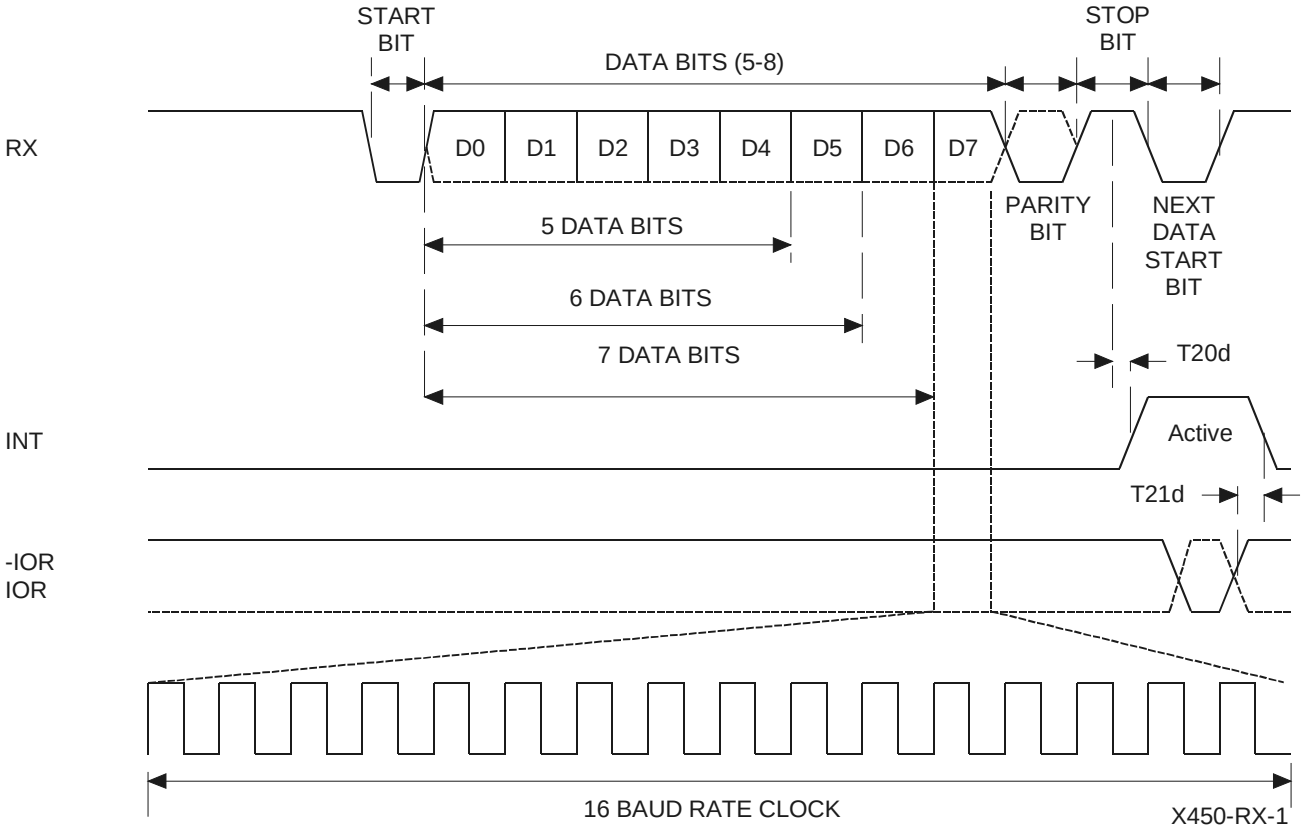
General Read Timing when -AS is tied to GND



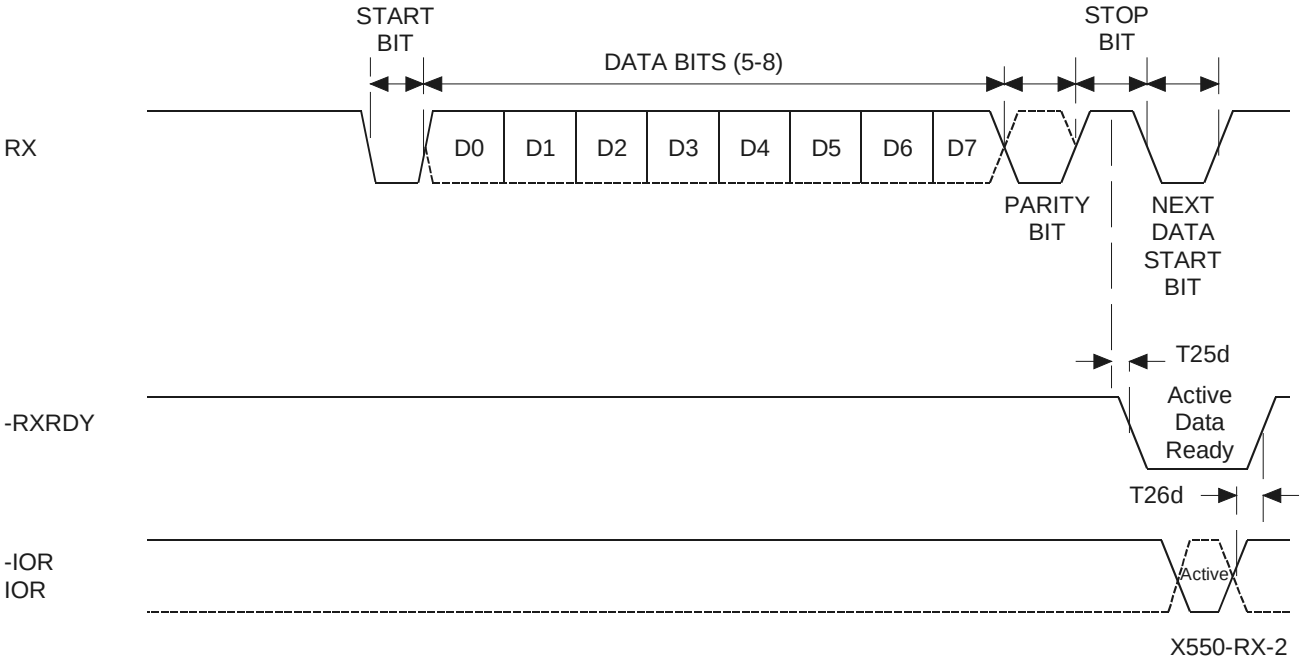
General Write Timing when -AS is tied to GND



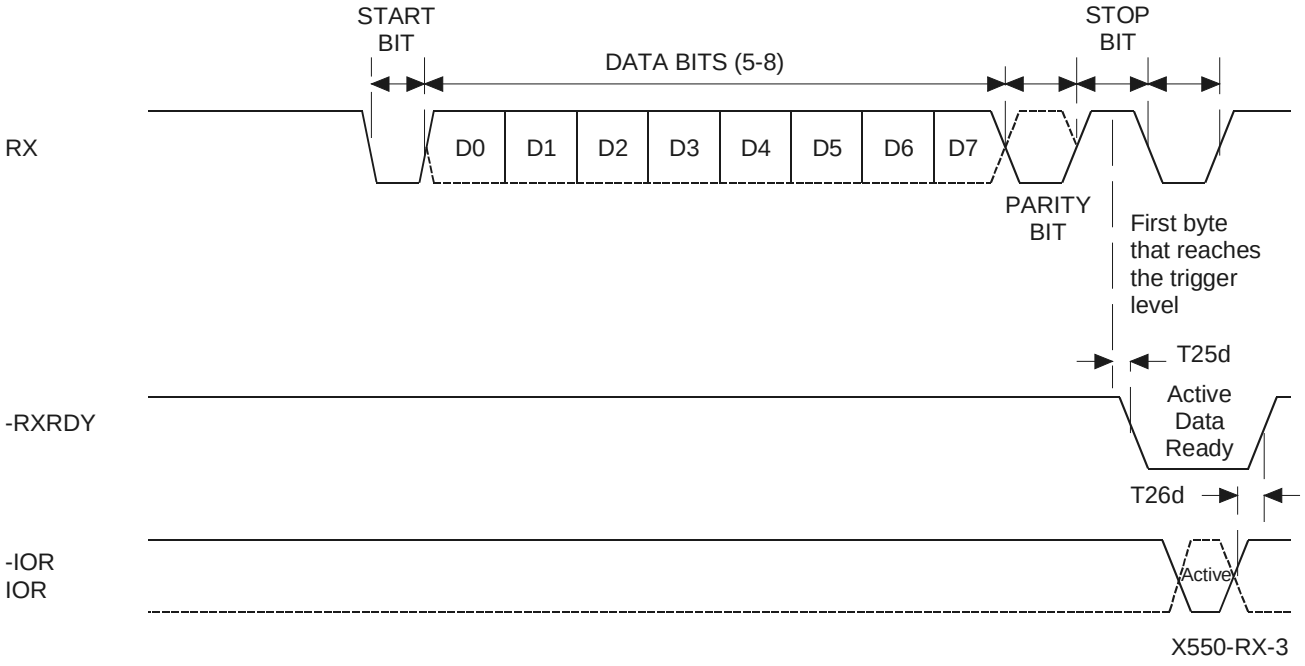
Modem input/output timing



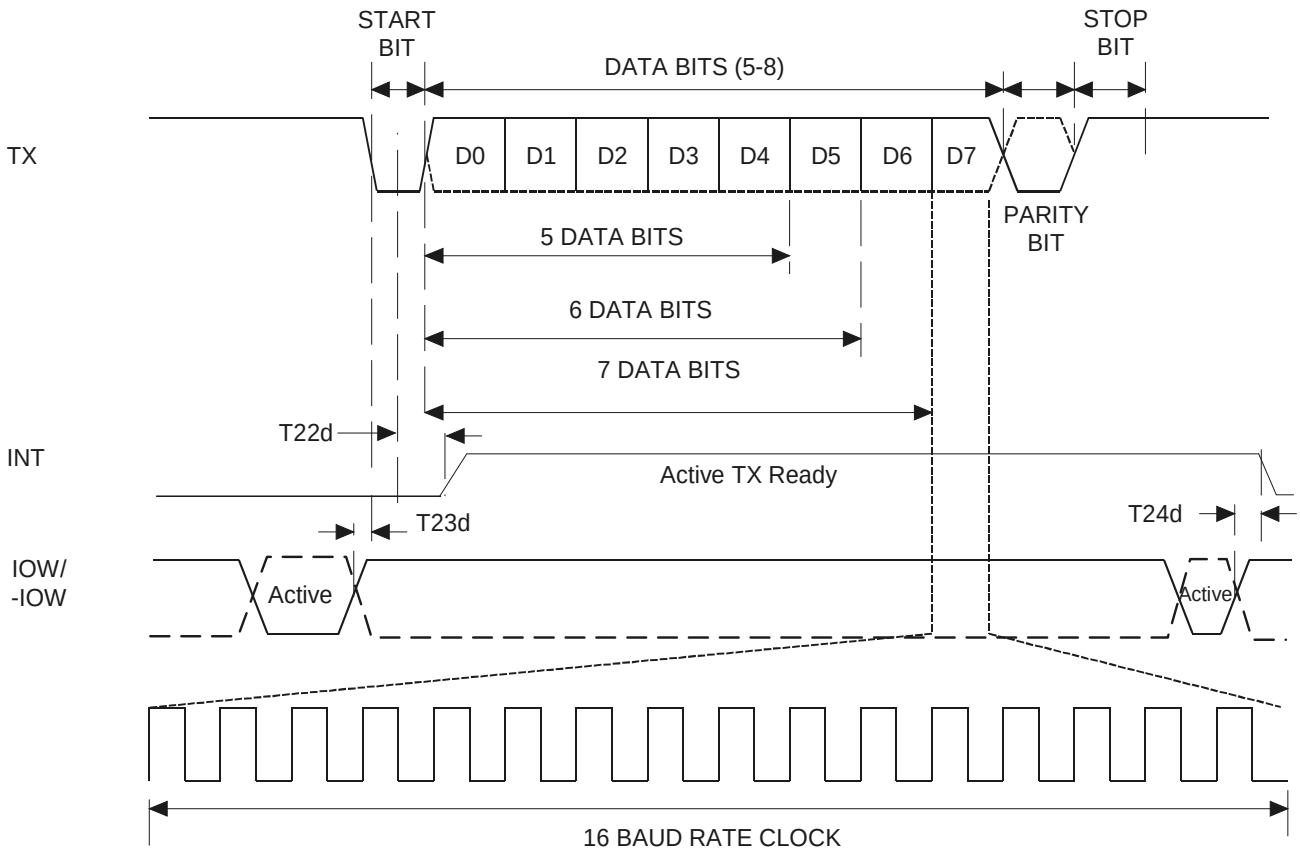
Receive timing



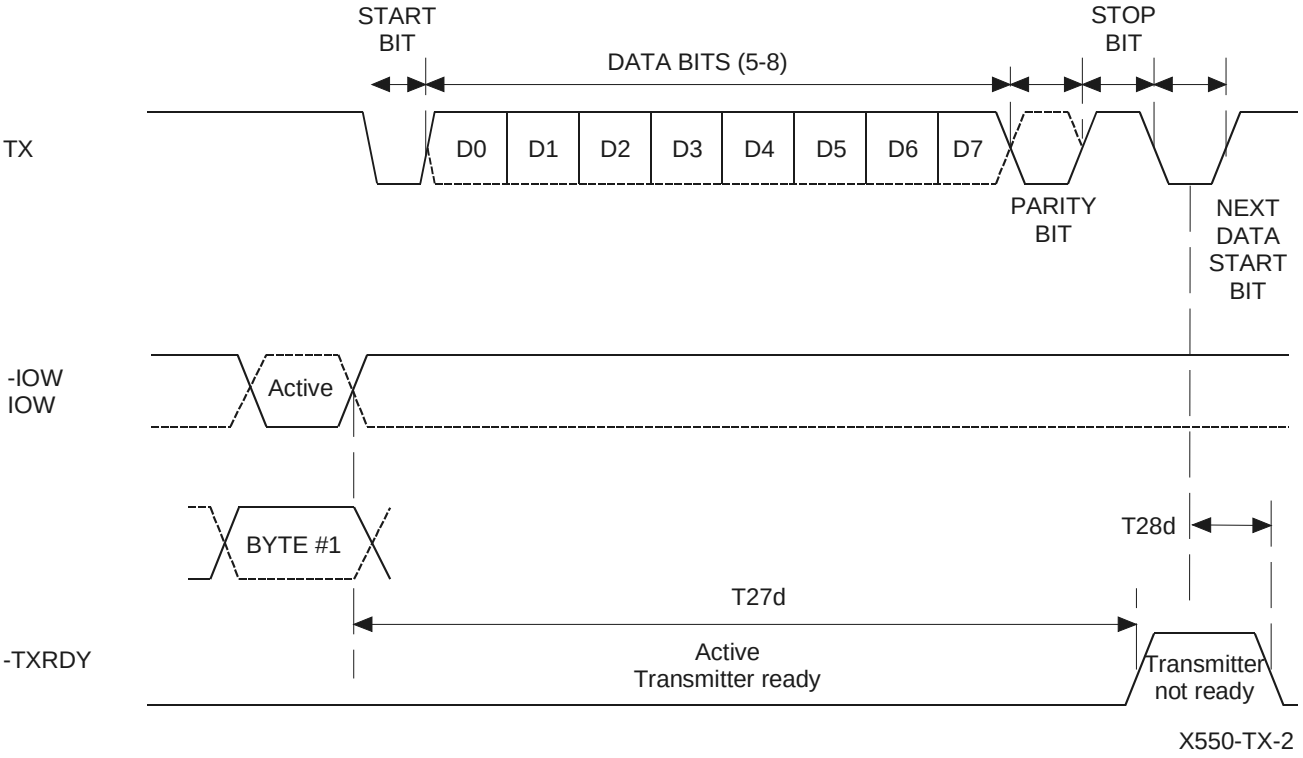
Receive ready timing in non FIFO mode



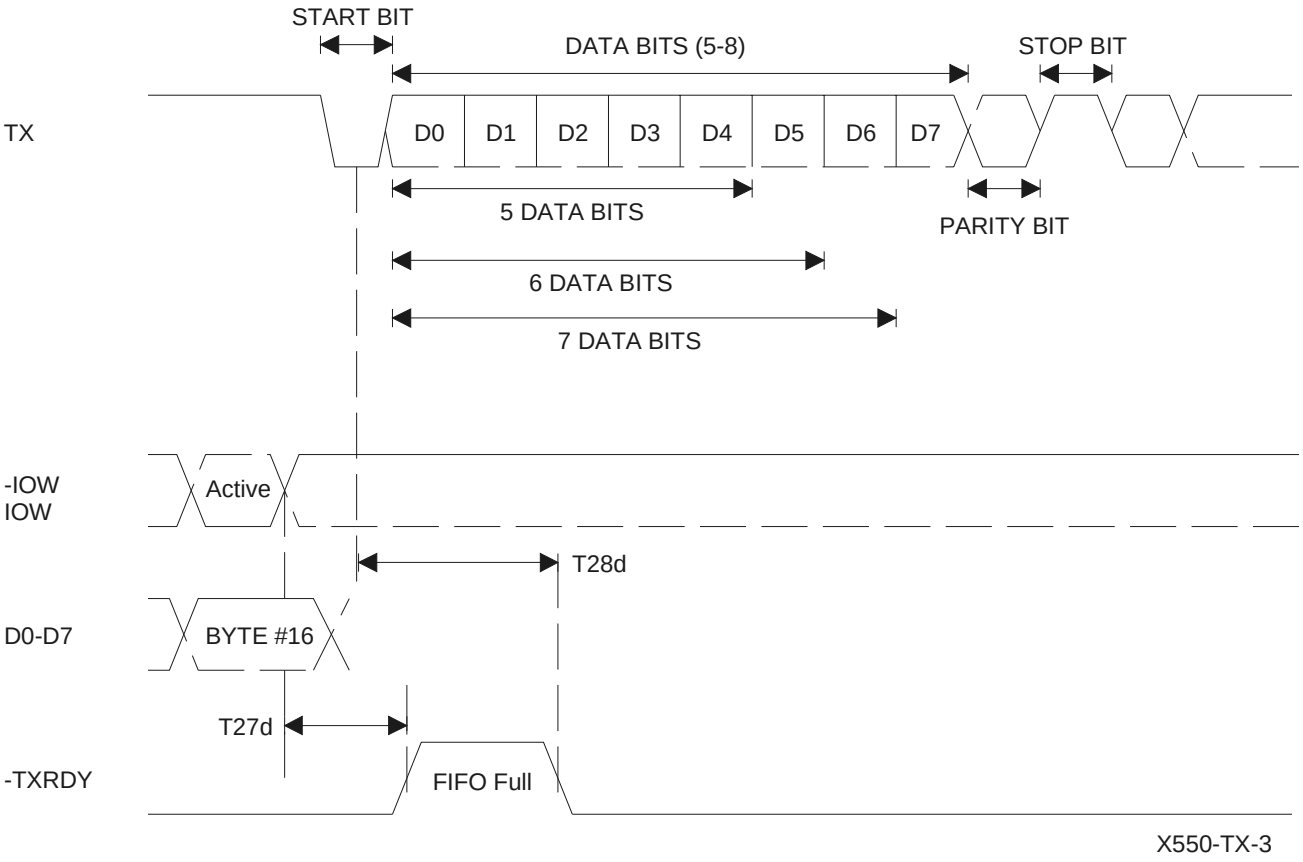
Receive ready timing in FIFO mode



Transmit timing



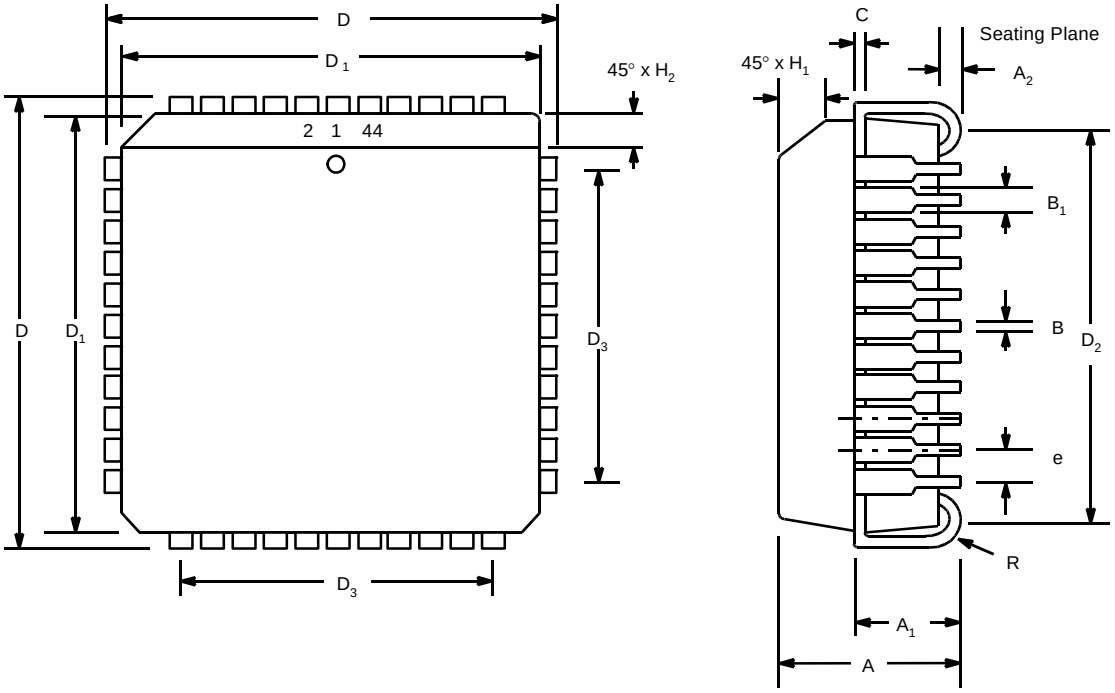
Transmit ready timing in non FIFO mode



Transmit ready timing in FIFO mode

PACKAGE OUTLINE DRAWING

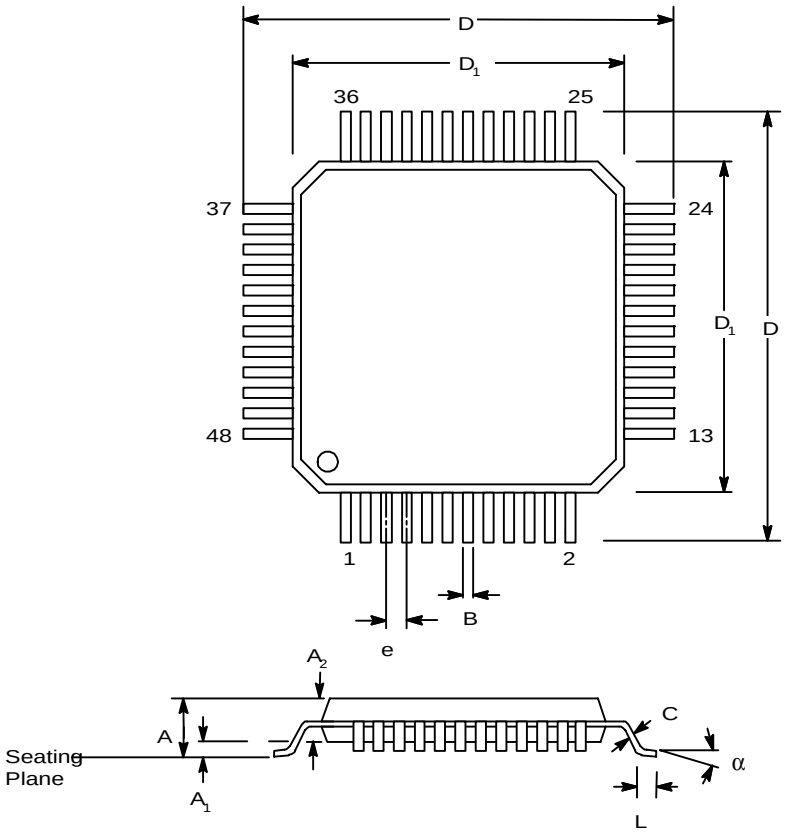
44LEAD PLASTIC LEADED CHIP CARRIER (PLCC)



Note: The control dimension is the inch column				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.090	0.120	2.29	3.05
A_2	0.020	-----	0.51	------
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D_1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ		12.70 typ	
e	0.50 BSC		1.27BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

PACKAGE OUTLINE DRAWING

48 LEAD THIN QUAD FLAT PACK
(TQFP)



Note: The control dimension is the millimeter column				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.039	0.047	1.00	1.20
A_1	0.002	0.006	0.05	0.15
A_2	0.037	0.041	0.95	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.20 BSC		0.50BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

EXPLANATION OF DATA SHEET REVISIONS:

FROM	TO	CHANGES	DATE
4.20	4.30	Added revision history. Added Device Status to front page.	Sept 2003
4.30	5.00	Updated AC Timing values for IOW, CS and IOR pulse widths and Read/Write cycle delays. This applies to devices with top mark date code of "B2 YYWW" and newer.	Feb 2005
5.00	5.01	Corrected the AC Timing values. Added Chip Select Width for clarification.	Apr 2005

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