A Microchip Technology Company

Serial Quad I/O (SQI) Flash Memory

SST26VF016 / SST26VF032

Data Sheet

The SST26VF016 / SST26VF032 Serial Quad I/O™ (SQI™) flash device utilizes a 4-bit multiplexed I/O serial interface to boost performance while maintaining the compact form factor of standard serial flash devices. Operating at frequencies reaching 80 MHz, the SST26VF016 / SST26VF032 enables minimum latency execute-in-place (XIP) capability without the need for code shadowing on an SRAM. The device's high performance and small footprint make it the ideal choice for mobile handsets, Bluetooth® headsets, optical disk drives, GPS applications and other portable electronic products. Further benefits are achieved with SST's proprietary, high-performance CMOS SuperFlash® technology, which significantly improves performance and reliability, and lowers power consumption for high bandwidth, compact designs.

Features

- **Single Voltage Read and Write Operations**
  - 2.7-3.6V
- **Serial Interface Architecture**
  - Nibble-wide multiplexed I/O's with SPI-like serial command structure
    - Mode 0 and Mode 3
  - Single-bit, SPI backwards compatible
    - Read, High-Speed Read, and JEDEC ID Read
- **High Speed Clock Frequency**
  - 80 MHz
    - 320 Mbit/s sustained data rate
- **Burst Modes**
  - Continuous linear burst
  - 8/16/32/64 Byte linear burst with wrap-around
- **Index Jump**
  - Jump to address index within 256 Byte Page
  - Jump to address index within 64 KByte Block
  - Jump to address index in another 64 KByte Block
- **Superior Reliability**
  - Endurance: 100,000 cycles
  - Greater than 100 years data retention
- **Low Power Consumption:**
  - Active Read current: 12 mA (typical @ 80 MHz)
  - Standby current: 8 µA (typical)
- **Fast Erase and Byte-Program:**
  - Chip-Erase time: 35 ms (typical)
  - Sector-/Block-Erase time: 18 ms (typical)
- **Page-Program**
  - 256 Bytes per page
  - Fast Page Program time in 1 ms (typical)
- **End-of-Write Detection**
  - Software polling the BUSY bit in status register
- **Flexible Erase Capability**
  - Uniform 4 KByte sectors
  - Four 8 KByte top parameter overlay blocks
  - Four 8 KByte bottom parameter overlay blocks
  - Two 32 KByte overlay blocks (one each top and bottom)
  - Uniform 64 KByte overlay blocks
    - SST26VF016 – 30 blocks
    - SST26VF032 – 62 blocks
- **Write-Suspend**
  - Suspend program or Erase operation to access another block/sector
- **Software Reset (RST) mode**
- **Software Write Protection**
  - Block-Locking
    - 64 KByte blocks, two 32 KByte blocks, and eight 8 KByte parameter blocks
- **Security ID**
  - One-Time Programmable (OTP) 256 bit, Secure ID
    - 64 bit Unique, factory pre-programmed identifier
    - 192 bit user-programmable
- **Temperature Range**
  - Industrial: -40°C to +85°C
- **Packages Available**
  - 8-contact WSON (6mm x 5mm)
  - 8-lead SOIC (200 mil)
- **All devices are RoHS compliant**

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Product Description

The Serial Quad I/O™ (SQI™) family of flash-memory devices features a 4-bit, multiplexed I/O interface that allows for low-power, high-performance operation in a low pin-count package. System designs using SQI flash devices occupy less board space and ultimately lower system costs.

All members of the 26 Series, SQI family are manufactured with SST proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST26VF016/032 significantly improve performance and reliability, while lowering power consumption. These devices write (Program or Erase) with a single power supply of 2.7-3.6V. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

SST26VF016/032 are offered in both 8-contact WSON (6 mm x 5 mm), and 8-lead SOIC (200 mil) packages. See Figure 2 for pin assignments.

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Block Diagram

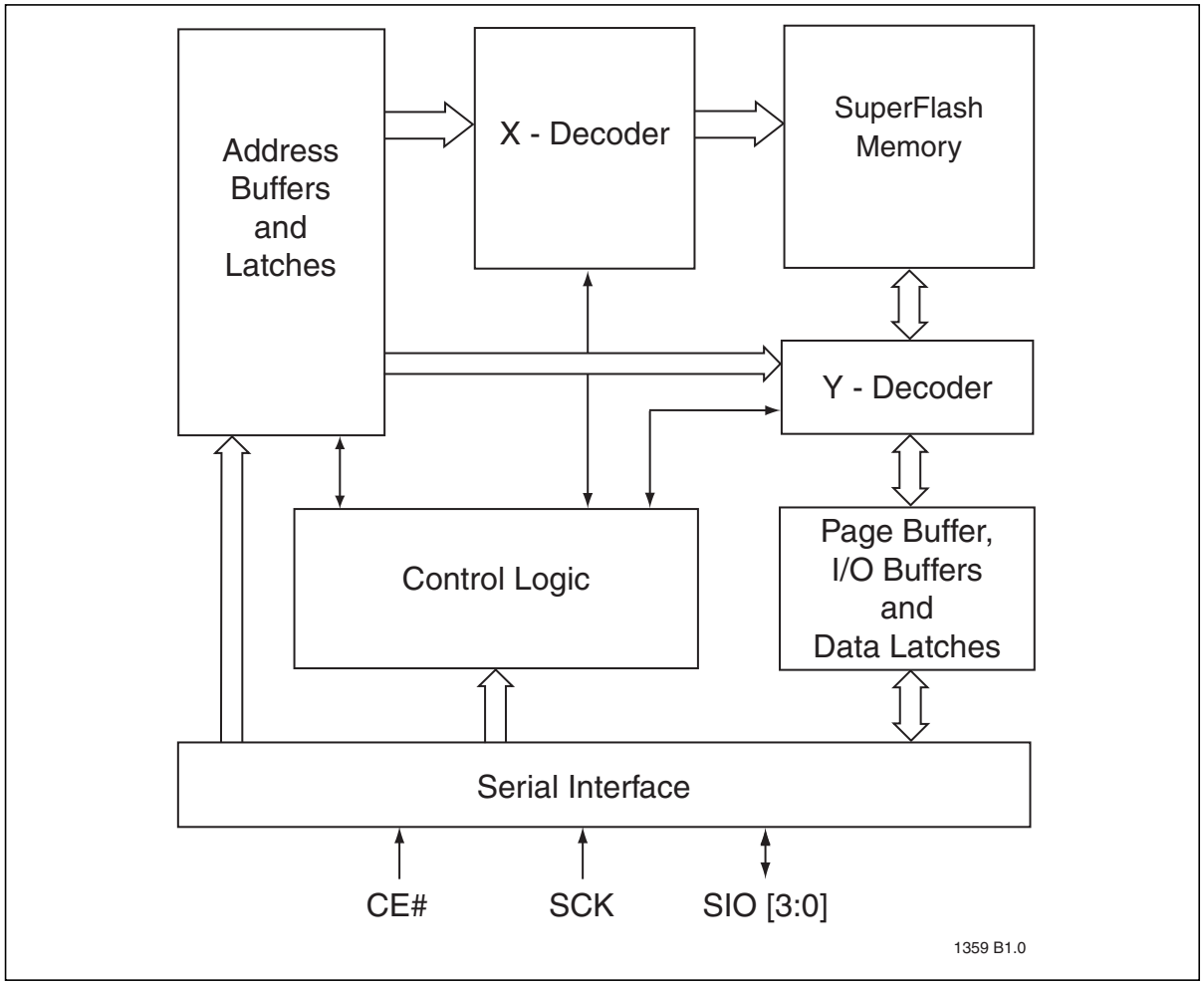


Figure 1: Functional Block Diagram

Pin Description

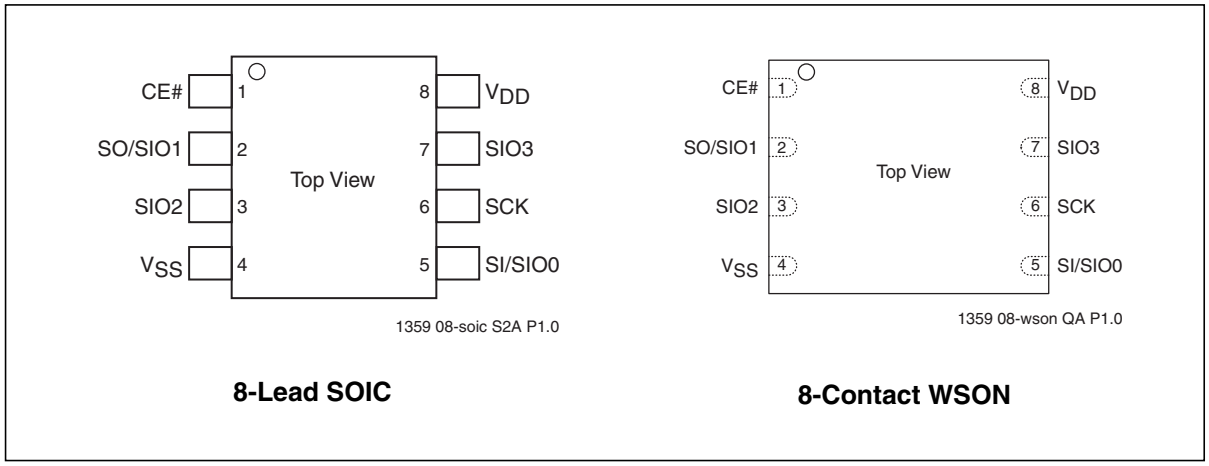


Figure 2: Pin Description for 8-lead SOIC and 8-contact WSON

Table 1: Pin Description

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SIO[3:0]	Serial Data Input/Output	To transfer commands, addresses, or data serially into the device or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. The EQIO command instruction configures these pins for Quad I/O mode.
SI	Serial Data Input for SPI mode	To transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock. SI is the default state after a power on reset.
SO	Serial Data Output for SPI mode	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. SO is the default state after a power on reset.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence; or in the case of Write operations, for the command/data input sequence.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V
V_{SS}	Ground	

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Memory Organization

The SST26VF016/032 SQI memory array is organized in uniform 4 KByte erasable sectors with eight 8 KByte parameters. In addition, the array also includes two 32 KByte and 30/62 64 KByte erasable overlay blocks. See Figure 3.

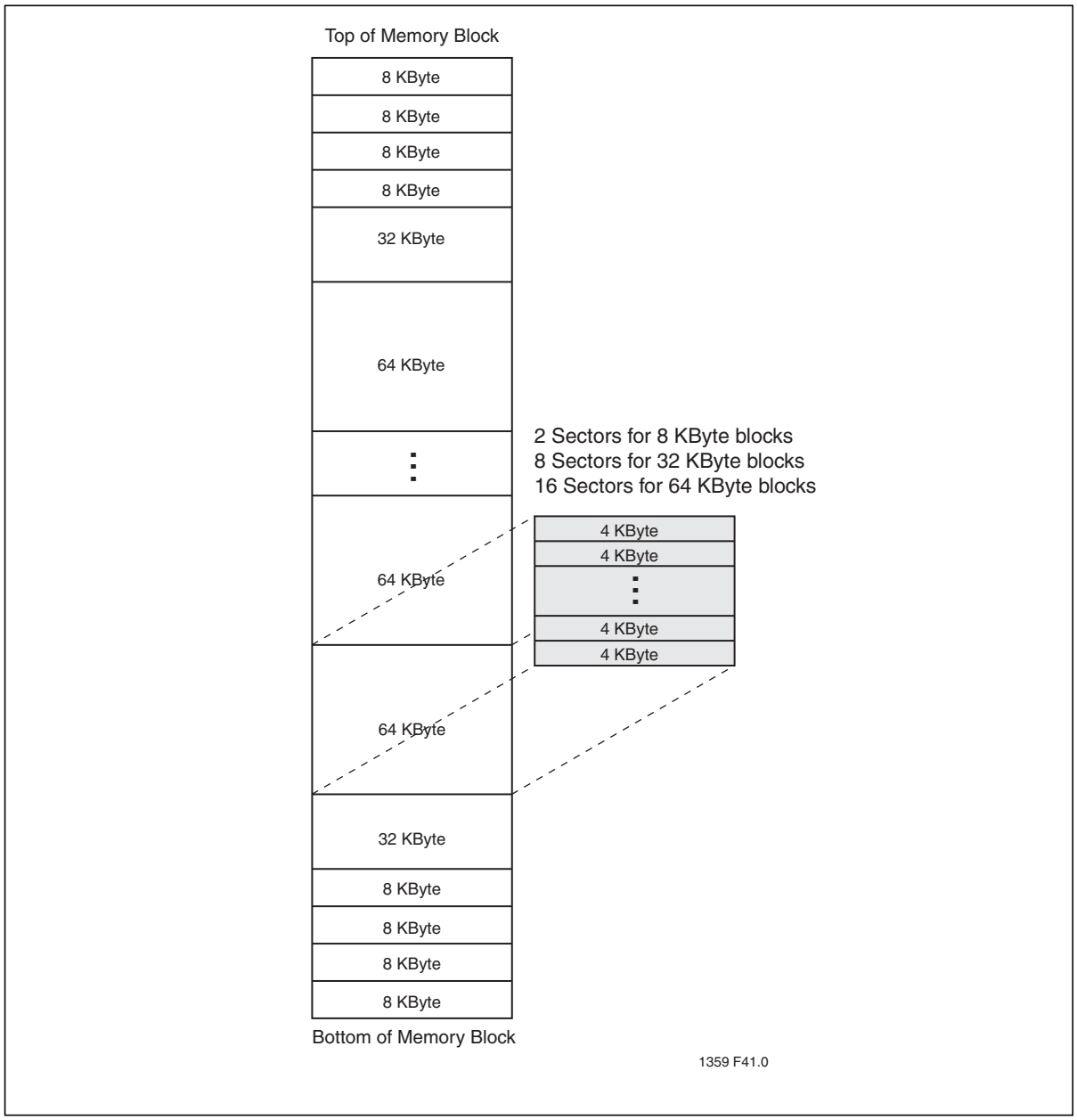


Figure 3: Memory Map

Device Operation

The SST26VF016/032 supports both Serial Peripheral Interface (SPI) bus protocol and the new 4-bit multiplexed Serial Quad I/O (SQI) bus protocol. To provide backward compatibility to traditional SPI Serial Flash devices, the device's initial state after a power-on reset is SPI bus protocol supporting only Read, High Speed Read, and JEDEC-ID Read instructions. A command instruction configures the device to Serial Quad I/O bus protocol. The dataflow in this bus protocol is controlled with four multiplexed I/O signals, a chip enable (CE#), and serial clock (SCK).

SQI Flash Memory protocol supports both Mode 0 (0,0) and Mode 3 (1,1) bus operations. The difference between the two modes, as shown in Figures 4 and 5, is the state of the SCK signal when the bus master is in Stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data I/O (SIO[3:0]) is sampled at the rising edge of the SCK clock signal for input, and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals as shown in Figure 4. The SST26VF016/032 use four multiplexed signals, SIO[3:0], for both data in and data out, as shown in Figure 5. This quadruples the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package.

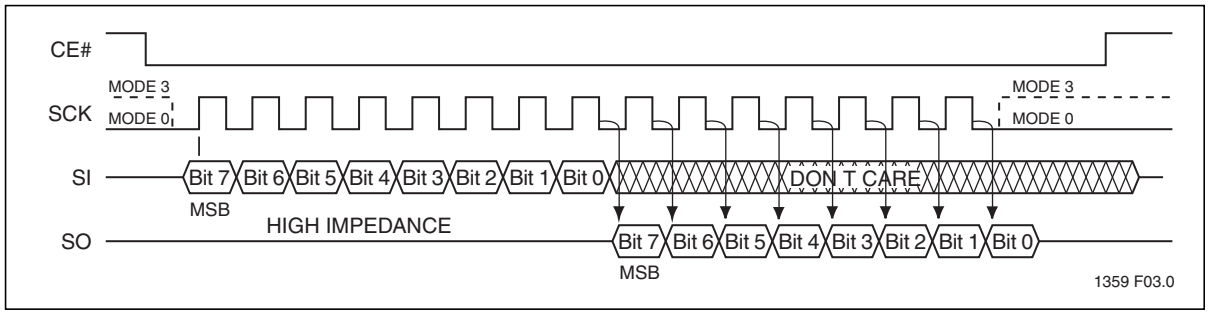


Figure 4: SPI Protocol (Traditional 25 Serial SPI Device)

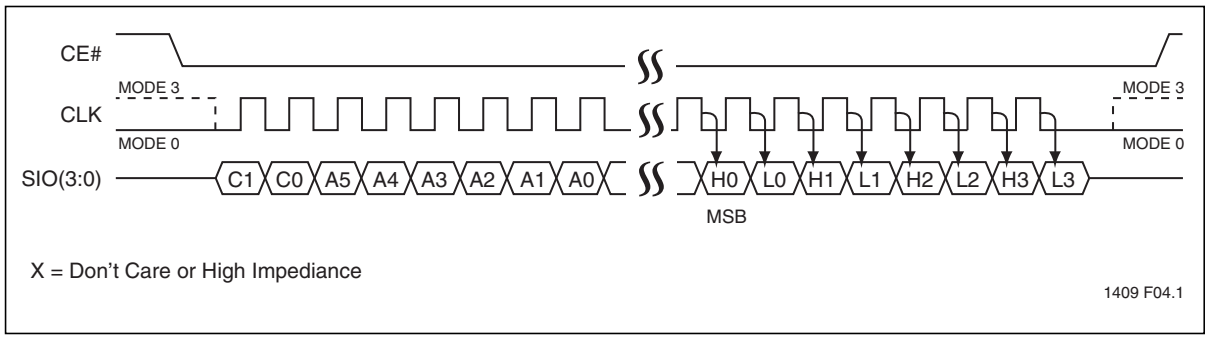


Figure 5: SQI Serial Quad I/O Protocol

Device Protection

The SST26VF016/032 have a Block-Protection register which provides a software mechanism to write-lock the array and write-lock, and/or read-lock, the parameter blocks. The Block-Protection Register is 48/80 bits wide per device: two bits each for the eight 8 KByte parameter blocks (write-lock and read-lock), and one bit each for the remaining 32 KByte and 64 KByte overlay blocks (write-lock). See Tables 8 - 9 for address range protected per register bit.

Each bit in the Block-Protection Register can be written to a '1' (protected) or '0' (unprotected). For the parameter blocks, the most significant bit is for read-lock, and the least significant bit is for write-lock. Read-locking the parameter blocks provides additional security for sensitive data after retrieval (e.g., after initial boot). If a block is read-locked all reads to the block return data 00H. All blocks are write-locked and read-unlocked after power-up or reset. The Write Block Locking Register command is a two cycle command requiring Write-Enable (WREN) to be executed prior to the Write Block-Protection Register command.

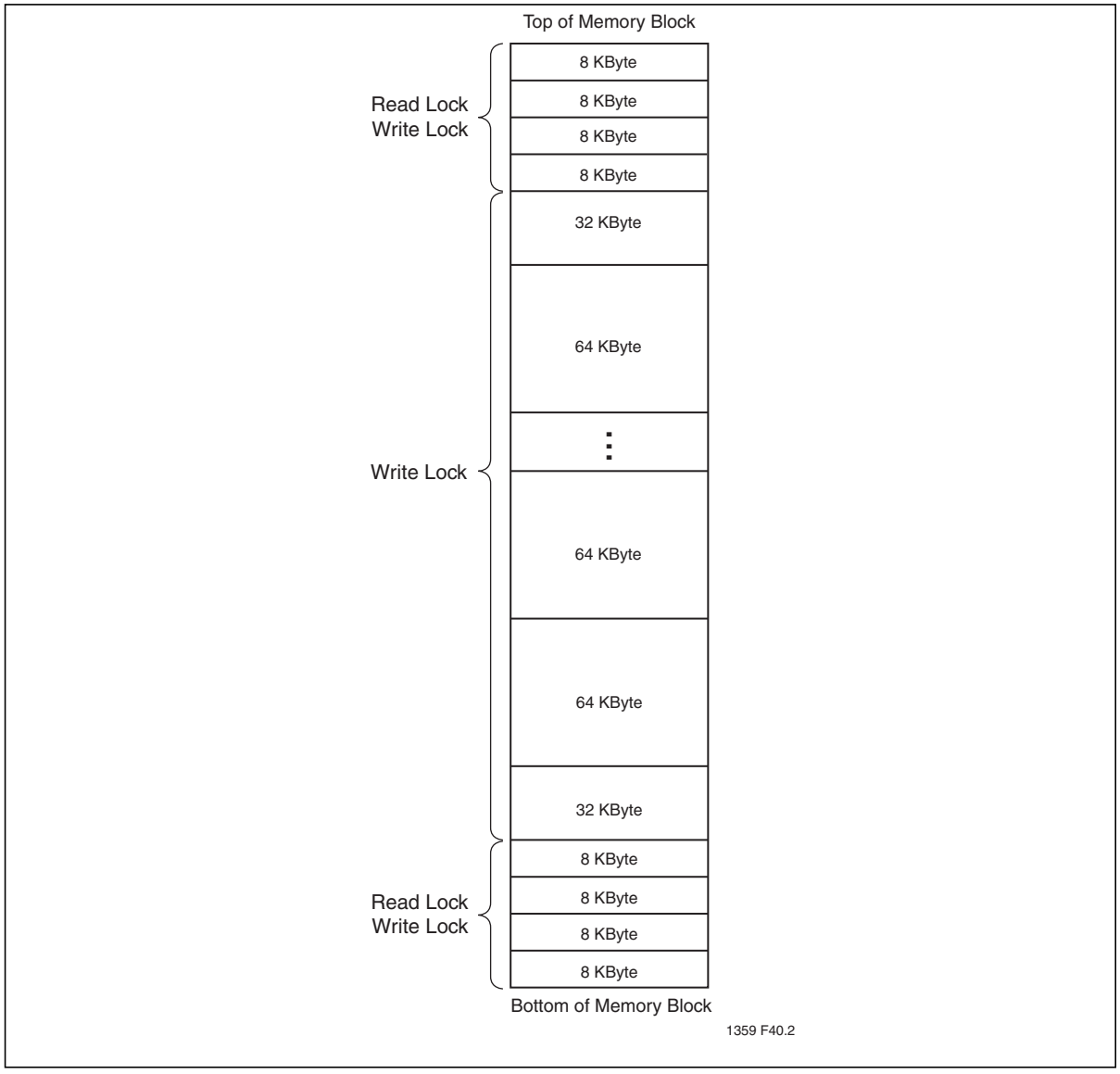


Figure 6: Block Locking Memory Map

Write-Protection Lock-Down

To prevent changes, the Block-Protection register can be set to Write-Protection Lock-Down using the Lock Down Block Protection Register (LPBR) command. Once the Write-Protection Lock-Down is enabled, the Block-Protection register can not be changed. To avoid inadvertent lock down, the WREN command must be executed prior to the LBPR command.

To reset Write-Protection Lock-Down, power cycle the device. The Write-Protection Lock-Down status may be read from the Status register.

Security ID

SST26VF016/032 offer a 256-bit Security ID (Sec ID) feature. The Security ID space is divided into two parts – one factory-programmed, 64-bit segment and one user-programmable 192-bit segment. The factory-programmed segment is programmed at SST with a unique number and cannot be changed. The user-programmable segment is left unprogrammed for the customer to program as desired.

Use the SecID Program command to program the Security ID using the address shown in Table 7. Once programmed, the Security ID can be locked using the Lockout Sec ID command. This prevents any future write to the Security ID.

The factory-programmed portion of the Security ID can't be programmed by the user; neither factory-programmed nor user-programmable areas can be erased.

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Status Register

The Status register is a read-only register that provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and whether an erase or program operation is suspended. During an internal Erase or Program operation, the Status register may be read to determine the completion of an operation in progress. Table 2 describes the function of each bit in the Status register.

Table 2: Status Register

Bit	Name	Function	Default at Power-up
0	RES	Reserved for future use	0
1	WEL	Write-Enable Latch status 1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0
2	WSE	Write Suspend-Erase status 1 = Erase suspended 0 = Erase is not suspended	0
3	WSP	Write Suspend-Program status 1 = Program suspended 0 = Program is not suspended	0
4	WPLD	Write Protection Lock-Down status 1 = Write Protection Lock-Down enabled 0 = Write Protection Lock-Down disabled	0
5	SEC[1]	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	0[1]
6	RES	Reserved for future use	0
7	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0

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1. The Security ID status will always be ‘1’ at power-up after a successful execution of the Lockout Sec ID instruction, otherwise default at power-up is ‘0’.

Write-Enable Latch (WEL)

The Write-Enable Latch (WEL) bit indicates the status of the internal memory's Write-Enable Latch. If the WEL bit is set to '1', the device is write enabled. If the bit is set to '0' (reset), the device is not write enabled and does not accept any memory Program or Erase, Protection Register Write, or Lock-Down commands. The Write-Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Reset
- Write-Disable (WRDI) instruction completion
- Page-Program instruction completion
- Sector-Erase instruction completion
- Block-Erase instruction completion
- Chip-Erase instruction completion
- Write-Block-Protection register instruction
- Lock-Down Block-Protection register instruction
- Program Security ID instruction completion
- Lockout Security ID instruction completion
- Write-Suspend instruction

Write Suspend Erase Status (WSE)

The Write Suspend-Erase Status (WSE) indicates when an Erase operation has been suspended. The WSE bit is '1' after the host issues a suspend command during an Erase operation. Once the suspended Erase resumes, the WSE bit is reset to '0.'

Write Suspend Program Status (WSP)

The Write Suspend-Program Status (WSP) bit indicates when a Program operation has been suspended. The WSP is '1' after the host issues a suspend command during the Program operation. Once the suspended Program resumes, the WSP bit is reset to '0.'

Write Protection Lockdown Status (WPLD)

The Write Protection-Lockdown Status (WPLD) bit indicates when the Block Protection register is locked-down to prevent changes to the protection settings. The WPLD is '1' after the host issues a Lock-Down Block Protection command. After a power cycle, the WPLD bit is reset to '0.'

Security ID Status (SEC)

The Security ID Status (SEC) bit indicates when the Security ID space is locked to prevent a Write command. The SEC is '1' after the host issues a Lockout SID command. Once the host issues a Lockout SID command, the SEC bit can never be reset to '0.'

Busy

The Busy bit determines whether there is an internal Erase or Program operation in progress. If the BUSY bit is '1', the device is busy with an internal Erase or Program operation. If the bit is '0', no Erase or Program operation is in progress.

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Instructions

Instructions are used to read, write (erase and program), and configure the SST26VF016/032. The instruction bus cycles are two nibbles each for commands (Op Code), data, and addresses. Prior to executing any write instructions, the Write-Enable (WREN) instruction must be executed. The complete list of the instructions is provided in Table 3.

All instructions are synchronized off a high to low transition of CE#. Inputs are accepted on the rising edge of SCK starting with the most significant nibble. CE# must be driven low before an instruction is entered and must be driven high after the last nibble of the instruction has been input (except for read instructions). Any low-to-high transition on CE# before receiving the last nibble of an instruction bus cycle, will terminate the instruction being entered and return the device to the standby mode.

Table 3: Device Operation Instructions for SST26VF016/032 (1 of 2)

Instruction	Description	Command Cycle[1]	Address Cycle(s)[2]	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
NOP	No Operation	00H	0	0	0	80 MHz
RSTEN	Reset Enable	66H	0	0	0	
RST[3]	Reset Memory	99H	0	0	0	
EQIO	Enable Quad I/O	38H	0	0	0	
RSTQIO[4]	Reset Quad I/O	FFH	0	0	0	
Read[5]	Read Memory	03H	3	0	1 to ∞	33 MHz
High-Speed Read[5]	Read Memory at Higher Speed	0BH	3	1	1 to ∞	80 MHz
Set Burst[6]	Set Burst Length	C0H	0	0	1	
Read Burst	nB Burst with Wrap	0CH	3	1	n to ∞	
Read PI[7]	Jump to address within 256 Byte page indexed by n	08H	1	1	1 to ∞	
Read I	Jump to address within block indexed by n	09H	2	2	1 to ∞	
Read BI	Jump to block Indexed by n	10H	1	2	1 to ∞	
JEDEC-ID [5,8]	JEDEC-ID Read	9FH	0	0	3 to ∞	
Quad J-ID[8]	Quad I/O J-ID Read	AFH	0	0	3 to ∞	
Sector Erase[9]	Erase 4 KBytes of Memory Array	20H	3	0	0	
Block Erase[10]	Erase 64, 32 or 8 KBytes of Memory Array	D8H	3	0	0	
Chip Erase	Erase Full Array	C7H	0	0	0	
Page Program	Program 1 to 256 Data Bytes	02H	3	0	1 to 256	
Write Suspend	Suspends Program/Erase	B0H	0	0	0	
Write Resume	Resumes Program/Erase	30H	0	0	0	
Read SID	Read Security ID	88H	1	1	1 to 32	
Program SID[11]	Program User Security ID area	A5H	1	0	1 to 24	
Lockout SID[11]	Lockout Security ID Programming	85H	0	0	0	
RDSR[12]	Read Status Register	05H	0	0	1 to ∞	
WREN	Write Enable	06H	0	0	0	
WRDI	Write Disable	04H	0	0	0	

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Table 3: Device Operation Instructions for SST26VF016/032 (Continued) (2 of 2)

Instruction	Description	Command Cycle[1]	Address Cycle(s)[2]	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
RBPR[13]	Read Block Protection Register	72H	0	0	1 to m/4	80 MHz
WBPR[11,13]	Write Block Protection Register	42H	0	0	1 to m/4	
LBPR[11]	Lock Down Block Protection Register	8DH	0	0	0	

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1. One BUS cycle is two clock periods (command, access, or data).
2. Address bits above the most significant bit of each density can be V_{IL} or V_{IH}.
3. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
4. Device accepts eight-clock command in SPI mode, or two-clock command in SQI mode.
5. After a power cycle, Read, High-Speed Read, and JEDEC-ID Read instructions input and output cycles are SPI bus protocol.
6. Burst length– n = 8 Bytes: Data(00H); n = 16 Bytes: Data(01H); n = 32 Bytes: Data(02H); n = 64 Bytes: Data(03H).
7. Address is 256 Bytes page align (2's complement)
8. The Quad J-ID read wraps the three Quad J-ID Bytes of data until terminated by a low-to-high transition on CE#
9. Sector Addresses: Use A_{MS} - A_{12}, remaining address are don't care, but must be set to V_{IL} or V_{IH}.
10. Blocks are 64 KByte, 32 KByte, or 8KByte, depending on location. Block Erase Address: A_{MS} - A_{16} for 64 KByte; A_{MS} - A_{15} for 32 KByte; A_{MS} - A_{13} for 8 KByte. Remaining addresses are don't care, but must be set to V_{IL} or V_{IH}.
11. Requires a prior WREN command.
12. The Read-Status register is continuous with ongoing clock cycles until terminated by a low-to-high transition on CE#.
13. Data is written/read from MSB to LSB. MSB = 48 for SST26VF016; 80 for SST26VF032

No Operation (NOP)

The No Operation command only cancels a Reset Enable command. NOP has no impact on any other command.

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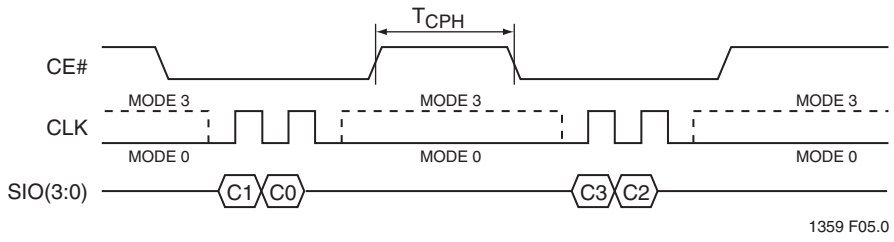
Reset-Enable (RSTEN) and Reset (RST)

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

To reset the SST26VF016/032, the host drives CE# low, sends the Reset-Enable command (66H), and drives CE# high. Next, the host drives CE# low again, sends the Reset command (99H), and drives CE# high, see Figure 7.

The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

A successful command execution will reset the burst length to 8 Bytes and all the bits in the Status register to their default states, except for bit 4 (WPLD) and bit 5 (SEC). A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations.



Note: C[1:0] = 66H; C[3:2] = 99H

Figure 7: Reset sequence

Read (33 MHz)

The Read instruction, 03H, is supported in SPI bus protocol only with clock frequencies up to 33 MHz. This command is not supported in SQI bus protocol. The device outputs the data starting from the specified address location, then continuously streams the data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically return to the beginning (wrap-around) of the address space.

Initiate the Read instruction by executing an 8-bit command, 03H, followed by address bits A23:A0. CE# must remain active low for the duration of the Read cycle. SIO2 and SIO3 must be driven V_{IH} for the duration of the Read cycle. See Figure 8 for Read Sequence.

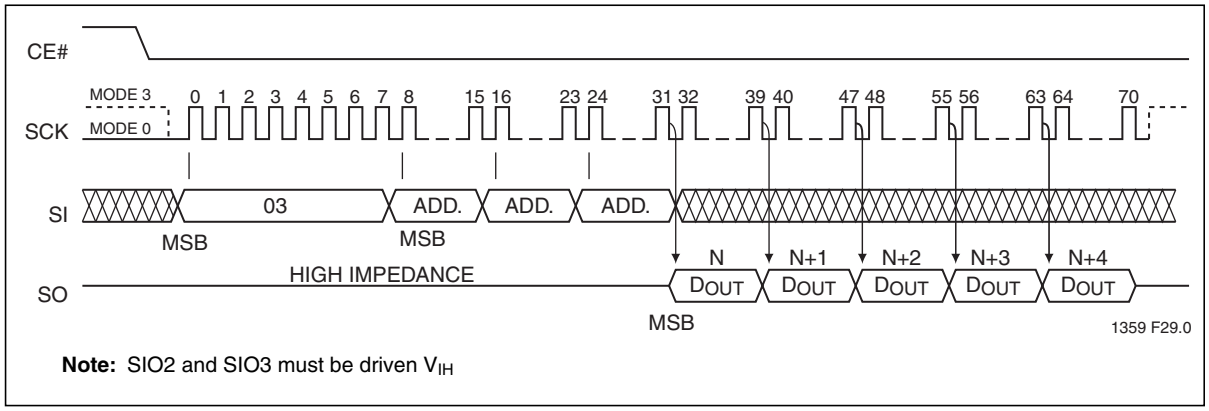


Figure 8: Read Sequence (SPI)

Enable Quad I/O (EQIO)

The Enable Quad I/O (EQIO) instruction, 38H, enables the flash device for SQI bus operation. upon completion of the instruction, all instructions thereafter will be 4-bit multiplexed input/output until a power cycle or a “Reset Quad I/O instruction” is executed. See Figure 9.

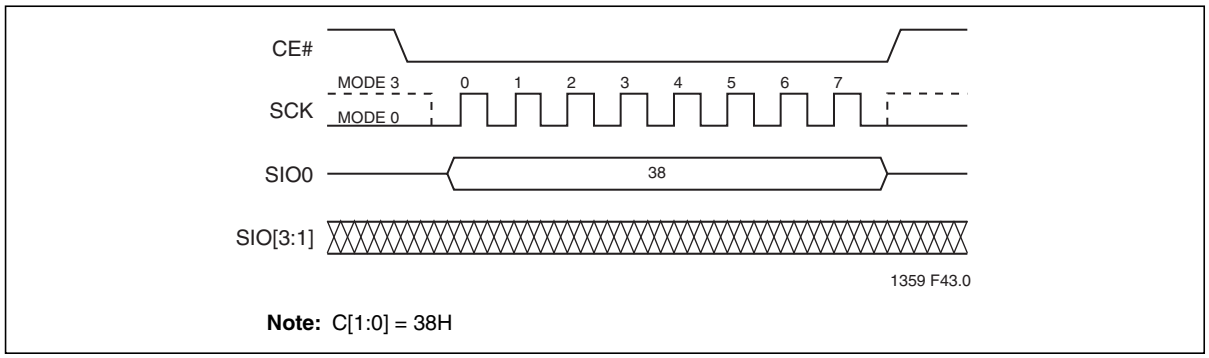


Figure 9: Enable Quad I/O Sequence

Reset Quad I/O (RSTQIO)

The Reset Quad I/O instruction, FFH, resets the device to 1-bit SPI protocol operation. To execute a Reset Quad I/O operation, the host drives CE# low, sends the Reset Quad I/O command cycle (FFH) then, drives CE# high. The device accepts either SPI (8 clocks) or SQI (2 clocks) command cycles. For SPI, SIO[3:1] are don't care for this command, but should be driven to V_{IH} or V_{IL}.

High-Speed Read (80 MHz)

The High-Speed Read instruction, 0BH, is supported in both SPI bus protocol and SQI protocol. On power-up, the device is set to use SPI.

Initiate High-Speed Read by executing an 8-bit command, 0BH, followed by address bits [A23-A0] and a dummy byte. CE# must remain active low for the duration of the High-Speed Read cycle. SIO2 and SIO3 must be driven V_{IH} for the duration of the Read cycle. See Figure 10 for the High-Speed Read sequence for SPI bus protocol.

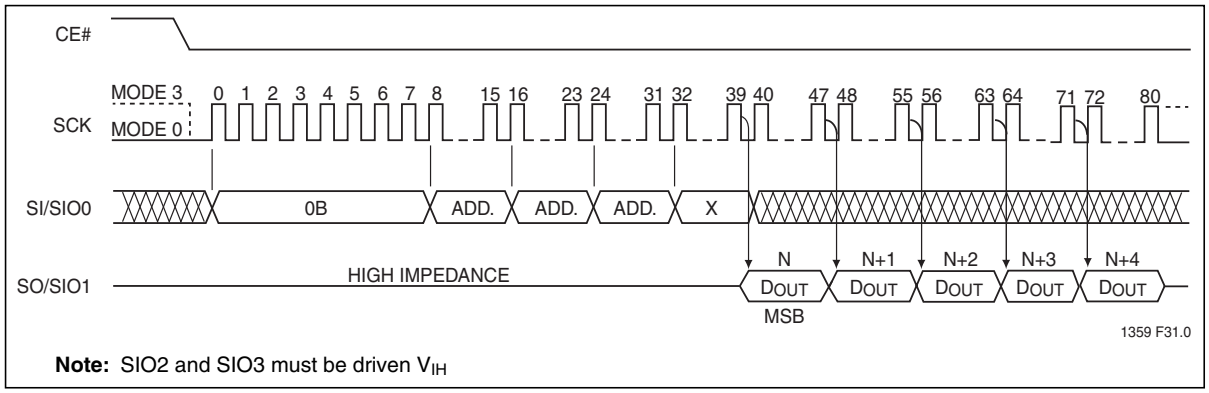


Figure 10: High-Speed Read Sequence (SPI)

In SQI protocol, the host drives CE# low then send the Read command cycle command, 0BH, followed by three address cycles and one dummy cycle. Each cycle is two nibbles (clocks) long, most significant nibble first.

After the dummy cycle, the Serial Quad I/O (SQI) Flash Memory outputs data on the falling edge of the SCK signal starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to address location 000000H.

During this operation, blocks that are Read-locked will output data 00H.

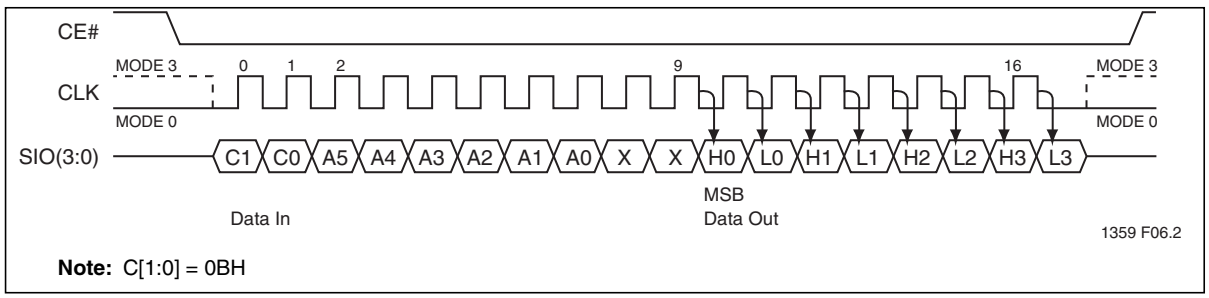


Figure 11: High-Speed Read Sequence (SQI)

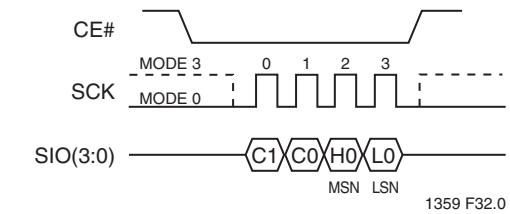
Set Burst

The Set Burst command specifies the number of bytes to be output during a Read Burst command before the device wraps around. To set the burst length the host drives CE# low, sends the Set Burst command cycle (C0H) and one data cycle, then drives CE# high. A cycle is two nibbles, or two clocks, long, most significant nibble first. After power-up or reset, the burst length is set to eight Bytes (00H). See Table 4 for burst length data and Figure 12 for the sequence.

Table 4: Burst Length Data

Burst Length	High Nibble (H0)	Low Nibble (L0)
8 Bytes	0h	0h
16 Bytes	0h	1h
32 Bytes	0h	2h
64 Bytes	0h	3h

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Note: MSN = Most Significant Nibble,
LSN = Least Significant Nibble

Figure 12: Set Burst Length Sequence

Read Burst

To execute a Read Burst operation the host drives CE# low, then sends the Read Burst command cycle (0CH), followed by three address cycles, and then one dummy cycle. Each cycle is two nibbles (clocks) long, most significant nibble first.

After the dummy cycle, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

During Read Burst, the internal address pointer automatically increments until the last byte of the burst is reached, then jumps to first byte of the burst. All bursts are aligned to addresses within the burst length, see Table 5. For example, if the burst length is eight Bytes, and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern would repeat until the command was terminated by a low-to-high transition on CE#.

During this operation, blocks that are Read-locked will output data 00H.

Table 5: Burst Address Ranges

Burst Length	Burst Address Ranges
8 Bytes	00-07H, 08-0FH, 10-17H, 18-1FH...
16 Bytes	00-0FH, 10-1FH, 20-2FH, 30-3FH...
32 Bytes	00-1FH, 20-3FH, 40-5FH, 60-7FH...
64 Bytes	00-3FH, 40-7FH, 80-BFH, C0-FFH

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Index Jump

Index Jump allows the host to read data using relative addressing instead of absolute addressing; in some cases this reduces the number of input clocks required to access data. The SST26VF016/032 support three Index Jump options:

- Read Page-Index-jump to address index within 256 Byte page
- Read Index-jump to address index within 64 KByte block
- Read Block-Index - jump to address index in another 64 KByte block.

Index Jumps following a Burst Read command are referenced from the last input address. For example, the device initiates a 64-Byte Read Burst instruction from address location 1EH and outputs an arbitrary number of Bytes. When the device issues a Read Page-Index instruction with 40H as the offset, the device will output data from address location 5EH. Index Jump operations following a High Speed Read (continuous read) instruction are referenced from the last address from which the full byte of data was output.

Data output by any of the Index-Jump commands follows the pattern of the last non-Index-Jump command. For example, a Read Page-Index command following a Read Burst, with 64-Byte wrap length, will continue to deliver data that wraps at 64-Byte boundaries after jumping to the address specified in the Read Page-Index command.

Read Page-Index (Read PI)

The Read Page-Index (Read PI) instruction increments the address counter within a page of 256 Bytes. To execute a Read PI operation the host drives CE# low then sends the Read PI command cycle (08H), one address cycle, and one dummy cycle. Each cycle is two nibbles (clocks) long, most significant nibble first.

The address cycle contain a two's complement number that specifies the number of bytes and direction the address pointer will jump. For example, to jump ahead 127 Bytes A1:A0 = 7FH; to jump back 127 Bytes A1:A0 = 81H.

The Read PI command does not cross 256 Byte page boundaries. If the jump distance exceeds the 256 Byte boundary, the address pointer wraps around to the beginning of the page, if the jump is forward, or to the end of the page, if the jump is backward. After the dummy cycle, the device outputs data on the falling edge of the SCK signal starting from the specified address location.

Read Index

The Read Index (Read I) instruction increments the address counter a specified number of bytes within a 64 KByte block. To execute a Read I operation the host drives CE# low then sends the Read I command cycle (09H), two address cycles, and two dummy cycles. Each cycle is two nibbles (clocks) long, most significant nibble first.

The address cycles contain a two's complement number that specifies the number of bytes and direction the address pointer will jump. For example, to jump ahead 256 Bytes, the address cycles would be 0100H; to jump back 256 Bytes, the address cycles would be FF00H.

The Read I command can not cross 64 KByte block boundaries, but it can cross boundaries of smaller blocks. If the jump distance exceeds the 64 KByte block boundary, the address pointer wraps around to the beginning of the block, if the jump is forward, and to the end of the block, if the jump is backward. After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location.

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Read Block Index (Read BI)

The Read Block Index (Read BI) instruction increments the address counter a specified number of 64 KByte blocks. To execute a Read BI operation the host drives CE# low, then sends the Read BI command cycle (10H), one address cycle, and two dummy cycles. Each cycle is two nibbles (clocks) long, most significant nibble first.

The address cycle contains a two's complement number specifying the number of blocks and the direction the address pointer will jump. The least significant address bits, A15:A0, do not change.

After the dummy cycle, the device outputs data on the falling edge of the SCK signal starting from the specified address location.

JEDEC-ID Read (SPI Protocol)

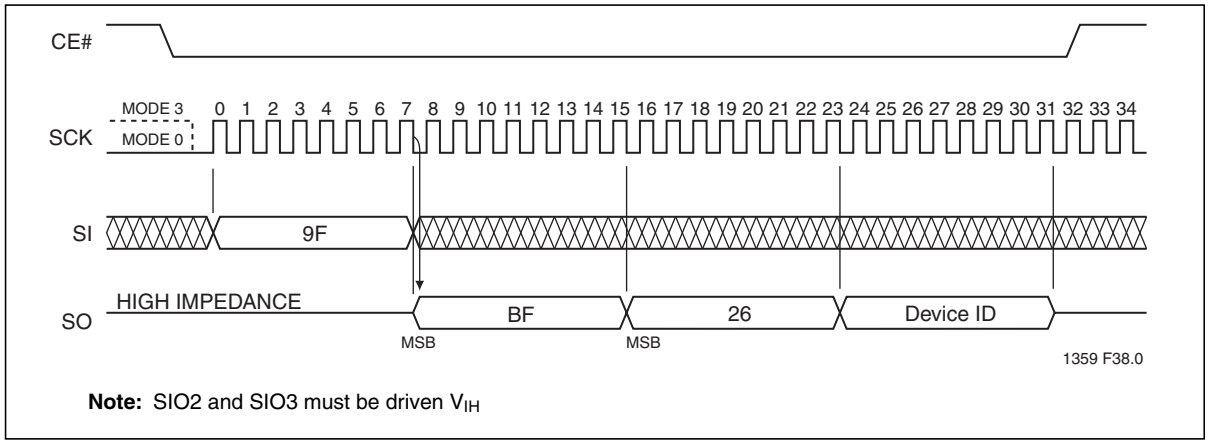
Using traditional SPI protocol, the JEDEC-ID Read instruction identifies the device as SST26VF016/032 and the manufacturer as SST. To execute a JECEC-ID operation the host drives CE# low then sends the JEDEC-ID command cycle (9FH). For SPI modes, each cycle is eight bits (clocks) long, most significant bit first.

Immediately following the command cycle the device outputs data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition on CE#. The device outputs three bytes of data: manufacturer, device type, and device ID, see Table 6. See Figure 13 for instruction sequence.

Table 6: Device ID Data Output

Product	Manufacturer ID (Byte 1)	Device ID	
		Device Type (Byte 2)	Device ID (Byte 3)
SST26VF016	BFH	26H	01H
SST26VF032	BFH	26H	02H

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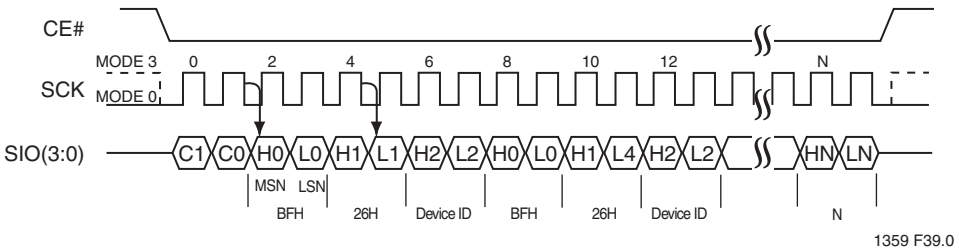
Note: SIO2 and SIO3 must be driven V_{IH}

Figure 13: JEDEC-ID Sequence (SPI Mode)

Quad J-ID Read (SQI Protocol)

The Quad J-ID Read instruction identifies the devices as SST26VF016/032 and manufacturer as SST. To execute a Quad J-ID operation the host drives CE# low and then sends the Quad J-ID command cycle (AFH). Each cycle is two nibbles (clocks) long, most significant nibble first.

Immediately following the command cycle the device outputs data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition of CE#. The device outputs three bytes of data: manufacturer, device type, and device ID, see Table 6. See Figure 14 for instruction sequence.



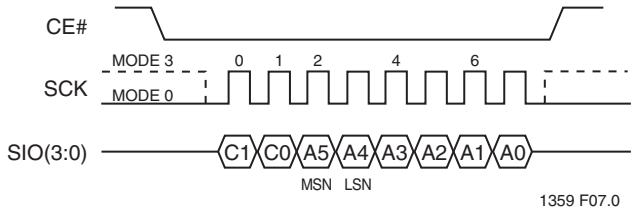
Note: MSN = Most significant Nibble; LSN= Least Significant Nibble
C[1:0]=AFH

Figure 14: Quad J-ID Read Sequence

Sector-Erase

The Sector-Erase instruction clears all bits in the selected 4 KByte sector to '1,' but it does not change a protected memory area. Prior to any write operation, the Write-Enable (WREN) instruction must be executed.

To execute a Sector-Erase operation, the host drives CE# low, then sends the Sector Erase command cycle (20H) and three address cycles, and then drives CE# high. Each cycle is two nibbles, or clocks, long, most significant nibble first. Address bits [A_{MS}:A_{12}] (A_{MS} = Most Significant Address) determine the sector address (SA_X); the remaining address bits can be V_{IL} or V_{IH}. Poll the BUSY bit in the Status register or wait T_{SE} for the completion of the internal, self-timed, Sector-Erase operation. See Figure 15 for the Sector-Erase sequence.



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble

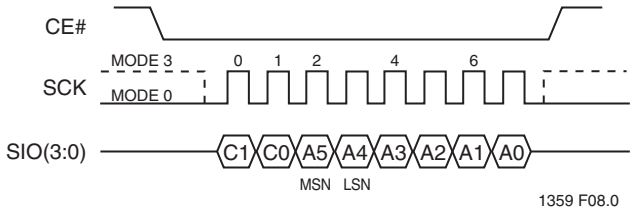
Figure 15: 4 KByte Sector-Erase Sequence

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Block-Erase

The Block-Erase instruction clears all bits in the selected block to '1'. Block sizes can be 8 KByte, 32 KByte or 64 KByte depending on address, see Figure 3, Memory Map, for details. A Block-Erase instruction applied to a protected memory area will be ignored. Prior to any write operation, execute the WREN instruction. Keep CE# active low for the duration of any command sequence.

To execute a Block-Erase operation, the host drives CE# low then sends the Block-Erase command cycle (D8H), three address cycles, then drives CE# high. Each cycle is two nibbles, or clocks, long, most significant nibble first. Address bits A_{MS}-A_{13} determine the block address; the remaining address bits can be V_{IL} or V_{IH}. For 32 KByte blocks, A_{14}:A_{13} can be V_{IL} or V_{IH}; for 64 KByte blocks, A_{15}:A_{13} can be V_{IL} or V_{IH}. Poll the BUSY bit in the Status register or wait T_{BE} for the completion of the internal, self-timed, Block-Erase operation See Figure 16 for the Block-Erase sequence.



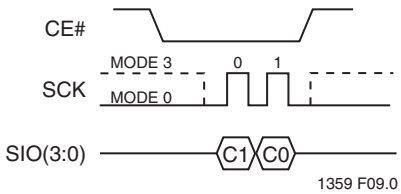
Note: MSN = Most Significant Nibble,
LSN = Least Significant Nibble
C[1:0] = D8H

Figure 16: Block-Erase Sequence

Chip-Erase

The Chip-Erase instruction clears all bits in the device to '1.' The Chip-Erase instruction is ignored if any of the memory area is protected. Prior to any write operation, execute the the WREN instruction.

To execute a Chip-Erase operation, the host drives CE# low, sends the Chip-Erase command cycle (C7H), then drives CE# high. A cycle is two nibbles, or clocks, long, most significant nibble first. Poll the BUSY bit in the Status register or wait T_{CE} for the completion of the internal, self-timed, Chip-Erase operation. See Figure 17 for the Chip Erase sequence.



Note: C[1:0] = C7H

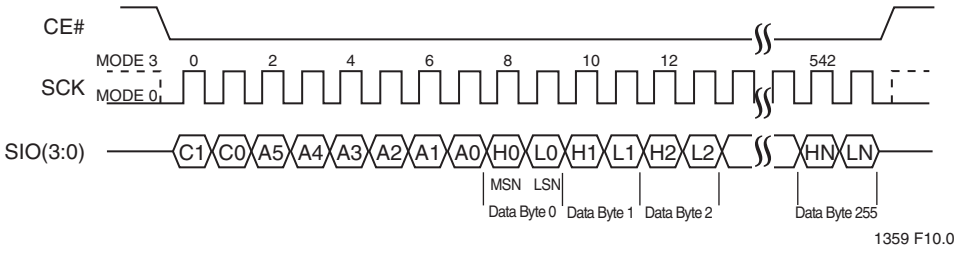
Figure 17: Chip-Erase Sequence

Page-Program

The Page-Program instruction programs up to 256 Bytes of data in the memory. The data for the selected page address must be in the erased state (FFH) before initiating the Page-Program operation. A Page-Program applied to a protected memory area will be ignored. Prior to the program operation, execute the WREN instruction.

To execute a Page-Program operation, the host drives CE# low then sends the Page Program command cycle (02H), three address cycles followed by the data to be programmed, then drives CE# high. The programmed data must be between 1 to 256 Bytes and in whole Byte increments; sending an odd number of nibbles will cause the last nibble to be ignored. Each cycle is two nibbles (clocks) long, most significant bit first. Poll the BUSY bit in the Status register or wait T_{PP} for the completion of the internal, self-timed, Page-Program operation. See Figure 18 for the Page-Program sequence.

When executing Page-Program, the memory range for the SST26VF016/032 is divided into 256 Byte page boundaries. The device handles shifting of more than 256 Bytes of data by maintaining the last 256 Bytes of data as the correct data to be programmed. If the target address for the Page-Program instruction is not the beginning of the page boundary (A7:A0 are not all zero), and the number of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
C[1:0] = 02H

Figure 18: Page-Program Sequence

Write-Suspend and Write-Resume

Write-Suspend allows the interruption of Sector-Erase, Block-Erase or Page-Program operations in order to erase, program, or read data in another portion of memory. The original operation can be continued with the Write-Resume command.

Only one write operation can be suspended at a time; if an operation is already suspended, the device will ignore the Write-Suspend command. Write-Suspend during Chip-Erase is ignored; Chip-Erase is not a valid command while a write is suspended.

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Write-Suspend During Sector-Erase or Block-Erase

Issuing a Write-Suspend instruction during Sector-Erase or Block-Erase allows the host to program or read any sector that was not being erased. The device will ignore any programming commands pointing to the suspended sector(s). Any attempt to read from the suspended sector(s) will output unknown data because the Sector- or Block-Erase will be incomplete.

To execute a Write-Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H), then drives CE# high. A cycle is two nibbles long, most significant nibble first. The Status register indicates that the erase has been suspended by changing the WSE bit from '0' to '1,' but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the BUSY bit in the Status register or wait T_{WS}.

Write-Suspend During Page Programming

Issuing a Write-Suspend instruction during Page Programming allows the host to erase or read any sector that is not being programmed. Erase commands pointing to the suspended sector(s) will be ignored. Any attempt to read from the suspended page will output unknown data because the program will be incomplete.

To execute a Write Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H), then drives CE# high. A cycle is two nibbles long, most significant nibble first. The Status register indicates that the programming has been suspended by changing the WSP bit from '0' to '1,' but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the BUSY bit in the Status register or wait T_{WS}.

Write-Resume

Write-Resume restarts a Write command that was suspended, and changes the suspend status bit in the Status register (WSE or WSP) back to '0'.

To execute a Write-Resume operation, the host drives CE# low, sends the Write Resume command cycle (30H), then drives CE# high. A cycle is two nibbles long, most significant nibble first. To determine if the internal, self-timed Write operation completed, poll the BUSY bit in the Status register, or wait the specified time T_{SE}, T_{BE} or T_{PP} for Sector-Erase, Block-Erase, or Page-Programming, respectively. The total write time before suspend and after resume will not exceed the uninterrupted write times T_{SE}, T_{BE} or T_{PP}.

Read Security ID

To execute a Read Security ID (SID) operation, the host drives CE# low, sends the Read Security ID command cycle (88H), one address cycle, and then one dummy cycle. Each cycle is two nibbles long, most significant nibble first.

After the dummy cycle, the device outputs data on the falling edge of the SCK signal, starting from the specified address location. The data output stream is continuous through all SID addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the last SID address is reached, then outputs 00H until CE# goes high.

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Program Security ID

The Program Security ID instruction programs one to 24 Bytes of data in the user-programmable, Security ID space. The device ignores a Program Security ID instruction pointing to an invalid or protected address, see Table 7. Prior to the program operation, execute WREN.

To execute a Program SID operation, the host drives CE# low, sends the Program Security ID command cycle (A5H), one address cycle, the data to be programmed, then drives CE# high. The programmed data must be between 1 to 24 Bytes and in whole Byte increments; sending an odd number of nibbles will cause the last nibble to be ignored. Each cycle is two nibbles long, most significant nibble first. To determine the completion of the internal, self-timed Program SID operation, poll the BUSY bit in the software status register, or wait T_{PSID} for the completion of the internal self-timed Program Security ID operation.

Table 7: Program Security ID

Program Security ID	Address Range
Pre-Programmed at factory	00H – 07H
User Programmable	08H – 1FH

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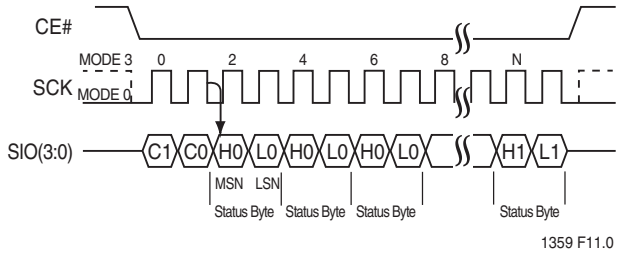
Lockout Security ID

The Lockout Security ID instruction prevents any future changes to the Security ID. To execute a Lockout SID, the host drives CE# low, sends the Lockout Security ID command cycle (85H), then drives CE# high. A cycle is two nibbles long, most significant nibble first. The user map polls the BUSY bit in the software status register or waits T_{PSID} for the completion of he Lockout Security ID operation.

Read-Status Register (RDSR)

The Read-Status register (RDSR) command outputs the contents of the Status register. The Status register may be read at any time even during a Write operation. When a Write is in progress, check the BUSY bit before sending any new commands to assure that the new commands are properly received by the device.

To execute a Read-Status-Register operation the host drives CE# low, then sends the Read-Status-Register command cycle (05H). Each cycle is two nibbles long, most significant nibble first. Immediately after the command cycle, the device outputs data on the falling edge of the SCK signal. The data output stream continues until terminated by a low-to-high transition on CE#. See Figure 19 for the RDSR instruction sequence.



Note: MSN = Most Significant Nibble; LSN = Least Significant Nibble
C[1:0] = 05H

Figure 19: Read-Status-Register (RDSR) Sequence

Write-Enable (WREN)

The Write-Enable (WREN) instruction sets the Write-Enable-Latch bit in the Status Register to '1,' allowing Write operations to occur. The WREN instruction must be executed prior to any of the following operations: Sector Erase, Block Erase, Chip Erase, Page Program, Program Security ID, Lockout Security ID, Write Block-Protection Register and Lockdown Block-Protection Register. To execute a Write Enable the host drives CE# low then sends the Write Enable command cycle (06H) then drives CE# high. A cycle is two nibbles (clocks) long, most significant nibble first. See Figure 20 for the WREN instruction sequence.

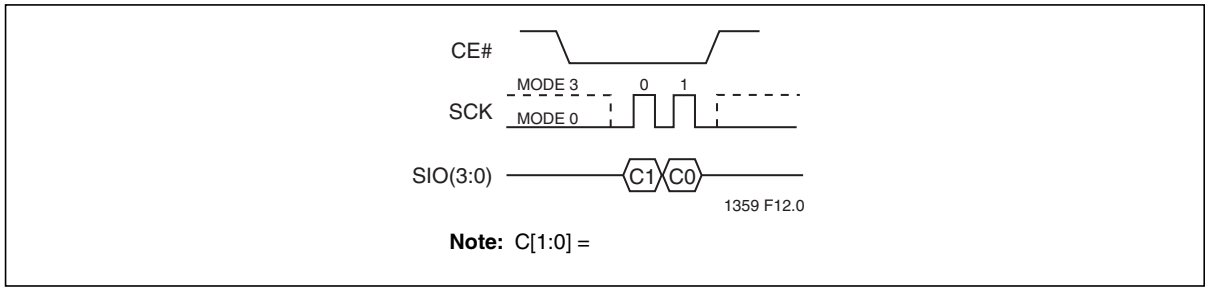


Figure 20: Write-Enable Sequence

Write-Disable (WRDI)

The Write-Disable (WRDI) instruction sets the Write-Enable-Latch bit in the Status Register to '0,' preventing Write execution without a prior WREN instruction. To execute a Write-Disable, the host drives CE# low, sends the Write Disable command cycle (04H), then drives CE# high. A cycle is two nibbles long, most significant nibble first.

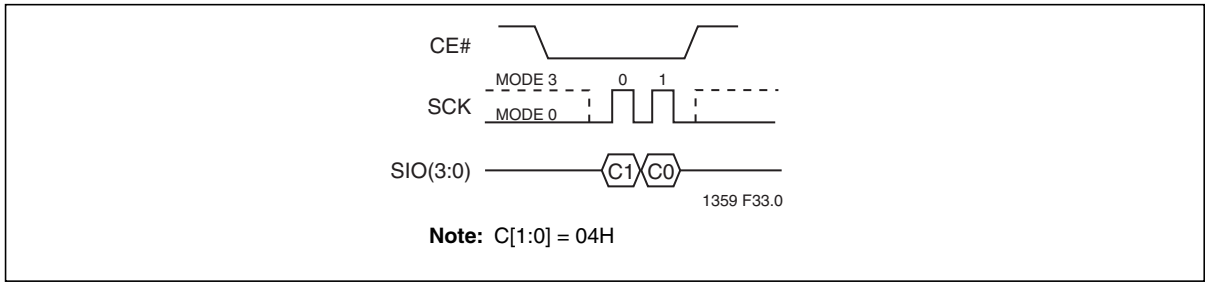
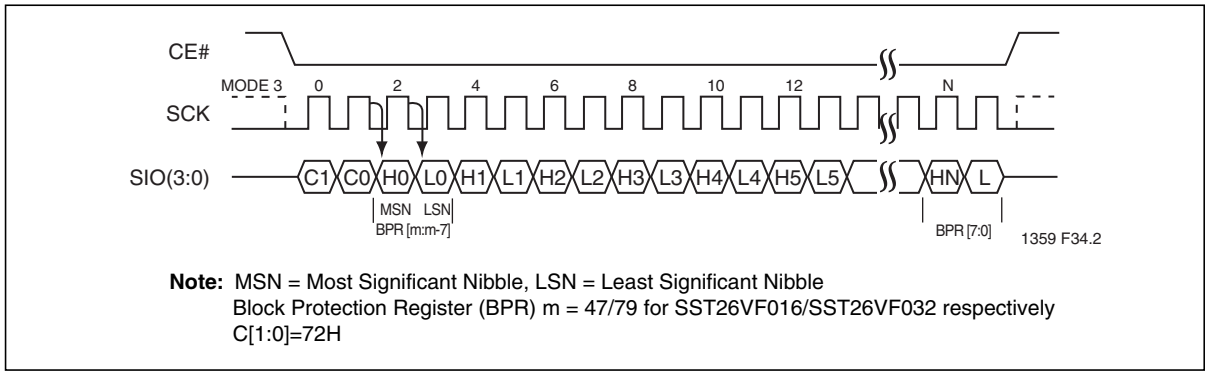


Figure 21: Write-Disable (WRDI) Sequence

Read Block-Protection Register (RBPR)

The Read Block-Protection Register instruction outputs the Block-Protection Register data which determines the protection status. To execute a Read Block-Protection Register operation, the host drives CE# low, and then sends the Read Block-Protection Register command cycle (72H). Each cycle is two nibbles long, most significant nibble first.

After the command cycle, the device outputs data on the falling edge of the SCK signal starting with the most significant nibble, see Tables 8 - 9 for definitions of each bit in the Block-Protection Register. The RBPR command does not wrap around. After all data has been output, the device will output 0H until terminated by a low-to-high transition on CE#. See Figure 22.

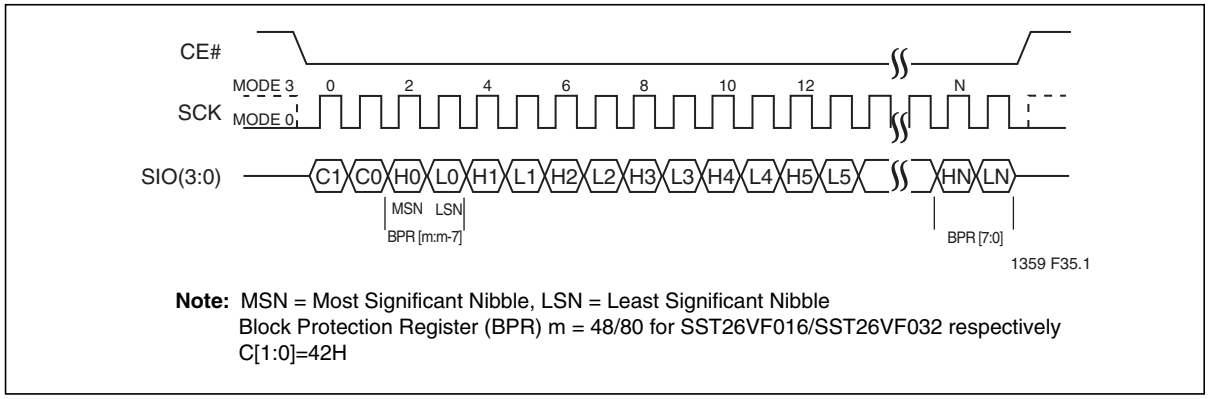


Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
Block Protection Register (BPR) m = 47/79 for SST26VF016/SST26VF032 respectively
C[1:0]=72H

Figure 22: Read Block Protection Register Sequence

Write Block-Protection Register (WBPR)

To execute a Write Block-Protection Register operation the host drives CE# low; sends the Write Block-Protection Register command cycle (42H); then sends six cycles of data for SST25VF016, or 10 cycles of data for SST25VF032, and finally drives CE# high. Each cycle is two nibbles long, most significant nibble first. See Tables 8 - 9 for definitions of each bit in the Block-Protection Register.



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
Block Protection Register (BPR) m = 48/80 for SST26VF016/SST26VF032 respectively
C[1:0]=42H

Figure 23: Write Block Protection Register Sequence

Table 8: Block-Protection Register for 26VF016[1]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock		
47	46	1FE000H - 1FFFFFH	8 KByte
45	44	1FC000H - 1FDFFFH	8 KByte
43	42	1FA000H - 1FBFFFH	8 KByte
41	40	1F8000H - 1F9FFFH	8 KByte
39	38	006000H - 007FFFH	8 KByte
37	36	004000H - 005FFFH	8 KByte
35	34	002000H - 003FFFH	8 KByte
33	32	000000H - 001FFFH	8 KByte
	31	1F0000H - 1F7FFFH	32 KByte
	30	008000H - 00FFFFH	32 KByte
	29	1E0000H - 1EFFFFH	64 KByte
	28	1D0000H - 1DFFFFH	64 KByte
	27	1C0000H - 1CFFFFH	64 KByte
	26	1B0000H - 1BFFFFH	64 KByte
	25	1A0000H - 1AFFFFH	64 KByte
	24	190000H - 19FFFFH	64 KByte
	23	180000H - 18FFFFH	64 KByte
	22	170000H - 17FFFFH	64 KByte
	21	160000H - 16FFFFH	64 KByte
	20	150000H - 15FFFFH	64 KByte
	19	140000H - 14FFFFH	64 KByte
	18	130000H - 13FFFFH	64 KByte
	17	120000H - 12FFFFH	64 KByte
	16	110000H - 11FFFFH	64 KByte
	15	100000H - 10FFFFH	64 KByte
	14	0F0000H - 0FFFFFH	64 KByte
	13	0E0000H - 0EFFFFH	64 KByte
	12	0D0000H - 0DFFFFH	64 KByte
	11	0C0000H - 0CFFFFH	64 KByte
	10	0B0000H - 0BFFFFH	64 KByte
	9	0A0000H - 0AFFFFH	64 KByte
	8	090000H - 09FFFFH	64 KByte
	7	080000H - 08FFFFH	64 KByte
	6	070000H - 07FFFFH	64 KByte
	5	060000H - 06FFFFH	64 KByte
	4	050000H - 05FFFFH	64 KByte
	3	040000H - 04FFFFH	64 KByte
	2	030000H - 03FFFFH	64 KByte
	1	020000H - 02FFFFH	64 KByte
	0	010000H - 01FFFFH	64 KByte

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1. All blocks are write-locked and read-unlocked after power-up or reset.

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Table 9: Block-Protection Register for 26VF032 (1 of 2)[1]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock		
79	78	3FE000H - 3FFFFFH	8 KByte
77	76	3FC000H - 3FDFFFH	8 KByte
75	74	3FA000H - 3FBFFFH	8 KByte
73	72	3F8000H - 3F9FFFH	8 KByte
71	70	006000H - 007FFFH	8 KByte
69	68	004000H - 005FFFH	8 KByte
67	66	002000H - 003FFFH	8 KByte
65	64	000000H - 001FFFH	8 KByte
	63	3F0000H - 3F7FFFH	32 KByte
	62	008000H - 00FFFFH	32 KByte
	61	3E0000H - 3EFFFFH	64 KByte
	60	3D0000H - 3DFFFFH	64 KByte
	59	3C0000H - 3CFFFFH	64 KByte
	58	3B0000H - 3BFFFFH	64 KByte
	57	3A0000H - 3AFFFFH	64 KByte
	56	390000H - 39FFFFH	64 KByte
	55	380000H - 38FFFFH	64 KByte
	54	370000H - 37FFFFH	64 KByte
	53	360000H - 36FFFFH	64 KByte
	52	350000H - 35FFFFH	64 KByte
	51	340000H - 34FFFFH	64 KByte
	50	330000H - 33FFFFH	64 KByte
	49	320000H - 32FFFFH	64 KByte
	48	310000H - 31FFFFH	64 KByte
	47	300000H - 30FFFFH	64 KByte
	46	2F0000H - 2FFFFFH	64 KByte
	45	2E0000H - 2EFFFFH	64 KByte
	44	2D0000H - 2DFFFFH	64 KByte
	43	2C0000H - 2CFFFFH	64 KByte
	42	2B0000H - 2BFFFFH	64 KByte
	41	2A0000H - 2AFFFFH	64 KByte
	40	290000H - 29FFFFH	64 KByte
	39	280000H - 28FFFFH	64 KByte
	38	270000H - 27FFFFH	64 KByte
	37	260000H - 26FFFFH	64 KByte
	36	250000H - 25FFFFH	64 KByte
	35	240000H - 24FFFFH	64 KByte
	34	230000H - 23FFFFH	64 KByte
	33	220000H - 22FFFFH	64 KByte
	32	210000H - 21FFFFH	64 KByte

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Table 9: Block-Protection Register for 26VF032 (Continued) (2 of 2)[1]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock		
	31	200000H - 20FFFFH	64 KByte
	30	1F0000H - 1FFFFFH	64 KByte
	29	1E0000H - 1EFFFFH	64 KByte
	28	1D0000H - 1DFFFFH	64 KByte
	27	1C0000H - 1CFFFFH	64 KByte
	26	1B0000H - 1BFFFFH	64 KByte
	25	1A0000H - 1AFFFFH	64 KByte
	24	190000H - 19FFFFH	64 KByte
	23	180000H - 18FFFFH	64 KByte
	22	170000H - 17FFFFH	64 KByte
	21	160000H - 16FFFFH	64 KByte
	20	150000H - 15FFFFH	64 KByte
	19	140000H - 14FFFFH	64 KByte
	18	130000H - 13FFFFH	64 KByte
	17	120000H - 12FFFFH	64 KByte
	16	110000H - 11FFFFH	64 KByte
	15	100000H - 10FFFFH	64 KByte
	14	0F0000H - 0FFFFFH	64 KByte
	13	0E0000H - 0EFFFFH	64 KByte
	12	0D0000H - 0DFFFFH	64 KByte
	11	0C0000H - 0CFFFFH	64 KByte
	10	0B0000H - 0BFFFFH	64 KByte
	9	0A0000H - 0AFFFFH	64 KByte
	8	090000H - 09FFFFH	64 KByte
	7	080000H - 08FFFFH	64 KByte
	6	070000H - 07FFFFH	64 KByte
	5	060000H - 06FFFFH	64 KByte
	4	050000H - 05FFFFH	64 KByte
	3	040000H - 04FFFFH	64 KByte
	2	030000H - 03FFFFH	64 KByte
	1	020000H - 02FFFFH	64 KByte
	0	010000H - 01FFFFH	64 KByte

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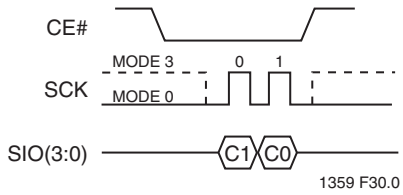
1. All blocks are write-locked and read-unlocked after power-up or reset.

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Lockdown Block-Protection Register (LBPR)

The Lockdown Block-Protection Register instruction prevents changes to the Block-Protection Register. Lockdown resets after power cycling; this allows the Block-Protection Register to be changed.

To execute a Lockdown Block-Protection Register, the host drives CE# low, then sends the Lockdown Block-Protection Register command cycle (8DH), then drives CE# high. A cycle is two nibbles long, most significant nibble first.



Note: C[1:0]=8DH

Figure 24: Lockdown Block-Protection Register

Electrical Specifications

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature. . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (T_A = 25°C). 1.0W
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[1]. . . . . 50 mA

1. Output shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{DD}
Industrial	-40°C to +85°C	2.7-3.6V

Table 10: AC Conditions of Test[1]

Input Rise/Fall Time	Output Load
3ns	C_L = 30 pF

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1. See Figure 29

Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 2.7V in less than 270 ms). See Table 11 and Figure 25 for more information.

Table 11: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	100	µs
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	100	µs

T11.0 25017

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

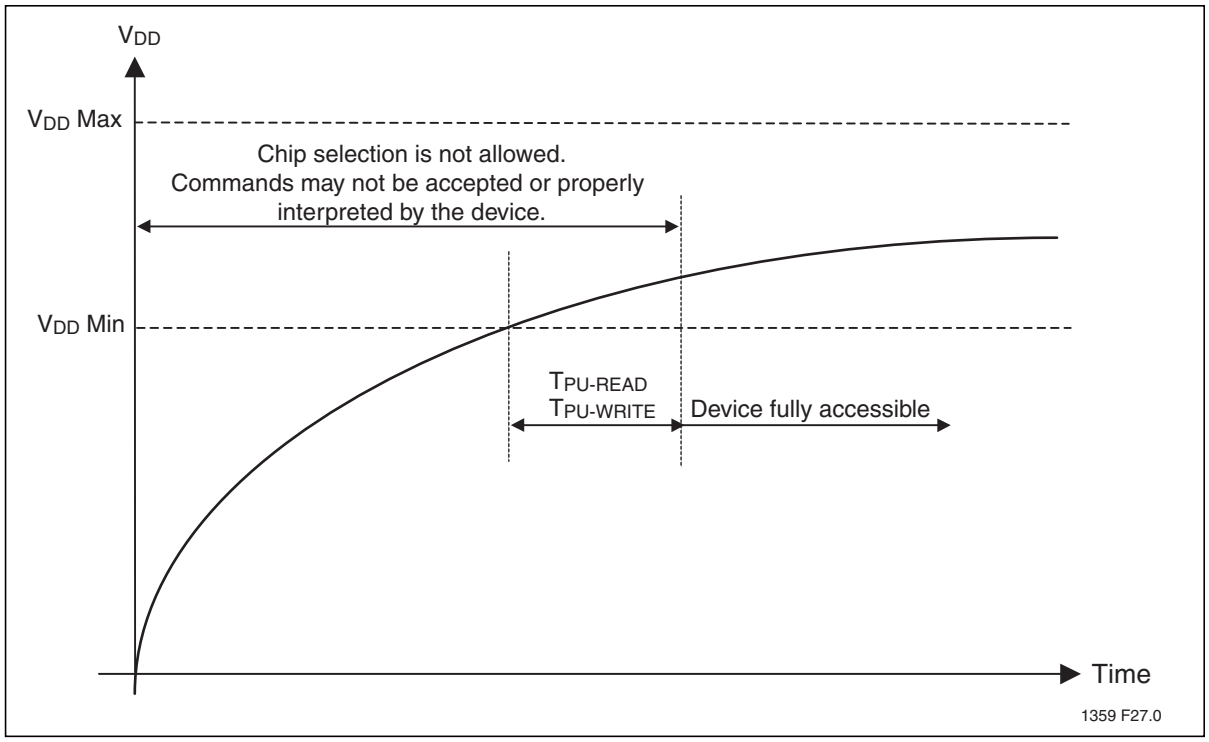


Figure 25: Power-up Timing Diagram

DC Characteristics

Table 12: DC Operating Characteristics (V_{DD} = 2.7- 3.6V)

Symbol	Parameter	Limits				Test Conditions
		Min	Typ	Max	Units	
I_{DDR}	Read Current		12	18	mA	V_{DD}=V_{DD} Min, CE#=0.1 V_{DD}/0.9 V_{DD}@33 MHz, SO=open
I_{DDW}	Program and Erase Current			30	mA	CE#=V_{DD}
I_{SB1}	Standby Current		8	15	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{LI}	Input Leakage Current			1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current			1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage			0.8	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}			V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage			0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2			V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

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Table 13: Capacitance (TA = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 14: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	100,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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AC Characteristics

Table 15: AC Operating Characteristics

Symbol	Parameter	Limits - 33 MHz		Limits - 80 MHz		Units
		Min	Max	Min	Max	
F_{CLK}	Serial Clock Frequency		33		80	MHz
T_{CLK}	Serial Clock Period	30		12.5		ns
T_{SCKH}	Serial Clock High Time	13		5.5		ns
T_{SCKL}	Serial Clock Low Time	13		5.5		ns
T_{SCKR}[1]	Serial Clock Rise Time (slew rate)	0.1		0.1		V/ns
T_{SCKF}[1]	Serial Clock Fall Time (slew rate)	0.1		0.1		V/ns
T_{CES}[2]	CE# Active Setup Time	12		5		ns
T_{CEH}[2]	CE# Active Hold Time	12		5		ns
T_{CHS}[2]	CE# Not Active Setup Time	10		3		ns
T_{CHH}[2]	CE# Not Active Hold Time	10		3		ns
T_{CPH}	CE# High Time	100		12.5		ns
T_{CHZ}	CE# High to High-Z Output		14		12.5	ns
T_{CLZ}	SCK Low to Low-Z Output	0		0		ns
T_{DS}	Data In Setup Time	3		3		ns
T_{DH}	Data In Hold Time	4		4		ns
T_{OH}	Output Hold from SCK Change	0		0		ns
T_V	Output Valid from SCK		12		6	ns
T_{SE}	Sector-Erase		25		25	ms
T_{BE}	Block-Erase		25		25	ms
T_{SCE}	Chip-Erase		50		50	ms
T_{PP}	Page-Program		1.5		1.5	ms
T_{PSID}	Program Security ID		0.2		0.2	ms
T_{WS}	Write-Suspend Latency		10		10	µs

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1. Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements
2. Relative to SCK.

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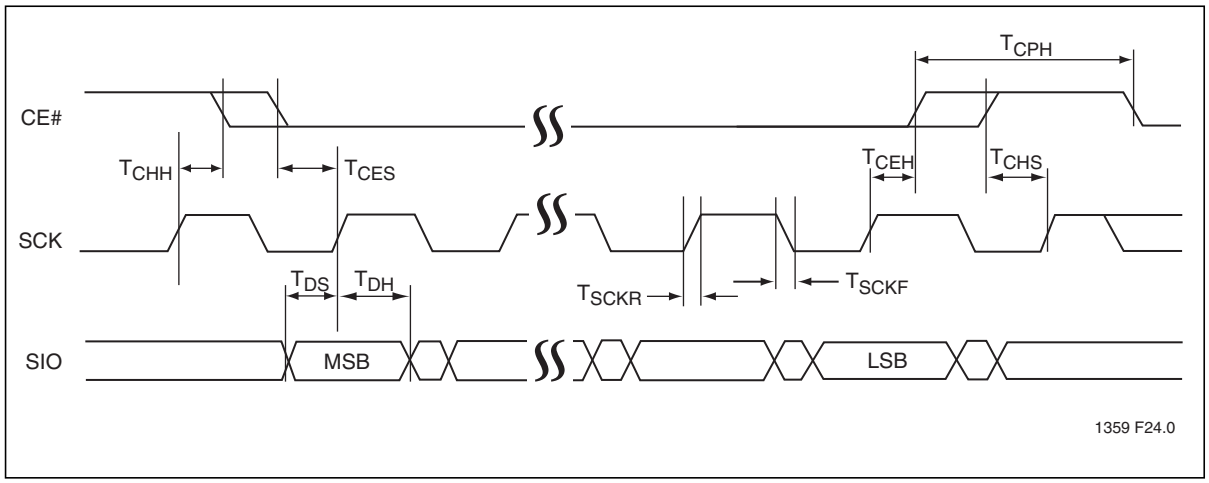


Figure 26: Serial Input Timing Diagram

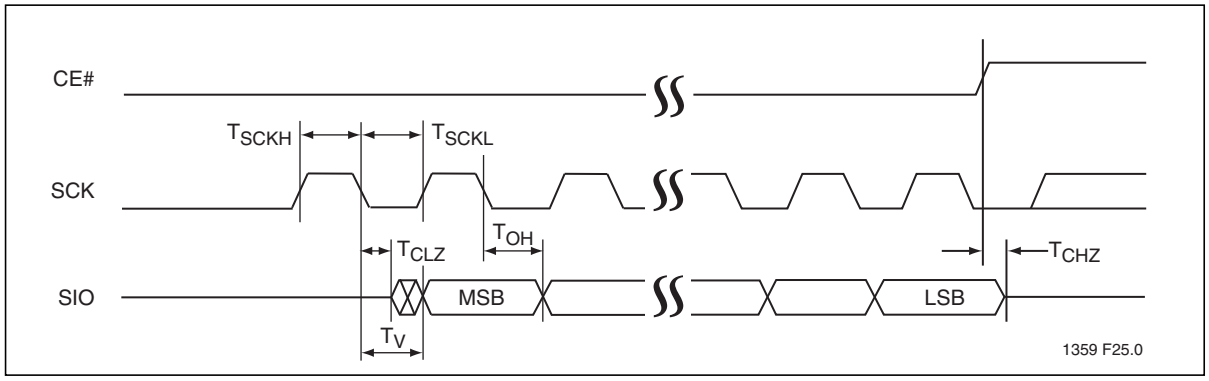
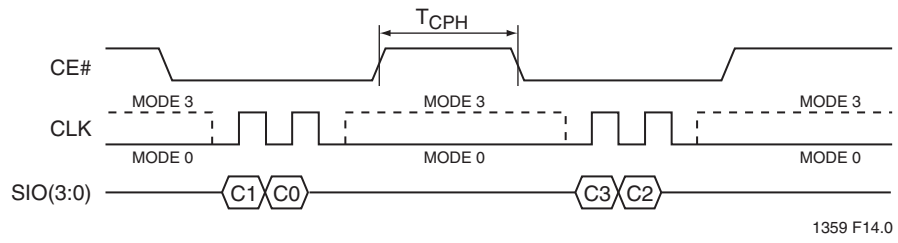


Figure 27: Serial Output Timing Diagram

Table 16: Reset Timing Parameters

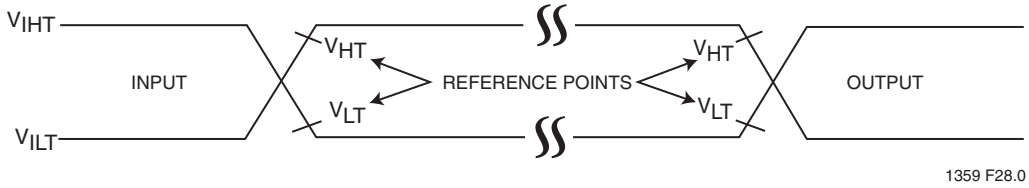
$T_{R(i)}$	Parameter	Minimum	Maximum	Units
$T_{R(o)}$	Reset to Read (non-data operation)		10	ns
$T_{R(p)}$	Reset Recovery from Program or Suspend		100	µs
$T_{R(e)}$	Reset Recovery from Erase		1	ms

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Note: C[1:0] = 55H; C[3:2] = AAH

Figure 28: Reset Timing Diagram

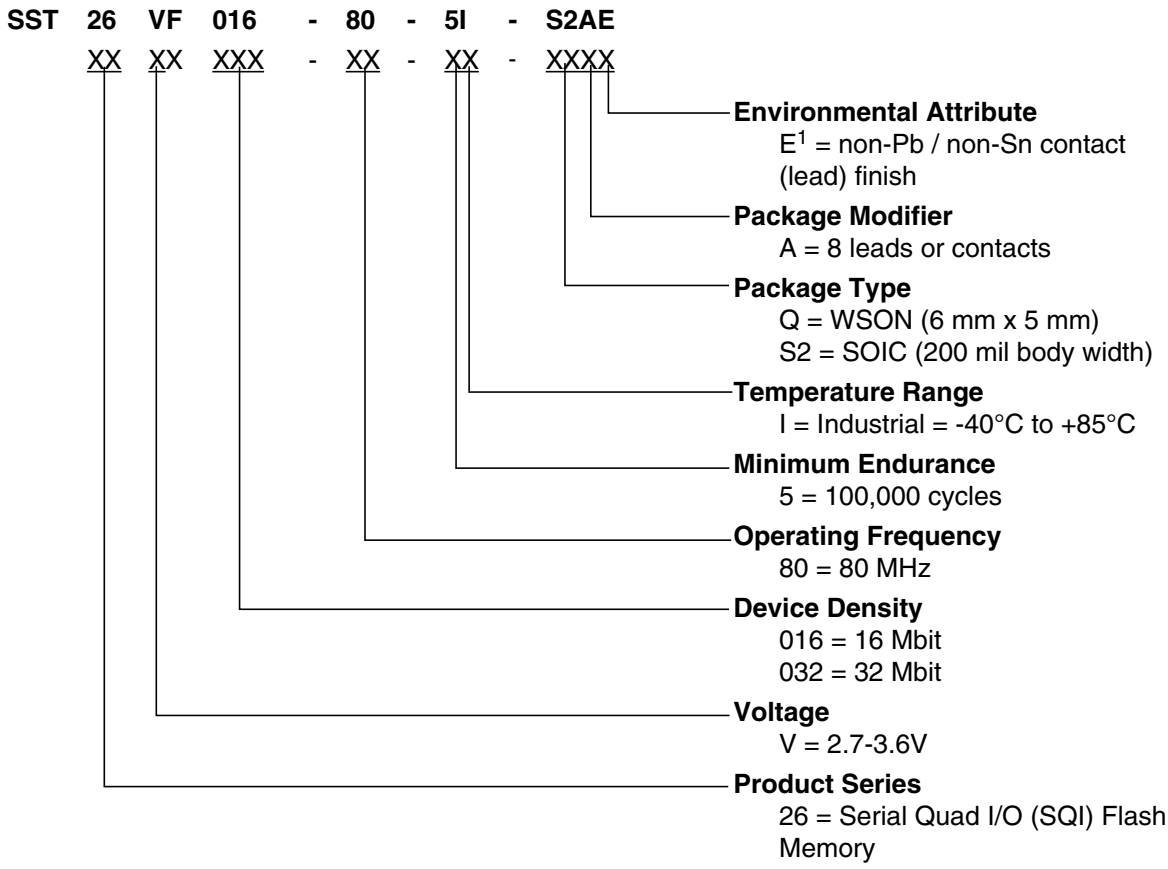


AC test inputs are driven at V_{IHT} ($0.9V_{DD}$) for a logic '1' and V_{ILT} ($0.1V_{DD}$) for a logic '0'. Measurement reference points for inputs and outputs are V_{HT} ($0.6V_{DD}$) and V_{LT} ($0.4V_{DD}$). Input rise and fall times (10% ↔ 90%) are <3 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test

Figure 29: AC Input/Output Reference Waveforms

Product Ordering Information



1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST26VF016

SST26VF016-80-5I-QAE SST26VF016-80-5I-S2AE

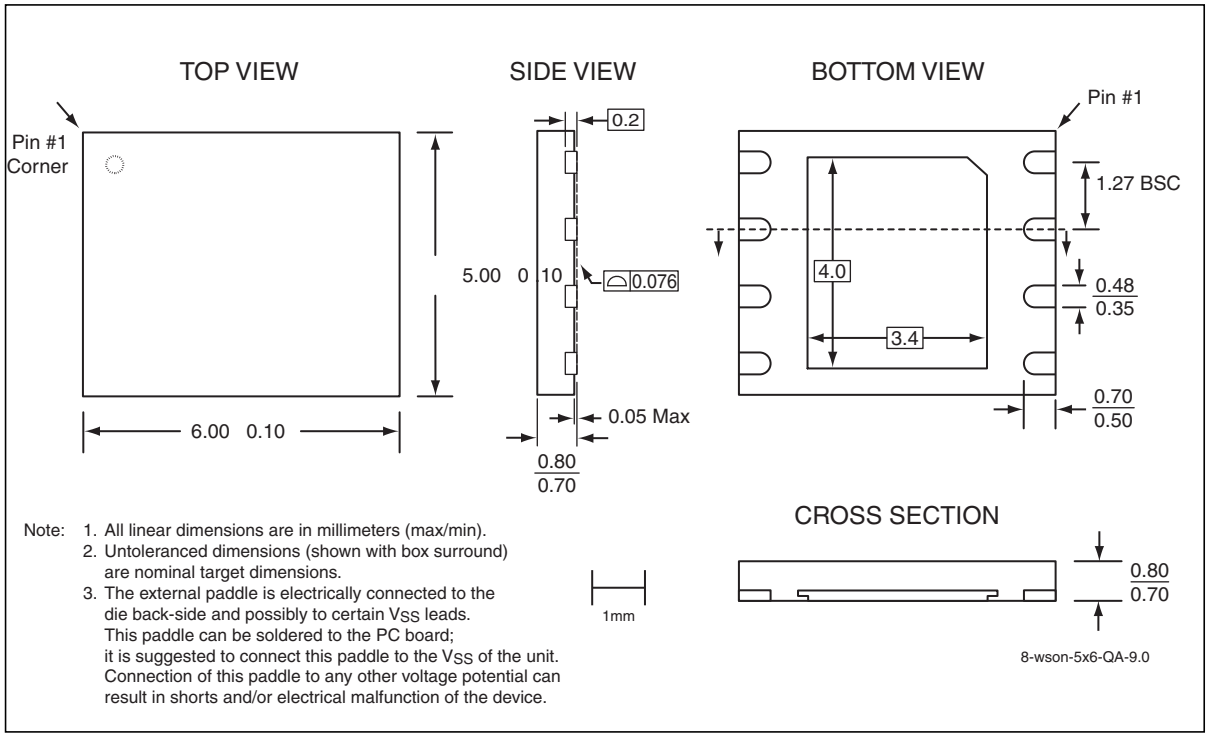
Valid combinations for SST26VF032

SST26VF032-80-5I-QAE SST26VF032-80-5I-S2AE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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Packaging Diagrams



Note:
1. All linear dimensions are in millimeters (max/min).
2. Untoleranced dimensions (shown with box surround) are nominal target dimensions.
3. The external paddle is electrically connected to the die back-side and possibly to certain V_{SS} leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the V_{SS} of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.

Figure 30: 8-Contact Very-very-thin, Small-outline, No-lead (WSON)
SST Package Code: QA

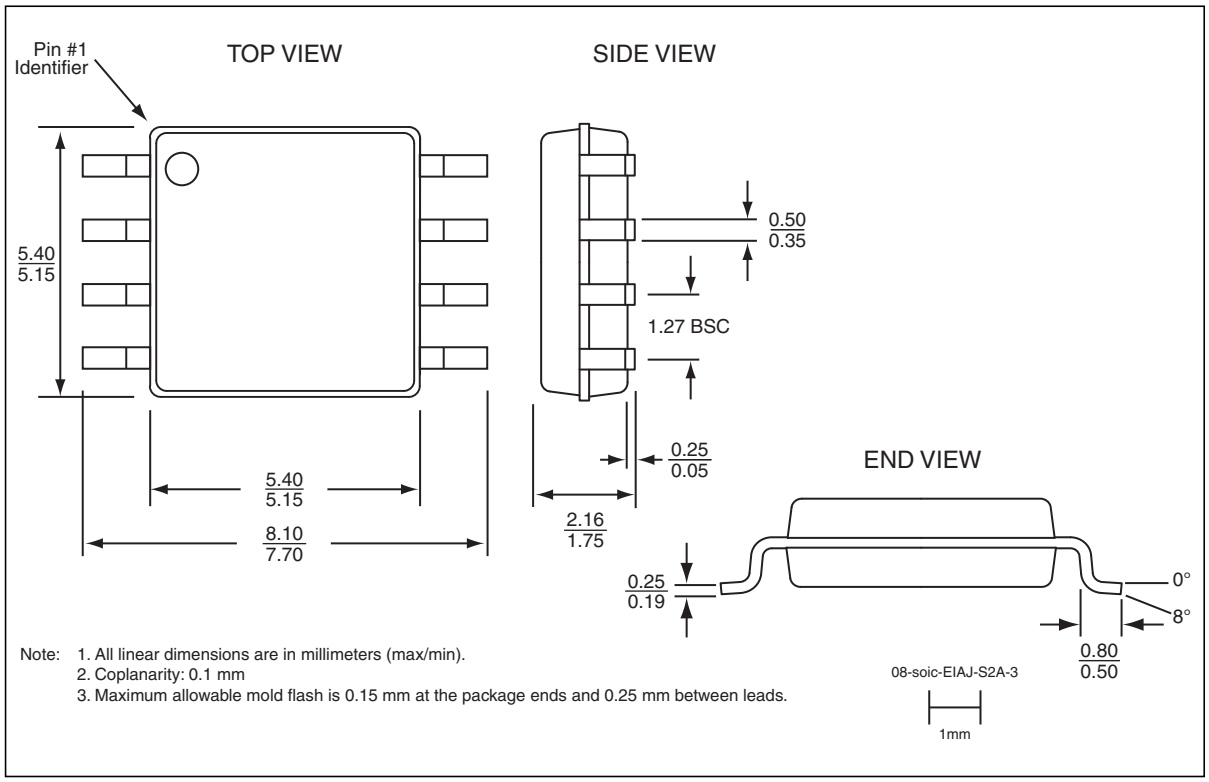


Figure 31: 8-Lead, Small Outline Integrated Circuit (SOIC)
SST Package Code: S2A

Table 17: Revision History

Number	Description	Date
00	• Initial release of data sheet	Apr 2008
01	• Revised “Product Ordering Information” on page 36 changing package codes QAF to QAE and S2AF to S2AE.	Dec 2008
02	• Revised “Features” and “Product Description” on page 2. • Updated Table 2 on page 9, Table 5 on page 16, Table 8 on page 26, Table 9 on page 27, Table 12 on page 32, Table 15 on page 33, and Table 16 on page 34. • Text changes to “Device Operation” on page 6, “Write-Enable Latch (WEL)” on page 10, “Reset-Enable (RSTEN) and Reset (RST)” on page 13, “High-Speed Read (80 MHz)” on page 15, “Read Block-Protection Register (RBPR)” on page 25, and “Write Block-Protection Register (WBPR)” on page 25. • Updated Figure 14 on page 19, Figure 19 on page 23, and Figure 22 on page 25.	Apr 2009
03	• Revised Table 15 on page 33; changed T_{CES} (80MHz) from 6ns to 5ns. • Changed document phase from Advance Information to Data Sheet	Jun 2009
04	• Applied new format	Nov 2009
05	• Updated Table 12 on page 32	Jun 2010
A	• Applied new document format • Released document under letter-revision system • Updated Spec Number S71359 to DS-25017	Apr 2011

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Memory sizes denote raw storage capacity; actual usable capacity may be less.

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