Not recommended for new designs.
Please use SST12LP15B

A Microchip Technology Company

2.4 GHz High-Power, High-Gain Power Amplifier

SST12LP15

Not Recommended for New Designs

The SST12LP15 is a high-power, high-gain power amplifier based on the highly-reliable InGaP/GaAs HBT technology. Easily configured for high-power, high-efficiency applications with superb power-added efficiency, it typically provides 35 dB gain with 26% power added efficiency @ POUT = 24 dBm for 802.11g and 29% power-added efficiency @ POUT = 25 dBm for 802.11b. The SST12LP15 has excellent linearity while meeting 802.11g spectrum mask at 24+ dBm, and is offered in 16-contact VQFN package.

Features

- **High Gain:**
  - Typically 35 dB gain across 2.4~2.5 GHz over temperature 0°C to +80°C
- **High linear output power:**
  - >29 dBm P1dB (Exceeding maximum rating of average output power, never measure with CW source! Pulsed single-tone source with <50% duty cycle is recommended.)
  - Meets 802.11g OFDM ACPR requirement up to 25 dBm
  - Added EVM~4% up to 23.5 dBm for 54 Mbps 802.11g signal
  - Meets 802.11b ACPR requirement up to 25 dBm
- **High power-added efficiency/Low operating current for both 802.11g/b applications**
  - ~26%/290 mA @ P_{OUT} = 24 dBm for 802.11g
  - ~29%/340 mA @ P_{OUT} = 25 dBm for 802.11b
- **Built-in Ultra-low I_{REF} power-up/down control**
  - I_{REF} <2 mA
- **Low idle current**
  - ~50 mA I_{CQ}
- **High-speed power-up/down**
  - Turn on/off time (10%~90%) <100 ns
  - Typical power-up/down delay with driver delay included <200 ns
- **High temperature stability**
  - ~1 dB gain/power variation between 0°C to +80°C
  - ~1 dB detector variation over 0°C to +80°C
- **Low shut-down current (< 0.1 µA)**
- **On-chip power detection**
- **25 dB dynamic range on-chip power detection**
- **Simple input/output matching**
- **Packages available**
  - 16-contact VQFN (3mm x 3mm)
  - Non-Pb (lead-free) packages available

Applications

- **WLAN (IEEE 802.11g/b)**
- **Home RF**
- **Cordless phones**
- **2.4 GHz ISM wireless equipment**

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Product Description

The SST12LP15 is a high-power, high-gain power amplifier based on the highly-reliable InGaP/GaAs HBT technology.

The SST12LP15 can be easily configured for high-power, high-efficiency applications with superb power-added efficiency while operating over the 2.4~2.5 GHz frequency band. It typically provides 35 dB gain with 26% power-added efficiency @ P_{OUT} = 24 dBm for 802.11g and 29% power-added efficiency @ P_{OUT} = 25 dBm for 802.11b.

The SST12LP15 has excellent linearity, typically ~4% added EVM at 23.5 dBm output power which is essential for 54 Mbps 802.11g operation while meeting 802.11g spectrum mask at 24+ dBm. SST12LP15 also has wide-range (>25 dB), temperature-stable (~1 dB over 80°C), single-ended/differential power detectors which lower users' cost on power control.

The power amplifier IC also features easy board-level usage along with high-speed power-up/down control. Ultra-low reference current (total I_{REF} <2 mA) makes the SST12LP15 controllable by an on/off switching signal directly from the baseband chip. These features coupled with low operating current make the SST12LP15 ideal for the final stage power amplification in battery-powered 802.11g/b WLAN transmitter applications.

The SST12LP15 is offered in 16-contact VQFN package. See Figure 2 for pin assignments and Table 1 for pin descriptions.

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Functional Blocks

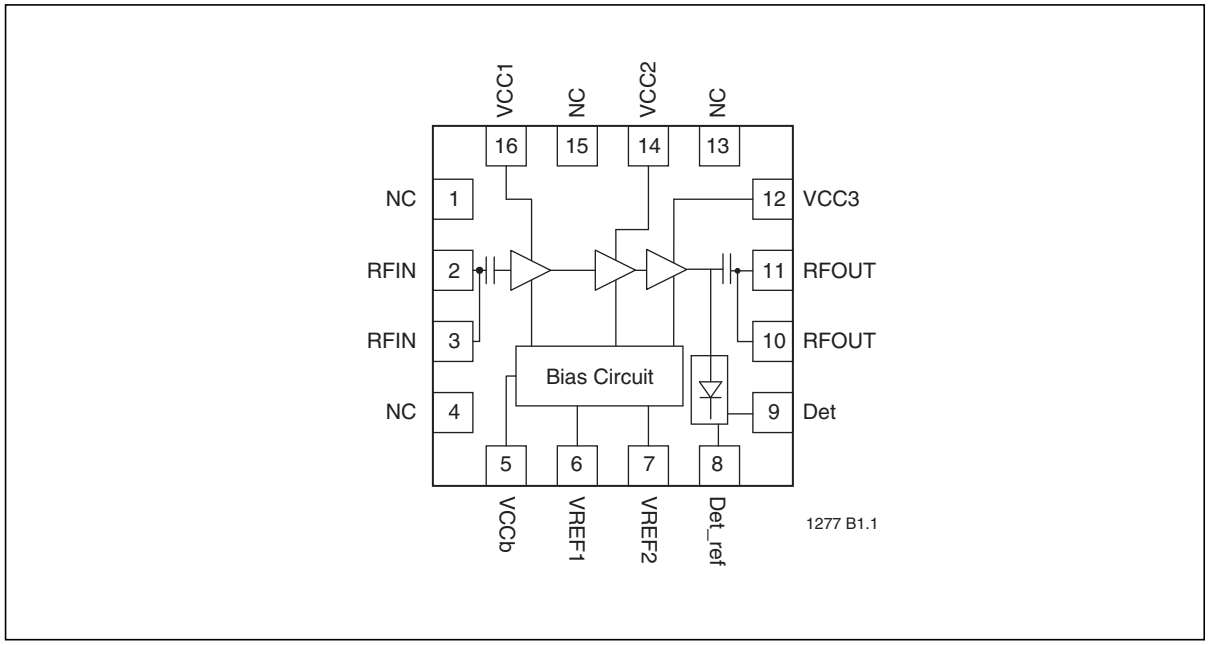

Figure 1: Functional Block Diagram

Pin Assignments

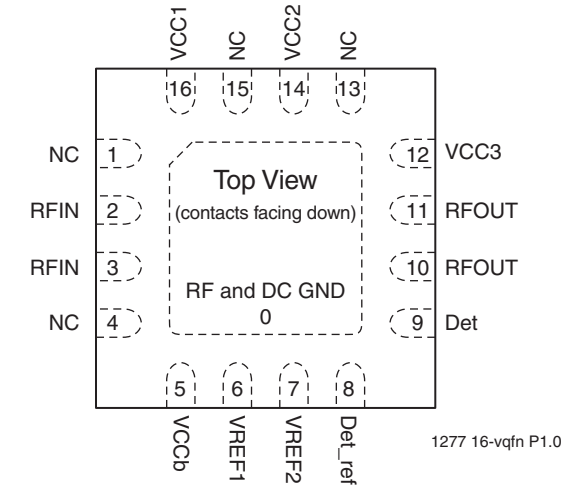

Figure 2: Pin Assignments for 16-contact VQFN

Pin Descriptions

Table 1: Pin Description

Symbol	Pin No.	Pin Name	Type[1]	Function
GND	0	Ground		The center pad should be connected to RF ground with several low inductance, low resistance vias.
NC	1	No Connection		Unconnected pins.
RFIN	2		I	RF input, DC decoupled
RFIN	3		I	RF input, DC decoupled
NC	4	No Connection		Unconnected pins.
VCCb	5	Power Supply	PWR	Supply voltage for bias circuit
VREF1	6		PWR	1st and 2nd stage idle current control
VREF2	7		PWR	3rd stage idle current control
Det_ref	8		O	On-chip power detector reference
Det	9		O	On-chip power detector
RFOUT	10		O	RF output
RFOUT	11		O	RF output
VCC3	12	Power Supply	PWR	Power supply, 3rd stage
NC	13	No Connection		Unconnected pins.
VCC2	14	Power Supply	PWR	Power supply, 2nd stage
NC	15	No Connection		Unconnected pins.
VCC1	16	Power Supply	PWR	Power supply, 1st stage

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1. I=Input, O=Output

Electrical Specifications

The AC and DC specifications for the power amplifier interface signals. Refer to Table 3 for the DC voltage and current specifications. Refer to Figures 3 through 11 for the RF performance.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Input power to pins 2 and 3 (P_{IN}) . . . . . +5 dBm
Average output power (P_{OUT}) . . . . . +28 dBm
Supply Voltage at pins 5, 12, 14, 16 (V_{CC}) . . . . . -0.3V to +4.6V
Reference voltage to pins 6 (V_{REF1}) and pin 7 (V_{REF2}) . . . . . -0.3V to +3.6V
DC supply current (I_{CC}) . . . . . 500 mA
Operating Temperature (T_A) . . . . . -40°C to +85°C
Storage Temperature (T_{STG}) . . . . . -40°C to +120°C
Maximum Junction Temperature (T_J) . . . . . +150°C
Surface Mount Solder Reflow Temperature: . . . . . "with-Pb" units[1]: 240°C for 3 seconds
. . . . . "non-Pb" units: 260°C for 3 seconds

1. Certain "with-Pb" package types are capable of 260°C for 3 seconds; please consult the factory for the latest information.

Table 2: Operating Range

Range	Ambient Temp	V_{DD}
Industrial	-40°C to +85°C	3.3V

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Table 3: DC Electrical Characteristics

Symbol	Parameter	Min.	Typ	Max.	Unit	Test Conditions
V_{CC}	Supply Voltage at pins 5, 12, 14, 16	3.0	3.3	4.2	V	
I_{CC}	Supply Current for 802.11g, 24 dBm			290	mA	
	for 802.11g, 25 dBm			340	mA	
I_{CQ}	Idle current for 802.11g to meet EVM<4% @ 23dBm		50		mA	
I_{OFF}	Shut down current			0.1	µA	
V_{REG1}	Reference Voltage for 1st Stage, with 110Ω resistor	2.75	2.8	2.85	V	
V_{REG2}	Reference Voltage for 2nd Stage, with 270Ω resistor	2.75	2.8	2.85	V	

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Table 4: AC Electrical Characteristics for Configuration

Symbol	Parameter	Min.	Typ	Max.	Unit
F_{L-U}	Frequency range	2400		2485	MHz
P_{OUT}	Output power @ PIN = -10 dBm 11b signals	25			dBm
	@ PIN = -11 dBm 11g signals		24		dBm
G	Small signal gain	35	36		dB
G_{VAR1}	Gain variation over band (2400~2485 MHz)			±0.5	dB
G_{VAR2}	Gain ripple over channel (20 MHz)		0.2		dB
Stability	Spurious output@ 25.5 dBm 54 Mbps OFDM signal when VSWR=6:1 all angle			-60	dBc
Output VSWR Rugged-ness	Survivable time@ 25.5 dBm (to 50Ω) 54 Mbps OFDM signal when VSWR=10:1 all angle	10			second
ACPR	Meet 11b spectrum mask	24	25		dBm
	Meet 11g OFDM 54 MBPS spectrum mask	24			dBm
Added EVM	@ 23.5 dBm output with 11g OFDM 54 MBPS signal		4		%
2f, 3f, 4f, 5f	Harmonics at 22 dBm, without trapping capacitors			-40	dBc

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Typical Performance Characteristics

Test Conditions: V_{CC} = 3.3V, T_A = 25°C

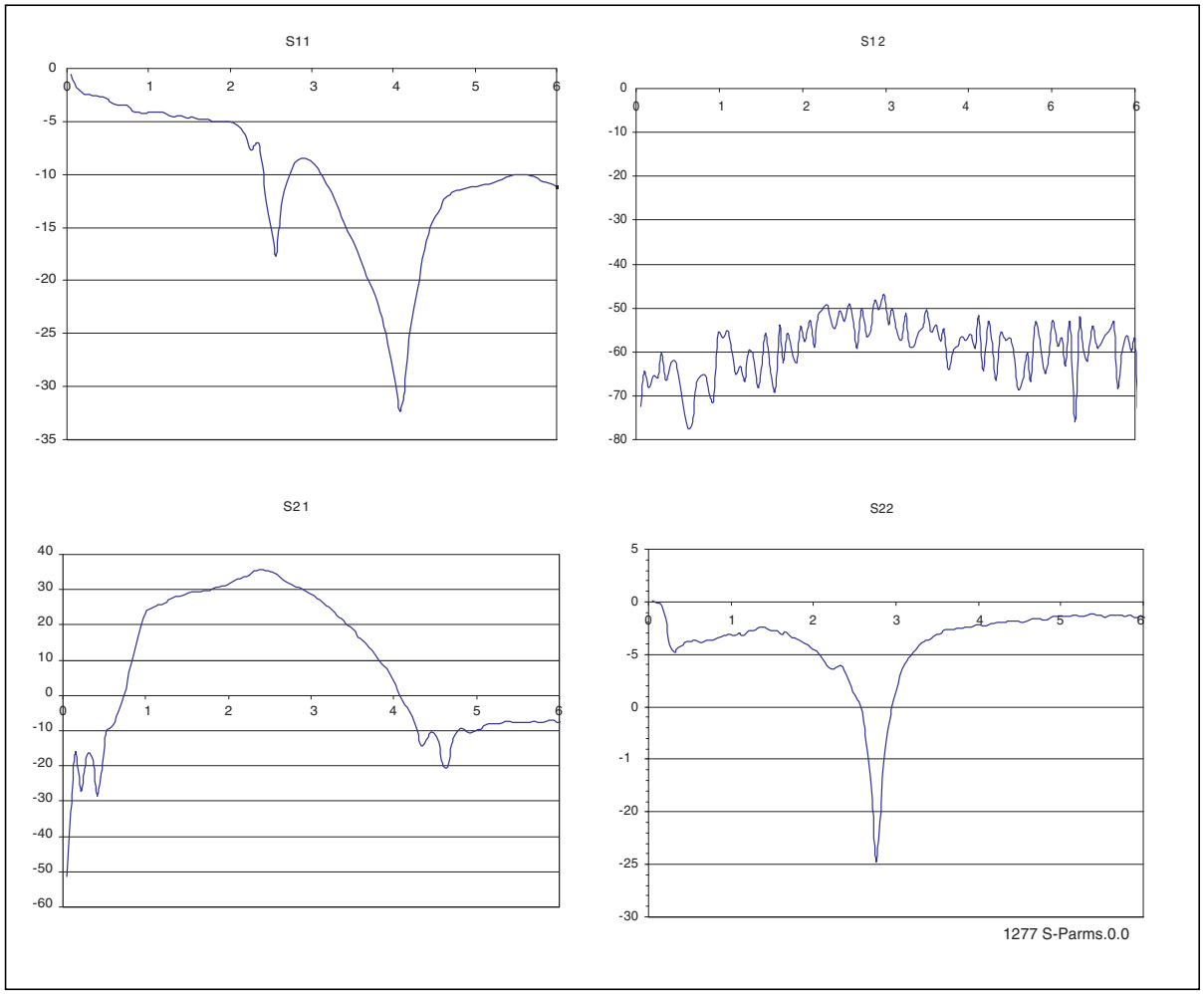

Figure 3: S-Parameters

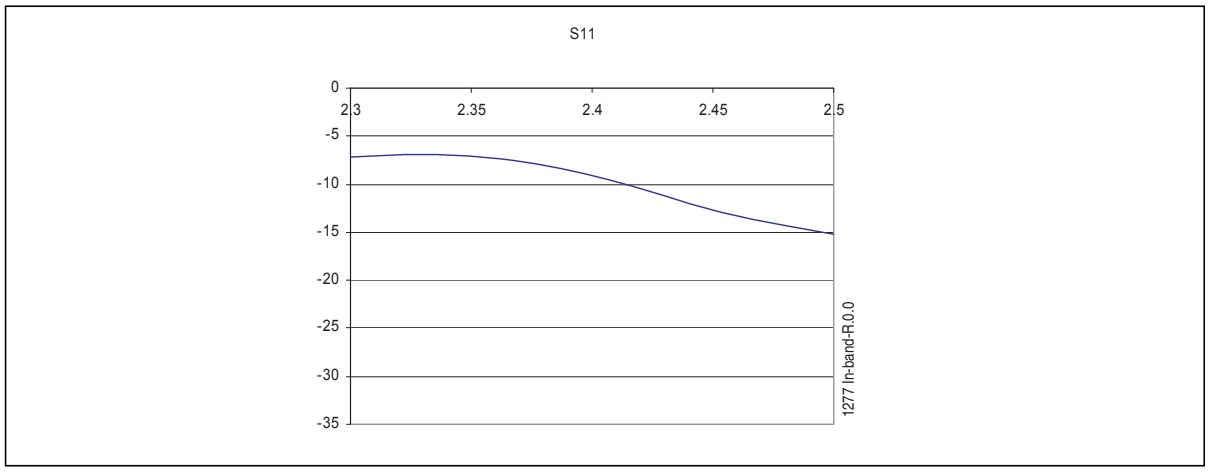

Figure 4: In-band Return Loss

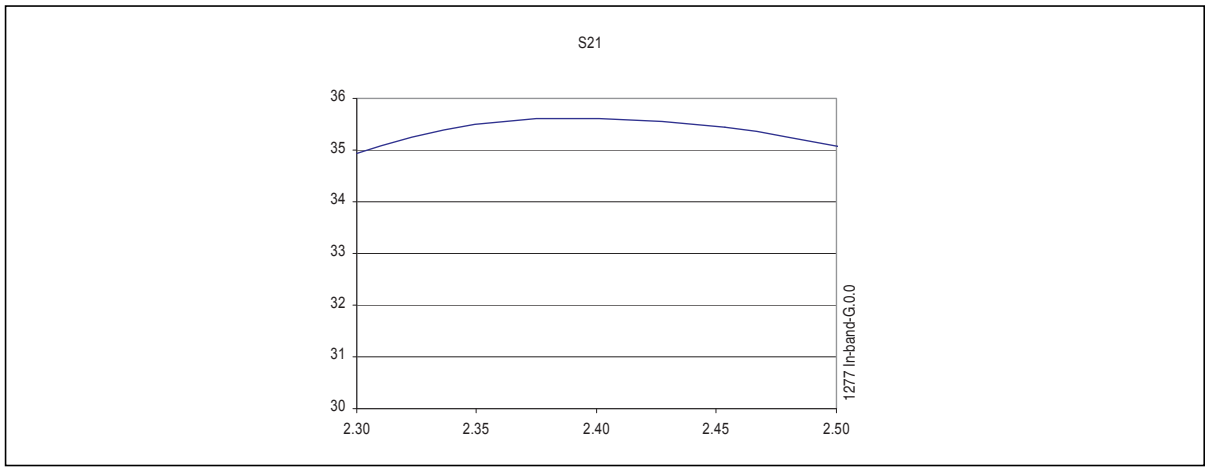

Figure 5: In-band Gain Flatness

Typical Performance Characteristics

Test Conditions: F1 = 2.45 GHz, F2 = 2.451 GHz

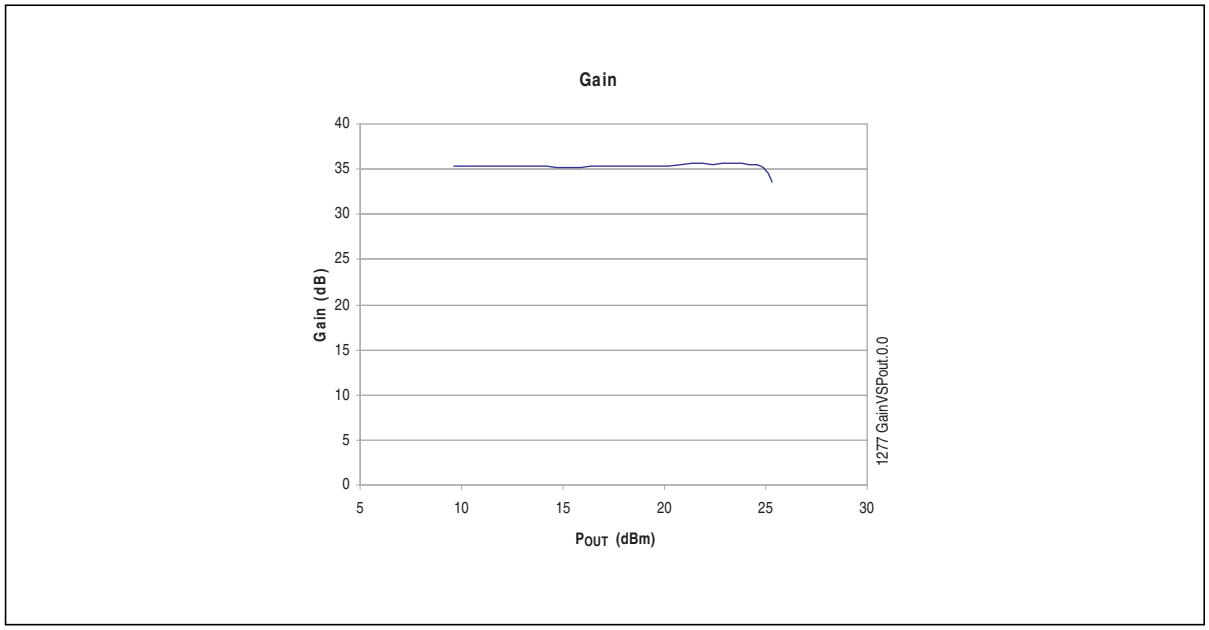

Figure 6: Gain vs. P_{OUT}

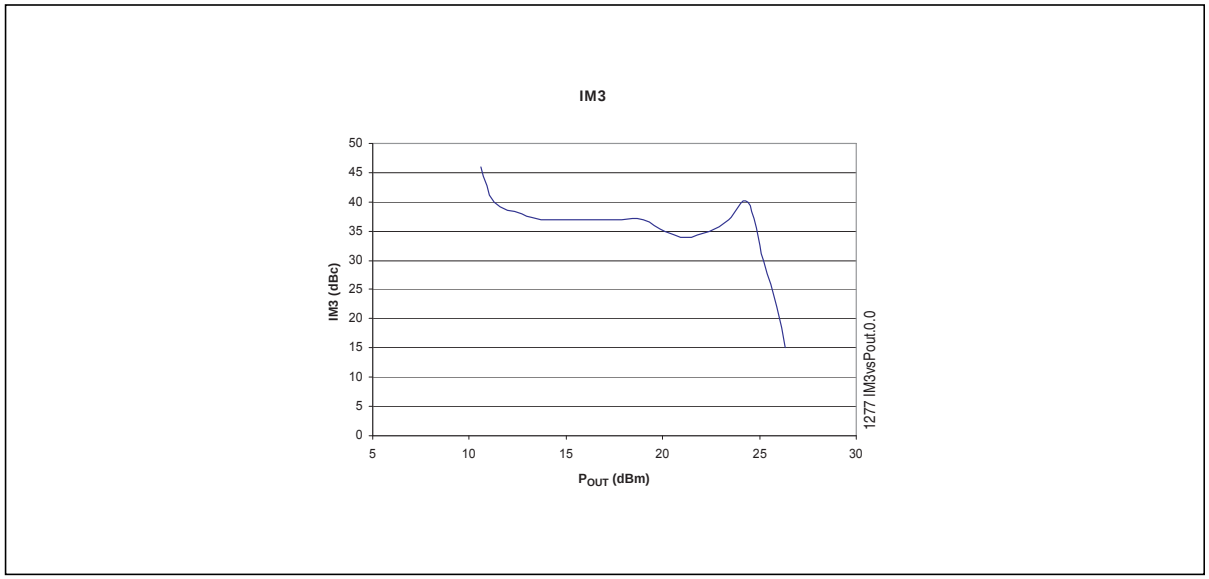

Figure 7: IM3 vs. P_{OUT}

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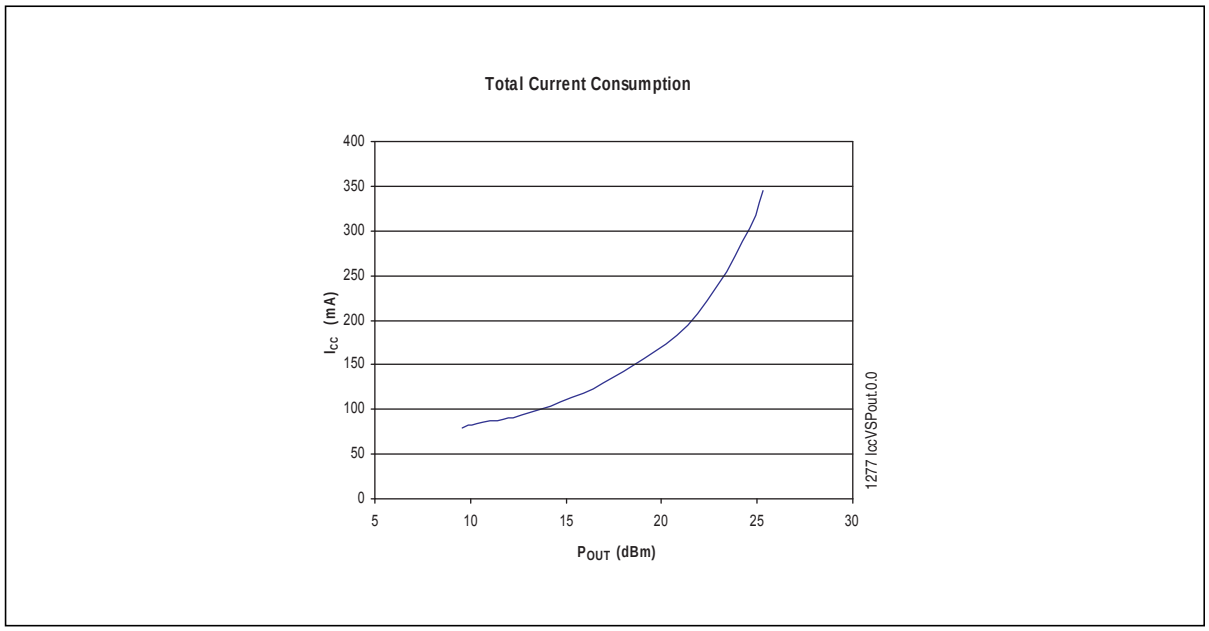


Figure 8: I_{CC} vs. P_{OUT}

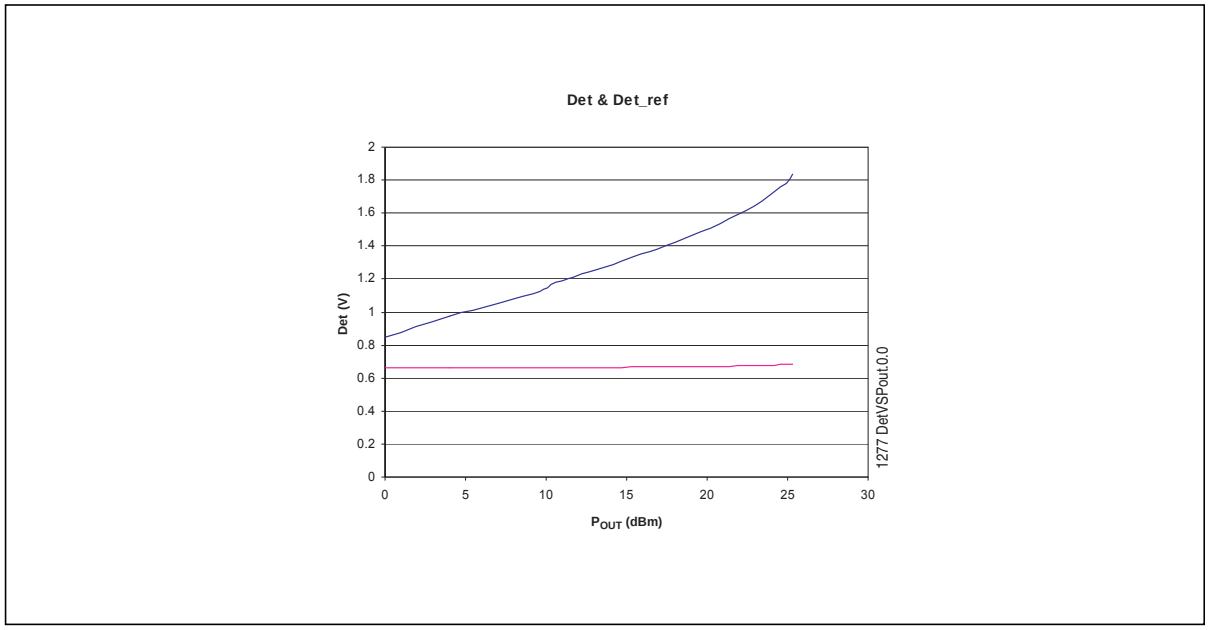


Figure 9: Detectors vs. P_{OUT}

Typical Performance Characteristics

Test Conditions: V_{CC} = 3.3V, T_A = 25°C, F = 2.45 GHz, 54 Mbps 802.11g OFDM signal

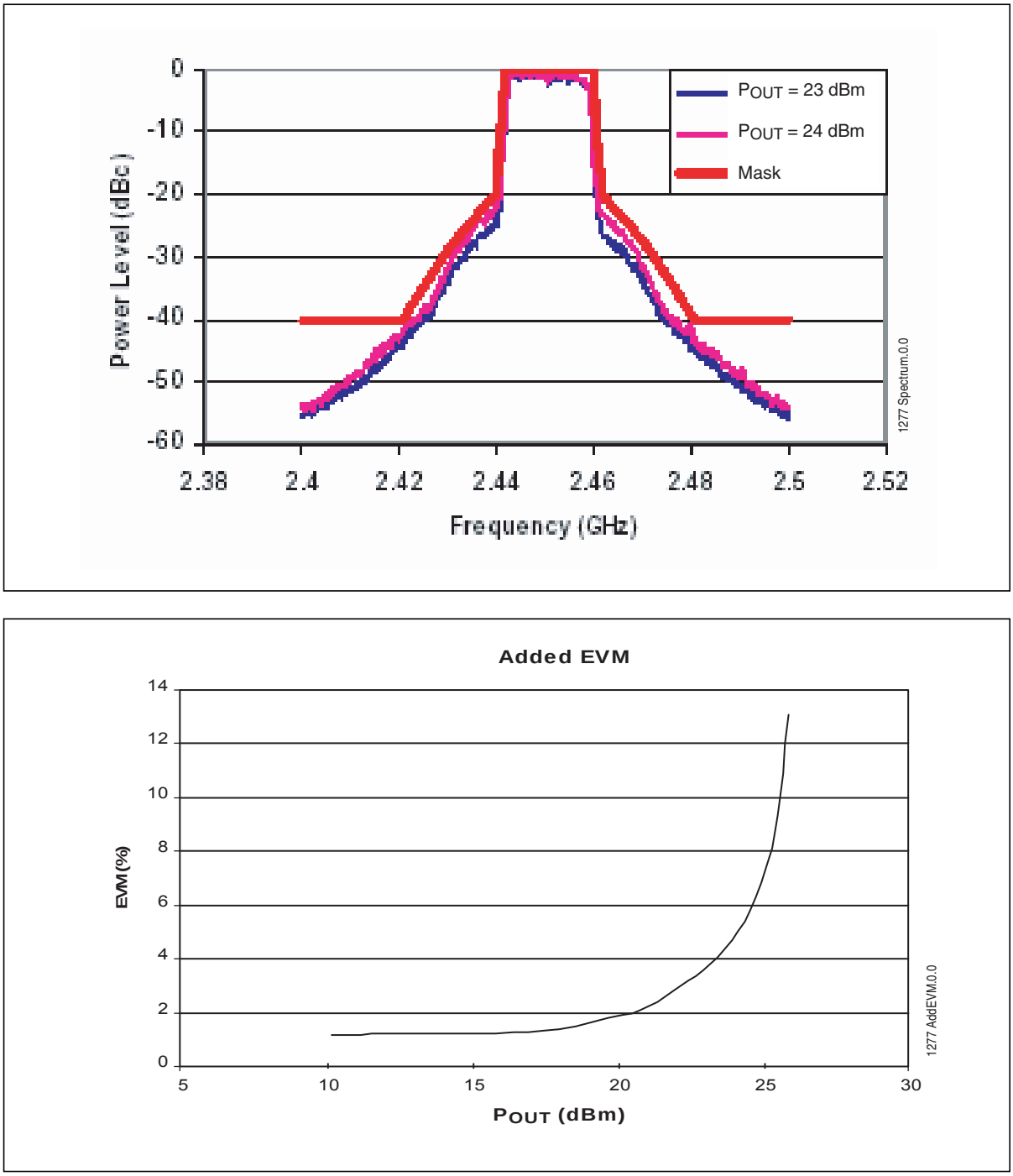


Figure 10:802.11g Spectrum at 23/24 dBm, DC current 240/290 mA

Typical Performance Characteristics

Test Conditions: V_{CC} = 3.3V, T_A=25°C, 1 Mbps 802.11B CCK signal

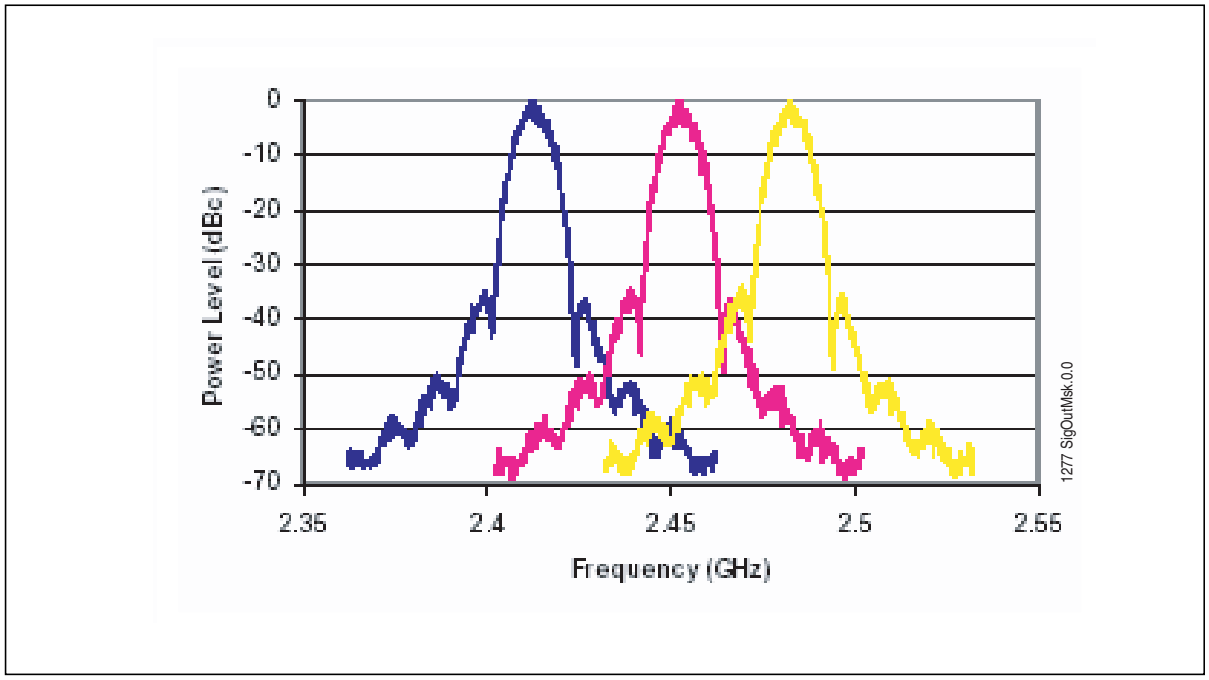


Figure 11:802.11B Signal Output Mask at 25 dBm, DC current 340 mA

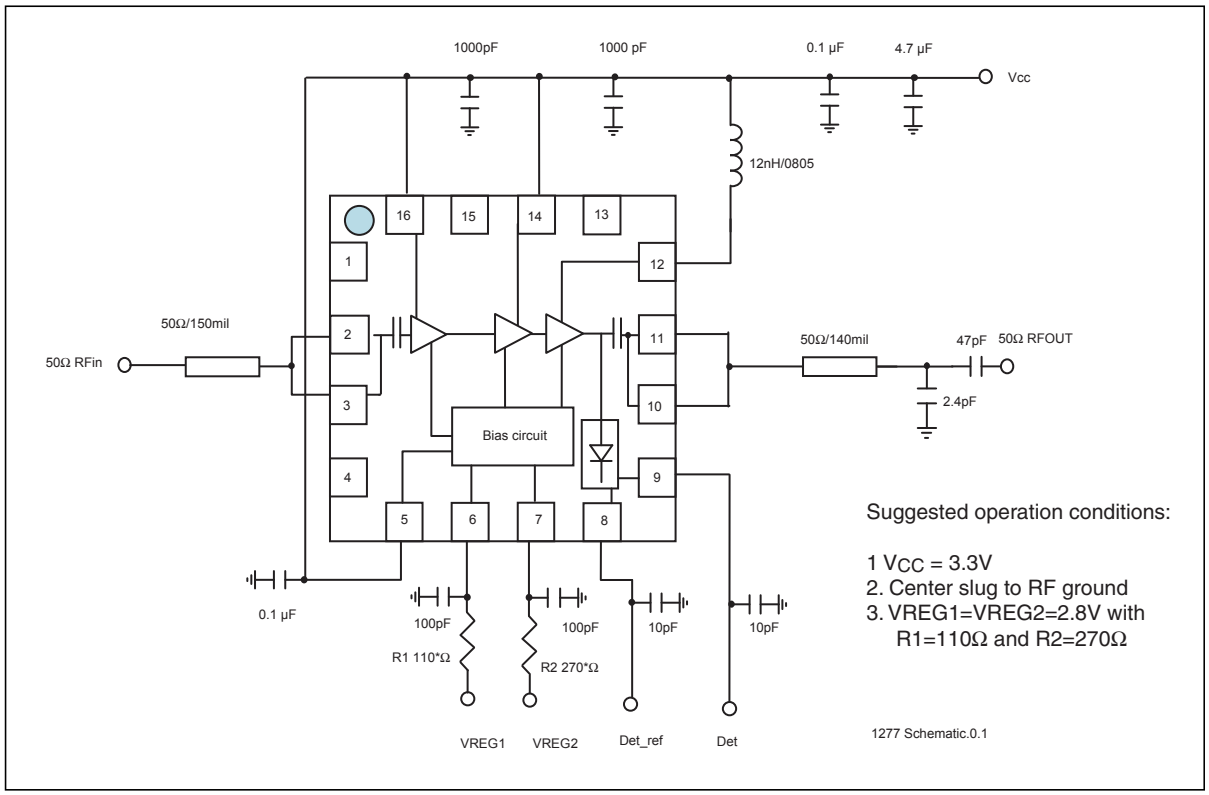
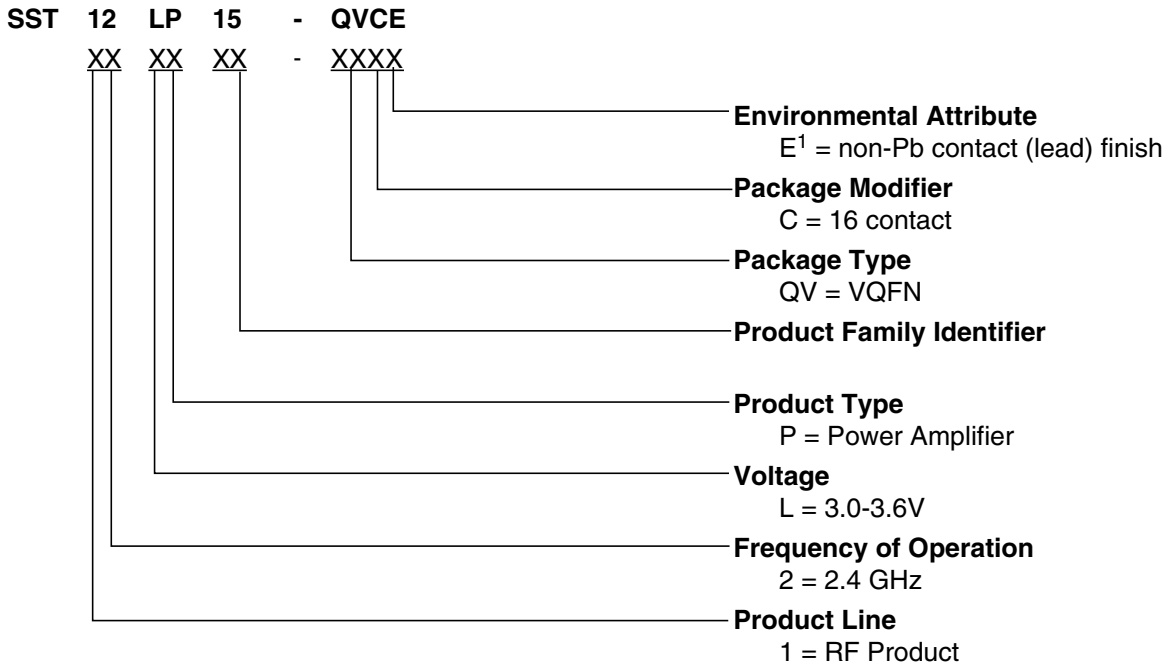


Figure 12: Typical Schematic for High-Power, High-Efficiency 802.11b/g Applications

Not Recommended for New Designs

Product Ordering Information



1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST12LP15

SST12LP15-QVC	SST12LP15-QVCE

SST12LP15 Evaluation Kits

SST12LP15-QVC-K	SST12LP15-QVCE-K

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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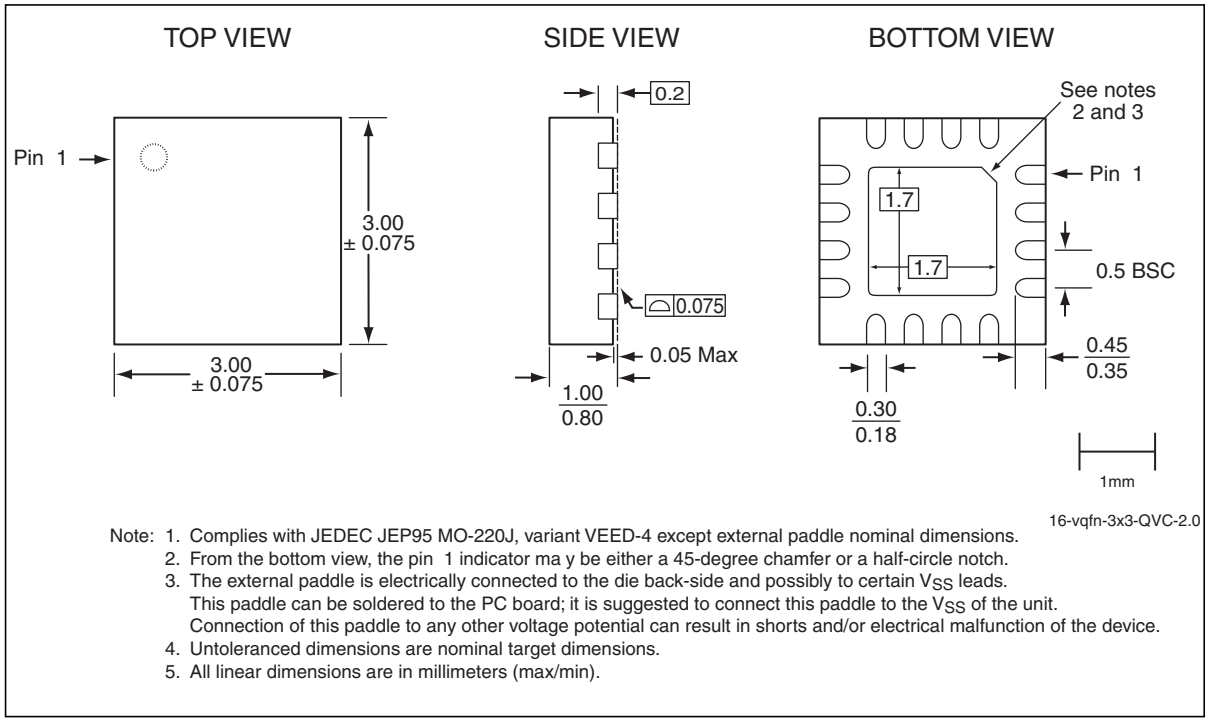
Packaging Diagrams



Note: 1. Complies with JEDEC JEP95 MO-220J, variant VEED-4 except external paddle nominal dimensions.
2. From the bottom view, the pin 1 indicator ma y be either a 45-degree chamfer or a half-circle notch.
3. The external paddle is electrically connected to the die back-side and possibly to certain V_{SS} leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the V_{SS} of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

Figure 13: 16-Contact Very-thin Quad Flat No-lead (VQFN)
SST Package Code: QVC

Table 5: Revision History

Revision	Description	Date
00	• S71277: SST conversion of data sheet GP1215	Jan 2005
01	• Updated document status from Preliminary Specification to Data Sheet	Apr 2008
02	• Updated “Contact Information” on page 12.	Feb 2009
A	• Applied new document format • Released document under letter revision system • Updated Spec number from S71277 to DS75030	Oct 2011

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Memory sizes denote raw storage capacity; actual usable capacity may be less.

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