2 W Filterless Class-D Stereo Audio Amplifier

SSM2304

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FEATURES

Filterless Class-D amplifier with built-in output stage
2 W into 4 Ω and 1.4 W into 8 Ω at 5.0 V supply with <10% THD
85% efficiency at 5.0 V, 1.4 W into 8 Ω speaker
Better than 98 dB SNR (signal-to-noise ratio)
Available in 16-lead, 3 mm × 3 mm LFCSP
Single-supply operation from 2.5 V to 5.0 V
20 nA ultralow shutdown current
Short-circuit and thermal protection
Pop-and-click suppression
Built-in resistors reduce board component count
Default fixed 18 dB gain and user-adjustable

APPLICATIONS

Notebooks and PCs
Mobile phones
MP3 players
Portable gaming
Portable electronics
Educational toys

GENERAL DESCRIPTION

The SSM2304 is a fully integrated, high efficiency, Class-D stereo audio amplifier. It is designed to maximize performance for portable applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.0 V supply. It is capable of delivering 2 W of continuous output power with less than 10% THD + N driving a 4 Ω load from a 5.0 V supply.

The SSM2304 features a high efficiency, low noise modulation scheme. It operates with 85% efficiency at 1.4 W into 8 Ω from a 5.0 V supply and has a signal-to-noise ratio (SNR) that is better than 98 dB. PDM modulation is used to provide lower EMI-radiated emissions compared with other Class-D architectures.

The SSM2304 has a micropower shutdown mode with a typical shutdown current of 20 nA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin.

The architecture of the device allows it to achieve a very low level of pop and click. This minimizes voltage glitches at the output during turn-on and turn-off, thus reducing audible noise on activation and deactivation.

The fully differential input of the SSM2304 provides excellent rejection of common-mode noise on the input. Input coupling capacitors can be omitted if the dc input common-mode voltage is approximately $V_{DD}/2$.

The SSM2304 also has excellent rejection of power supply noise, including noise caused by GSM transmission bursts and RF rectification.

The SSM2304 has a preset gain of 18 dB, which can be reduced by using external resistors.

The SSM2304 is specified over the commercial temperature range (−40°C to +85°C). It has built-in thermal shutdown and output short-circuit protection. It is available in a 16-lead, 3 mm × 3 mm lead-frame chip scale package (LFCSP).

FUNCTIONAL BLOCK DIAGRAM

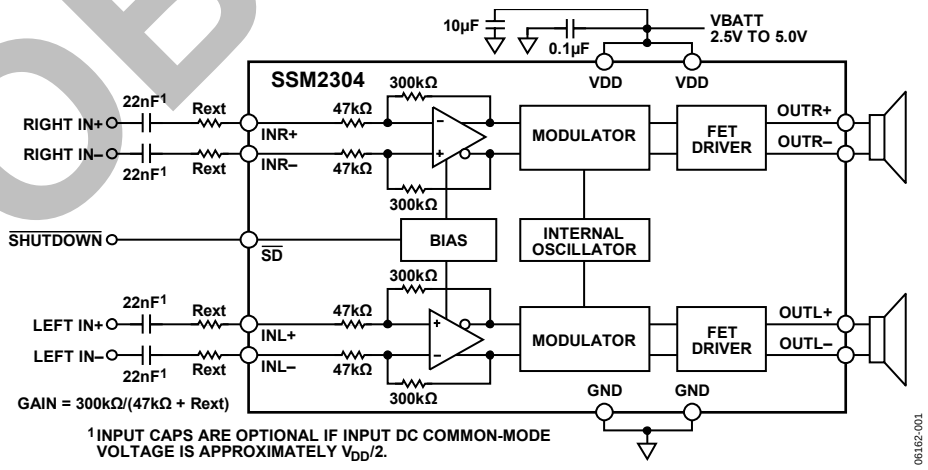


Figure 1.

Rev. 0

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Absolute Maximum Ratings ... 4
Thermal Resistance ... 4
ESD Caution ... 4
Pin Configuration and Function Descriptions ... 5
Typical Performance Characteristics ... 6
Typical Application Circuits ... 12
Application Notes ... 13
Overview ... 13
Gain Selection ... 13
Pop-and-Click Suppression ... 13
EMI Noise ... 13
Layout ... 14
Input Capacitor Selection ... 14
Proper Power Supply Decoupling ... 14
Evaluation Board Information ... 15
Introduction ... 15
Board Description ... 15
Getting Started ... 18
What to Test ... 18
PCB Layout Guidelines ... 19
Outline Dimensions ... 20
Ordering Guide ... 20

REVISION HISTORY

12/06—Revision 0: Initial Version

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SPECIFICATIONS

V_{DD} = 5.0 V; T_A = 25°C; R_L = 4 Ω, 8 Ω; gain = 18 dB; unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.8		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.4		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.9		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.615		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.35		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.275		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		2.4		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.53		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.1		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.77		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.45		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.35		W
Efficiency	η	P_{OUT} = 2 W, 4 Ω, V_{DD} = 5.0 V		75		%
		P_{OUT} = 1.4 W, 8 Ω, V_{DD} = 5.0 V		85		%
Total Harmonic Distortion + Noise	THD + N	P_O = 2 W into 4 Ω each channel, f = 1 kHz, V_{DD} = 5.0 V		0.2		%
		P_O = 1 W into 8 Ω each channel, f = 1 kHz, V_{DD} = 3.6 V		0.25		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} − 1	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz		60		dB
Channel Separation	X_{TALK}	P_O = 100 mW, f = 1 kHz		78		dB
Average Switching Frequency	f_{SW}			1.8		MHz
Differential Output Offset Voltage	V_{OOS}			2.0		mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.0	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V,	70	85		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV rms at 217 Hz, inputs ac GND, C_{IN} = 0.01 µF, input referred		68		dB
Supply Current	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		7.0		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		6.5		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		5.2		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN						
Closed-Loop Gain	Av	Rext = 0		18		dB
Differential Input Impedance	Z_{IN}	$\overline{SD}$ = VDD		47		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} ≥ 1 mA		1.2		V
Input Voltage Low	V_{IL}	I_{SY} ≤ 300 nA		0.5		V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		30		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, inputs are ac grounded, A_V = 6 dB, R_L = 4 Ω, A weighting		22		µV
Signal-to-Noise Ratio	SNR	P_{OUT} = 2.0 W, R_L = 4 Ω		102		dB

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ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-lead, 3 mm × 3 mm LFCSP	44	31.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

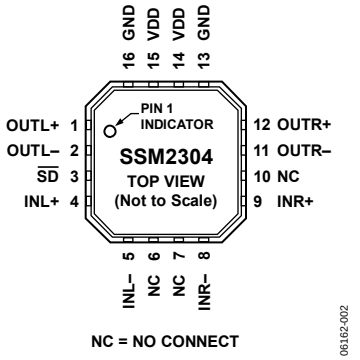


Figure 2. SSM2304 LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUTL+	Inverting Output for Left Channel.
2	OUTL–	Noninverting Output for Left Channel.
3	$\overline{SD}$	Shutdown Input. Active low digital input.
4	INL+	Noninverting Input for Left Channel.
5	INL–	Inverting Input for Left Channel.
6	NC	No Connect.
7	NC	No Connect.
8	INR–	Inverting Input for Right Channel.
9	INR+	Noninverting Input for Right Channel.
10	NC	No Connect
11	OUTR–	Noninverting Output for Right Channel.
12	OUTR+	Inverting Output for Right Channel.
13	GND	Ground for Output Amplifiers.
14	VDD	Power Supply for Output Amplifiers.
15	VDD	Power Supply for Output Amplifiers.
16	GND	Ground for Output Amplifiers.

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TYPICAL PERFORMANCE CHARACTERISTICS

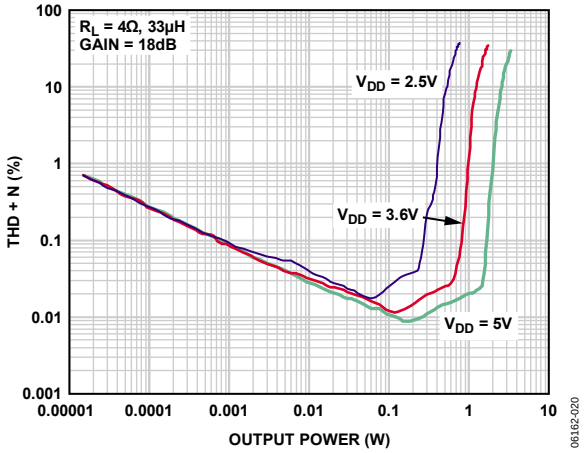


Figure 3. THD + N vs. Output Power into 4 Ω, A_V = 18 dB

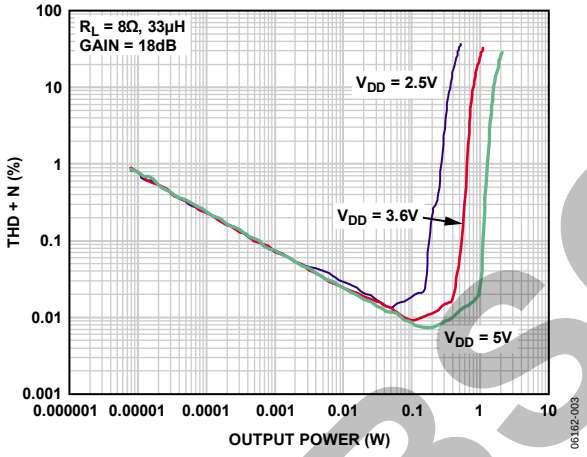


Figure 4. THD + N vs. Output Power into 8 Ω, A_V = 18 dB

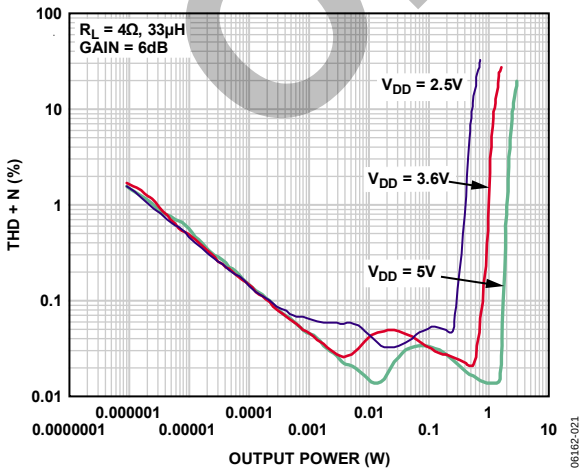


Figure 5. THD + N vs. Output Power into 4 Ω, A_V = 6 dB

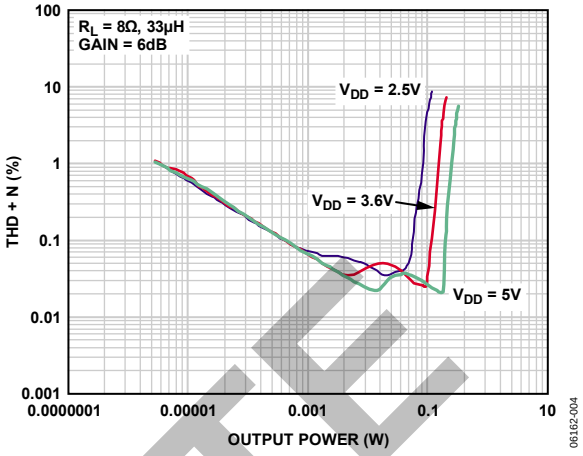


Figure 6. THD + N vs. Output Power into 8 Ω, A_V = 6 dB

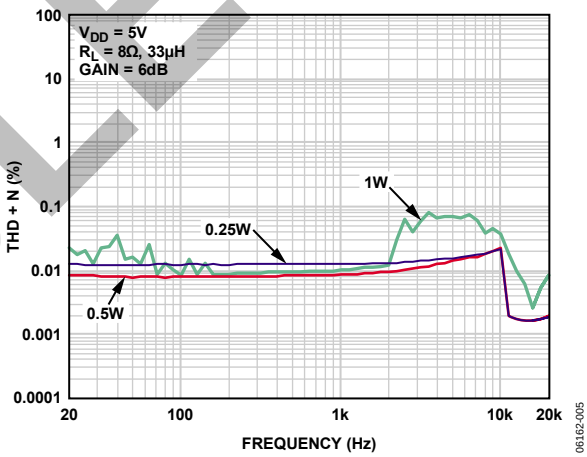


Figure 7. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω, A_V = 6 dB

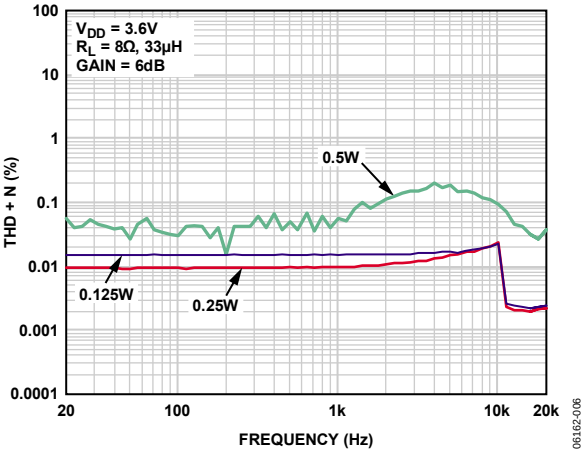


Figure 8. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω, A_V = 6 dB

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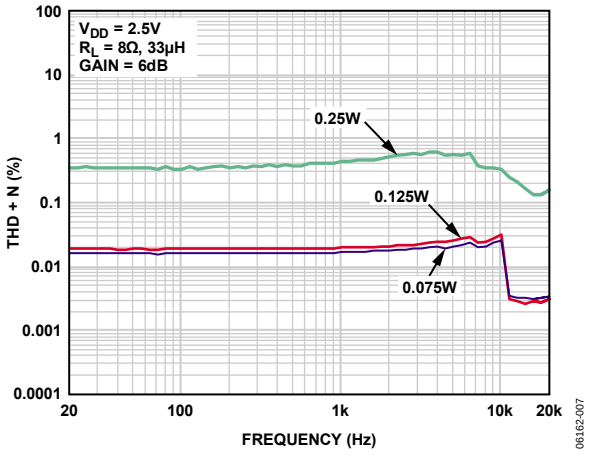


Figure 9. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω, A_V = 6 dB

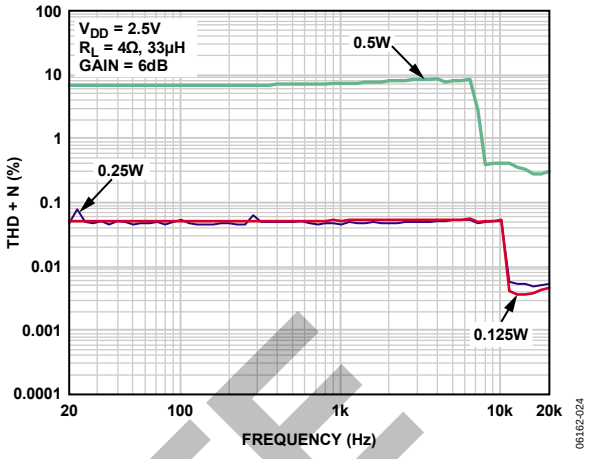


Figure 12. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω, A_V = 6 dB

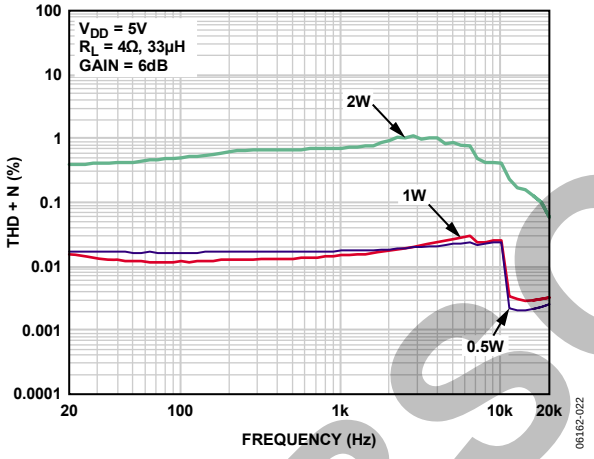


Figure 10. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω, A_V = 6 dB

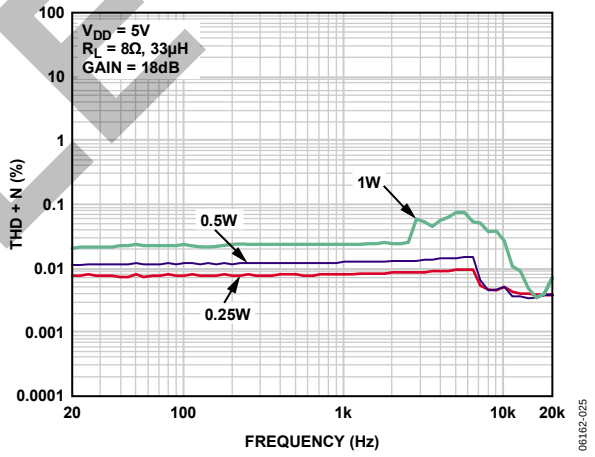


Figure 13. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω, A_V = 18 dB

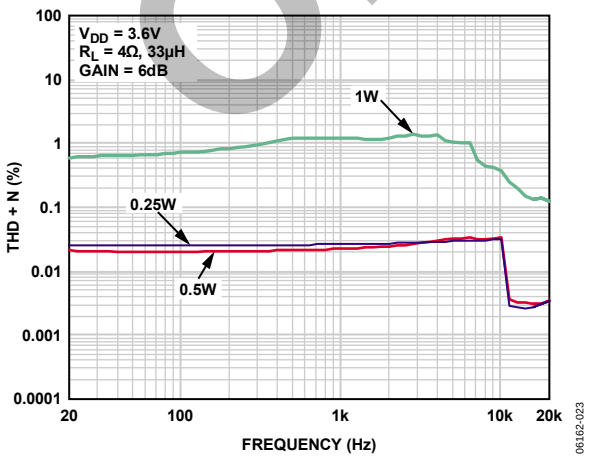


Figure 11. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω, A_V = 6 dB

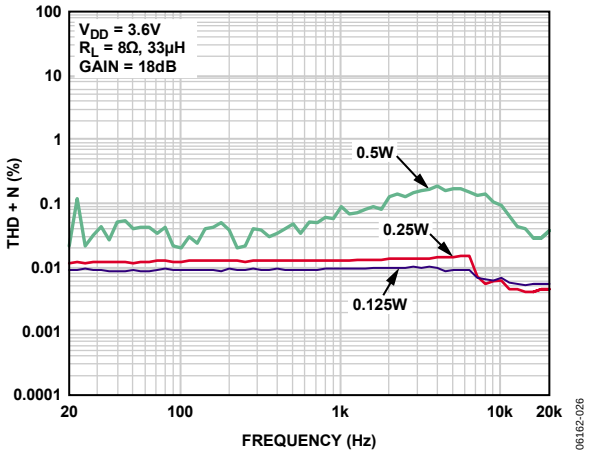


Figure 14. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω, A_V = 18 dB

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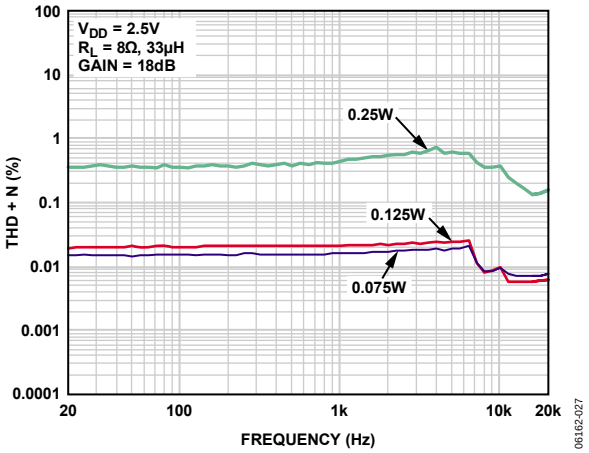


Figure 15. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω, A_V = 18 dB

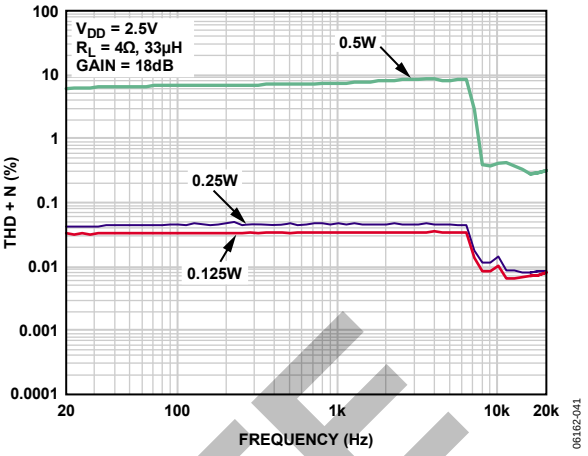


Figure 18. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω, A_V = 18 dB

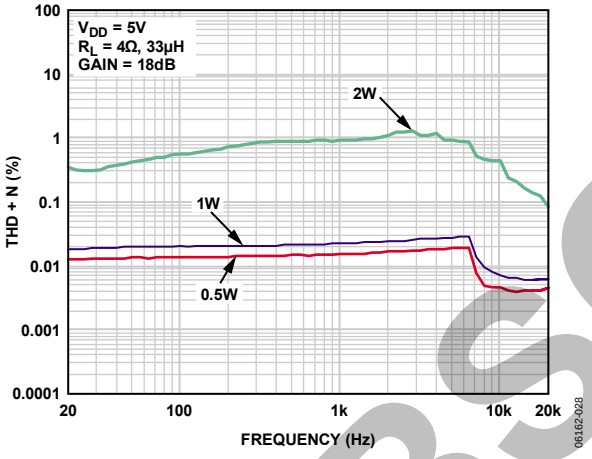


Figure 16. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω, A_V = 18 dB

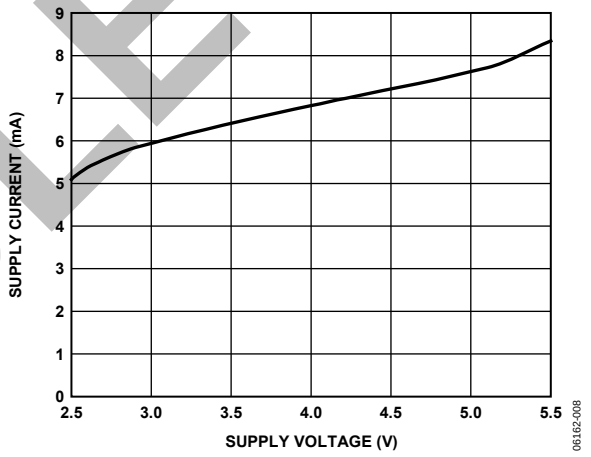


Figure 19. Supply Current vs. Supply Voltage, No Load

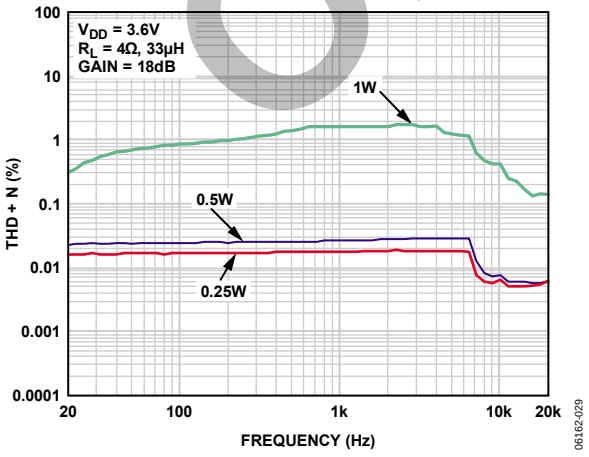


Figure 17. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω, A_V = 18 dB

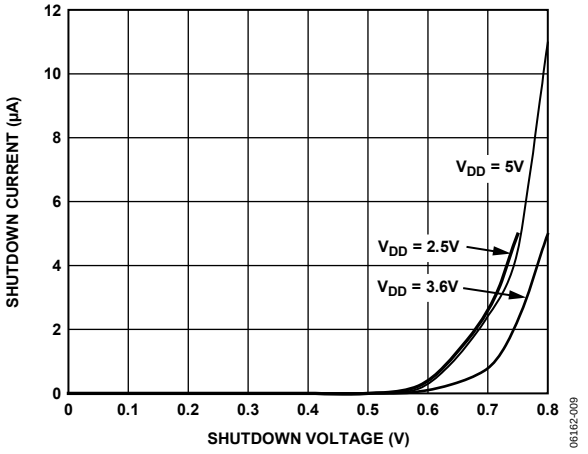


Figure 20. Supply Current vs. Shutdown Voltage

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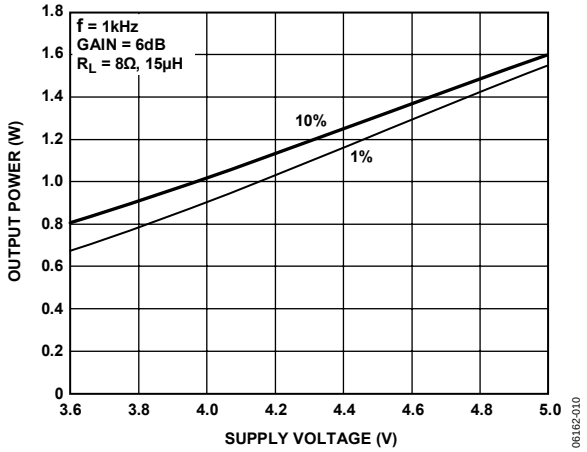


Figure 21. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, A_V = 6 dB

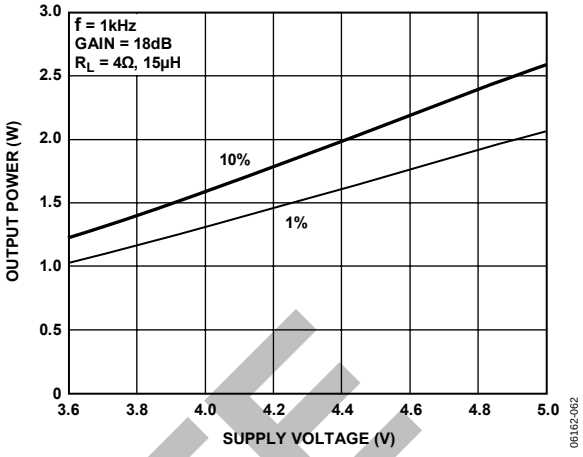


Figure 24. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, A_V = 18 dB

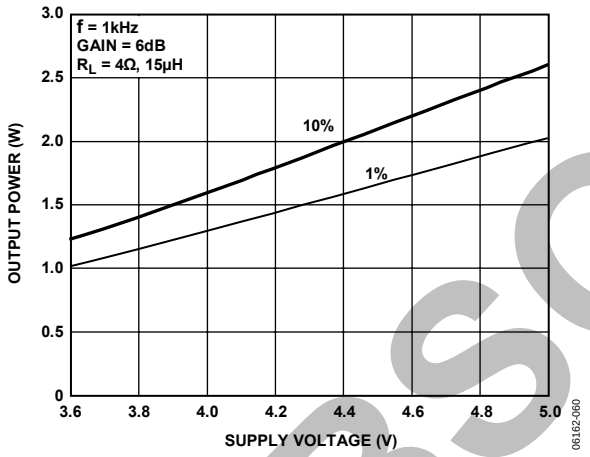


Figure 22. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, A_V = 6 dB

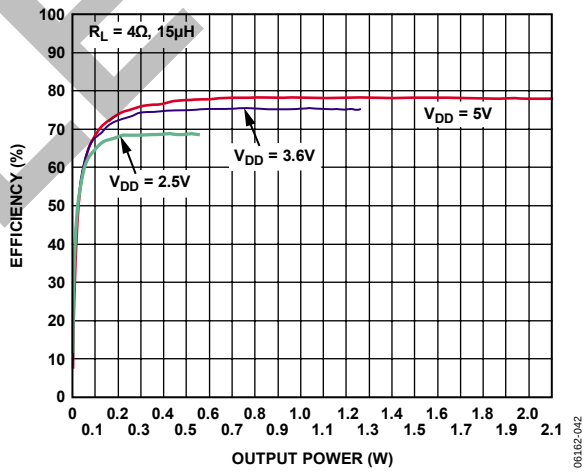


Figure 25. Efficiency vs. Output Power into 4 Ω

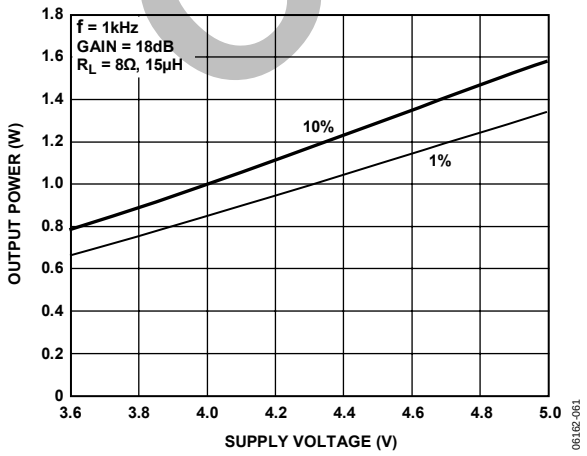


Figure 23. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, A_V = 18 dB

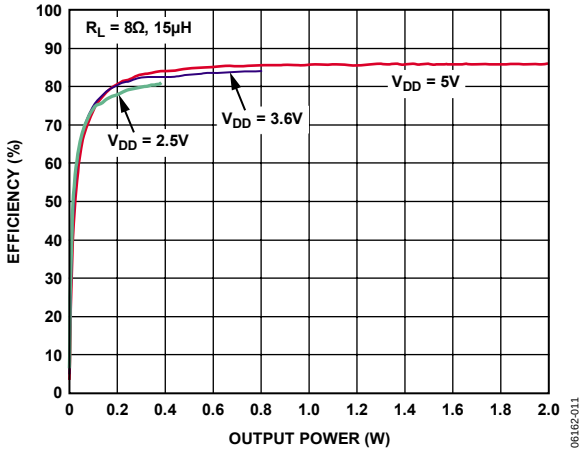


Figure 26. Efficiency vs. Output Power into 8 Ω

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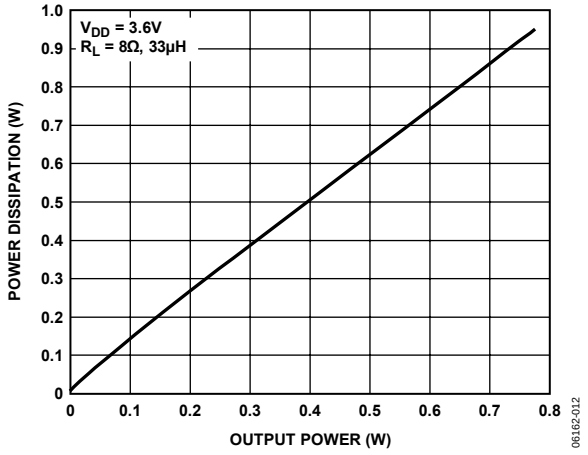


Figure 27. Power Dissipation vs. Output Power at V_{DD} = 3.6 V, R_L = 8 Ω

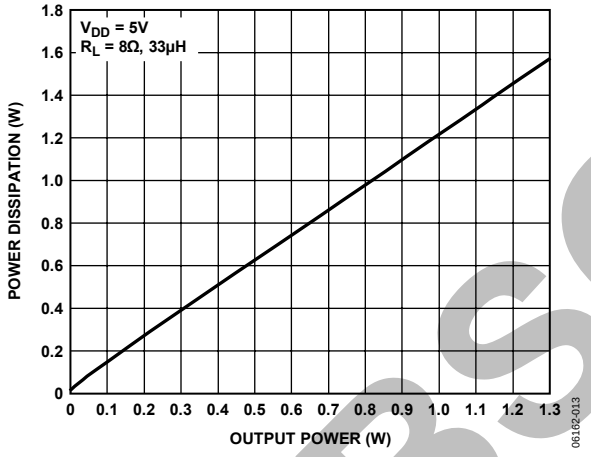


Figure 28. Power Dissipation vs. Output Power at V_{DD} = 5.0 V, R_L = 8 Ω

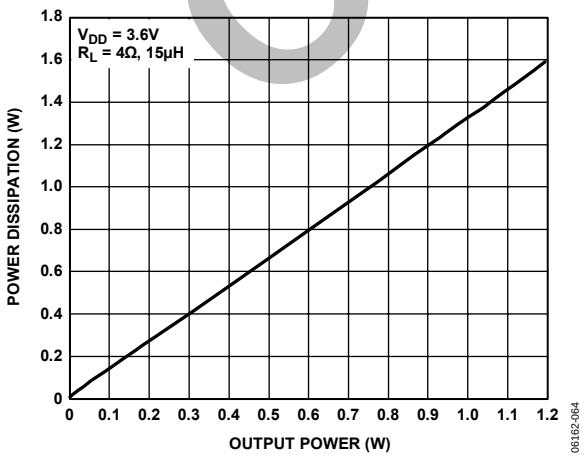


Figure 29. Power Dissipation vs. Output Power at V_{DD} = 3.6 V, R_L = 4 Ω

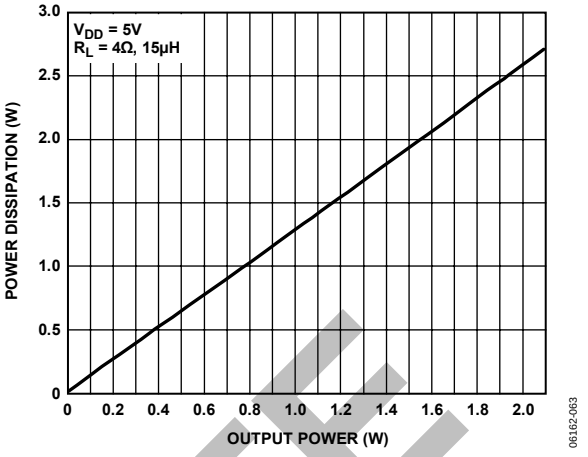


Figure 30. Power Dissipation vs. Output Power at V_{DD} = 5.0 V, R_L = 8 Ω

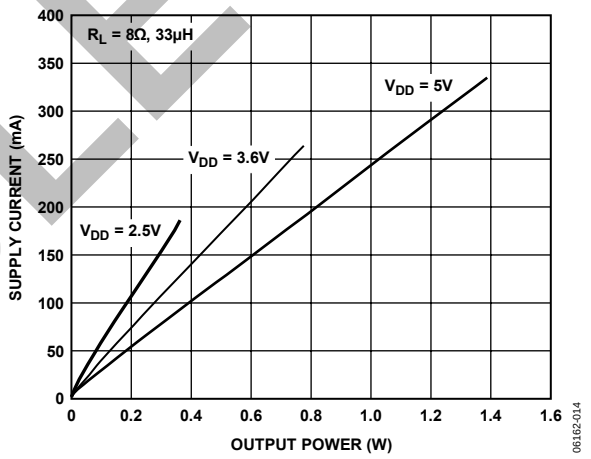


Figure 31. Output Power vs. Supply Current, One Channel

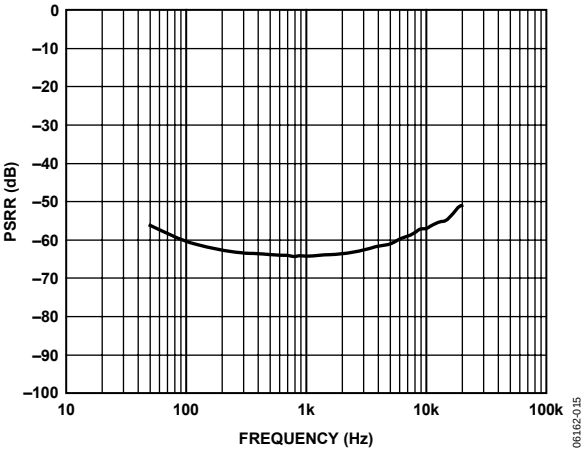


Figure 32. Power Supply Rejection Ratio vs. Frequency

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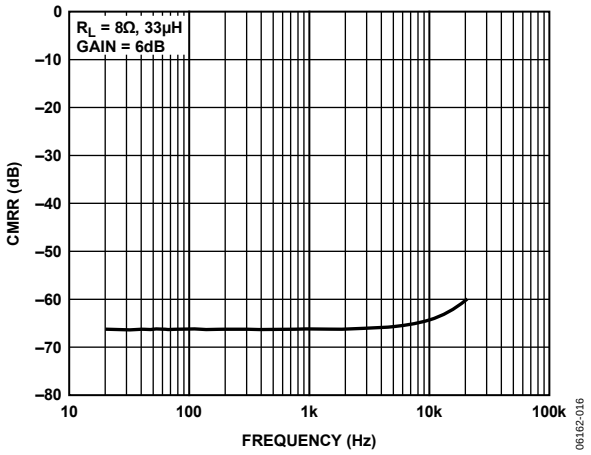


Figure 33. Common-Mode Rejection Ratio vs. Frequency

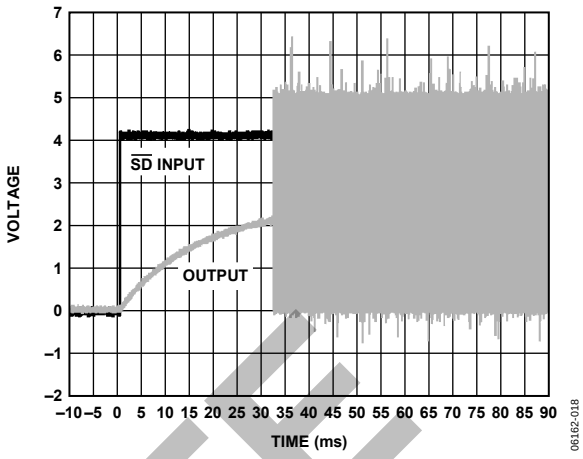


Figure 35. Turn-On Response

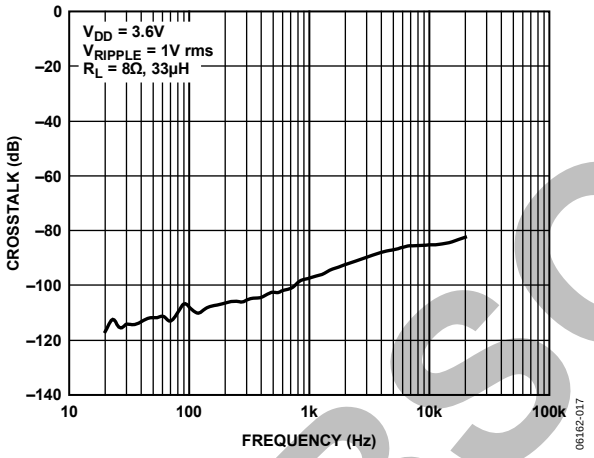


Figure 34. Crosstalk vs. Frequency

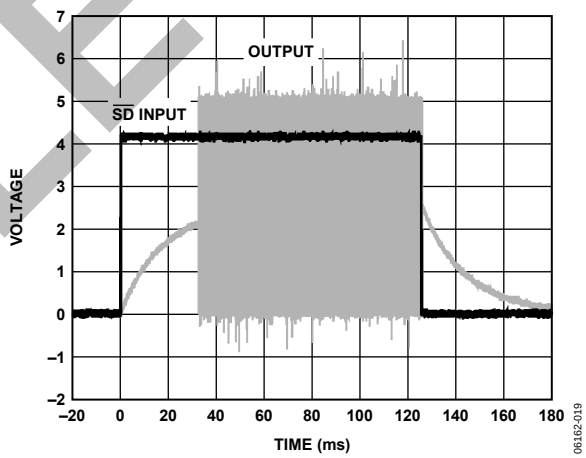


Figure 36. Turn-Off Response

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TYPICAL APPLICATION CIRCUITS

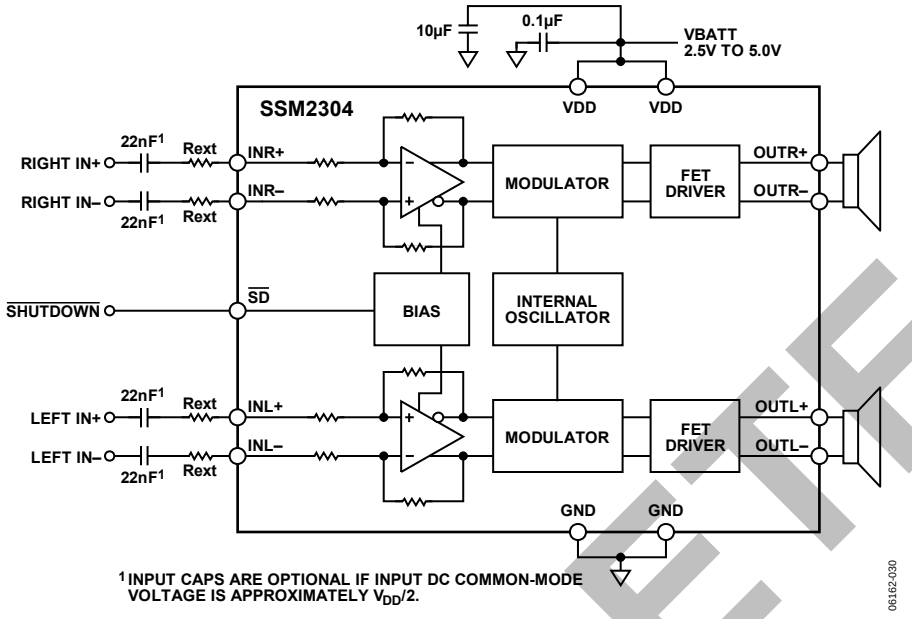


Figure 37. Stereo Differential Input Configuration

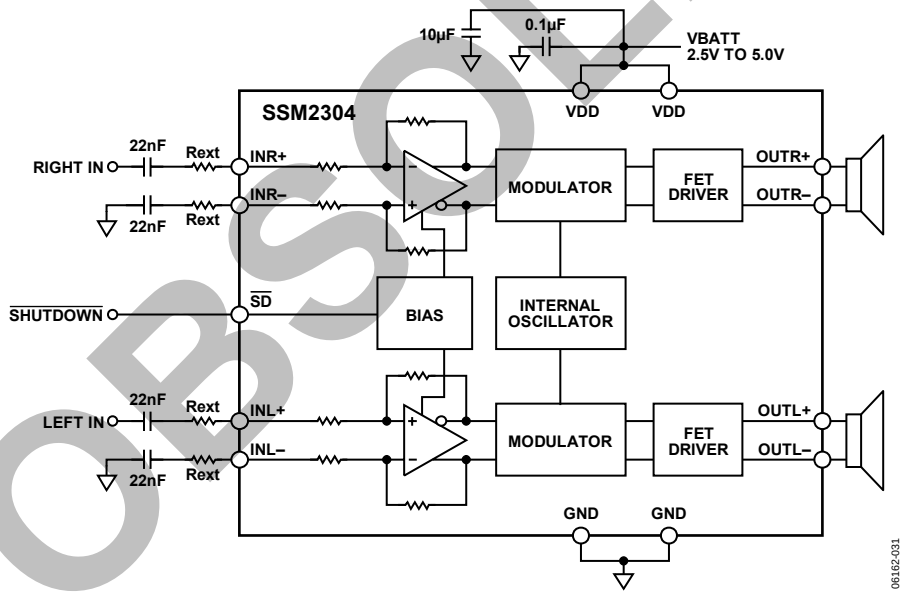


Figure 38. Stereo Single-Ended Input Configuration

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APPLICATION NOTES

OVERVIEW

The SSM2304 stereo Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external components count, conserving board space and thus reducing systems cost. The SSM2304 does not require an output filter, but instead relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square-wave output. While most Class-D amplifiers use some variation of pulse-width modulation (PWM), the SSM2304 uses a Σ-Δ modulation to determine the switching pattern of the output devices. This provides a number of important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do. Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies; that is, reducing EMI emission that might otherwise be radiated by speakers and long cable traces. The SSM2304 also offers protection circuits for overcurrent and temperature protection.

GAIN SELECTION

The SSM2304 has a pair of internal resistors that set an 18 dB default gain for the amplifier.

It is possible to adjust the SSM2304 gain by using external resistors at the input. To set a gain lower than 18 dB refer to Figure 37 for differential input configuration and Figure 38 for single-ended configuration. The external gain configuration is calculated as

External Gain Settings = 376 kΩ/(47 kΩ + Rext)

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system, therefore as not coming from the system input signal. Such transients can be generated when the amplifier system changes its operating mode. For example, the following can be sources of audible transients: system power-up/power-down, mute/unmute, input source change, and sample rate change. The SSM2304 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

EMI NOISE

The SSM2304 uses a proprietary modulation and spread-spectrum technology to minimize EMI emissions from the device. Figure 39 shows SSM2304 EMI emission starting from 100 kHz to 30 MHz. Figure 40 shows SSM2304 EMI emission from 30 kHz to 2 GHz. These figures clearly describe the SSM2304 EMI behavior as being well below the FCC regulation values, starting from 100 kHz and passing beyond 1 GHz of frequency. Although the overall EMI noise floor is slightly higher, frequency spurs from the SSM2304 are greatly reduced.

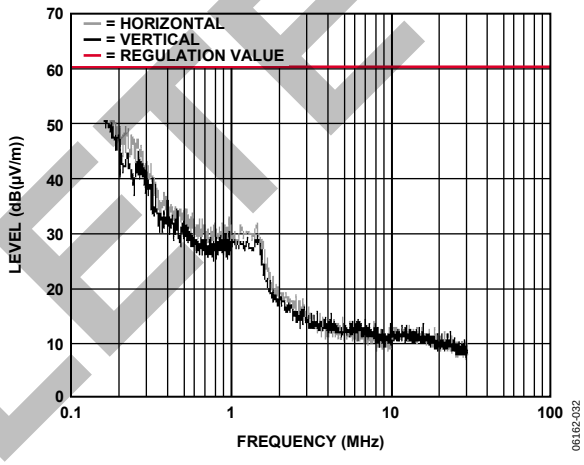


Figure 39. EMI Emissions from SSM2304

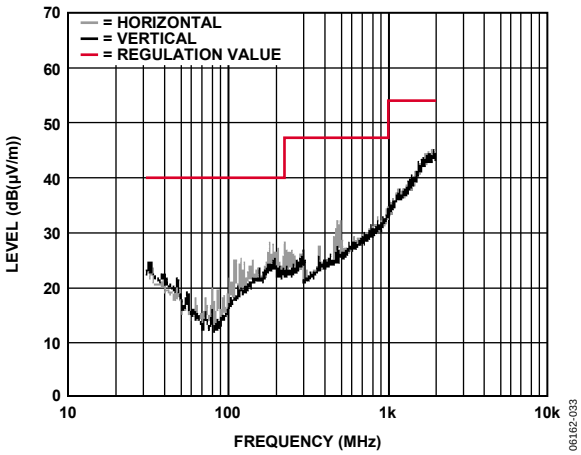


Figure 40. EMI Emissions from SSM2304

The measurements for Figure 39 and Figure 40 were taken with a 1 kHz input signal, producing 0.5 W output power into an 8 Ω load from a 3.6 V supply. Cable length was approximately 5 cm. The EMI was detected using a magnetic probe touching the 2" output trace to the load.

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LAYOUT

As output power continues to increase, care needs to be taken to lay out PCB traces and wires properly between the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mil for every inch of track length for lowest DCR, and use 1 oz or 2 oz of copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Proper grounding guidelines helps to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins should be as wide as possible to maintain the minimum trace resistances. It is also recommended to use a large-area ground plane for minimum impedances. Good PCB layouts also isolate critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency ones. Properly designed multilayer printed circuit boards can reduce EMI emission and increase immunity to RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for ground plane, whereas the ground plane side of a double-side board is often disrupted with signal crossover. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and, similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes nor analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM2304 will not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed (Figure 37), or if using a single-ended source (Figure 38). If high-pass filtering is needed at the input, the input capacitor along with the input resistor of the SSM2304 will form a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

Input capacitor can have very important effects on the circuit performance. Not using input capacitors degrades the output offset of the amplifier as well as the PSRR performance.

PROPER POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. Although the actual switching frequency can range from 10 kHz to 100 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input needs to be decoupled with a good quality low ESL and low ESR capacitor—usually around 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transients noises, use a 0.1 µF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitor as close as possible to the SSM2304 helps maintain efficiency performance.

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EVALUATION BOARD INFORMATION

INTRODUCTION

This section describes how to configure and use the SSM2304 Evaluation Board Revision 3.0.

There are several ways to connect the audio signal to the amplifier on the evaluation board. For example, the signal can be connected in single-ended or differential mode, and the output signals can be taken either after the ferrite beads or the inductors.

BOARD DESCRIPTION

The SSM2304 evaluation board has a complete application circuit for driving two stereo loudspeakers.

The silkscreen layer of the evaluation board is shown in Figure 41 with other top layers, including top copper, top solder mask, and multilayer (vias).

Figure 42 shows the top silkscreen layer only. There is no component in the bottom side; therefore, there is no bottom silkscreen layer.

Figure 43 shows the top layers without the silkscreen layer.

Figure 44 shows the bottom layers, including bottom copper, bottom solder mask, and multilayer (vias).

Figure 45 shows the mirrored bottom layers.

The schematic is shown in Figure 46.

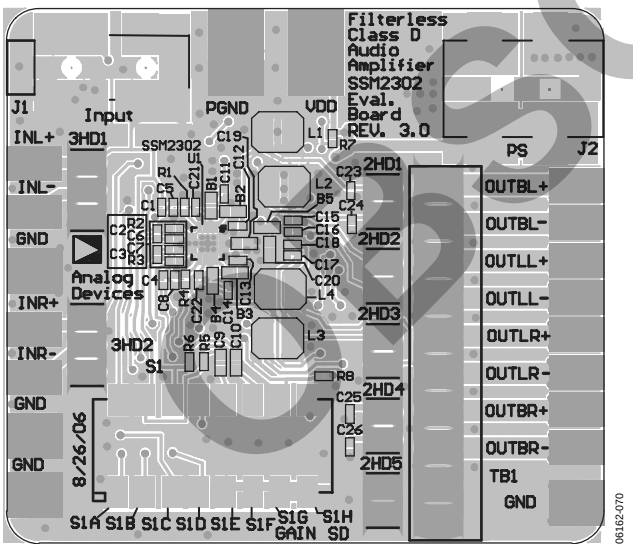


Figure 41. Top Silkscreen Layer with Other Top Layers

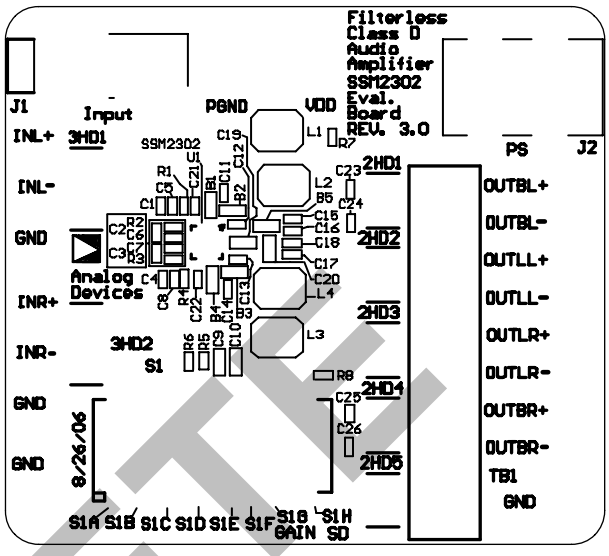


Figure 42. Top Silkscreen

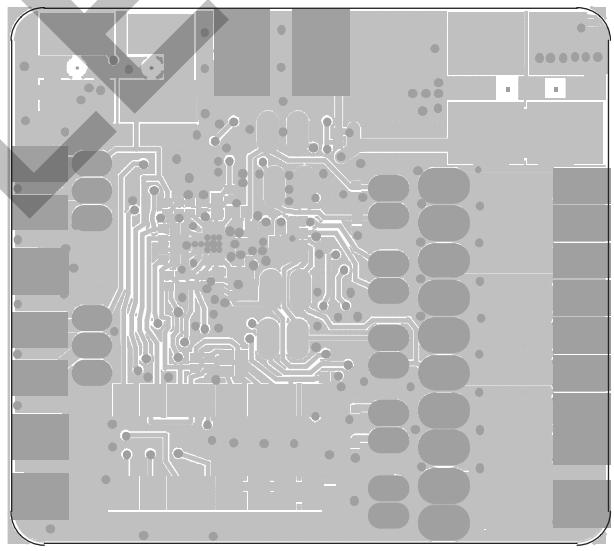


Figure 43. Top Layers Without Top Screen Layer

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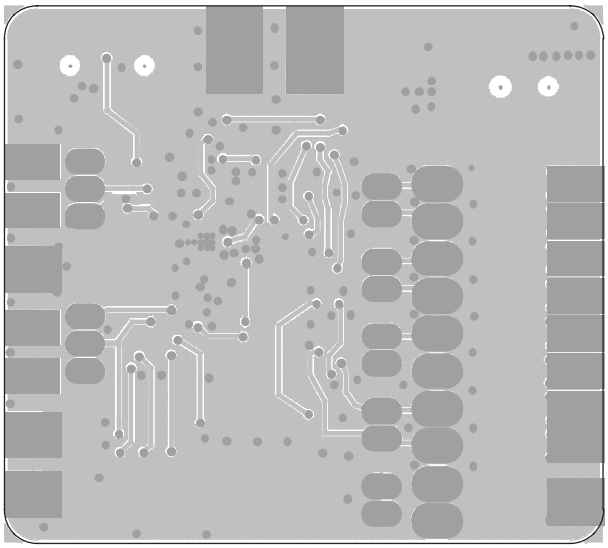


Figure 44. Bottom Layers

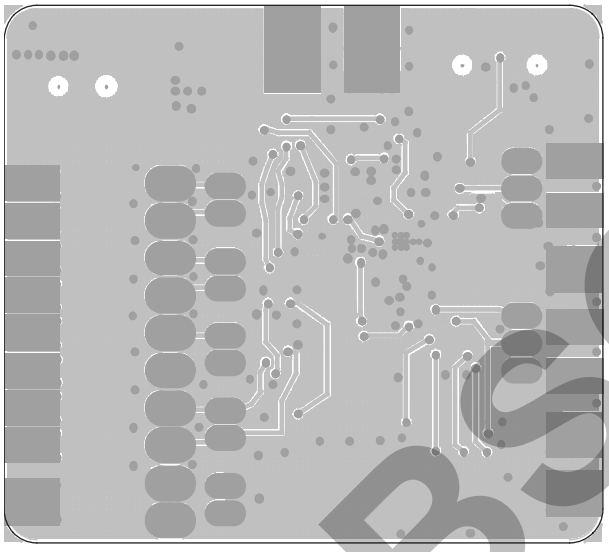


Figure 45. Mirrored Bottom Layers

On the upper left corner of the schematic shown in Figure 46, there is an audio stereo jack connector (3.5 mm), J1. This jack is compatible with standard stereo audio signals. It uses a conventional audio stereo signal connector/cable to obtain audio signals from common appliances, such as DVD players, personal computers, TVs, and so on. Because this connector only provides single-ended audio signals, turn Switches S1E and S1F to the upper positions when this input connector is utilized to ac short circuit the negative input ports to ground (see the schematic in Figure 46).

When differential mode audio signals are used as the input signal source, either use Headers 3HD1 and 3HD2 or the soldering pads located on the left side of the board and turn Switches S1E and S1F to the off position (lower position). The top header is for the left channel signals and the lower is for the right channel signals. There are two ground soldering pads on the lower left corner.

The lower side of the board has a switch bank and its corresponding channels are listed in Table 5

Table 5. Switch Channels

Switch Name	Corresponding Channel
S1A	Left positive
S1B	Left negative
S1C	Right negative
S1D	Right positive

When the switches listed in Table 5 are placed in the upper positions, their corresponding coupling capacitors are shorted; when the switches are placed in the lower positions, the coupling capacitors are inserted in the signal paths.

As previously described, Switches S1E and S1F are used to ac short circuit the left and right channel negative input ports to ground, respectively. This function is only needed when driving the input ports in single-ended mode. After shortening the negative input ports to ground, the noise picked up by the input port connections will be conducted to the ground.

S1G is not connected for the SSM2304.

S1H controls the shutdown function. The upper position shuts down the amplifier, and the lower position turns on the amplifier.

The upper right corner has a dc power jack connector. The center pin is for the positive terminal. It is compatible with 3 V to 5 V voltage, and the maximum peak current is approximately 1.2 A when driving a 4 Ω load (for SSM2304 only) and 0.6 A when driving an 8 Ω load with an input voltage of 5 V.

There are two solder pads in the upper center edge area for connecting the power supply voltages by clipping or soldering.

All the output ports are located on the right side of the board and marked with the corresponding names. Please see the legend on the board in Figure 42 and the schematic in Figure 46.

There are three ways to connect the output signals to the loads (the loudspeakers): using the four 2-pin headers, the terminal block, or the soldering pads.

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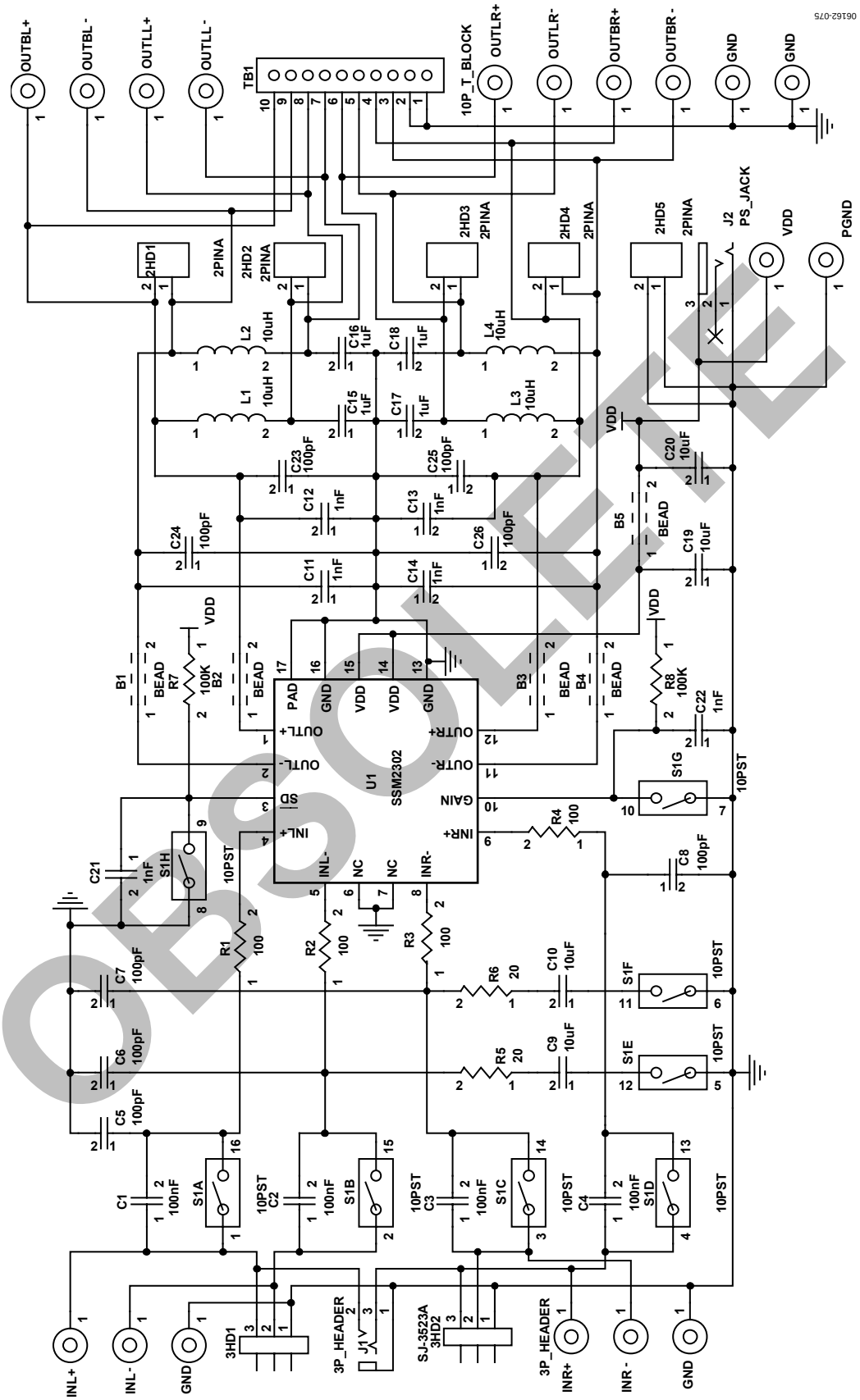


Figure 46. Schematic of SSM2304 Evaluation Board Rev. 3.0

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GETTING STARTED

To ensure proper operation, follow these steps:

1. Verify that the control switches are at the proper positions.
2. Put S1H, the shutdown control, in the lower position to turn on the amplifier.
3. Put S1G, the gain selection, in the upper position for higher gain and in the lower position for lower gain.
4. Connect the power supply with the right polarity and proper voltage.
5. Connect the loads to the proper output ports. Depending on the application, use nodes OUTBL+, OUTBL−, OUTBR+, and OUTBR− to connect the loads after the beads or use nodes OUTLL+, OUTLL−, OUTLR+, and OUTLR− to connect the loads after the inductors.

WHAT TO TEST

1. EMI (electromagnetic interference). Connect wires for the speakers that are the length required for the application and perform the EMI test.
2. Signal-to-noise ratio.
3. Output noise. Use an A-weighting filter to filter the output before the measurement meter.
4. Maximum output power.
5. Efficiency.
6. Component selections.

Selecting the correct components is the key for achieving the performance required at the cost budgeted.

1. Input coupling capacitor selection. Capacitors C1, C2, C3, and C4 should be large enough to couple the low frequency signal components in the incoming signal, but small enough to filter out unnecessary low frequency signals. For music signals, the cutoff frequency is often chosen between 20 Hz and 30 Hz. The cutoff frequency is calculated by

   $$C = 1/(2\ Rfc)$$

   where R is 150k, and fc is the cutoff frequency.
2. Input serial resistors (R1, R2, R3, and R4). These resistors are not necessary for the amplifier to operate and are only needed when special gain values are required. Using resistors of too high a value increases the input noise.
3. Output beads (B1, B2, B3, and B4). The output beads are necessary components for filtering out the EMIs caused at the switching output nodes. Ensure that these beads have enough current conducting capability while providing sufficient EMI attenuation. The current rating needed for an 8 Ω load is about 600 mA, and the impedance for 100 MHz must be greater than 600 Ω. In addition, the lower the DCR (dc resistance) of these beads, the better for minimizing their power consumptions. The recommended bead is described in Table 6.
4. Output shunting capacitors for the beads. There are two groups of these capacitors: C11, C12, C13, and C14 and C23, C24, C25, and C26. The former is for filtering out the lower frequency EMIs (those up to 250 MHz), and the latter is for filtering out the higher frequency EMIs (those greater than 250 MHz). Use small size (0603 or 0402) multilayer ceramic capacitors of a X7R or COG (NPO) material. The higher the value of these capacitors, the lower the residual EMI level at the output and the higher the quiescent current at the power supply. It is recommend to use 500 pF to 1 nF values for the first group of capacitors and 100 pF to 200 pF for the second group of capacitors.
5. Output inductors. Some users do not allow high frequency EMIs in the system and prefer using inductors to filter the output of the high frequency components at the output nodes. Choose an inductance greater than 2.2 µH for these inductors. The higher the inductance, the lower the EMI at the output and the lower the quiescent current at the power supply. However, higher inductance also corresponds with higher power consumption by the inductors when the output power level is high. It is recommended to use 2.2 µH to 10 µH inductors; the current rating must be greater than 600 mA (saturation current) for an 8 Ω load. Table 7 describes the recommended inductors.

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Table 6.

Part No.	Manufacturer	Z (Ω)	I_{MAX} (mA)	DCR (Ω)	Size (mm)
MPZ1608S601A	TDK	600	1000	0.15	1.6 × 0.8 × 0.8

Table 7.

Part No.	Manufacturer	L (µH)	I_{MAX} (mA)	DCR (Ω)	Size (mm)
LQH32CN4R7M53	Murata Manufacturing Co., Ltd.	4.7	650	0.15	3.2 × 2.5 × 1.55
LQH32CN3R3M53	Murata Manufacturing Co., Ltd.	3.3	710	0.12	3.2 × 2.5 × 1.55
LQH32CN2R2M53	Murata Manufacturing Co., Ltd.	2.2	790	0.1	3.2 × 2.5 × 1.55
SD3118-100-R	Cooper Bussmann, Inc.	10	900	0.3	3.1 × 3.1 × 1.8
ELL4LM100M	Panasonic Corporation	10	690	0.18	3.8 × 3.8 × 1.8
LBC2518T2R2M	Taiyo Yuden Co., Ltd.	2.2	630	0.13	2.5 × 1.8 × 2
1033AS-4R7M	Toko Inc.	4.7	680	0.31	3.8 × 3.8 × 1

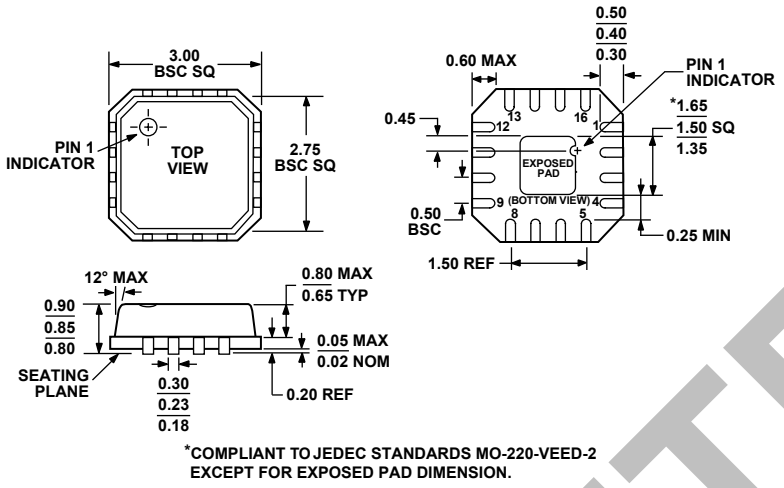
PCB LAYOUT GUIDELINES

To keep the EMI within the allowable limits and ensure that the amplifier chip operates within the temperature limits, adhere to the following guidelines.

1. Place nine vias onto the thermal pad of the amplifier. The outer diameter of the vias should be 0.5 mm and the inner diameter should be 0.33 mm. Use a PCB area of at least 2 cm × 2 cm or an equivalent area on the back side of the PCB layer as the heat sink (see Figure 41, Figure 42, and Figure 43). If there are internal layers available within the PCB, allocate an area as large as possible for the ground plane(s) and connect these vias to the plane(s).
2. Place the EMI filtering beads, B1, B2, B3, and B4, as close to the amplifier chip as possible. The same principle applies to the output inductors, L1, L2, L3, and L4, if they are included in the application design.
3. Place C11, C12, C13, and C14, the decoupling capacitors for the beads, as close to the amplifier chip as possible and connect their ground terminals together as close as possible. The same principle applies to the decoupling capacitors for the inductors, C15, C16, C17, and C18, if they are included in the application design.
4. Place C19, the decoupling capacitor for the power supply, as close to the amplifier chip as possible and connect its ground terminal directly to the IC's ground pins, Pins 13 and 16.
5. Place C20, the decoupling capacitor for the power supply, as close to the amplifier chip as possible and connect its ground terminal to the PCB ground area containing the power supply traces.
6. Place B5, the bead for the power supply, as close to the amplifier chip as possible, keeping it on the same side of the PCB as the chip.
7. The ferrite beads can block an EMI of up to 160 MHz in frequency. To eliminate EMIs greater than the 160 MHz, place a small capacitor, such as 100 pF, in parallel with the decoupling capacitors, C11, C12, C15, and C16, at least 20 mm from the 1 nF decoupling capacitor. Ideally, the ground terminals of these capacitors are connected to the ground terminals or the PCB traces, which are placed as close to the output loads (loudspeakers) as possible. In this way, the PCB connecting trace between these two capacitors serves as an inductor for filtering out the high frequency component.
8. Decouple the input port nodes and the digital pins, Pins 3, 4, 5, 8, 9, and 10, with small capacitors, such as 100 pF. These capacitors are not necessary, but can lower the EMI from these pins. The ground terminals of these capacitors should be connected to the chip ground as close as possible (see Figure 41, Figure 42, and Figure 43).
9. Ground the unconnected pins, Pins 6 and 7.
10. Connect the ground pins, Pins 6, 7, 13, and 16, to the thermal pad and place grounding vias as shown in Figure 41, Figure 42, and Figure 43.
11. Use a solid polygon plane on the other side of the PCB for the area of the vias that are placed on the thermal pad of the chip (see Figure 44 or Figure 45).
12. Keep the PCB traces for high EMI nodes on the same side of the PCB and as short as possible. The high EMI nodes are Pins 1, 2, 11, and 12 of the SSM2304.

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OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 47. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-3)
Dimensions shown in millimeters

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
SSM2304CPZ-REEL[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	A1F
SSM2304CPZ-REEL7[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	A1F
SSM2304Z-EVAL[1]		Evaluation Board		

[1] Z = Pb-free part.

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