Filterless High Efficiency Mono 1.4 W Class-D Audio Amplifier

Preliminary Technical Data

SSM2301

FEATURES

Filterless Class-D amplifier with built-in output stage
1.4 W into 8 Ω at 5.0 V supply with less than 1% THD
85% efficiency at 5.0 V, 1.4 W into 8 Ω speaker
Better than 98 dB SNR (signal-to-noise ratio)
Single-supply operation from 2.5 V to 5.0 V
20 nA ultralow shutdown current
Short-circuit and thermal protection
Available in 8-lead, 3 mm × 3 mm LFCSP
Pop-and-click suppression
Built-in resistors reduce board component count
Fixed and user-adjustable gain configurations

APPLICATIONS

Mobile phones
MP3 players
Portable gaming
Portable electronics
Educational toys

GENERAL DESCRIPTION

The SSM2301 is a fully integrated, high efficiency, Class-D audio amplifier. It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.0 V supply. It is capable of delivering 1.4 W of continuous output power with less than 1% THD + N driving an 8 Ω load from a 5.0 V supply.

The SSM2301 features a high efficiency, low noise modulation scheme that does not require any external LC output filters. The modulation continues to provide high efficiency even at low output power. It operates with 85% efficiency at 1.4 W into 8 Ω from a 5.0 V supply and has a signal-to-noise ratio (SNR) that is better than 93 dB. Spread-spectrum modulation is used to provide lower EMI-radiated emissions compared with other Class-D architectures.

The SSM2301 has a micropower shutdown mode with a maximum shutdown current of 30 nA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin.

The device also includes pop-and-click suppression circuitry. This minimizes voltage glitches at the output during turn-on and turn-off, thus reducing audible noise on activation and deactivation.

The fully differential input of the SSM2301 provides excellent rejection of common-mode noise on the input. Input coupling capacitors can be omitted if the dc input common-mode voltage is approximately $V_{DD}/2$.

The SSM2301 also has excellent rejection of power supply noise, including noise caused by GSM transmission bursts and RF rectification. PSRR is typically 63 dB at 217 Hz.

The gain can be set to 6 dB or 12 dB utilizing the gain control select pin connected respectively to ground or V_{DD}. Gain can also be adjusted externally by using an external resistor.

The SSM2301 is specified over the comercial temperature range (−40°C to +85°C). It has built-in thermal shutdown and output short-circuit protection. It is available in an 8-lead, 3 mm × 3 mm lead-frame chip scale package (LFCSP).

FUNCTIONAL BLOCK DIAGRAM

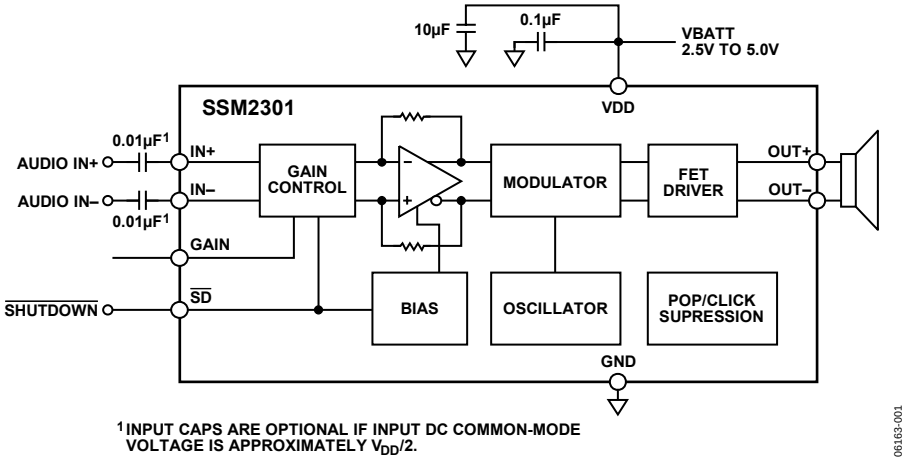


Figure 1.

Rev. PrH
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REVISION HISTORY

7/06—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω, unless otherwise noted

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.4		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.615		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.275		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.53		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.77		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.35		W
Efficiency	η	P_{OUT} =1.4 W, 8 Ω, V_{DD} = 5.0 V		85		%
Total Harmonic Distortion + Noise	THD + N	P_O = 1 W into 8 Ω, f = 1 kHz, V_{DD} = 5.0 V		0.1		%
		P_O = 0.5 W into 8 Ω, f = 1 kHz, V_{DD} = 3.6 V		0.04		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} − 1	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz		55		dB
Average Switching Frequency	f_{SW}			1.8		MHz
Differential Output Offset Voltage	V_{OOS}	G = 6 dB; G = 12 dB		2.0		mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.0	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V, 50 Hz, input floating/ground	70	85		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz, inputs ac GND, C_{IN} = 0.01 µF, input referred		63		dB
Supply Current	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		5.5		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		4.5		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		4.0		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN CONTROL						
Closed-Loop Gain	Av0	GAIN pin = 0 V		6		dB
	Av1	GAIN pin = V_{DD}		12		dB
Differential Input Impedance	Z_{IN}	$\overline{SD}$ = VDD,		150		KΩ
		$\overline{SD}$ = GND		210		KΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} ≥ 1 mA		1.2		V
Input Voltage Low	V_{IL}	I_{SY} ≤ 300 nA		0.5		V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		30		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		KΩ
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 2.5 V to 5.0 V, f = 20 Hz to 20 kHz, inputs are ac grounded, sine wave, A_V = 6 dB, A weighting		35		µV
Signal-to-Noise Ratio	SNR	P_{OUT} = 1.4 W, R_L = 8 Ω		98		dB

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-lead, 3 mm × 3 mm LFCSP	62	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

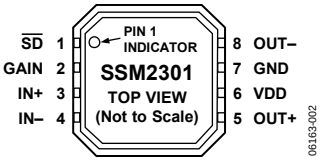


Figure 2. SSM2301 LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{SD}$	Shutdown Input. Active low digital input.
2	GAIN	Gain Selection. Digital input.
3	IN+	Noninverting Input.
4	INL–	Inverting Input.
5	OUT+	Noninverting Output.
6	VDD	Power Supply.
7	GND	Ground.
8	OUT–	Inverting Output.

TYPICAL PERFORMANCE CHARACTERISTICS

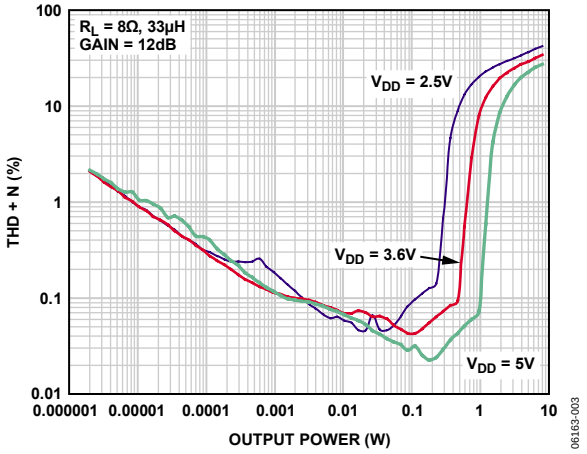


Figure 3. THD + N vs. Output Power into 8 Ω, A_V = 12 dB

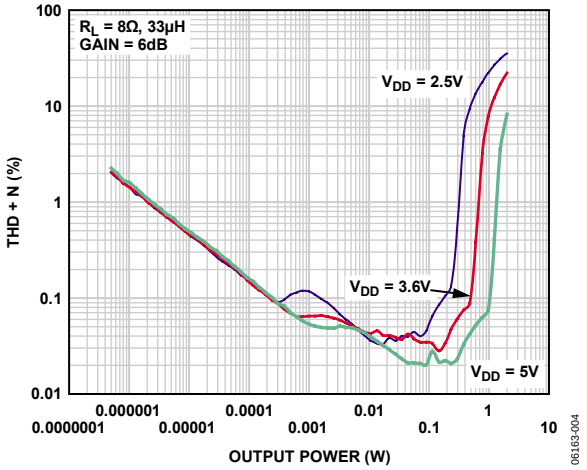


Figure 4. THD + N vs. Output Power into 8 Ω, A_V = 6 dB

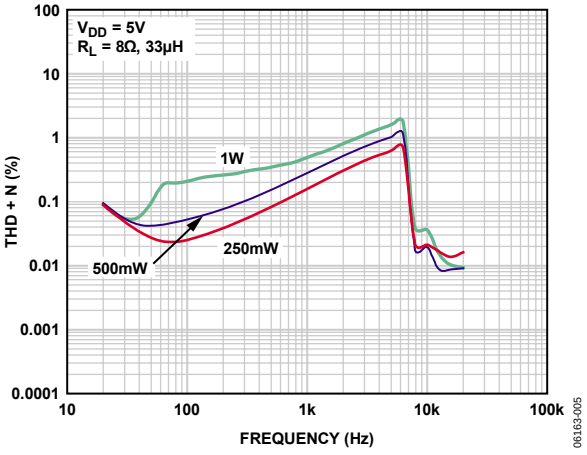


Figure 5. THD + N vs. Frequency, V_{DD} = 5.0 V

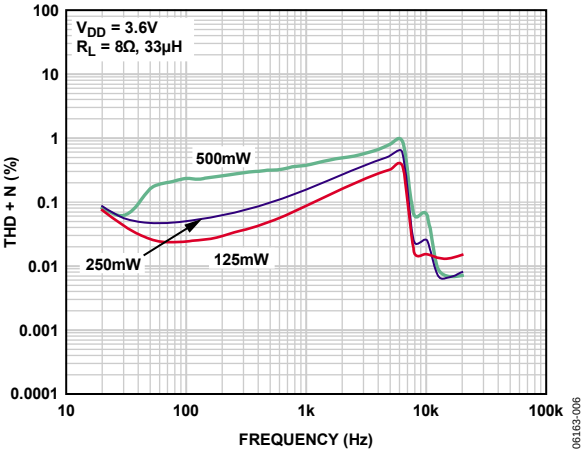


Figure 6. THD + N vs. Frequency, V_{DD} = 3.6 V

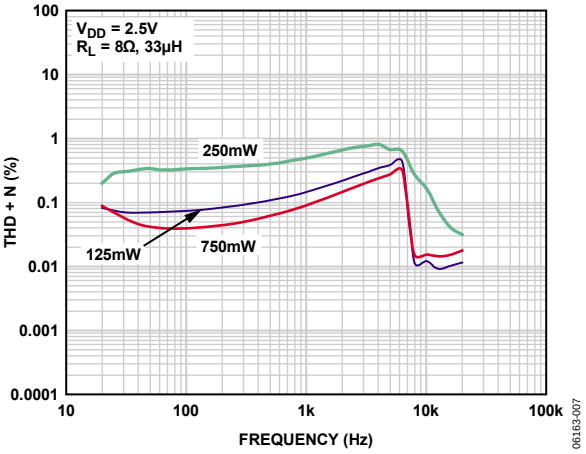


Figure 7. THD + N vs. Frequency, V_{DD} = 2.5 V

TBD

Figure 8. Supply Current vs. Supply Voltage, No Load

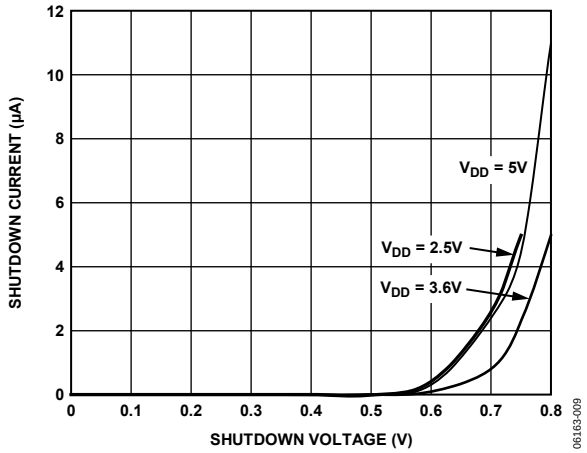


Figure 9. Supply Current vs. Shutdown Voltage

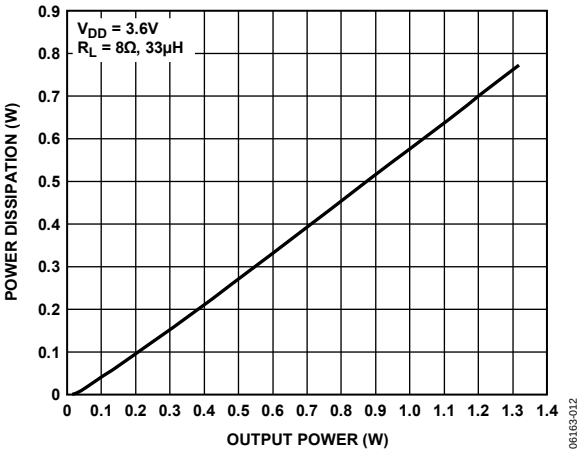


Figure 12. Power Dissipation vs. Output Power at V_{DD} = 3.6 V

TBD

Figure 10. Maximum Output Power vs. Supply Voltage

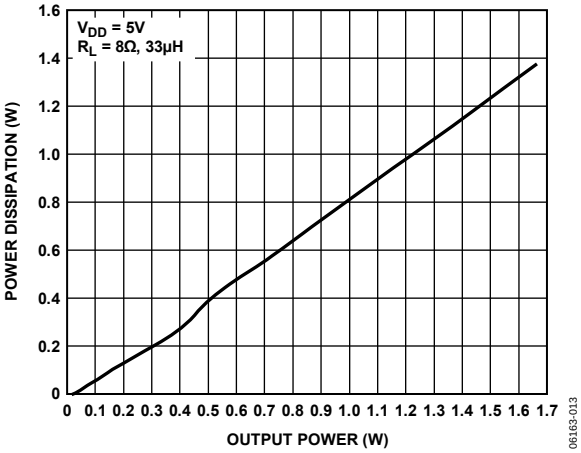


Figure 13. Power Dissipation vs. Output Power at V_{DD} = 5.0 V

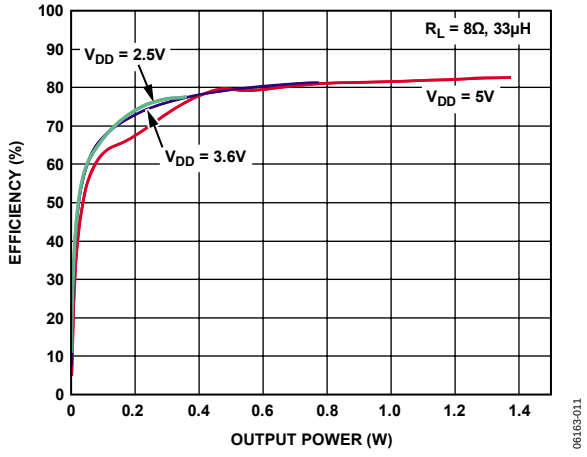


Figure 11. Efficiency vs. Output Power into 8 Ω

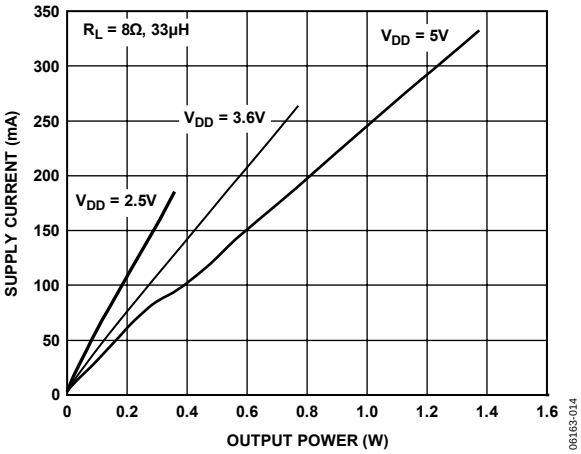


Figure 14. Output Power vs. Supply Current, One Channel

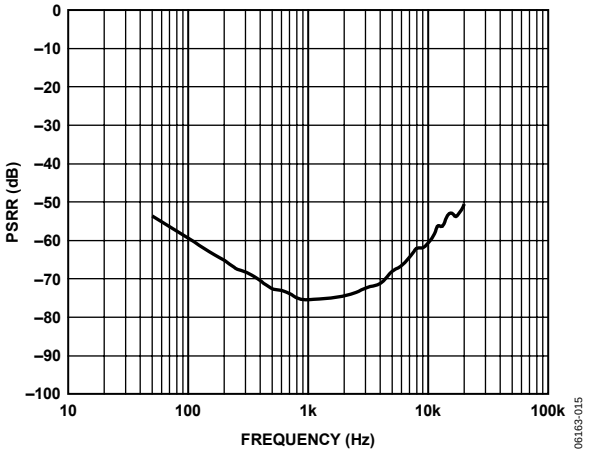


Figure 15. Power Supply Rejection Ratio vs. Frequency

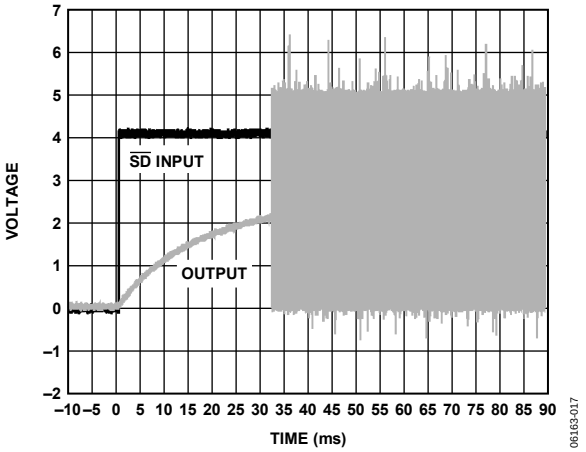


Figure 17. Turn-On Response

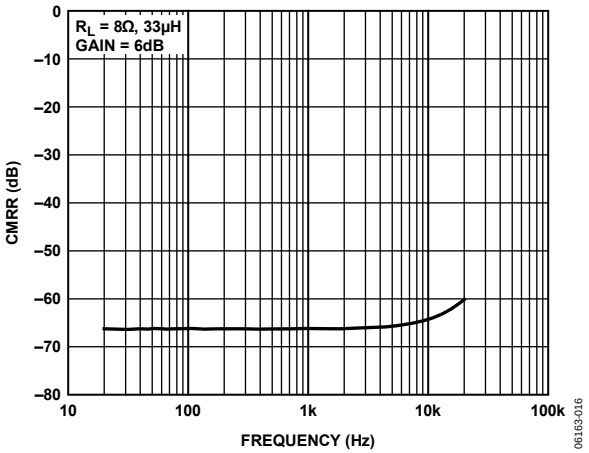


Figure 16. Common-Mode Rejection Ratio vs. Frequency

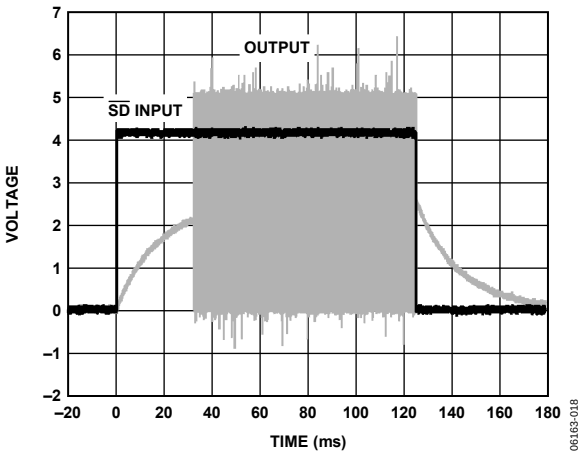


Figure 18. Turn-Off Response

TYPICAL APPLICATION CIRCUITS

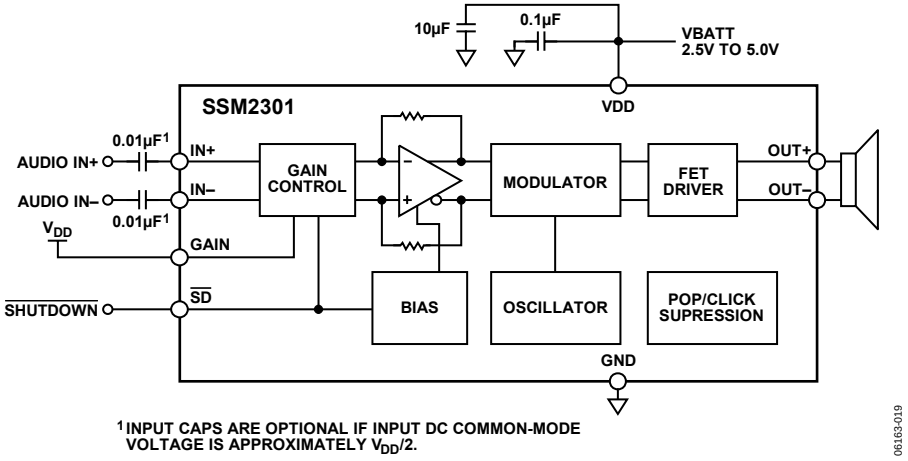


Figure 19. Differential Input Configuration, Gain = 12 dB

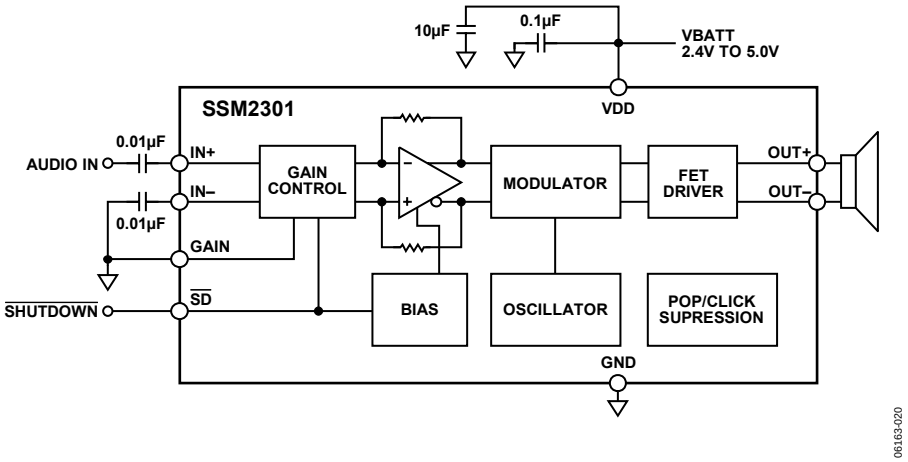


Figure 20. Single-Ended Input Configuration, Gain = 6 dB

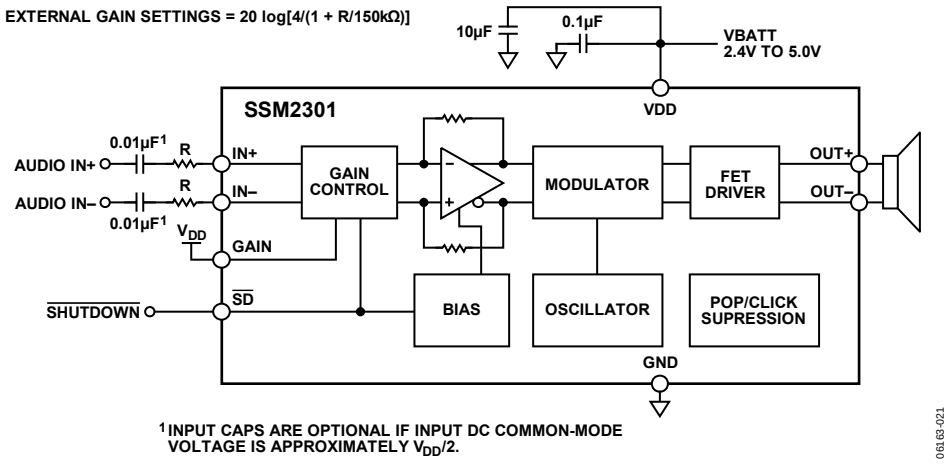


Figure 21. Differential Input Configuration, User-Adjustable Gain

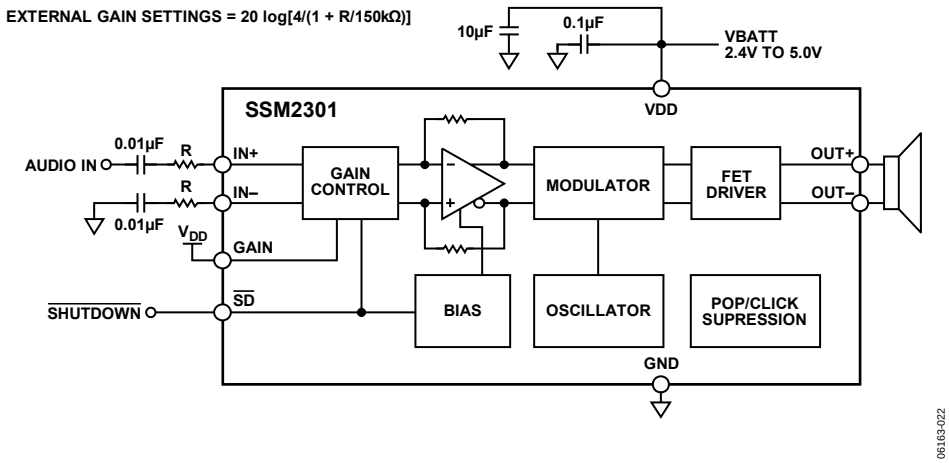


Figure 22. Single-Ended Input Configuration, User-Adjustable Gain

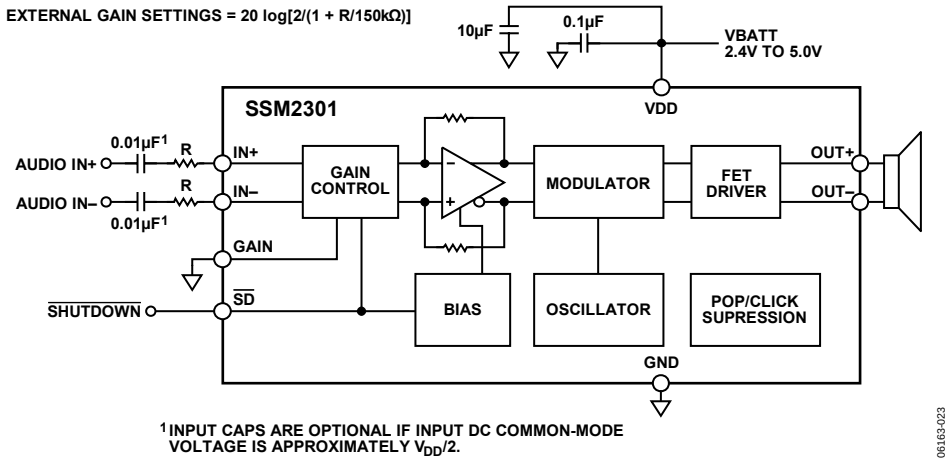


Figure 23. Differential Input Configuration, User-Adjustable Gain

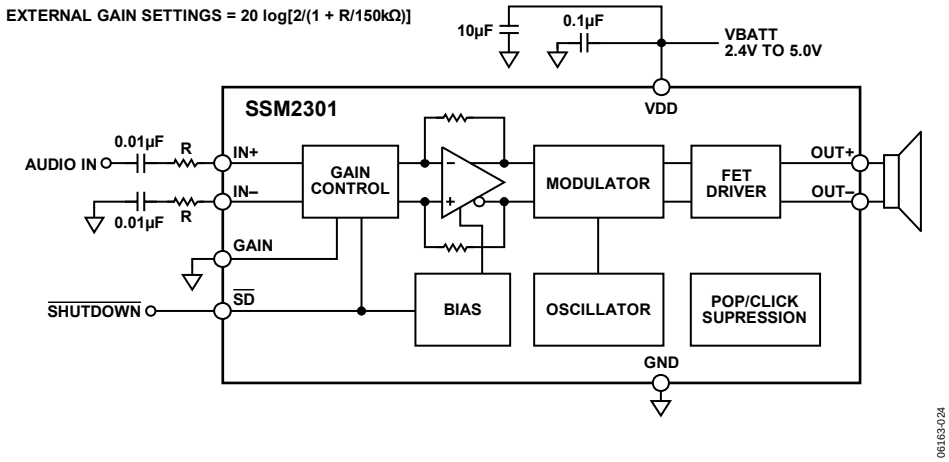


Figure 24. Single-Ended Input Configuration, User-Adjustable Gain

APPLICATION NOTES

OVERVIEW

The SSM2301 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external components count, conserving board space and thus reducing systems cost. The SSM2301 does not require an output filter, but instead relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square-wave output. While most Class-D amplifiers use some variation of pulse-width modulation (PWM), the SSM2301 uses a Σ-Δ modulation to determine the switching pattern of the output devices. This provides a number of important benefits. Σ-Δ modulators do not produces a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do. Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies; that is, reducing EMI emission that might otherwise be radiated by speakers and long cable traces. The SSM2301 also offers protection circuits for overcurrent and temperature protection.

GAIN SELECTION

Pulling the GAIN pin high of the SSM2301 sets the gain of the speaker amplifier to 12 dB; pulling it low sets the gain of the speaker amplifier to 6 dB.

It is possible to adjust the SSM2301 gain by using external resistors at the input. To set a gain lower than 12 dB refer to Figure 21 for differential input configuration and Figure 22 for single-ended configuration. For external gain configuration from a fixed 12 dB gain, use the following formula:

$$External\ Gain\ Settings = 20 \log[4/(1 + R/150\ k\Omega)]$$

To set a gain lower than 6 dB refer to Figure 23 for differential input configuration and Figure 24 for single-ended configuration. For external gain configuration from a fixed 6 dB gain, use the following formula:

$$External\ Gain\ Settings = 20 \log[2/(1 + R/150\ k\Omega)]$$

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system, therefore as not coming from the system input signal. Such transients can be generated when the amplifier system changes its operating mode. For example, the following can be sources of audible transients: system power-up/power-down, mute/unmute, input source change, and sample rate change. The SSM2301 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

LAYOUT

As output power continues to increase, care needs to be taken to lay out PCB traces and wires properly between the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mil for every inch of track length for lowest DCR, and use 1 oz or 2 oz of copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins should be as wide as possible to maintain the minimum trace resistances. It is also recommended to use a large-area ground plane for minimum impedances. Good PCB layouts also isolate critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency ones. Properly designed multilayer printed circuit boards can reduce EMI emission and increase immunity to RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for ground plane, whereas the ground plane side of a double-side board is often disrupted with signal crossover. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and, similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes nor analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM2301 will not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed (Figure 19), or if using a single-ended source (Figure 20). If high-pass filtering is needed at the input, the input capacitor along with the input resistor of the SSM2301 will form a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

Input capacitor can have very important effects on the circuit performance. Not using input capacitors degrades the output offset of the amplifier as well as the PSRR performance.

PROPER POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. Although the actual switching frequency can range from 10 kHz to 100 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input needs to be decoupled with a good quality low ESL and low ESR capacitor—usually around 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transients noises, use a 0.1 µF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitor as close as possible to the SSM2301 helps maintain efficiency performance.

EVALUATION BOARD INFORMATION

INTRODUCTION

The SSM2301 audio power amplifier is a complete low power, Class-D, stereo audio amplifier capable of delivering 1.4 W/channel into 8 Ω load. In addition to the minimal parts required for the application circuit, measurement filters are provided on the evaluation board so that conventional audio measurements can be made without additional components.

This section provides an overview of Analog Devices SSM2301 evaluation board. It includes a brief description of the board as well as a list of the board specifications.

Table 5. SSM2301 Evaluation Board Specifications

Parameter	Specification
Supply Voltage Range, V_{DD}	2.5 V to 5.0 V
Power Supply Current Rating	1.5 A
Continuous Output Power, P_O (R_L = 8 Ω, f = 1 kHz, 22 kHz BW)	1.4 W
Minimum Load Impedance	8 Ω

OPERATION

Use the following steps when operating the SSM2301 evaluation board.

Power and Ground

1. Set the power supply voltage between 2.5 V and 5.0 V. When connecting the power supply to the SSM2301 evaluation board, make sure to attach the ground connection to the GND header pin first and then connect the positive supply to the VDD header pin.

Inputs and Outputs

1. Ensure that the audio source is set to the minimum level.
2. Connect the audio source to Inputs IN± and IN±.
3. Connect the speakers to Outputs OUT± and OUT±.

Gain Control

The gain select header controls the gain setting of the SSM2301.

1. Select jumper to LG for 6 dB gain.
2. Select jumper to HG for 12 dB gain.

External Gain Settings

It is possible to adjust the SSM2301 gain using external resistors at the input. To set a gain lower than 12 dB refer to Figure 21 and Figure 22 on the product data sheet for proper circuit configuration. For external gain configuration from a fixed 12 dB gain, use the following formula:

$$External\ Gain\ Settings = 20 \log[4/(1 + R/150\ k\Omega)]$$

To set a gain lower than 6 dB refer to Figure 23 and Figure 24 on the product data sheet for proper circuit configuration. For external gain configuration from a fixed 6 dB gain, use the following formula:

$$External\ Gain\ Settings = 20 \log[2/(1 + R/150\ k\Omega)]$$

Shutdown Control

The shutdown select header controls the shutdown function of the SSM2301. The shutdown pin on the SSM2301 is active low, meaning that a low voltage (GND) on this pin places the SSM2301 into shutdown mode.

1. Select jumper to 1-2 position. Shutdown pulled to V_{DD}.
2. Select jumper to 2-3 position. Shutdown pulled to GND.

Input Configurations

1. For differential input configuration with input capacitors do not place a jumper on J2 and J3.
2. For differential input configuration without input capacitors place a jumper on J2 and J3.

SSM2301 APPLICATION BOARD SCHEMATIC

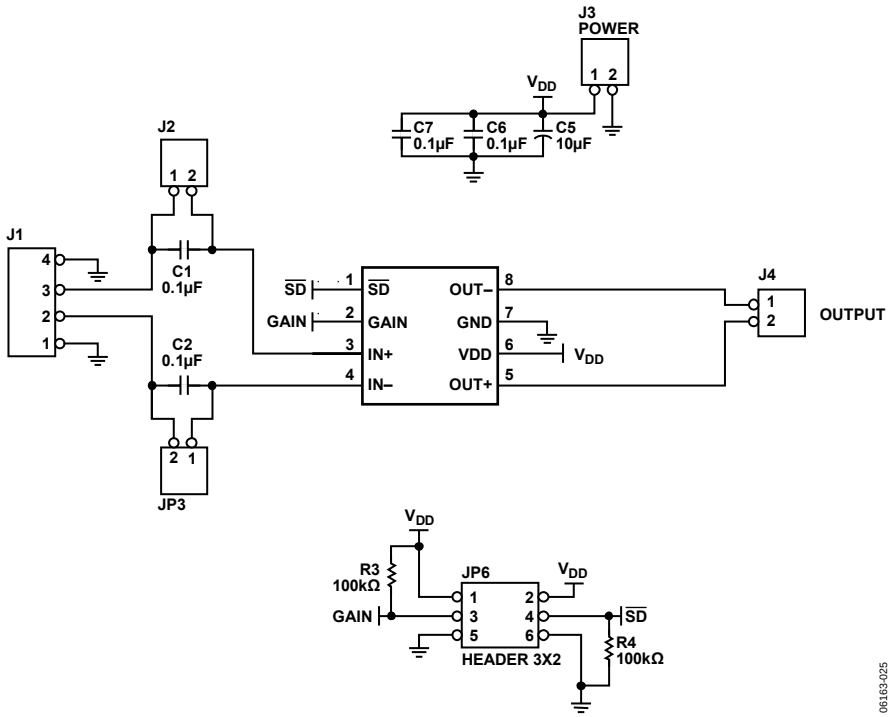


Figure 25. SSM2301 Application Board Schematic

SSM2301 STEREO CLASS-D AMPLIFIER EVALUATION MODULE COMPONENT LIST

Table 6.

Reference	Description	Footprint	Quantity	Manufacturer/Part Number
C6, C7	Capacitor, 0.1 µF	0603	2	Murata Manufacturing Co., Ltd./GRM18
C5	Capacitor, 10 µF	0805	1	Murata Manufacturing Co., Ltd./GRM21
C1, C2, C3, C4	Capacitor, 1 nF	0402	4	Murata Manufacturing Co., Ltd./GRM15
R3, R4	Resistor, 100 kΩ	0603	2	Vishay/CRCW06031003F
L1, L2,	Ferrite bead	0402	2	Murata Manufacturing Co., Ltd./BLM15EG121
U1	IC, SSM2301	3.0 mm × 3.0 mm	1	SSM2301CSPZ
EVAL BOARD	PCB evaluation board		1	

SSM2301 APPLICATION BOARD LAYOUT

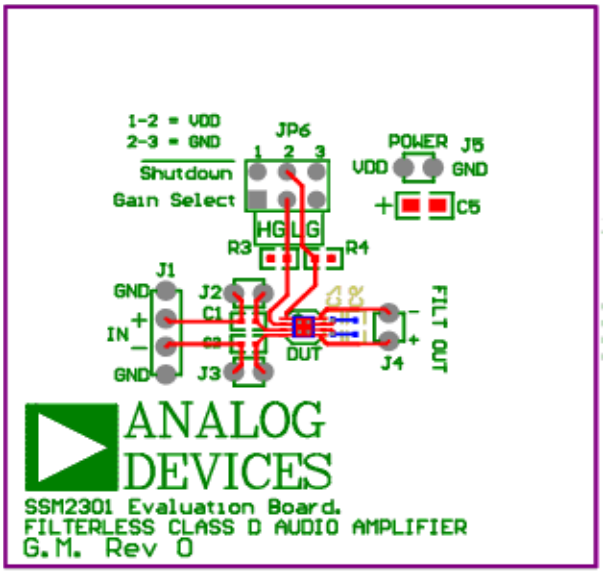


Figure 26. SSM2301 Application Board Layout

OUTLINE DIMENSIONS

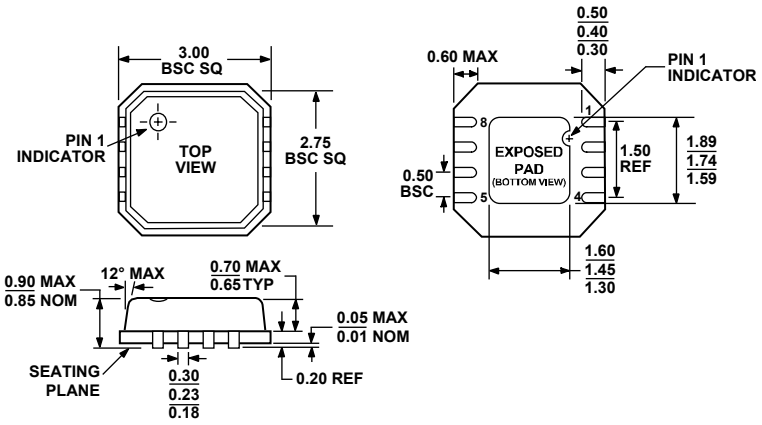


Figure 27. 16-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
SSM2301CPZ-R2[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	A1C
SSM2301CPZ-REEL[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	A1C
SSM2301CPZ-REEL7[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	A1C

[1] Z = Pb-free part.

NOTES

NOTES

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