SSL3401HN

Low voltage dimmable controller for LED lighting

Rev. 2 — 28 January 2014 Product data sheet

1. General description

The SSL3401HN is a Switched Mode Power Supply (SMPS) controller IC. It operates in combination with a phase cut dimmer and a 12 V (AC or DC) low voltage electronic or magnetic transformer. It is designed to drive LED devices and include a dimmer conduction phase detector.

The chip includes a hysteretic controller for the power converter. It is most suitable for use with a linear LED current source. Two embedded Proportional-Integral (PI) controllers and a 0.052 % resolution PWM generator, adjusted by the dimmer conduction phase, ensure excellent LED current stability for a dimming range from 100 % to less than 5 %. It also minimizes the power loss across the LED current source.

Several protection mechanisms are available:

- OverVoltage Protection (OVP)
- Coil Current Limitation (CCL)
- Short LED protection (SLED)
- Open LED protection (OLED)
- UnderVoltage LockOut (UVLO)
- Advanced adaptive OverTemperature Protection (OTP)

2. Features and benefits

- Easy migration to existing lighting control infrastructure
- Support most available dimming and low-voltage transformation solutions
- Excellent stability of LED current
- Double PI controllers to enhance the line regulation of the LED current
- Optimized dimming curve for low-voltage transformer compatibility
- Automatic supply frequency detection for seamless operation with 50 Hz, 60 Hz or DC sources
- Dimmer conduction angle detection
- Coil current limitation
- Temperature roll-back protection
- OverVoltage Protection
- Power-On-Reset (POR)
- Shorted LED protection
- Open LED detection

3. Applications

- General LED lighting with various power requirements
- Dimmable 12 V MR16 and AR111 applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		2.6	3.3	3.6	V
I_{DD}	supply current		-	10	-	mA
$V_{fbck(min)}$	minimum feedback voltage	minimum voltage over 1 AC supply cycle in steady state closed loop configuration; full output power	-	0.625	-	V
$f_{sw(PWM)}$	PWM switching frequency		-	12.5	-	kHz
V_{hys}	hysteresis voltage	comparator; positive hysteresis; V_{ACMPx} = 1.5 V				
		Pin HYSTSET set HIGH or not connected	-	20	-	mV
		Pin HYSTSET set LOW	-	10	-	mV
		comparator; negative hysteresis; V_{ACMPx} = 1.5 V				
		Pin HYSTSET set HIGH or not connected	-	−20	-	mV
		Pin HYSTSET set LOW	-	−10	-	mV
$I_{O(sc)H}$	HIGH-level short-circuit output current	pin BSTDRVx; V_{OH} = 0 V	-	-	−45	mA
$I_{O(sc)L}$	LOW-level short-circuit output current	pin BSTDRVx; V_{OH} = 3.3 V	-	-	50	mA
$V_{th(scp)LED}$	LED short-circuit protection threshold voltage	pin FB	-	2.4	3.9	V
$V_{th(ovp)}$	overvoltage protection threshold voltage	pin OVP	-	1.90	-	V
$V_{ovp(hys)}$	overvoltage protection voltage hysteresis	pin OVP	-	0.55	-	V
T_{amb}	ambient temperature	operating	0	-	105	°C
$T_{th(otp)}$	overtemperature protection threshold temperature	die junction temperature	-	125	-	°C

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5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SSL3401HN/1	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	HVQFN33

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6. Block diagram

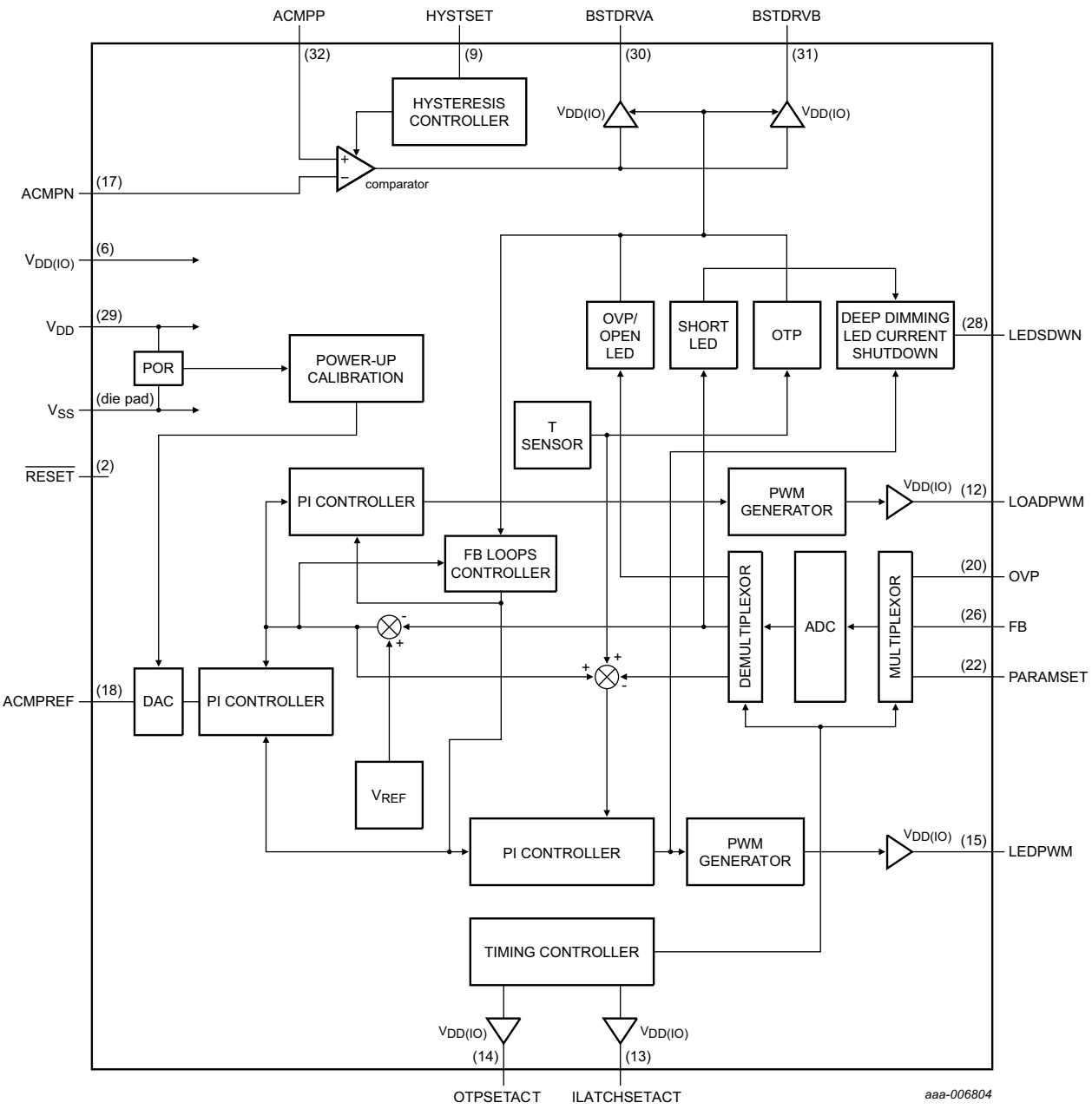


Fig 1. SSL3401HN block diagram

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7. Pinning information

7.1 Pinning

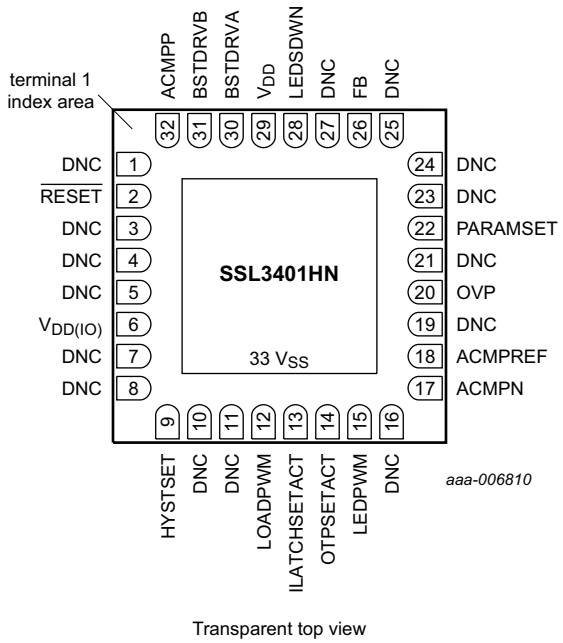


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Reset state	Description
DNC	1	-	-	do not connect
$\overline{\text{RESET}}$	2	input	-	reset if LOW
DNC	3	-	-	do not connect
DNC	4	-	-	do not connect
DNC	5	-	-	do not connect
$V_{DD(IO)}$	6	power	-	3.3 V I/O supply voltage
DNC	7	-	-	do not connect
DNC	8	-	-	do not connect
HYSTSET	9	input	-	comparator hysteresis level setting (high hysteresis level if pin is left open or set HIGH, low hysteresis level if pin is set LOW)
DNC	10	-	-	do not connect
DNC	11	-	-	do not connect
LOADPWM	12	output	H	output load control (input pin at reset)
ILATCHSETACT	13	input	-	input latching current setting control
OTPSETACT	14	input	-	overtemperature setting control

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Reset state	Description
LEDPWM	15	output	H	LED current control (input pin at reset)
DNC	16	supply	-	do not connect
ACMPN	17	input	-	analog comparator negative input
ACMPREF	18	output	H	analog comparator reference voltage
DNC	19	-	-	do not connect
OVP	20	input	-	overvoltage protection sensing input
DNC	21	-	-	do not connect
PARAMSET	22	input	-	input latching current and OTP setting input
DNC	23	-	-	do not connect
DNC	24	-	-	do not connect
DNC	25	-	-	do not connect
FB	26	input	-	feedback loop input voltage
DNC	27	-	-	do not connect
LEDSDWN	28	output	H	LED current deep dimming control
V_{DD}	29	power	-	3.3 V supply voltage
BSTDRVA	30	output	H	power MOSFET driver output
BSTDRVB	31	output	H	power MOSFET driver output
ACMPP	32	input	-	analog comparator positive input
V_{SS}	33	ground	-	die pad ground terminal

8. Functional description

8.1 Supply

The SSL3401HN operates with a 3.3 V typical supply. The IC core and the interface pins are supplied by two different supply pins V_{DD} and $V_{DD(IO)}$. These pins are not connected internally in the IC. They must all be connected externally to the main supply.

8.2 State diagram

The SSL3401HN has two modes:

- Reset
- Active

8.2.1 Reset mode

The chip enters the reset state:

- At the power start-up phase
- When V_{DD} drops below the V_{DD} POR threshold voltage ($V_{th(POR)}$)
- When the $\overline{\text{RESET}}$ pin is set LOW

All registers are cleared to their default values.

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If V_{DD} is below the POR rising edge threshold voltage, the SSL3401HN remains in Reset mode. Otherwise, the IC enters the Active mode.

During the Reset mode, all interface pins are configured as input with a weak pull-up current. External pull-down resistors are required for those pins which must be LOW during this phase.

8.2.2 Active mode

Active mode is the normal operating mode when V_{DD} exceeds the POR rising edge threshold voltage and pin $\overline{\text{RESET}}$ is set HIGH or left open.

After leaving Reset mode, an initialization phase occurs. This phase consists of:

- The calibration of the internal DAC and ADC converters based on the internal reference voltage
- The reading of parameter external parameter settings (if available)
- The detection of the comparator external common-mode offset
- The calculation of parameter values required for IC operation

The application power supply type detection (AC or DC) and the supply frequency (50 Hz or 60 Hz) detection are executed.

The boost driver outputs BSTDRVA and BSTDRVB are active only after the DAC calibration and the comparator common-mode offset detection are completed.

After the initialization phase, the feedback loops are active and all protection circuits are on and continuously monitoring for abnormal events.

8.3 Power MOSFET control

The SSL3401HN is designed for use with an external inverting MOSFET driver. Depending on the input impedance of the external driver, a single output or double outputs can be used from the SSL3401HN.

8.4 Input current control

The input current is controlled by setting a voltage at the comparator negative input. The positive input is connected to the coil current sensing resistor R_{ICBST}. A V_{DD} referred level shifter is inserted between R_{ICBST} and the positive input of the comparator. It consists of resistors with the same nominal value. The SSL3401HN detects and compensates automatically for the level shifter offset as well as for gain because of variation in the resistance value.

Optionally, an input latching current can be created to improve compatibility with leading-edge dimmers.

The average input current, with the latching current set to zero, is set to 1.1 A with a 200 mΩ R_{ICBST}. This setting is adequate for a 7.5 W input power system. With a different input power level, the R_{ICBST} value must be scaled proportionally to get an optimum start-up behavior and dimming sensitivity range. The equivalent R_{ICBST} value can be calculated with Equation 1:

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$$R_{ICBST} = 0.20 \times \frac{7.5}{P_{input}} \quad (1)$$

Different input latching current values can be set via external resistors. Table 4 shows the latching current value as a function of the output voltage of the input latching current setting resistor divider, $V_{set(l)latch}$ = (V_{DD} * RSET2 / (RSET2 + RSET3)), with R_{ICBST} = 200 mΩ and V_{DD} = 3.3 V.

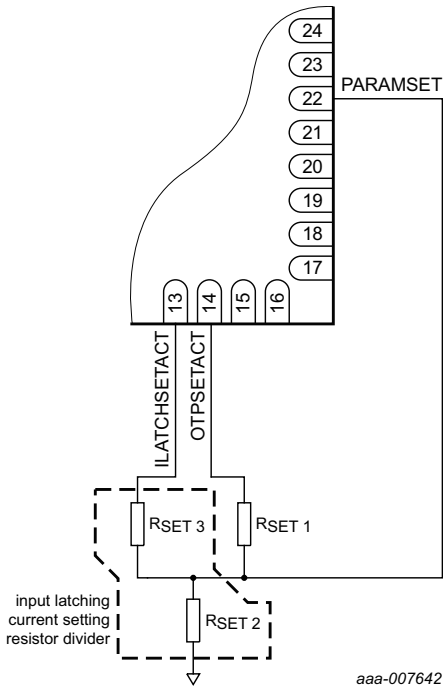


Fig 3. Latching current setting

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Table 4. Latching current setting

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{set(I)latch}$	latching current setting voltage	latching current = +0.00 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	0	-	0.20	V
		latching current = +0.5 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	0.20	-	0.41	V
		latching current = +0.75 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	0.41	-	0.61	V
		latching current = +1.00 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	0.61	-	0.82	V
		latching current = +1.25 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	0.82	-	1.03	V
		latching current = +1.50 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	1.03	-	1.23	V
		latching current = +1.75 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	1.23	-	1.54	V
		latching current = +2.00 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	1.54	-	1.85	V
		latching current = +2.25 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	1.85	-	2.16	V
		latching current = +2.5 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	2.16	-	2.47	V
		latching current = 0 A; V_{DD} = 3.3 V; R_{ICBST} = 200 mΩ	2.47	-	V_{DD}	V

The average and latching input current vary in inverse proportion to R_{ICBST}.

The system input signal is a rectified 50 Hz sine wave signal. The latching current, in the form of a transient input peak current, occurs once every 10 ms at the start of the sine wave signal with a decay time constant of 250 µs.

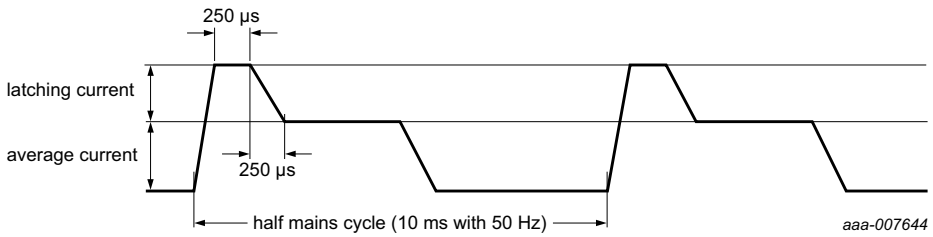


Fig 4. Latching current

8.5 LED current control

The SSL3401HN provides a Pulse Width Modulated (PWM) signal to control the LED current. The signal is continuously LOW for the maximum LED current setting and HIGH for the minimum LED current setting. The frequency is set to 12 kHz. If it concerns a DC supply, it is set continuously LOW. The IC automatically detects the supply type (AC or DC).

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During the initialization phase, the PWM signal has a 100 % duty cycle. When the initialization phase is completed, the PWM duty cycle is set according to the required output power. The setting depends on the dimmer conduction angle in the event of a phase cut dimmed AC supply.

A properly designed application causes the duty cycle, defined as T_{LOW}/T_{period}, to increase when LED current increases.

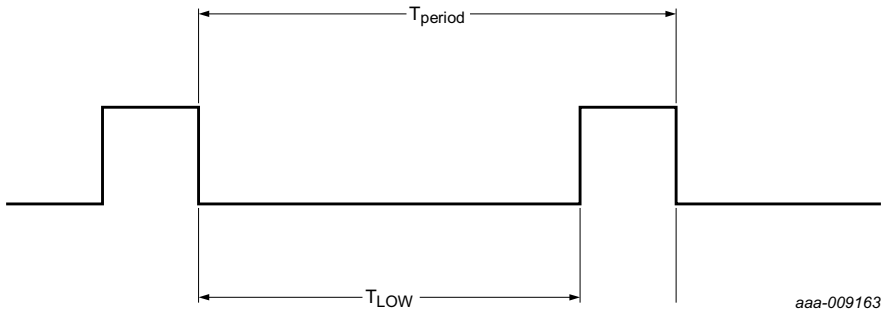


Fig 5. PWM duty cycle definition

8.6 Output load control

The SSL3401HN provides a Pulse Width Modulation (PWM) signal to control the output load resistor (R_{LOAD}). The signal is continuously HIGH for the maximum output load power setting (lowest resistor value) and LOW for the minimum output load power setting (open resistor).

A properly designed application causes the duty cycle, defined as T_{LOW}/T_{period} (Figure 5), to decrease when the output load power increases.

The output load resistor (R_{LOAD}) is aimed at limiting the boost output voltage (V_{BST}) overshoot in case of a sudden increase in input power. The optimum total R_{LOAD} value is $R_{LOAD} = V_{BST} / (I_{LEDMAX} * 0.3)$.

8.7 Feedback loop control

The SSL3401HN incorporates three independent proportional-integral (PI) feedback loop controllers. All of them act on an error signal, as a result of the difference between the minimum voltage on the FB pin and a predefined setpoint (0.625 V). The minimum voltage is computed during a time interval equal to the supply time period: 10 ms for a rectified 50 Hz supply and 8.3 ms for a rectified 60 Hz supply. The PI controller output value is then updated once per supply time period or 10 ms in a DC supply.

The first PI controller sets an analog signal at the ACMPREF pin to control the coil current of the hysteretic boost converter.

The second PI controller adjusts the duty cycle of the LED current PWM signal (LEDPWM).

The third PI controller output is a PWM signal (LOADPWM). It can be used to improve the line rejection and thus the LED current stability.

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If the input power, based on the default input current, is lower than the maximum LED power + system losses, the LED current PWM is adjusted. Otherwise, the input current is adjusted to maintain the system power balance. The maximum LED power is equal to $V_{LED(max)} \times I_{LED(max)}$. $I_{LED(max)}$ is the maximum LED current when the LED current PWM signal is continuously LOW. $V_{LED(max)}$ is the voltage across the LED string when biased with $I_{LED(max)}$.

The optimum values of the LED current, the boost output capacitor C_{bus}, and the coil current sensing resistor R_{ICBST} can be calculated with Equation 2 and Equation 3:

$$\frac{I_{LED}}{C_{bus}} = \frac{0.2\ A}{330\ \mu F} \tag{2}$$

$$R_{ICBST} \times C_{bus} = 0.24\ \Omega \times 330\ \mu F \tag{3}$$

8.8 Protection circuits

Several protection circuits are integrated to protect the device and the application against defects.

The SSL3401HN embedded protection circuits are:

- OverVoltage Protection (OVP)
- Coil Current Limitation (CCL)
- OverTemperature Protection (OTP)
- Open LED protection (OLED)
- Shorted LED protection (SLED)
- Power-On Reset protection (POR)

8.8.1 Overvoltage protection

Every 41.667 µs, the OVP detector checks if the voltage on the OVP pin exceeds a preset threshold $V_{th(ovp)}$.

If the voltage on the OVP pin exceeds $V_{th(OVP)}$, the boost converter is disabled. Normal operation is resumed once the voltage on the OVP pin drops to < $V_{th(ovp)} - V_{ovp(hys)}$. When OVP is active, the feedback loops and the LED current control are frozen.

8.8.2 Coil current limitation

The device is equipped with a peak coil current limiting function to avoid excessive current in the inductor.

The voltage on the ACMPREF pin is limited. The limitation ensures that the average coil current does not exceed $I_{lim(L)M}$ = 1.1 A * 200 mΩ / R_{ICBST}. The coil current limitation disregards the latching current. Thus, if a latching current is set, the maximum coil current equals $I_{lim(L)M}$ plus the input latching current.

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8.8.3 Overtemperature protection

During normal operation, at an ambient temperature up to 100 °C, the die temperature must not exceed 105 °C. SSL3401HN features a temperature roll-back protection to maintain the maximum temperature to a predefined set point by adjusting the LED current.

Internally, the IC senses the junction temperature of the die every 10 ms for a 50 Hz supply and 8.3 ms for a 60 Hz supply. A feedback loop decreases the LED current by adjusting the LED PWM control signal to maintain the junction temperature at a maximum value of 20 °C below the OTP threshold. The maximum LED current reduction is 80 % of its maximum value during normal operation.

If the chip temperature exceeds the predefined OTP threshold, the protection is triggered. The boost converter is disabled and the LED PWM signal is set HIGH to shut down the LED current immediately. Once the OTP is triggered, normal operation resumes only when the chip temperature drops 30 °C below the OTP threshold.

The OTP, fallback, and recovery thresholds can be set via external resistors. Table 5 gives the OTP threshold value as a function of the output voltage of the OTP setting resistor divider: $V_{set(otp)} = (V_{DD} \times RSET2/(RSET2 + RSET1))$.

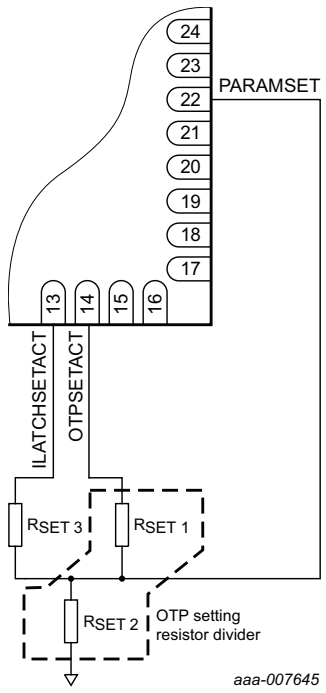


Fig 6. OTP threshold setting

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Table 5. OTP threshold setting

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{set(otp)}$	overtemperature protection setting voltage	OTP = 120.0 °C; V_{DD} = 3.3 V	0	-	0.20	V
		OTP = 107.5 °C; V_{DD} = 3.3 V	0.20	-	0.41	V
		OTP = 110.0 °C; V_{DD} = 3.3 V	0.41	-	0.61	V
		OTP = 112.5 °C; V_{DD} = 3.3 V	0.61	-	0.82	V
		OTP = 115.0 °C; V_{DD} = 3.3 V	0.82	-	1.03	V
		OTP = 117.5 °C; V_{DD} = 3.3 V	1.03	-	1.23	V
		OTP = 122.5 °C; V_{DD} = 3.3 V	1.23	-	1.54	V
		OTP = 125.0 °C; V_{DD} = 3.3 V	1.54	-	1.85	V
		OTP = 127.5 °C; V_{DD} = 3.3 V	1.85	-	2.16	V
		OTP = 130.0 °C; V_{DD} = 3.3 V	2.16	-	2.47	V
		OTP = 120.0 °C; V_{DD} = 3.3 V	2.47	-	V_{DD}	V

8.8.4 Open LED protection

Open LED protection works in combination with the OVP protection. If the LED string is open, the boost output voltage increases until OVP is triggered (see Section 8.8.1).

8.8.5 Shorted LED protection

The protection is triggered if the voltage on pin FB continuously exceeds 2.1 V for a time period > 500 ms. This voltage is measured every 10 ms for 50 Hz (AC or DC supply) and every 8.3 ms for 60 Hz (AC). The boost converter is disabled and the LED PWM signal is set HIGH to switch off the LED current source. Normal operation is only resumed after a POR or a chip reset by setting the $\overline{\text{RESET}}$ pin to LOW.

8.8.6 Power-on reset

A voltage supervisor constantly monitors the supply to pin V_{DD}. If the voltage on pin V_{DD} drops below the falling POR threshold level, the chip enters the Reset state and cannot operate.

The chip enters Active mode when the voltage on pin V_{DD} exceeds the POR rising threshold value.

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8.9 LED selection

The LED forward voltage is crucial to obtaining the full dimmer and transformer compatibility performance. An LED voltage that is too low may cause transient short between the input voltage and the boost output voltage, which affects the light stability.

Use an LED with a typical forward voltage of > 26.6 V, at the actual application maximum LED current and an LED junction temperature of 80 °C. This same minimum LED voltage limit becomes 27.7 V if the measurement point is a junction temperature of 25 °C. Included in the calculation are:

- Temperature derating
- Aging effect
- V_f spread = −10 %
- Mains voltage variation = +10 %
- Transformer output voltage spread = +10 %

Only the application component rating and/or thermal dissipation constraints determine the LED voltage upper limit.

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9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)		[2]	–0.5	4.6	V
$V_{DD(IO)}$	input/output supply voltage		[2]	–0.5	4.6	V
V_I	input voltage	5 V tolerant I/O; pins: $\overline{\text{RESET}}$, LOADPWM, GAINSETACT, OTPSETACT, LEDPWM, LEDSDWN, BSTDRVA, and BSTDRVB; only valid when the $V_{DD(IO)}$ is present		–0.5	+5.5	V
		3 V tolerant I/O; pins without overvoltage protection: ACMPREF, OVP		–0.5	+3.6	V
V_{ia}	analog input voltage	pins ACMPP, ACMPN, and PARAMSET	[3][4] [5]	–0.5 V	4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{lu}	latch-up current	$-(0.5\ V_{DD(IO)}) < V_I < (1.5\ V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{amb}	ambient temperature	operating		0	105	°C
T_{stg}	storage temperature			–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[6]	–2000	+2000	V
		charge device model; all pins	[7]	–500	+500	V

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Table 6. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{act(ov)ESD}$	ESD overvoltage activation voltage	for LVTSCR-based ESD pin protection	[8]			
		1 ns to 10 ns rise time		8.2	-	V
		> 10 ns rise time		> 8.5	-	V
latch-up			[9]	-	-	-

[1] The following applies to the limiting values:

a) This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, take conventional precautions to avoid applying static charge > the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 7) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] An ADC input voltage exceeding 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[4] If the comparator is configured with the common-mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[5] Connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[7] Charge device model: Equivalent to charging the IC up to 1 kV and the subsequent discharging of each pin down to 0 V over a 1 Ω resistor.

[8] Not characterized.

[9] In accordance with NX4-00100.

10. Static characteristics

Table 7. Static characteristics

T_{amb} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)			2.6	3.3	3.6	V
$V_{DD(IO)}$	input/output supply voltage			2.6	3.3	3.6	V
I_{DD}	supply current	$V_{DD(3V3)} = V_{DD(IO)} = 3.3$ V			10		mA
Pin RESET							
I_{IL}	LOW-level input current	$V_I = 0$ V;					
		2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		–15	–50	–85	µA
		$V_{DD(IO)} < V_I < 5$ V		0	0	0	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$;		-	0.5	1000	nA
V_I	input voltage	pin configured to provide a digital function; 5 V tolerant pins	[2]	0	-	5.0	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V

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Table 7. Static characteristics *...continued*

T_{amb} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{hys}	hysteresis voltage	3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		0.4	-	-	V
Pins LOADPWM, GAINSETACT, OTPSETACT, LEDPWM, LEDSDWN							
V_I	input voltage	pin configured to provide a digital function; 5 V tolerant pins	[2]	0	-	5.0	V
V_O	output voltage			0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; I_{OH} = −4 mA		0.85$V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.15$V_{DD(IO)}$	V
I_{OH}	HIGH-level output current	V_{OH} = $V_{DD(IO)}$ − 0.4 V; 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		4	-	-	mA
$I_{O(sc)H}$	HIGH-level short-circuit output current	V_{OH} = 0 V	[3]	-	-	−45	mA
$I_{O(sc)L}$	LOW-level short-circuit output current	V_{OL} = $V_{DD(IO)}$	[3]	-	-	50	mA
Pins BSTDRVA, BSTDRVB							
I_{IL}	LOW-level input current	V_I = 0 V;		−15	−50	−85	µA
I_{IH}	HIGH-level input current	V_I = $V_{DD(IO)}$; 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		-	0.5	1000	nA
V_O	output voltage			0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; I_{OH} = −4 mA		0.85$V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.15$V_{DD(IO)}$	V
I_{OH}	HIGH-level output current	V_{OH} = $V_{DD(IO)}$ − 0.4 V; 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 2.6 V ≤ $V_{DD(IO)}$ ≤ 3.6 V		4	-	-	mA
$I_{O(sc)H}$	HIGH-level short-circuit output current	V_{OH} = 0 V	[3]	-	-	−45	mA
$I_{O(sc)L}$	LOW-level short-circuit output current	V_{OL} = $V_{DD(IO)}$	[3]	-	-	50	mA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

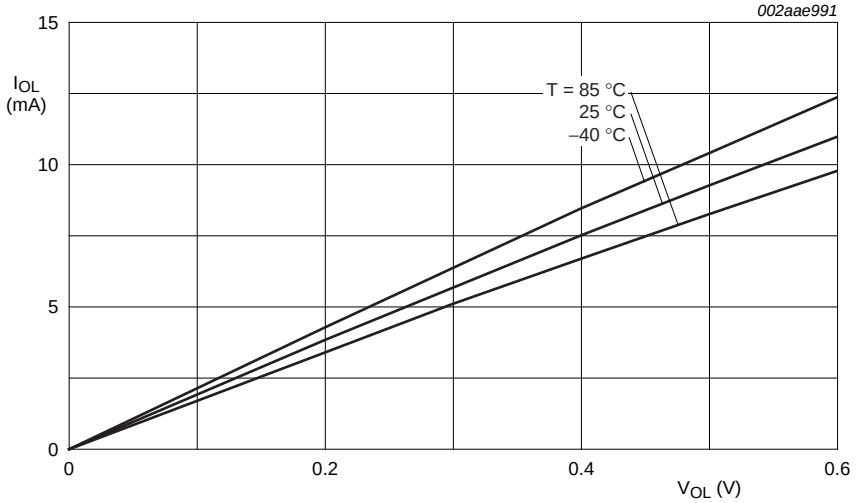
[2] All supply voltages must be present.

[3] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

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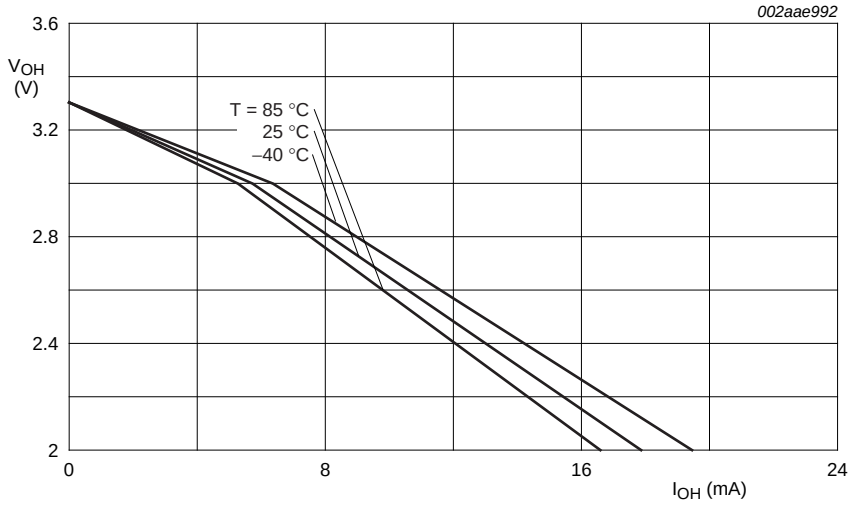
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10.1 Electrical pin characteristics



Conditions: $V_{DD(IO)}$ = 3.3 V

Fig 7. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: $V_{DD(IO)}$ = 3.3 V; standard port pins.

Fig 8. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

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11. Dynamic characteristics

11.1 Power supply fluctuations

If the input voltage ($V_{DD(3V3)}$) to the internal regulator fluctuates, the SSL3401HN is held in reset during a brownout condition as long as the UVLO circuit is operating. The settling times of the BOD and POR circuits, which constitute the UVLO, determine the minimum time the supply level must remain in the shallow or deep brownout condition to ensure that the internal reset is asserted properly.

Table 8. UVLO circuits settling characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_s	settling time	power drop:				
		from active level to shallow brownout level; ($0.9\ V \leq V_{DD(3V3)} \leq 2.4\ V$)	5	-	-	µs
		from active level to deep brownout level ($0 < V_{DD(3V3)} < 0.9\ V$)	12	-	-	µs

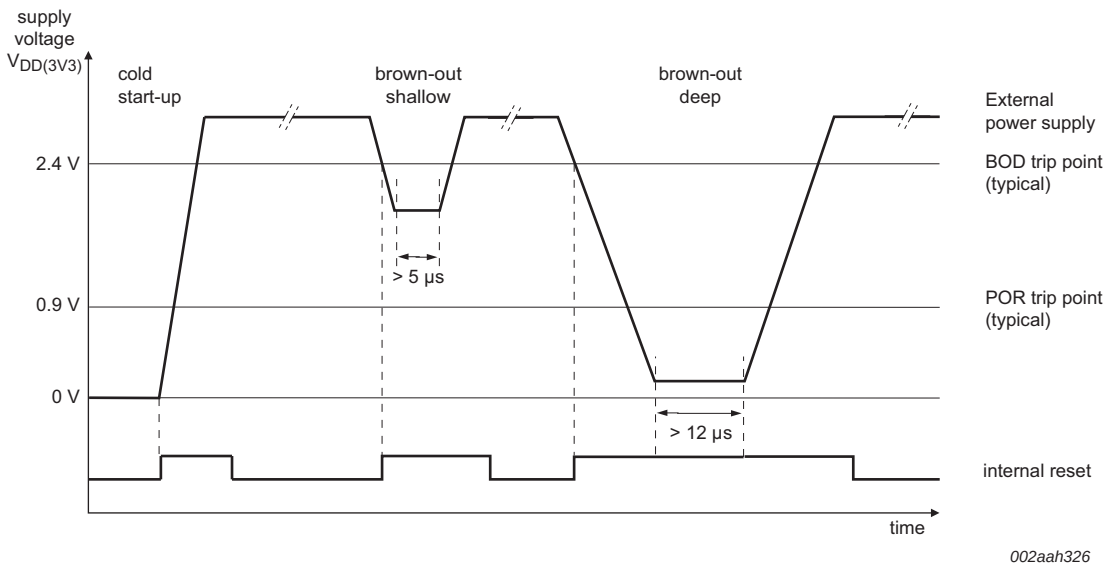


Fig 9. UVLO timing

11.2 I/O pins

Table 9. Dynamic characteristic: digital I/O pins[1]

T_{amb} = 25 °C; 3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; load capacitor = 30 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time		2.5	-	5.0	ns
t_f	fall time		2.0	-	4.5	ns

[1] Simulated results.

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12. Analog characteristics

Table 10. BOD static characteristics

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	assertion	-	2.52	-	V
		deassertion	-	2.66	-	V

Table 11. ADC static characteristics

T_{amb} = 35 °C unless otherwise specified; $V_{DD(3V3)}$ = 2.7 V to 3.6 V; V_{SS} = 0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		0	-	$V_{DD(3V3)}$	V
C_i	input capacitance		-	-	4	pF
R_i	input resistance		-	415	-	kΩ

Table 12. DAC static and dynamic characteristics

$V_{DD(3V3)}$ = 2.7 V to 3.6 V; T_{amb} = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_L	load capacitance		-	-	200	pF
R_L	load resistance		1	-	-	kΩ
R_O	output resistance		-	< 40		Ω
t_s	settling time		-	-	1	µs
V_O	output voltage	output voltage range with less than 1 LSB deviation; with minimum R_L connected to ground or power supply	0.3	-	$V_{DD(3V3)}$ − 0.3	V
		with minimum R_L connected to ground or power supply	0.175	-	$V_{DD(3V3)}$ − 0.175	V

Table 13. Comparator characteristics

$V_{DD(3V3)}$= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{I(cm)}$	common-mode input voltage		0	-	$V_{DD(3V3)}$	V
ΔV_O	output voltage variation		0	-	$V_{DD(3V3)}$	V
V_{offset}	offset voltage	V_{IC} = 0.1 V	-	−4 to +4.2	-	mV
		V_{IC} = 1.5 V	-	±2	-	mV
		V_{IC} = 2.8 V	-	±2.5		mV

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Table 13. Comparator characteristics *…continued*

$V_{DD(3V3)}$= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
t_{PD}	propagation delay	HIGH to LOW; $V_{DD(3V3)}$ = 3.0 V	[1]				
		V_{IC} = 0.1 V; 50 mV overdrive input		-	129	140	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	112	130	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	151	170	ns
		LOW to HIGH; $V_{DD(3V3)}$ = 3.0 V;	[1]				
		V_{IC} = 0.1 V; 50 mV overdrive input		-	232	240	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	210	230	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	166	190	ns
V_{hys}	hysteresis voltage	comparator; positive hysteresis; V_{ACMPx} = 1.5 V	[2]				
		Pin HYSTSET set HIGH or not connected		-	20	-	mV
		Pin HYSTSET set LOW		-	10	-	mV
		comparator; negative hysteresis; V_{ACMPx} = 1.5 V					
		Pin HYSTSET set HIGH or not connected		-	−20	-	mV
		Pin HYSTSET set LOW		-	−10	-	mV

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = −40 °C to +85 °C.

[2] Input hysteresis is relative to the reference input channel.

Table 14. Protection characteristics

$V_{DD(3V3)}$= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{lim(L)M}$	peak inductor current limit	240 mΩ coil current sensing resistor; latching current disabled	-	1.7	-	A
$V_{th(scp)LED}$	LED short-circuit protection threshold voltage	pin FB		1.8		V
$t_{prot(sc)LED}$	LED short-circuit protection time	voltage at pin FB continuously exceeding $V_{th(sledp)}$; 50 Hz AC supply	-	500	-	ms
$V_{th(ovp)}$	overvoltage protection threshold voltage	pin OVP	-	1.9	-	V
$V_{ovp(hys)}$	overvoltage protection voltage hysteresis	pin OVP		0.55		V
$T_{act(th_fold)}$	thermal foldback activation temperature	die junction temperature	-	105	-	°C
$T_{th(otp)}$	overtemperature protection threshold temperature	die junction temperature	-	125	-	°C

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13. Application information

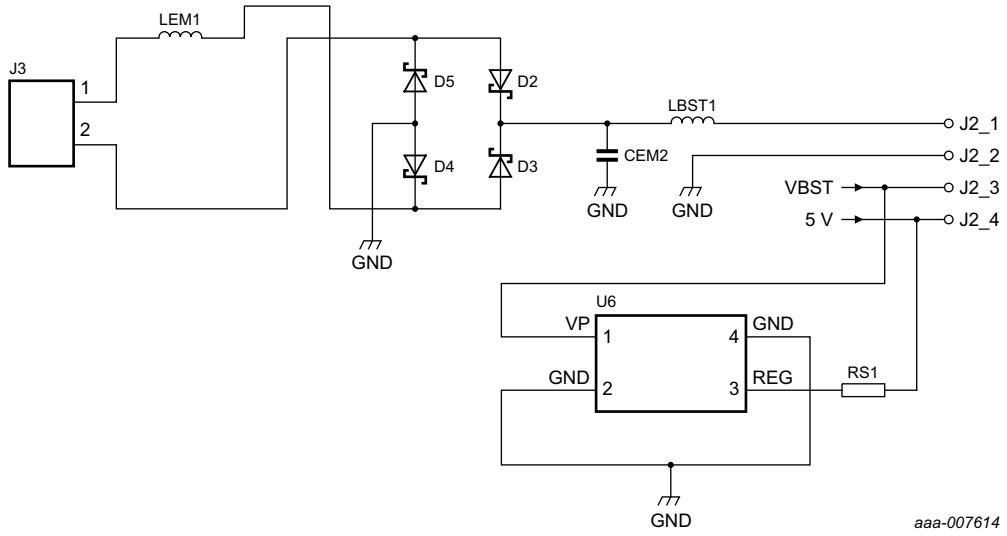


Fig 10. Application diagram - input stage

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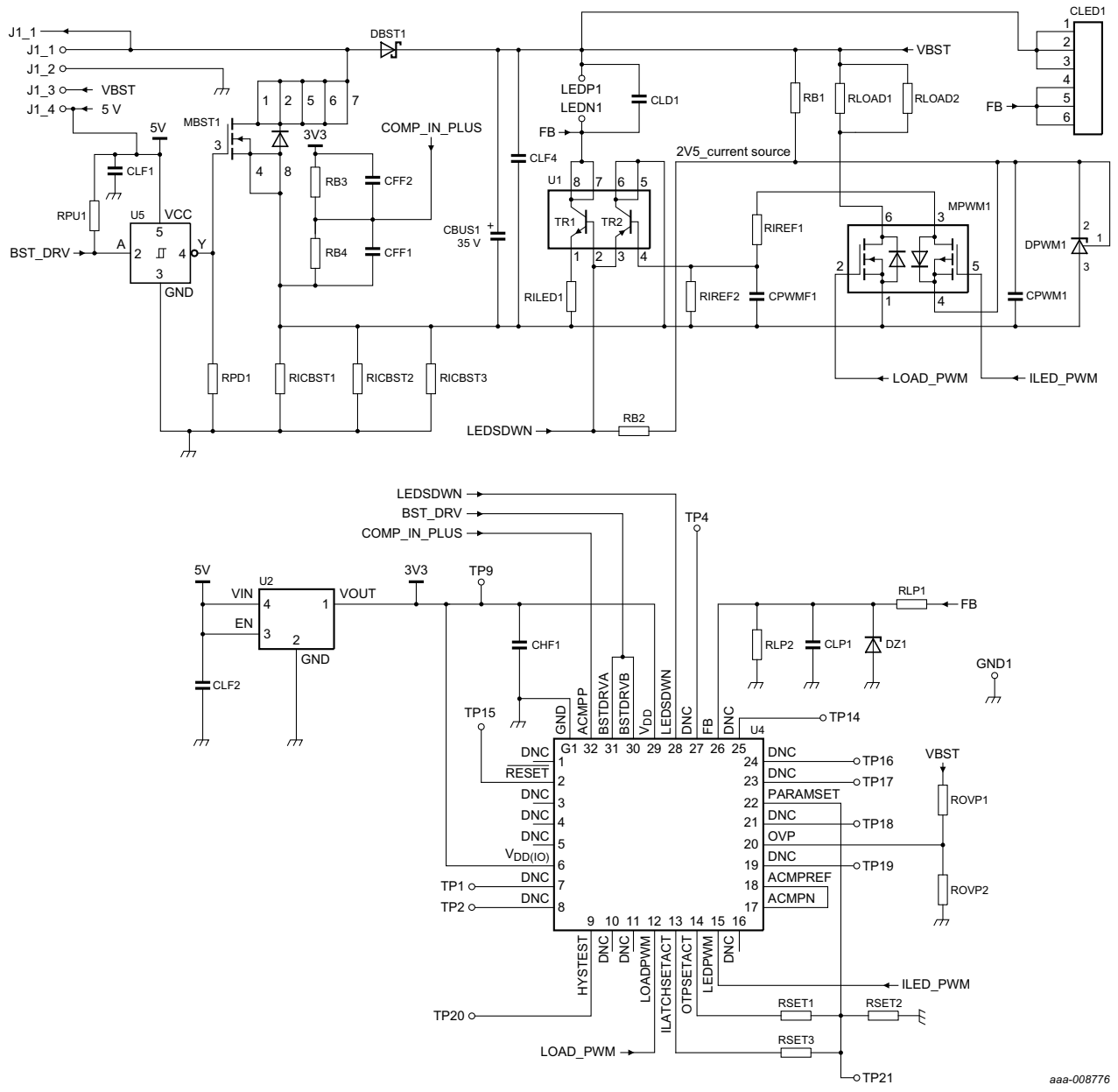


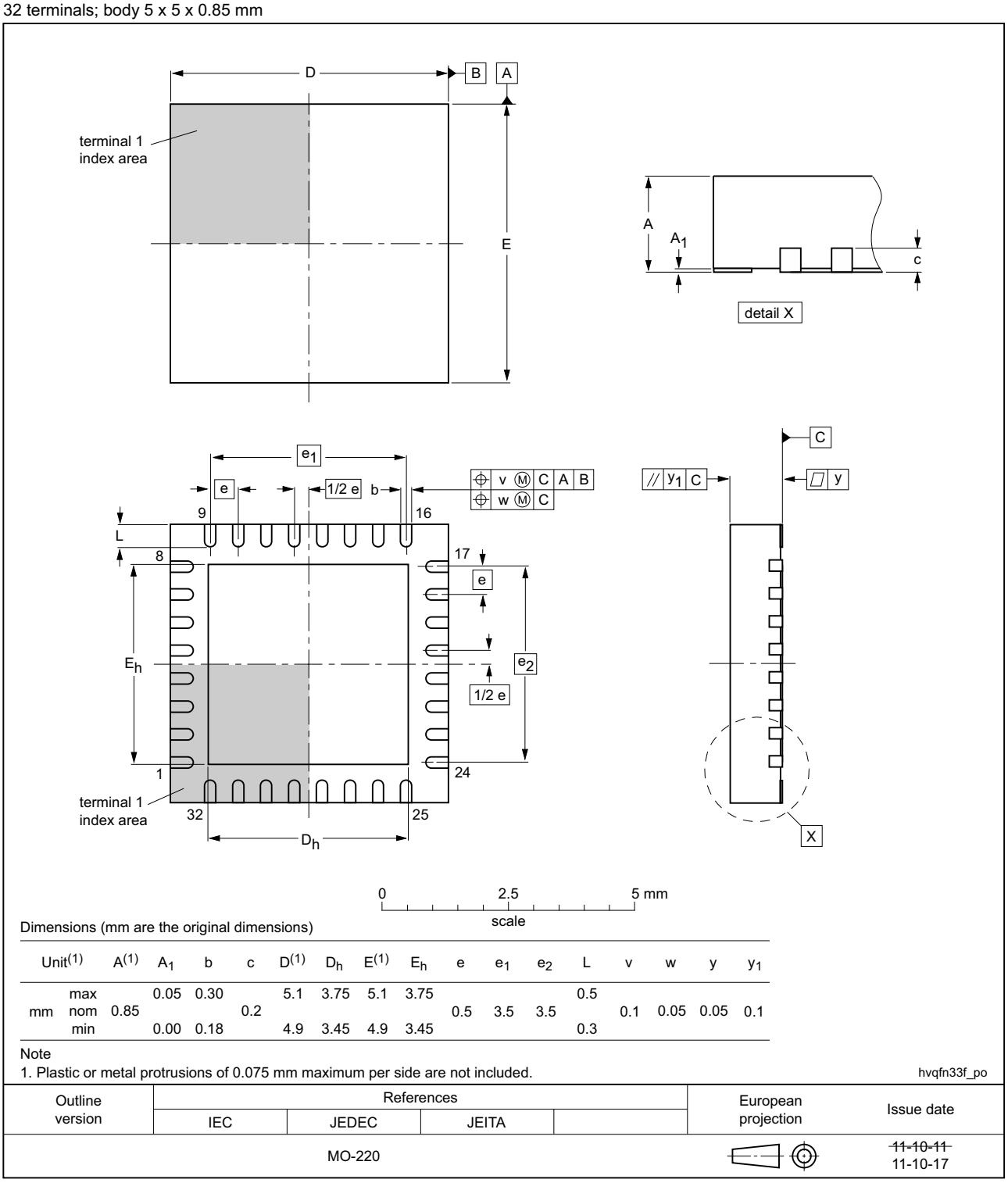
Fig 11. Application diagram - boost part and IC part

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14. Package outline

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads;
32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

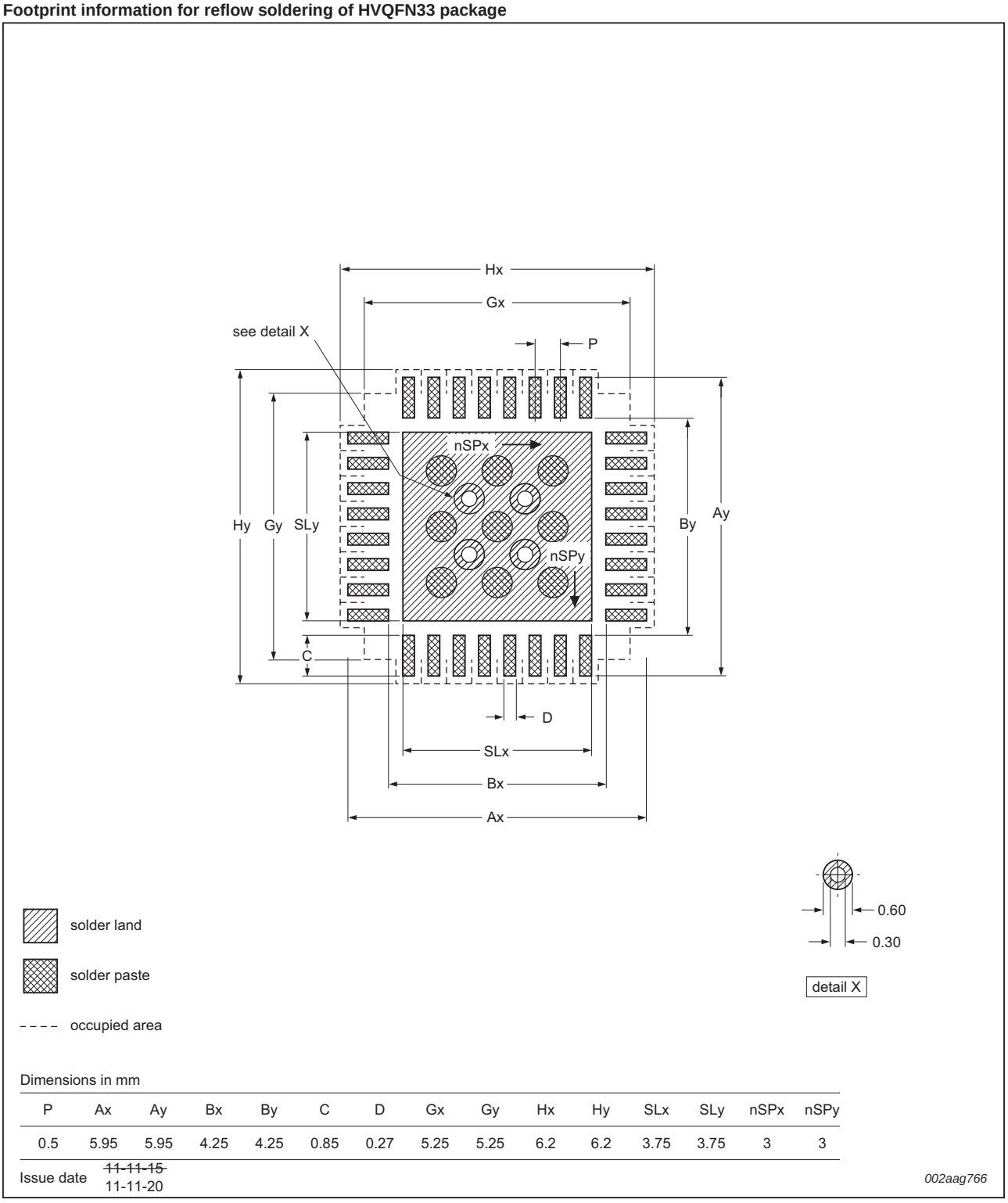
Fig 12. Package outline HVQFN33

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15. Soldering

Footprint information for reflow soldering of HVQFN33 package



Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

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Fig 13. Reflow soldering of the HVQFN33 (5x5) package

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16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SSL3401HN v.2	20140128	Product data sheet	-	SSL3401HN v.1.1
Modifications:	• The data sheet status has changed from Preliminary to Product.			
SSL3401HN v.1.1	20131118	Preliminary data sheet	-	SSL3401HN v.1
SSL3401HN v.1	20131023	Preliminary data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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