SSF1030

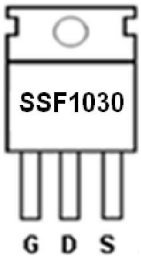
100V N-Channel MOSFET

Main Product Characteristics

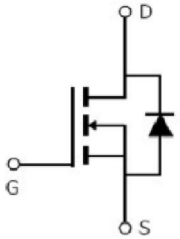
V_{DSS}	100V
R_{DS}(on)	20.5mΩ (typ.)
I_D	45A ①



TO-220



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175℃ operating temperature
- Lead free product

Description

These N-Channel enhancement mode power field effect transistors are produced using proprietary MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	45 ①	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V	32 ①	
I_{DM}	Pulsed Drain Current ②	180	
P_D @TC = 25°C	Power Dissipation ③	163	W
	Linear Derating Factor	1.08	W/°C
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.27mH	88	mJ
I_{AS}	Avalanche Current @ L=0.27mH	25.5	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C

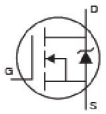
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	0.92	°C/W
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	°C/W

Electrical Characteristics @T_A=25℃ unless otherwise specified

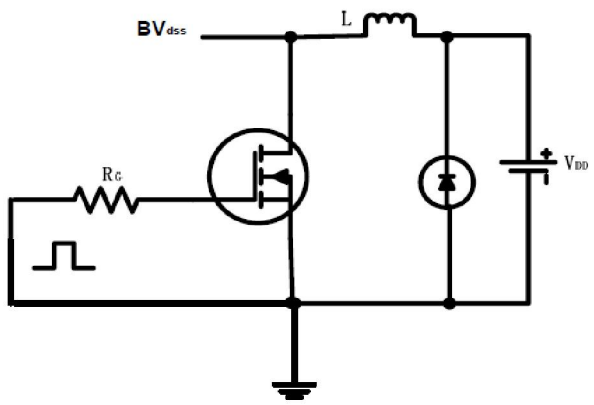
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	100	—	—	V	V_{GS} = 0V, I_D= 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	20.5	22	mΩ	V_{GS}=10V,I_D =30A
		—	44.4	—		T_J = 125°C
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
		—	2.56	—		T_J = 125°C
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} =100V,V_{GS} = 0V
		—	—	50		T_J = 125°C
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} =20V
		—	—	-100		V_{GS} = -20V
Q_g	Total gate charge	—	46.3	—	nC	I_D = 30A,
Q_{gs}	Gate-to-Source charge	—	12.0	—		V_{DS}=30V,
Q_{gd}	Gate-to-Drain("Miller") charge	—	16.9	—		V_{GS} = 10V
$t_{d(on)}$	Turn-on delay time	—	13.9	—	nS	V_{GS}=10V, V_{DD} =30V,
t_r	Rise time	—	13.2	—		R_L=15Ω,
$t_{d(off)}$	Turn-Off delay time	—	37.8	—		R_{GEN}=2.55Ω
t_f	Fall time	—	11.1	—		I_D =2A
C_{iss}	Input capacitance	—	2042	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	144	—		V_{DS} = 25V
C_{rss}	Reverse transfer capacitance	—	114	—		f = 1MHz

Source-Drain Ratings and Characteristics

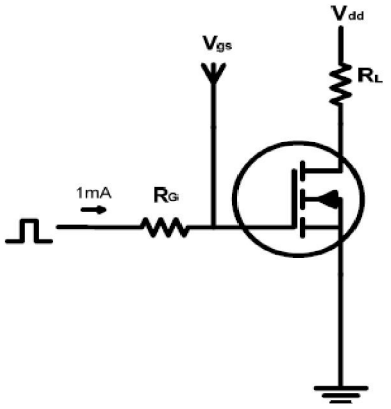
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	60 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	240	A	
V_{SD}	Diode Forward Voltage	—	0.91	1.3	V	I_S=30A, V_{GS}=0V, T_J = 25°C
t_{rr}	Reverse Recovery Time	—	45.1	—	nS	T_J = 25°C, I_F =30A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	101	—	nC	

Test Circuits and Waveforms

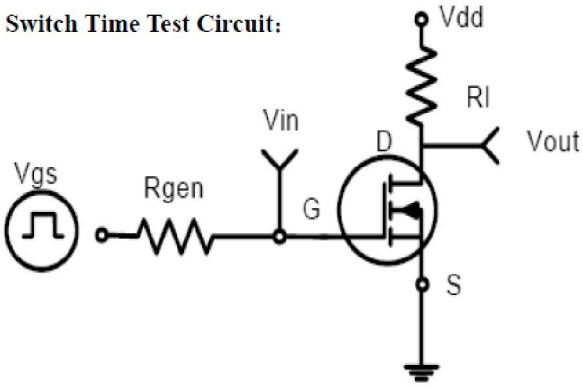
EAS test circuits:



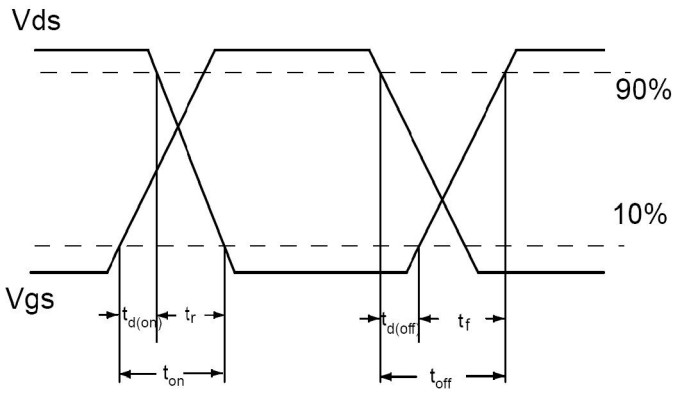
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Notes:

①Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

Typical Electrical and Thermal Characteristics

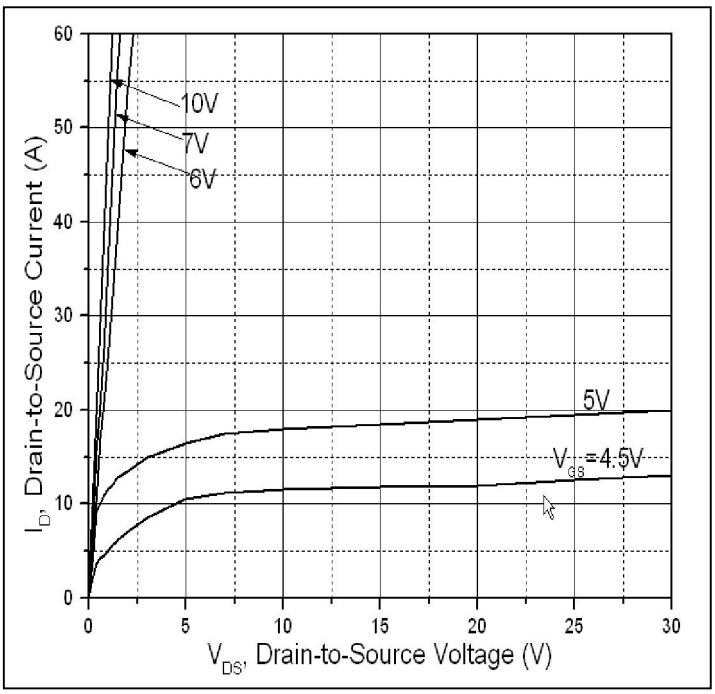


Figure 1: Typical Output Characteristics

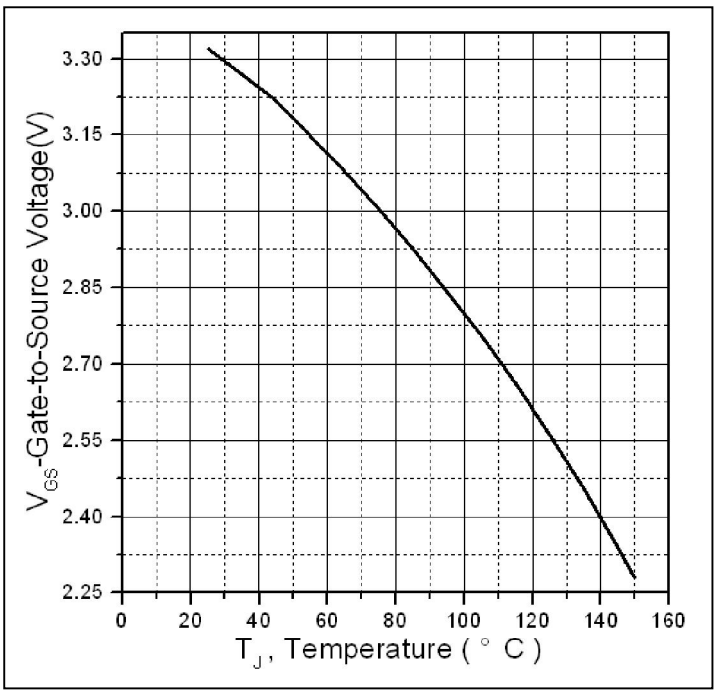


Figure 2. Gate to source cut-off voltage

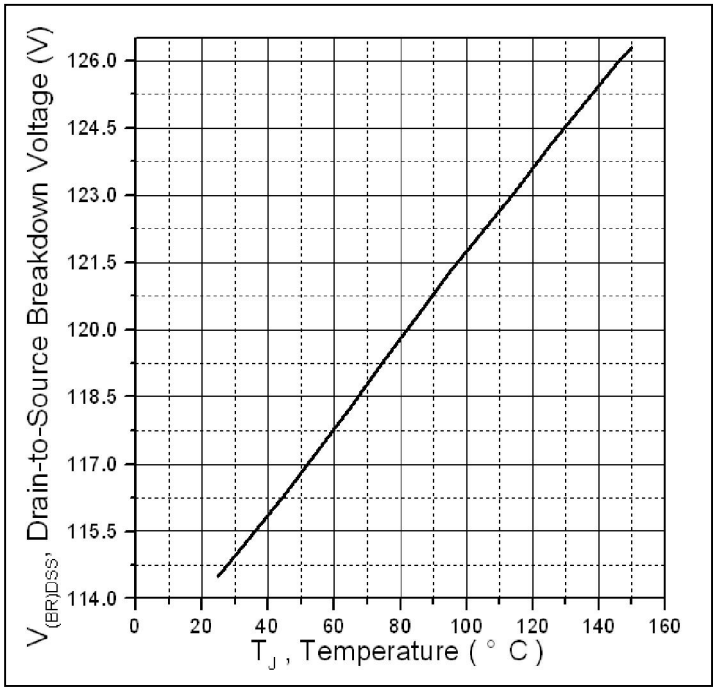


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

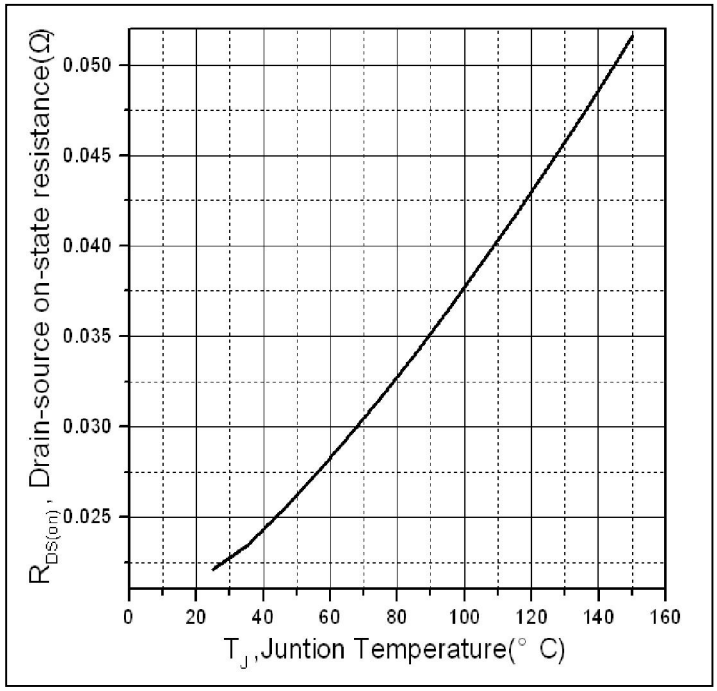


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristics

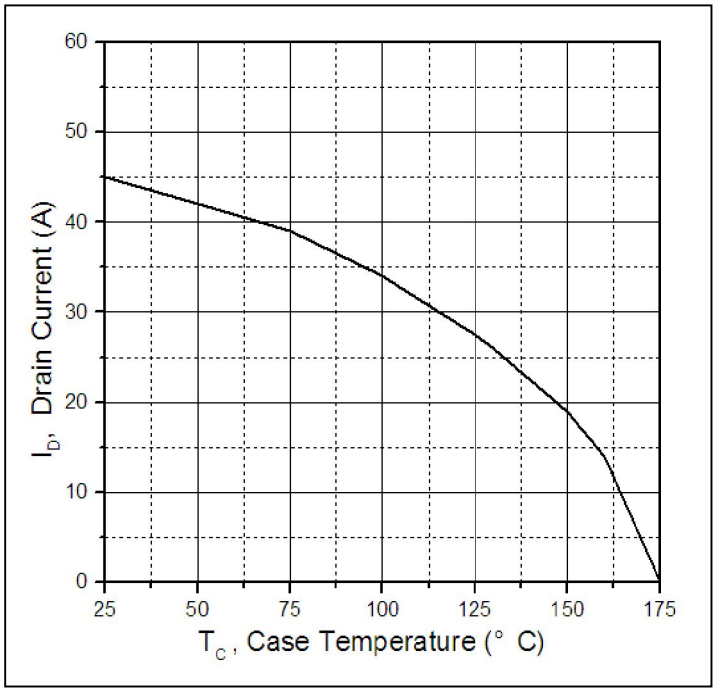


Figure 5. Maximum Drain Current Vs. Case Temperature

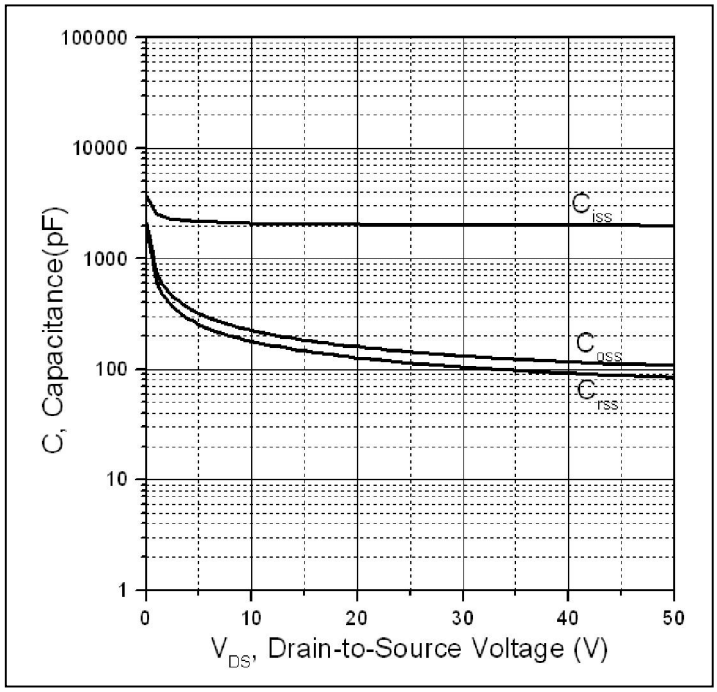


Figure 6.Typical Capacitance Vs. Drain-to-Source Voltage

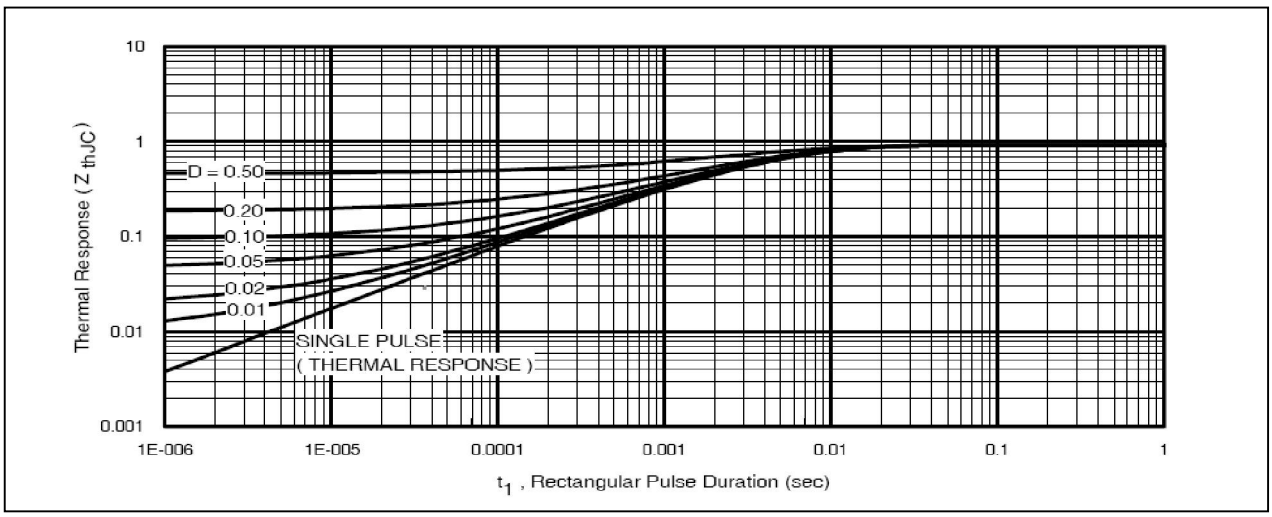
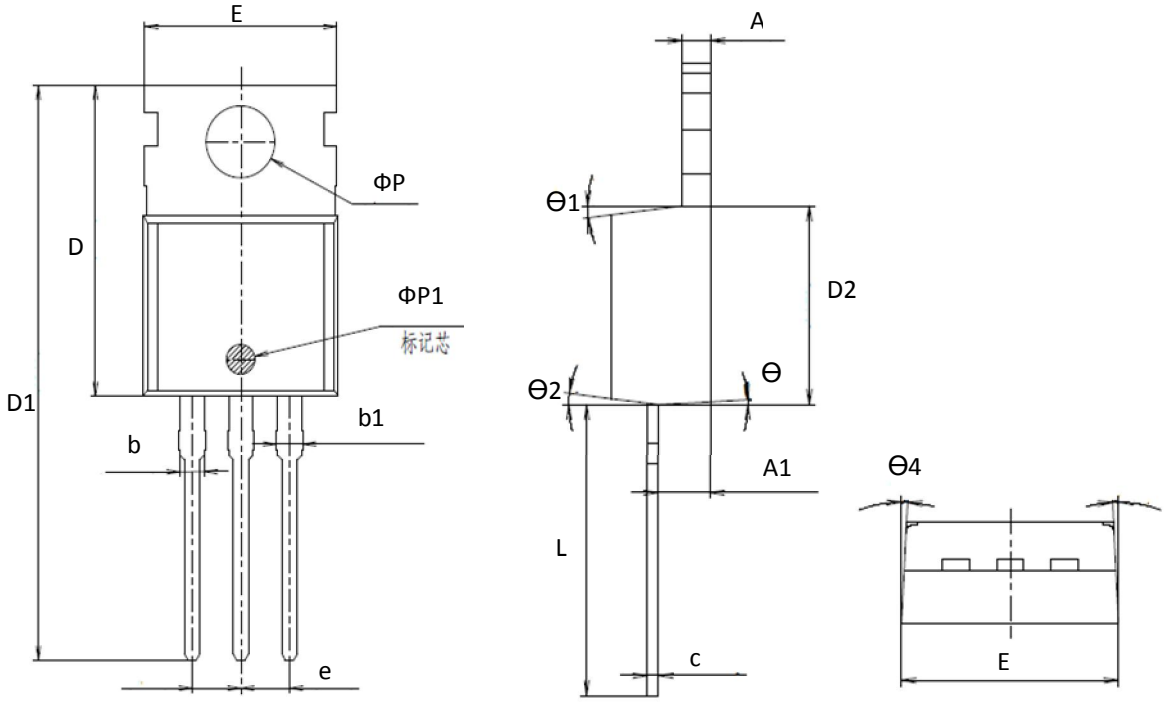


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data

TO-220 PACKAGE OUTLINE DIMENSION_GN



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	1.300	-	-	0.051	-
A1	2.200	2.400	2.600	0.087	0.094	0.102
b	-	1.270	-	-	0.050	-
b1	1.270	1.370	1.470	0.050	0.054	0.058
c	-	0.500	-	-	0.020	-
D	-	15.600	-	-	0.614	-
D1	-	28.700	-	-	1.130	-
D2	-	9.150	-	-	0.360	-
E	9.900	10.000	10.100	0.390	0.394	0.398
E1	-	10.160	-	-	0.400	-
ΦP	-	3.600	-	-	0.142	-
ΦP1		1.500			0.059	
e		2.54BSC			0.1BSC	
L	12.900	13.100	13.300	0.508	0.516	0.524
Θ1	-	7^0	-	-	7^0	-
Θ2	-	7^0	-	-	7^0	-
Θ3	-	3^0	-	5^0	7^0	9^0
Θ4	-	3^0	-	1^0	3^0	5^0

Ordering and Marking Information

Device Marking: SSF1030

Package (Available)

TO-220

Operating Temperature Range

C : -55 to175 ºC

Devices per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 175℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=125℃ or 175℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices