LVDS

SR-A2D30 Series

PATENT PENDING

Description

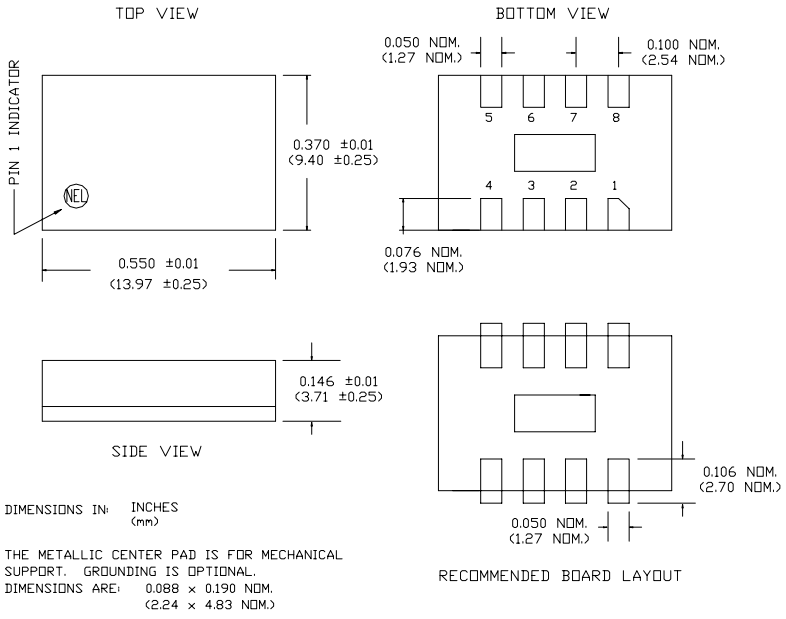
The **SR-A2D30 Series** of quartz crystal oscillators provides a LVDS compatible signal. This device uses multiple ground pins for improved signal integrity.

Features

- Wide frequency range - 250.0MHz to 750.0MHz
- Patent Pending, harmonic multiplication for extremely low jitter
- High frequency output eliminates the need for PLL multiplication
- Stabilities over temperatures as low as ±20ppm eliminates SAW oscillator temperature problems
- 3.3V and 2.5V version available
- High Reliability - NEL HALT/HASS qualified for crystal oscillator start-up conditions
- User specified tolerance available
- Cover connected to ground
- Will withstand SMD reflow temperatures of 183°C for 4 minutes maximum
- High shock resistance, to 1000g

Electrical Connection

Pin	Connection
1	V_{CC}
2	Ground
3	NC or Ground
4	Q Output
5	/Q Output
6	Ground
7	Ground
8	Enable



NEL FREQUENCY CONTROLS, INC.

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SR-A2D30 Series Continued
LVDS

Rev. B

Operating Conditions and Output Characteristics

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Frequency	-----	-----	250.0MHz	-----	750.0MHz
Duty Cycle(1)	-----	@ 50% points	45/55%	-----	55/45%
Logic 0 (1)	V_{OL}	-----	0.925V	-----	-----
Logic 1(1)	V_{OH}	-----	-----	-----	1.474V
Differential Voltage Swing(1)	$V_{DIFF-OUT}$	-----	500mV	700mV	-----
Rise & Fall Time (1)	tr,tf	20-80%V_O	-----	-----	300 psec
RMS Random Jitter(5)	-----	-----	-----	-----	1 psec
Enable Voltage(2)	----	with V_{EE}=0V	-----	-----	0.8V
Disable Voltage	-----	with V_{EE}=0V	2.0V	-----	-----
Frequency Stability(3)	dF/F	Overall conditions including: voltage, calibration, temp., 10 yr aging, shock, vibration	-100ppm	-----	+100ppm
Phase Noise(4)	-----	@100Hz	-----	-----	-80 dBc/Hz
	-----	@1kHz	-----	-----	-115 dBc/Hz
	-----	@10kHz	-----	-----	-130 dBc/Hz
	-----	@100kHz	-----	-----	-130 dBc/Hz
	-----	@1MHz	-----	-----	-135 dBc/Hz
	-----	@10MHz	-----	-----	-135 dBc/Hz

General Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Supply Voltage	V_{CC}	3.3V±5%	3.135V	3.3V	3.465V
Supply Current	I_{CC}	-----	0.0 mA	-----	120 mA
Output current	I_O	Low level Output Current	0.0 mA	-----	±50.0 mA
Operating temperature	T_A	------	0°C	-----	70°C
Storage temperature	T_S	-----	-55°C	-----	125°C
Input: Logic High (ECL) - Disables V_{EE} or Open - Enables					
Lead temperature	T_L	Soldering, 10 sec.	-----	-----	300°C
Load	50 Ohm to V_{CC}-2V or Thevenin Equivalent, Bias Required				
Start-up time	t_S	-----	-----	2 ms	10 ms

Environmental and Mechanical Characteristics

Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Thermal Shock	Per MIL-STD-833, Method 1011, Condition A
Vibration	0.060" double amplitude 10 Hz to 55 Hz, 35g's 55Hz to 2000 Hz
Soldering Condition	300°C for 10 seconds

Footnotes:
1) With load of 100 ohms across differential outputs.
2) Open to Enable pin also enables the output.
3) Standard frequency stability (others available)
4) Phase Noise characterization available. Phase Noise is frequency dependant, phase noise specification references a 1.0GHz part.
5) RMS jitter bandwidth of 12kHz to 20MHz

Creating a Part Number

SR - A2D3X - FREQ

Package Code
SR 8 pad 9x14mm SMD

Input Voltage

Code	Specification
A	3.3V
B	2.5V

Tolerance/Performance

0	±100ppm 0-70°C
1	±50ppm 0-70°C
7	±25ppm 0-70°C
9	Customer Specific
A	±20ppm 0-70°C
B	±50ppm -40 to +85°C
C	±100ppm -40 to +85°C

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