

FEATURES

- 400 MWPS nominal conversion rate
- RS-343-A compatible
- Complete video controls: Sync, Blank, Bright and Reference White (Force High)
- 10 KH, 100K ECL compatible
- Single power supply
- Registered data and video controls
- Differential current outputs
- Stable on-chip bandgap reference
- 50 and 75 ohm output drive
- ESD-protected data and control inputs

APPLICATIONS

- Raster graphics
- High-resolution color or monochrome displays to 2k x 2k pixels
- Medical electronics: CAT, PET, MR imaging displays
- CAD/CAE workstations
- Solids modeling
- General-purpose high-speed D/A conversion
- Digital synthesizers
- Automated test equipment
- Digital transmitters/modulators

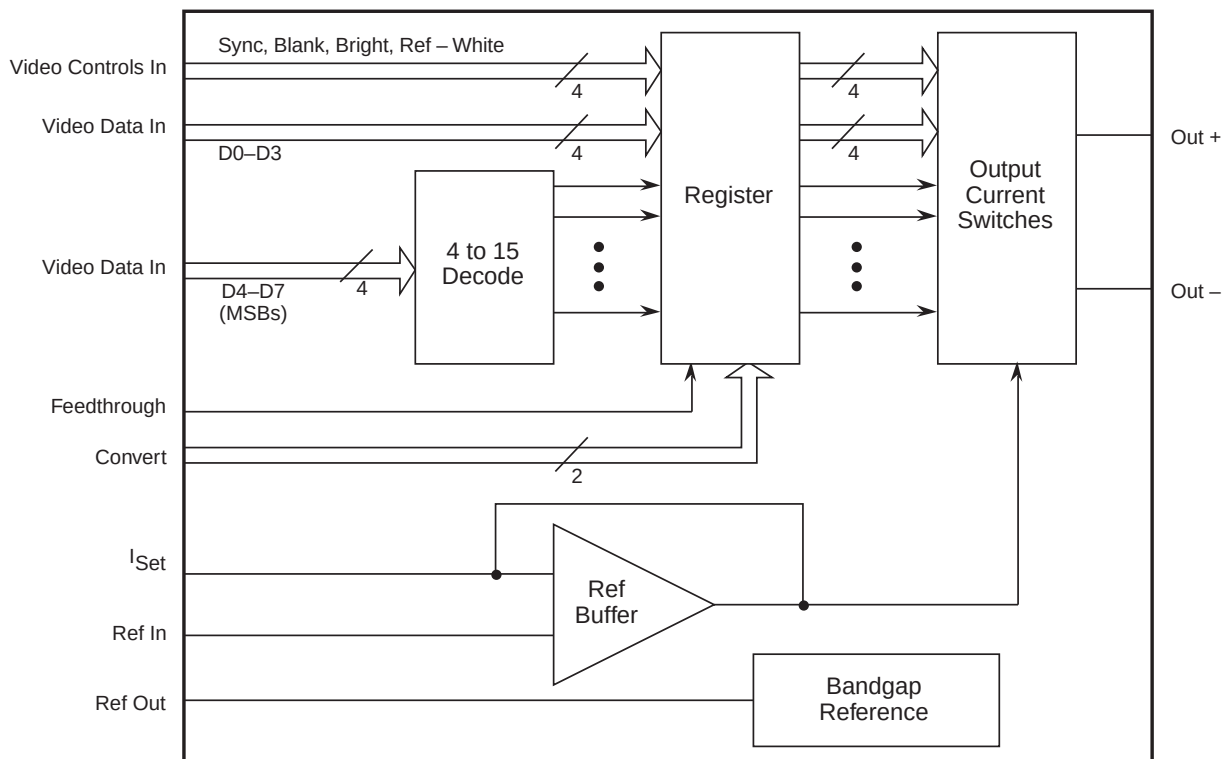
GENERAL DESCRIPTION

The SPT5140 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at 400 MWPS. Complete with video controls — Sync, Blank, Reference White (Force High), Bright — the SPT5140 directly drives doubly-terminated 50 or 75 ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The

SPT5140 includes an internal precision bandgap reference which can drive two other SPT5140s in an RGB graphics system.

The SPT5140 is available in a 24-lead PDIP package in the industrial temperature range of -25°C to $+85^{\circ}\text{C}$. Contact the factory for military temperature and /883 versions.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25 °C

Supply Voltages

V_{EE} (measured to V_{CC}) –7.0 to 0.5 V

Input Voltages

CONV, Data, and Controls V_{EE} to 0.5 V
(measured to V_{CC})

Ref+ (measured to V_{CC}) V_{EE} to 0.5 V

Ref– (measured to V_{CC}) V_{EE} to 0.5 V

Temperature

Operating, ambient –25 to +85 °C

junction + 175 °C

Lead, soldering (10 seconds) + 300 °C

Storage –60 to + 150 °C

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

V_{CC} = ground, V_{EE} = –5.2 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, C_C = 0 pF, I_{Set} = 1.105 mA, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	SPT5140 TYP	MAX	UNITS
DC Electrical Characteristics						
Integral Linearity Error	1.0 mA < I _{Set} < 1.3 mA	VI	–0.37 –0.95		+0.37 +0.95	% FS LSB
Differential Linearity Error	1.0 mA < I _{Set} < 1.3 mA	VI	–0.2 –0.5		+0.2 +0.5	% FS LSB
Gain Error		VI	–6.5		+6.5	% FS
Gain Error Tempco		V		150		PPM/°C
Bandgap Tempco		V		100		PPM/°C
Input Capacitance, I _{Set} , Ref Out		V		5		pF
Compliance Voltage, + Output		VI	–1.2		1.5	V
Compliance Voltage, – Output		VI	–1.2		1.5	V
Equivalent Output Resistance		VI	20			kΩ
Output Capacitance		V		9		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, – Output		IV	45			mA
Output Offset Current		VI		0.05	0.5	LSB
Input Voltage, Logic High		VI	–1.0			V
Input Voltage, Logic Low		VI			–1.5	V
Convert Voltage, Common Mode Range (V _{ICM})		IV	–0.5		–2.5	V
Convert Voltage, Differential (V _{IDF})		IV	0.4		1.2	V
Input Current, Logic Low, Data and Controls		VI		35	120	μA
Input Current, Logic High, Data and Controls		VI		40	120	μA
Input Current, Convert		VI		2	60	μA
Reference Voltage Measured to V _{CC}		VI	–1.3	–1.2	–1.0	V
Reference Output Current		VI	–50			μA
Input Capacitance, Data and Controls		V		3		pF
Power Supply Sensitivity		VI	–120	+20	+120	μA/V
Supply Current		VI		155	220	mA

ELECTRICAL SPECIFICATIONS

V_{CC} = ground, V_{EE} = $-5.2\text{ V} \pm 0.3\text{ V}$, $T_A = T_{MIN}$ to T_{MAX} , $C_C = 0\text{ pF}$, $I_{Set} = 1.105\text{ mA}$, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Characteristics ($R_L = 37.5\text{ ohms}$, $C_L = 5\text{ pF}$, $T_A = +25\text{ }^\circ\text{C}$, $I_{Set} = 1.105\text{ mA}$)						
Maximum Conversion Rate		IV	385	400		MWPS
Rise Time	10% to 90% G.S.	IV			900	ps
Rise Time	10% to 90% G.S. $R_L = 25\text{ ohms}$	IV			600	ps
Current Settling Time, Clocked Mode (t_{SI})	To 0.2% G.S.	V		4		ns
Current Settling Time, Clocked Mode (t_{SI})	To 0.2% G.S. $R_L = 25\text{ }\Omega$	V		3		ns
Clock to Output Delay, Clocked Mode (t_{DSC})	$T_A = T_{MIN}$ to T_{MAX}	IV IV		2.2	4 4.5	ns ns
Part-to-Part Clock to Output Delay Skew, Clocked Mode	$T_A = T_{MIN}$ to T_{MAX}	IV			1.5	ns
Data to Output Delay, Transparent Mode (t_{DST})	$T_A = T_{MIN}$ to T_{MAX}	IV IV		3.2	6 6	ns ns
Glitch Energy	Area = $1/2\text{ VT}$	V		4		pV-s
Convert Pulse Width (t_{PWH} , t_{PWL})		IV	1.3			ns
Reference Bandwidth, -3 dB		V		1.25		MHz
Set-up Time, Data and Controls (t_S)		IV	1.0			ns
Hold Time, Data and Controls (t_H)		IV	0.5			ns
Slew Rate	20% to 80% G.S.	V		700		V/ μS
Clock Feedthrough		IV			-48	dB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

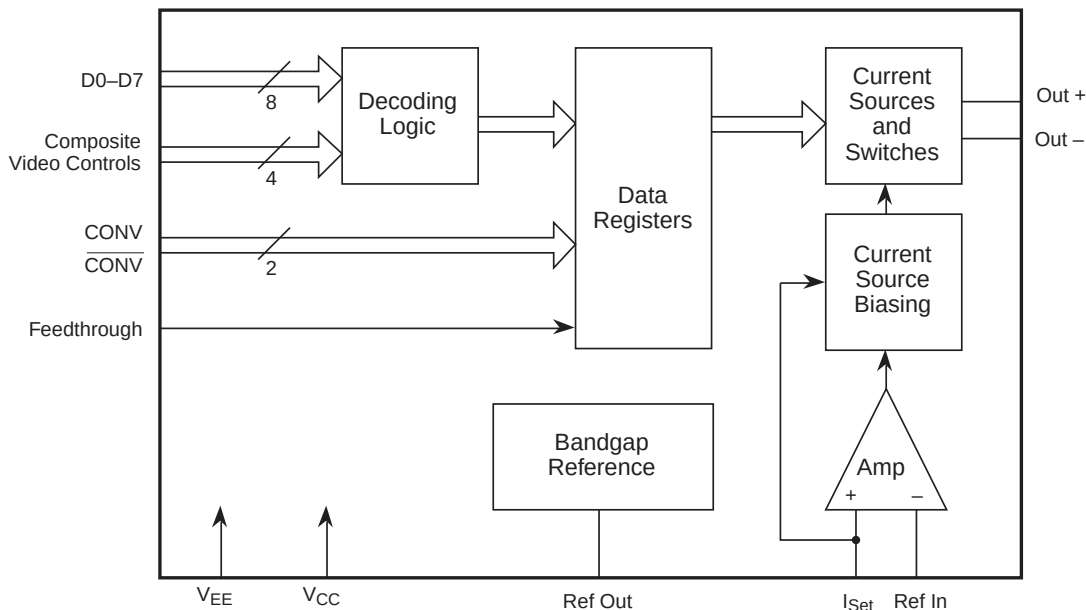
All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL

I	100% production tested at the specified temperature.
II	100% production tested at $T_A = +25\text{ }^\circ\text{C}$, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at $T_A = +25\text{ }^\circ\text{C}$. Parameter is guaranteed over specified temperature range.

TEST PROCEDURE

Figure 1 – Functional Diagram



APPLICATION INFORMATION

The SPT5140 is a high-speed video digital-to-analog converter capable of up to 400 MWPS conversion rates. This makes the devices suitable for driving 2048 X 2048 pixel displays at update rates of 60 to 90 Hz.

In addition, the SPT5140 includes an internal bandgap reference which may be used to drive two other SPT5140s if desired.

The SPT5140 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The SPT5140 is segmented so that the four MSBs of the input data are separated into a parallel “thermometer” code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

MSB currents are then summed with the LSBs that provide a one-sixteenth of full-scale contribution to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls — Sync, Blank, Reference White (Force High) and Bright — are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation of the video control and

data inputs. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered video DACs.

TYPICAL INTERFACE CIRCUIT

GENERAL

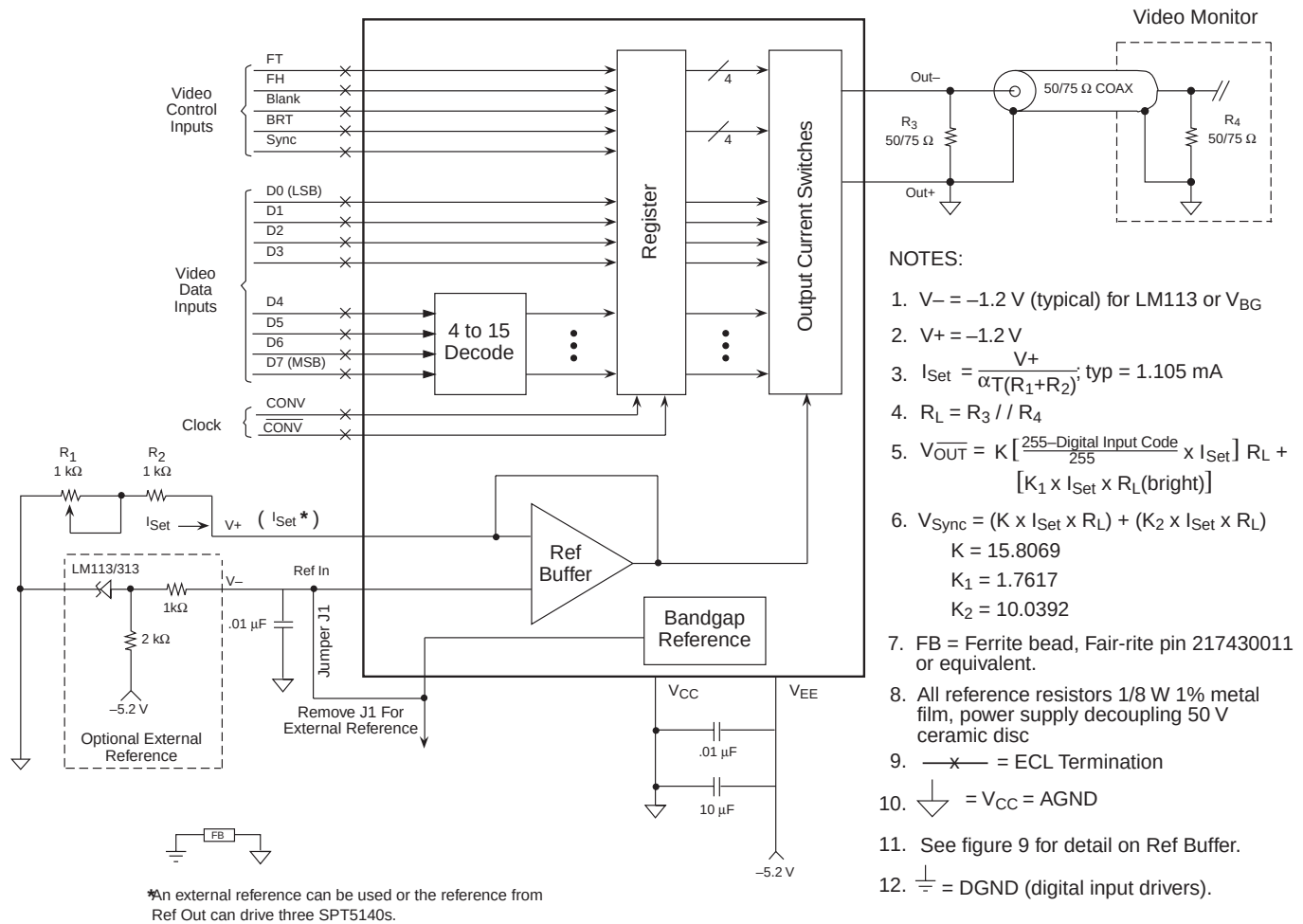
A typical interface circuit using the SPT5140 in a color raster application is shown in figure 2. The SPT5140 requires few external components and is extremely easy to use. The very high operating speeds of the SPT5140 require good circuit layout, decoupling of supplies, and proper design of transmission lines. The following considerations should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the SPT5140. Note that all ECL inputs are terminated as closely to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 ohms, which is easily terminated using a 330 ohm resistor to V_{EE} and a 220 ohm resistor to ground. This arrangement gives a Thevenin equivalent termination of 130 ohms to -2 volts without the need for a -2 volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended.

Figure 2 – Typical Interface Circuit



OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a doubly terminated 50 or 75 ohm load transmission system as shown. The source impedances of the SPT5140 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CC} , which is connected to the source termination resistor R_S .

POWER CONSIDERATIONS

The SPT5140 operates from a single -5.2 V standard supply. Proper bypassing of the supplies will augment the SPT5140's inherent supply noise rejection characteristics. As shown in figure 2, each supply pin should be bypassed as close to the device as possible with 0.01 μF and 10 μF capacitors.

The SPT5140 has two analog (V_{EE}) power supply pins. Both supply pins should be properly bypassed as mentioned previously. This device also has two analog (V_{CC}) ground pins. Both ground pins should be tied to the analog ground plane. Power and ground pins must be connected in all applications. If a +5 V power source is required, the ground pins (V_{CC}) become the positive supply pins while the supply pins (V_{EE}) become the ground pins. The relative polarities of the other input and output voltages must be maintained.

REFERENCE CONSIDERATIONS

The SPT5140 has two reference inputs (Ref In and I_{Set}) and one reference output (Ref Out). The input pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See figure 9.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{Set}), the full-scale output may be adjusted by varying the reference current. I_{Set} is controlled through the (I_{Set}) input on the SPT5140. A method and equations to set I_{Set} are shown in figure 2. The SPT5140 can use an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the Ref In should be driven through a resistor to minimize offsets caused by bias current. The value for I_{Set} can be varied with the 500 to 1k Ω trimmer to change the full-scale output. A double 50 ohm load (25 ohm) can be driven if I_{Set} is increased by 50% above for doubly-terminated 75 ohm video applications.

DATA INPUTS AND VIDEO CONTROLS

The SPT5140 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low, so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than eight bits are used.

The SPT5140 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output

Figure 3 – Timing Diagram

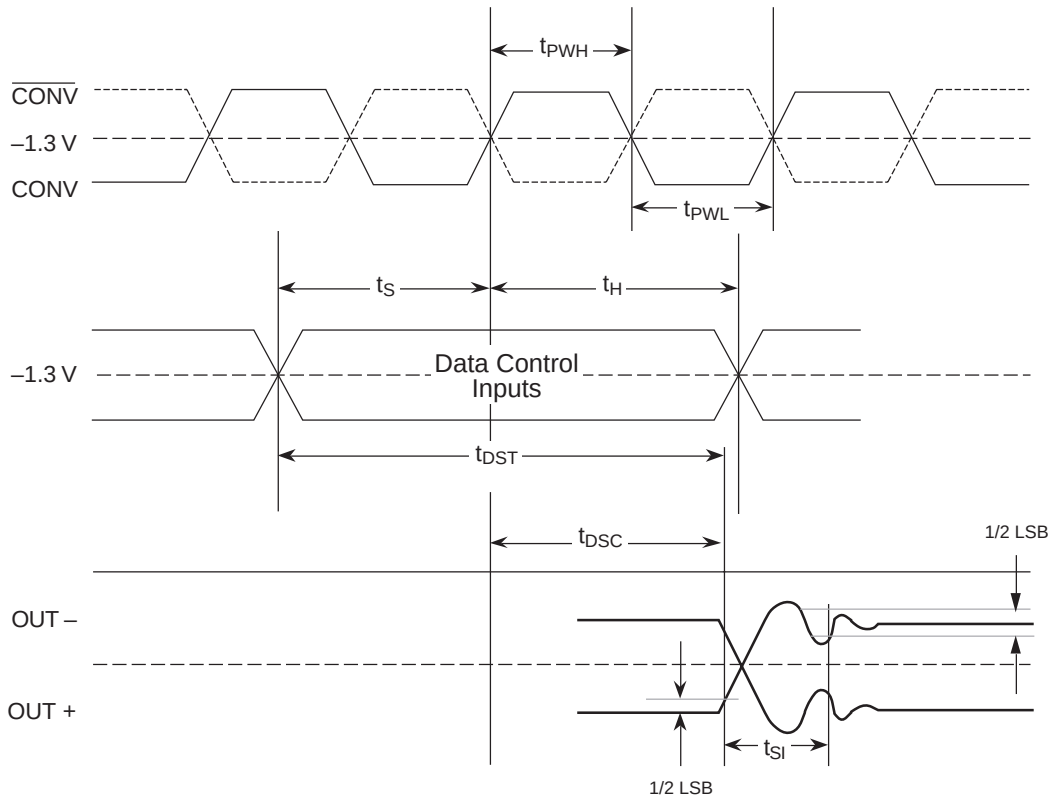


Table I – Video Control Operation (Output values for setup = 10 IRE and 75 ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out – (mA)	Out – (V)	Out – (IRE)	Description
1	X	X	X	X	28.57	–1.071	–40	Sync Level
0	1	X	X	X	20.83	–0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	–0.073	100	Normal High Level
0	0	0	0	000...	19.40	–0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	–0.073	100	Normal High Level
0	0	0	1	000...	17.44	–0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_S before, and a hold time of t_H after, the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors. (See figure 3.)

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in

RS-343-A. Table I shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (figure 4).

Reference White video level output is provided by Force High, which drives the internal digital data to full-scale output or 100 IRE units. Bright gives an additional 10% of full-scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

Figure 4 – Video Output Waveform for Standard Load

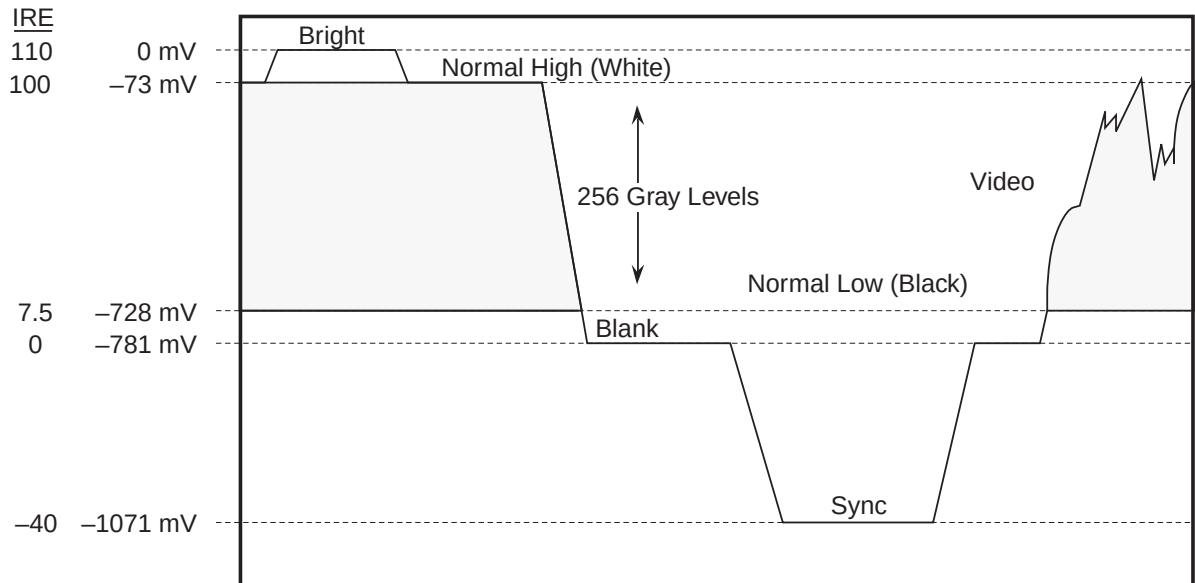
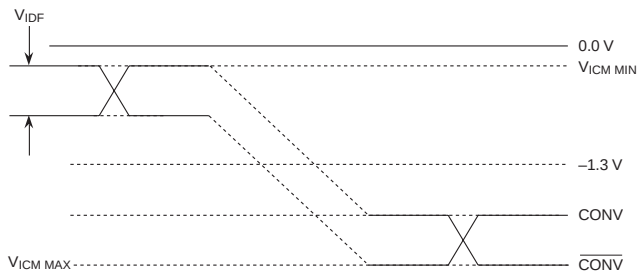


Figure 5 – CONVert, CONVert Switching Levels



CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONVert and $\overline{\text{CONVert}}$ (figure 5). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the SPT5140. Since the actual switching threshold of CONVert is determined by $\overline{\text{CONVert}}$, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONVert}}$. The switching threshold of CONVert is set by this bias voltage.

ANALOG OUTPUTS

The SPT5140 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full-scale output can be changed by setting I_{Set} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 ohm load to standard video levels. In the standard configuration of figure 6, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The Out- output (figure 4) will provide a video output waveform with the Sync pulse bottom at the -1.07 V level. The Out+ is inverted with Sync up.

Figure 6A – Standard Load

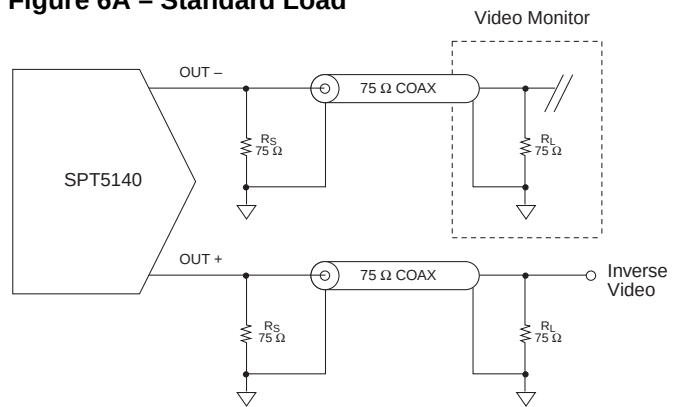


Figure 6B – Test Load

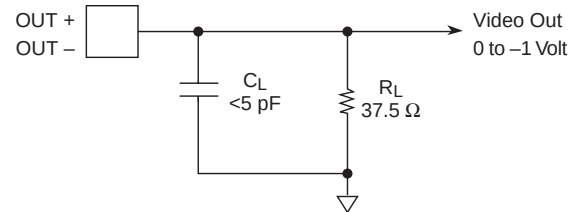


Figure 7 – Burn-In Circuit

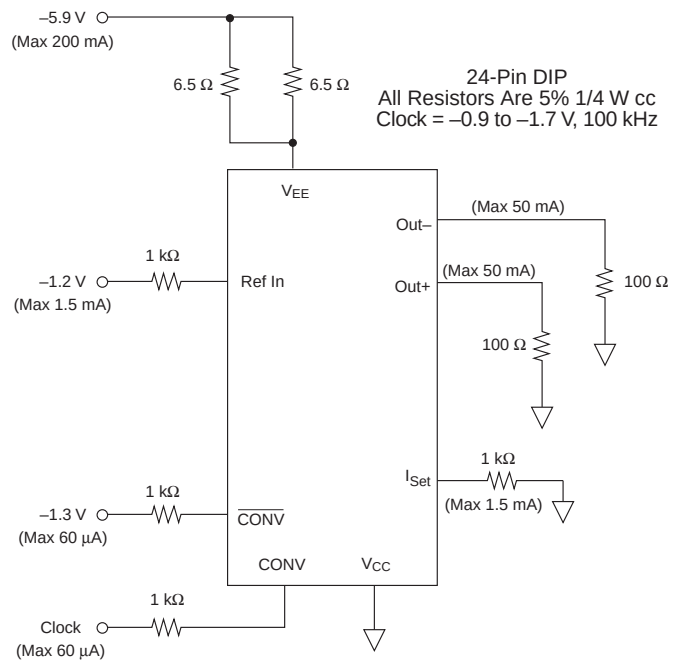
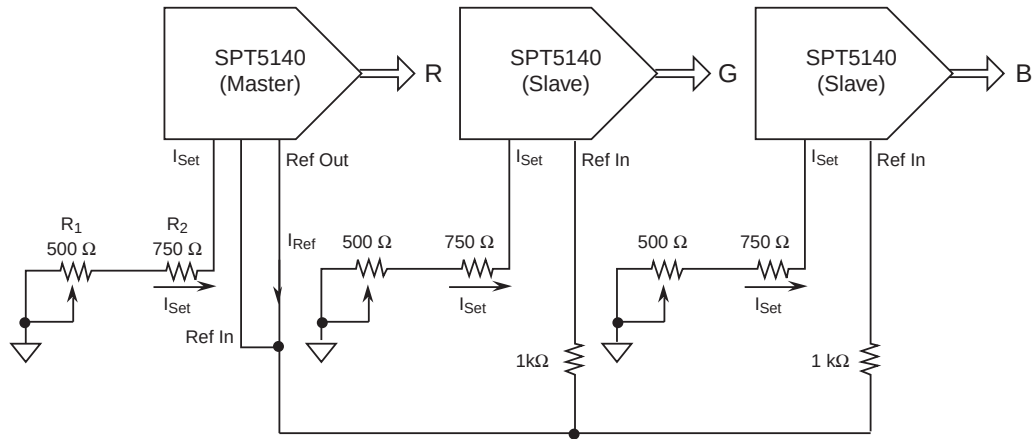


Figure 8 – Typical RGB Graphics System



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch and improve TC tracking.

The SPT5140 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 μA to an external load, such as two other DAC reference inputs.

The circuits shown in figure 8 illustrate how a single SPT5140 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the SPT5140's reference output.

Figure 9 – DAC Output Circuit

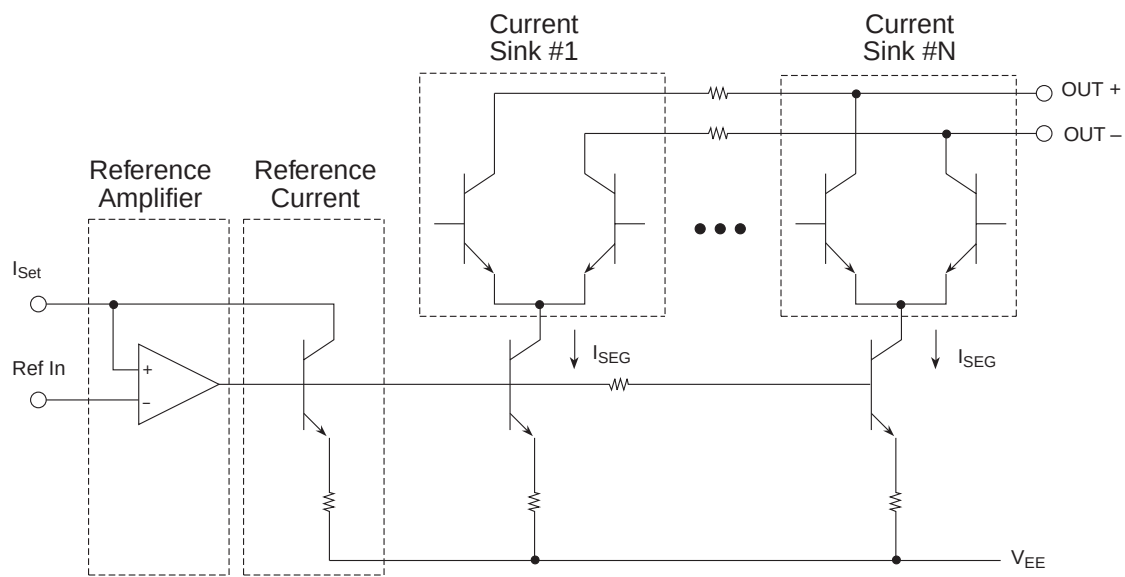
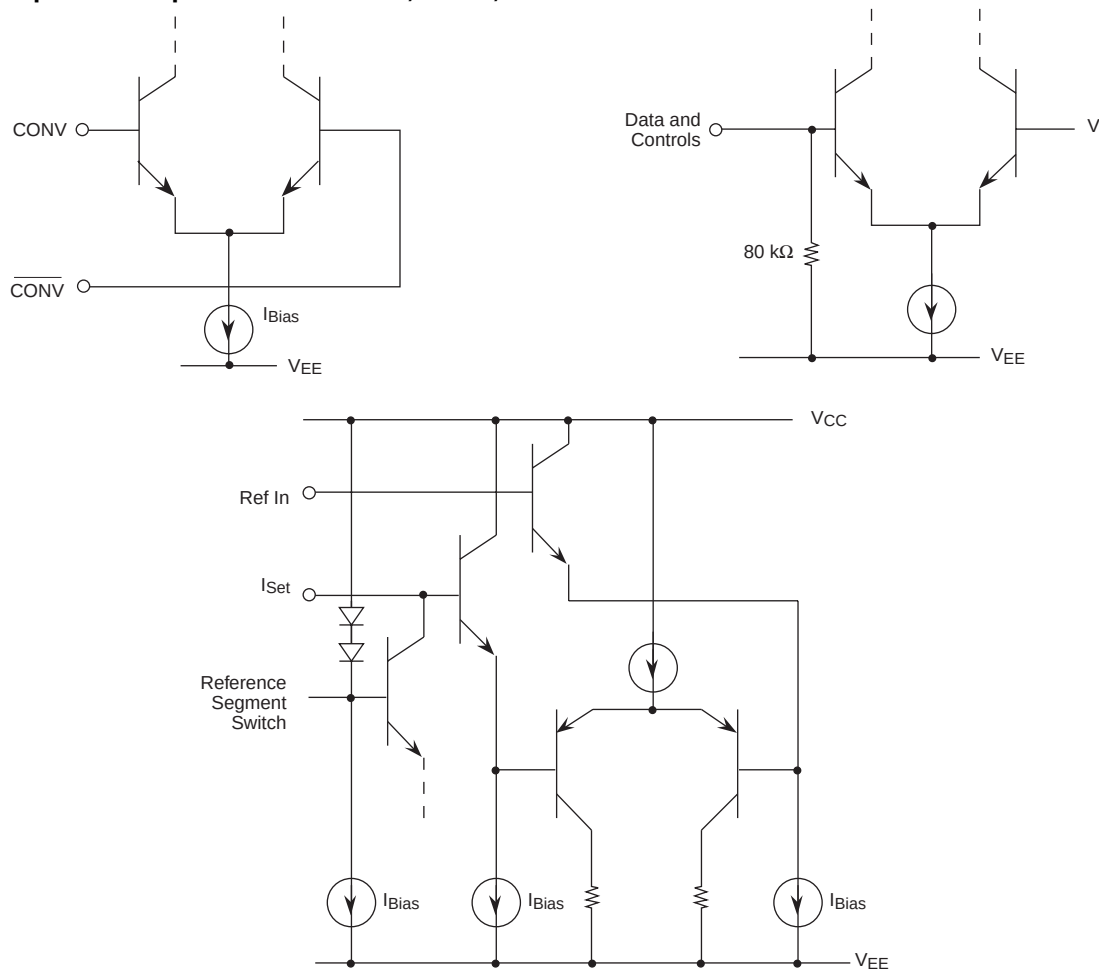
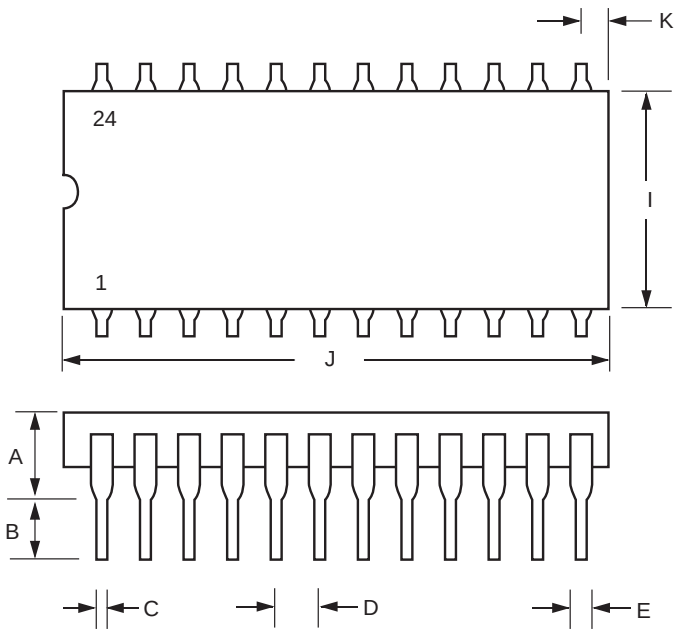


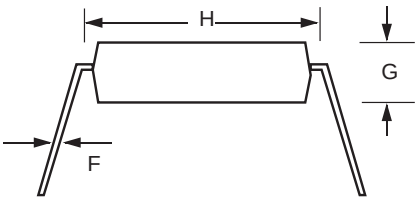
Figure 10 – Equivalent Input Circuits – Data, Clock, Controls and Reference



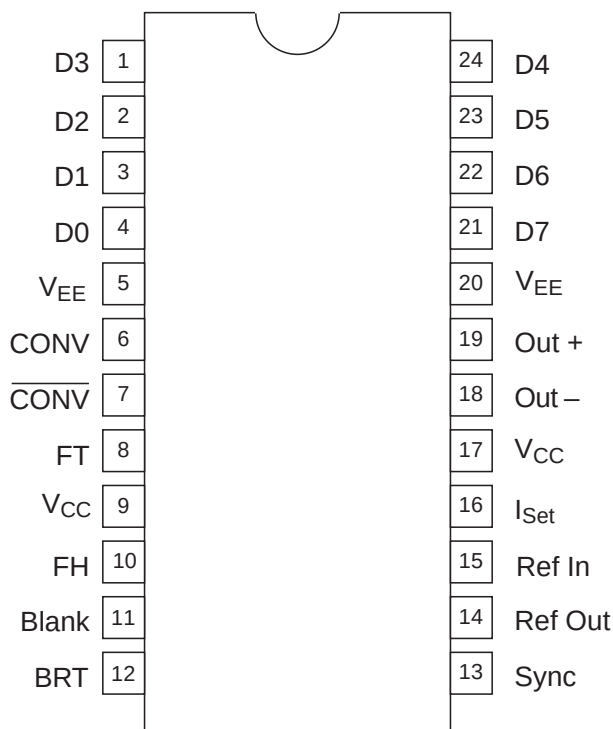
PACKAGE OUTLINE 24-Lead PDIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.190		4.83
B	0.125	0.135	3.18	3.43
C	0.015	0.022	0.38	0.56
D	0.100 typ		2.54 typ	
E	0.055	0.065	1.40	1.65
F	0.008	0.012	0.20	0.30
G	0.150 typ		3.81 typ	
H	0.600	0.625	15.24	15.88
I	0.530	0.550	13.46	13.97
J	1.245	1.255	31.62	31.88
K	0.070	0.080	1.78	2.03



PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
V _{EE}	Negative Supply
CONV	Convert Clock Input
$\overline{\text{CONV}}$	Convert Clock Input Complement
FT	Register Feedthrough Control
V _{CC}	Positive Supply
FH	Data Force High Control
Blank	Video Blank Input
BRT	Video Bright Input
Sync	Video Sync Input
Ref Out	Reference Output
Ref In	Reference Input
I _{Set}	Reference Current
Out -	Output Current Negative
Out +	Output Current Positive
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT5140SIN	-25 to +85 °C	24L PDIP

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Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.