



SPN3006

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN3006 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN3006 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

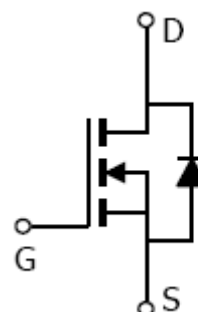
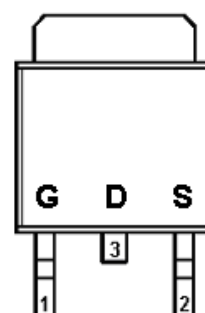
- ◆ 30V/30A, $R_{DS(ON)} = 4.7\text{m}\Omega @ V_{GS} = 10\text{V}$
- ◆ 30V/15A, $R_{DS(ON)} = 7.5\text{m}\Omega @ V_{GS} = 4.5\text{V}$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252 package design

APPLICATIONS

- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

PIN CONFIGURATION

TO-252



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN3006T252RGB	TO-252	SPN3006

※ SPN3006T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	30	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current	TA=25°C	I _D	80	A
	TA=100°C		57	
Pulsed Drain Current		I _{DM}	160	A
Avalanche Current		I _{AS}	48	A
Single Pulse Avalanche Energy		E _{AS}	259	mJ
Power Dissipation	TA=25°C	P _D	6	W
Operating Junction Temperature		T _J	150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient (t ≤ 10s)		R _{θJA}	25	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

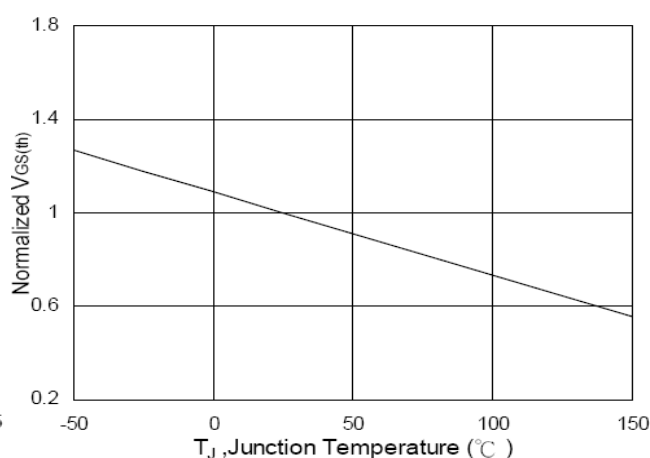
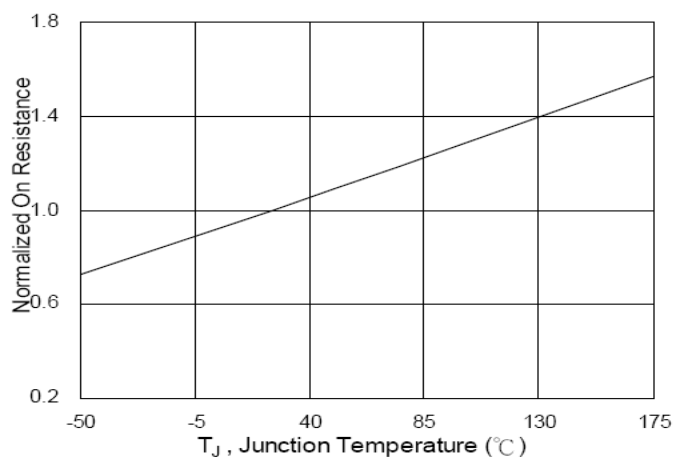
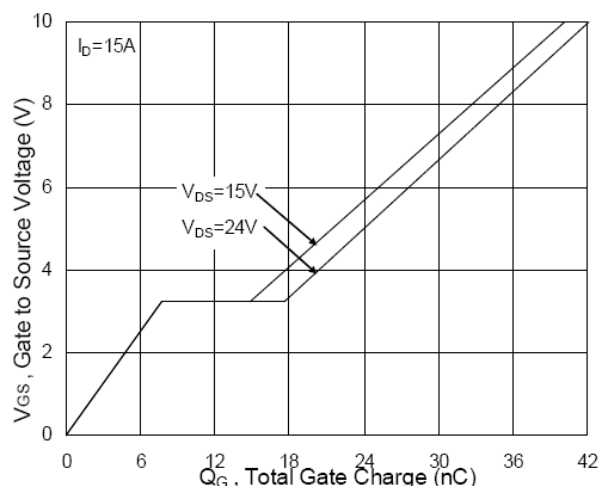
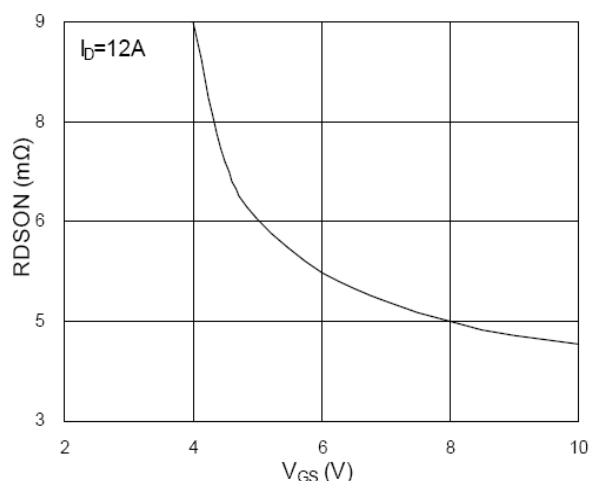
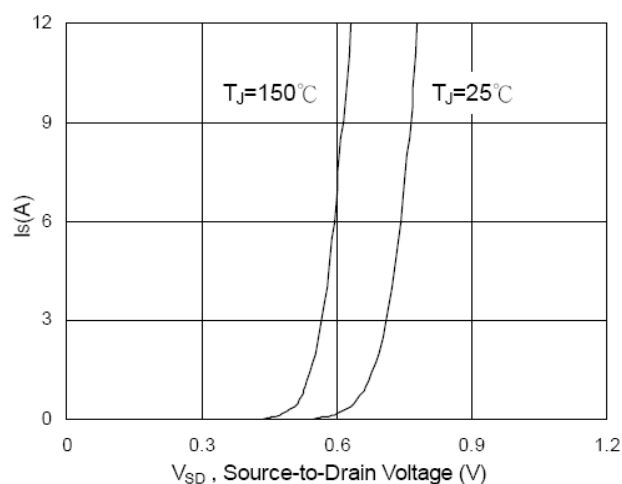
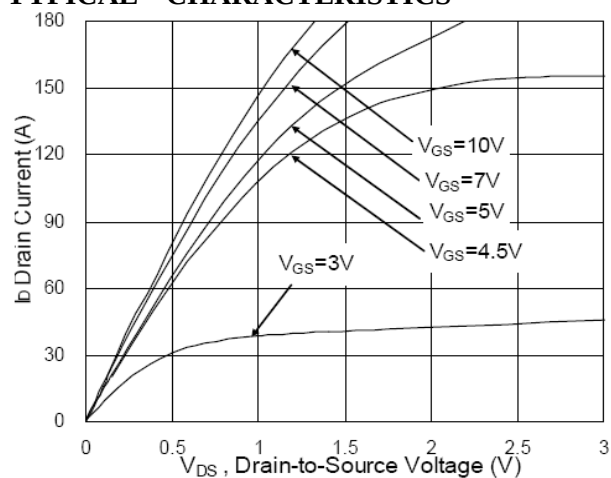
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V			1	μA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C			5	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =10V			80	A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =30A		4.7	5.5	mΩ
		V _{GS} =4.5V, I _D =15A		7.5	9	
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =30A		22		S
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V			1	V
Single Pulse Avalanche Energy	E _{AS}	V _{DD} =25V, L=0.1mH, I _{AS} =24A	60			mJ
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, V _{GS} =4.5V I _D =15A		20	18	nC
Gate-Source Charge	Q _{gs}			7.6		
Gate-Drain Charge	Q _{gd}			7.2		
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V f=1MHz		2300		pF
Output Capacitance	C _{oss}			265		
Reverse Transfer Capacitance	C _{rss}			210		
Turn-On Time	t _{d(on)}	V _{DD} =15V, I _D =15A, V _{GEN} =10V R _G =3.3Ω		7.8	15	nS
	t _r			15	12	
Turn-Off Time	t _{d(off)}			37	30	
	t _f			10.6	15	



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TYPICAL CHARACTERISTICS





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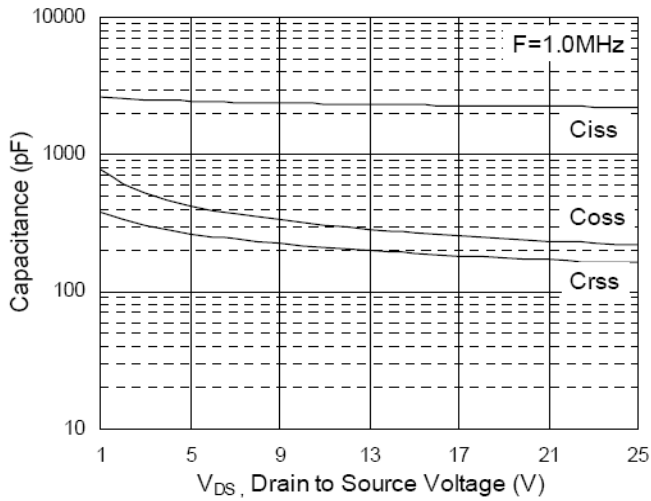


Fig. 7 Typical Capacitance Characteristics

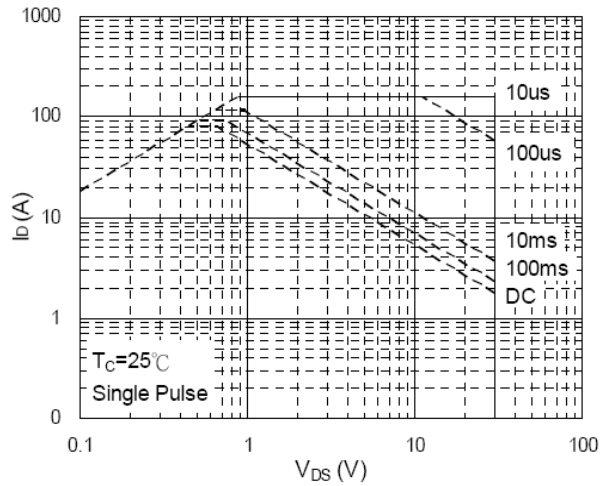


Fig. 8 Maximum Safe Operation Area

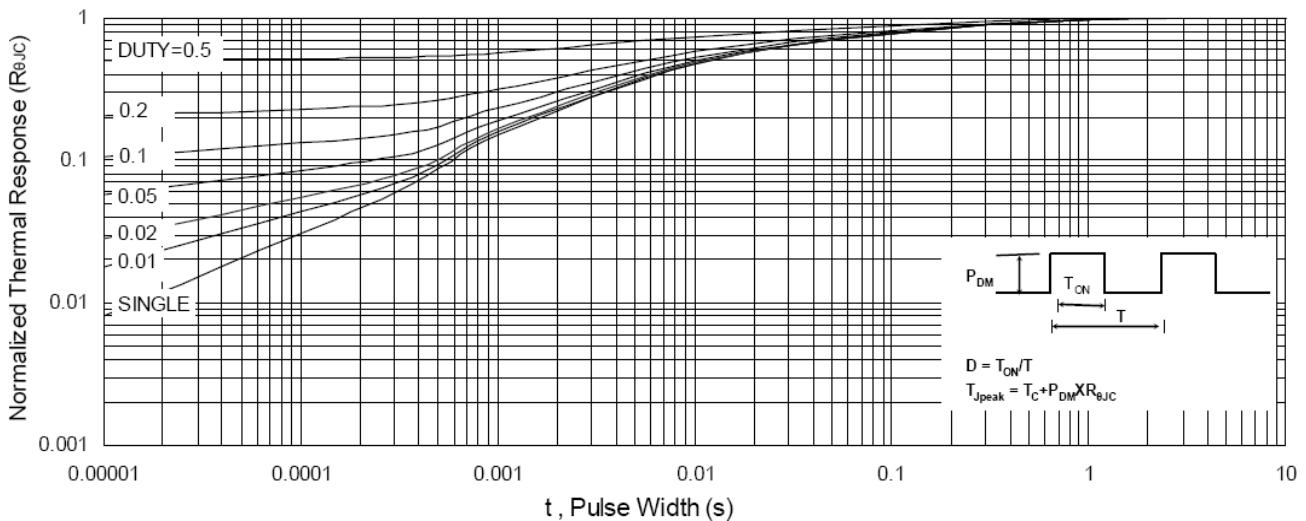


Fig. 9 Effective Transient Thermal Impedance

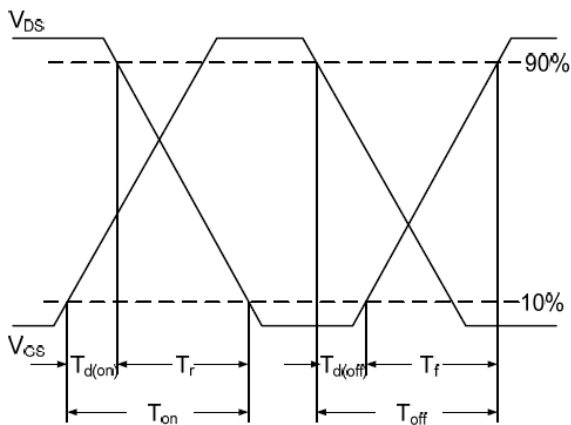


Fig. 10 Switching Time Waveform

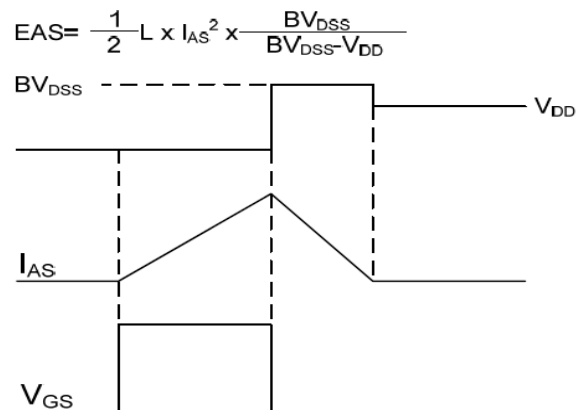


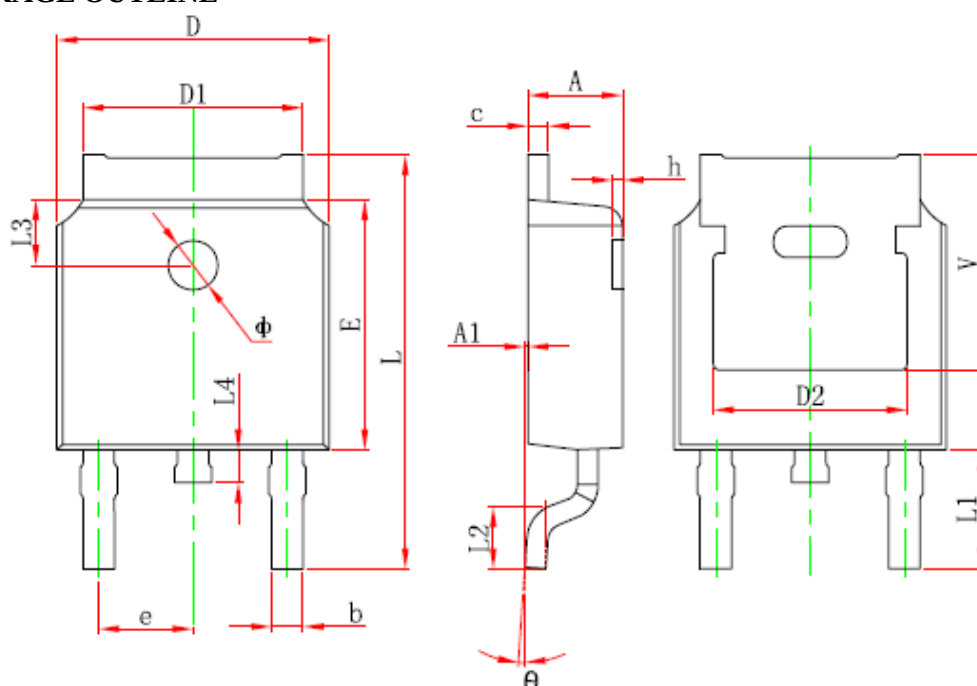
Fig. 11 Unclamped Inductive Waveform



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TO-252 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	



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