UM1699
User manual

SPC563M-DISP Discovery+ evaluation board

Introduction

The SPC563M-DISP Discovery kit helps you to discover SPC56 M line Power Architecture® Microcontrollers.

The discovery board is based on SPC563M64L7, a 32-bit Power Architecture Book E compliant e200z335 CPU core with 1.5Mbyte on-chip in an LQFP176 package.

The numerous interfaces including CAN/SCI/K-LINE/DSPI/GPIO make the SPC56M-Discovery an excellent starter kit for customer quick evaluation and project development.

The SPC56 M family is designed to address cost sensitive powertrain and transmission applications.

The SPC56 M line key functionality is Time processing units (eTPU) a coprocessor to create events in sync with internal or external signals without flooding the CPU with interrupt to serve.

Free ready-to-run application firmware examples are available inside SPC5Studio at *www.st.com* to support quick evaluation and development.

Contents

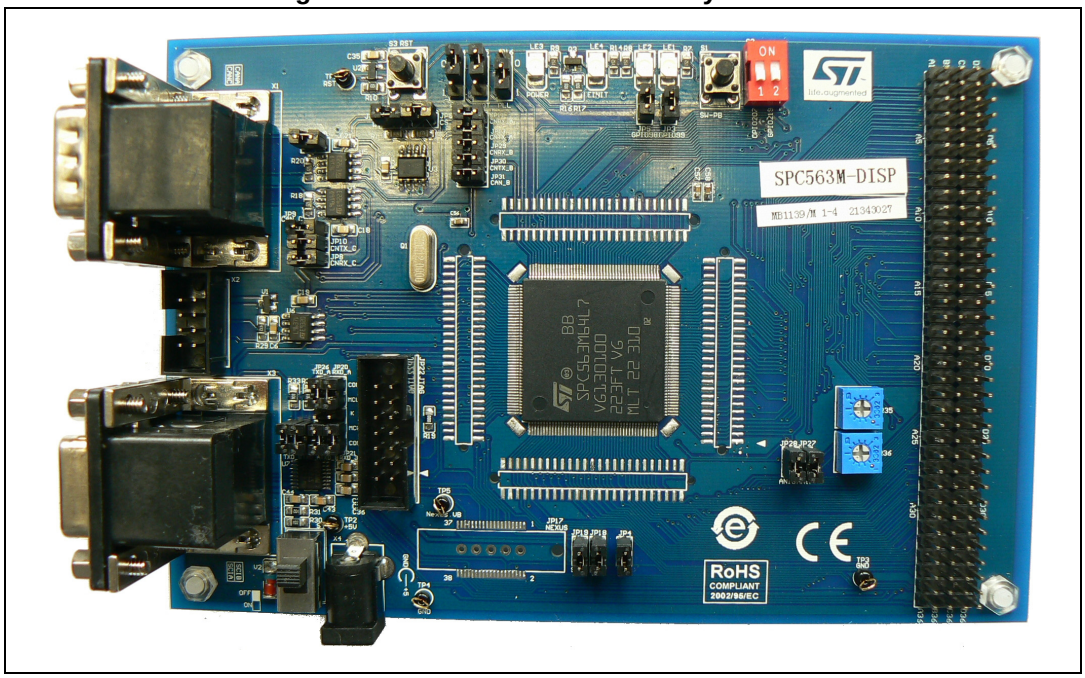
List of tables

List of figures

1 SPC563M-DISP with SPC563M64L7

1.1 SPC563M-DISP Discovery board

Figure 1. SPC563M-DISP Discovery+ board



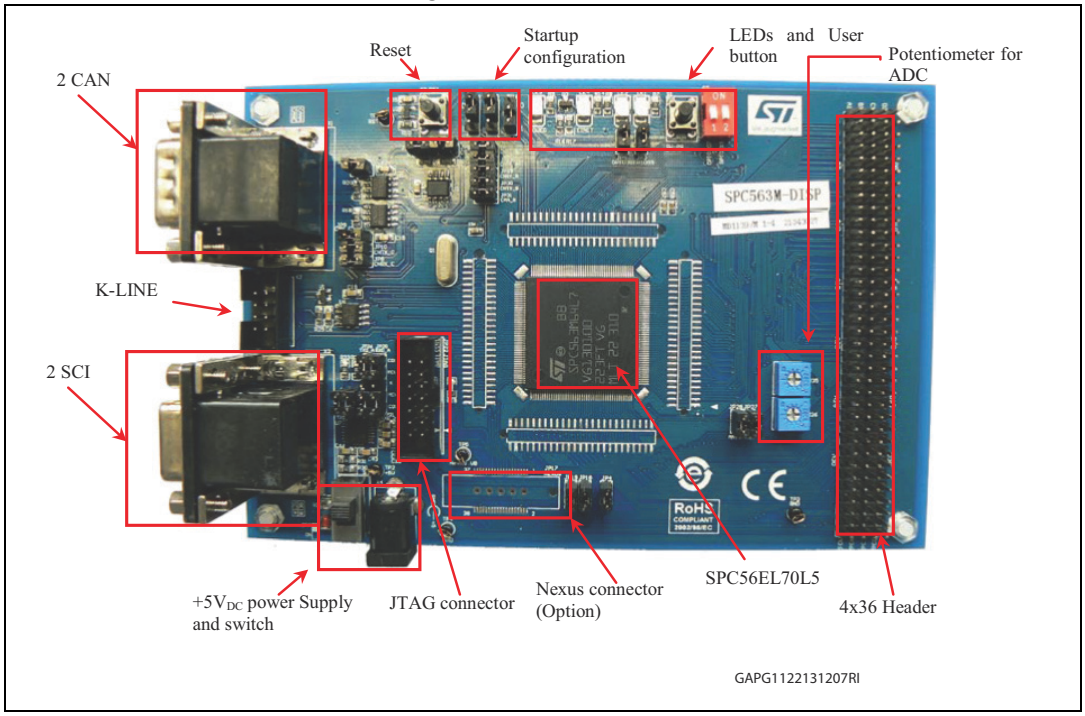
The content of hardware of SPC563M-DISP with SPC563M64L7 consists of:

- SPC563M-DISP Discovery board (*Figure 1: SPC563M-DISP Discovery+ board*).
- Power Supply (Mains: 90-240V_{AC} - Output: 5V_{DC}).

The PCB, the components and all HW parts assembled in the board meet requirements of the applicable RoHS directives.

2 Hardware overview

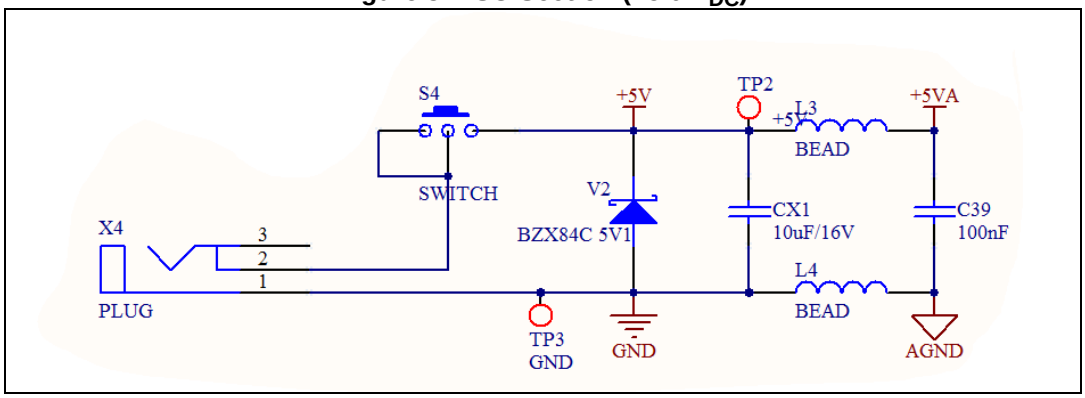
Figure 2. HW overview



2.1 5V DC power supply

The 5 V DC voltage is used to supply the whole board including SPC563M64L7 and communication interface transceiver chips. A zener diode, rating 5.1 V, closed to the power supply connector is used to protect the chips for high voltage (wrong connection) in a short time. On the board a slide switch for quickly switching on/off is present.

Figure 3. PSU Section (+5.0 V_{DC})



The test point TP2 is available to measure the DC input voltage levels (+5V) while TP3 is connected to GND.

2.2 Device startup configuration

When the MCU is power-on, it will latch the status of pin WKPCFG, BOOTCFG1 & PLLREF.

- “WKPCFG” determines the weak pull up/down configuration of eMIOS and eTPUpins
- “BOOTCFG1” is for boot selection
- “PLLREF” set the source of clock reference input & external circuit related to clock source.

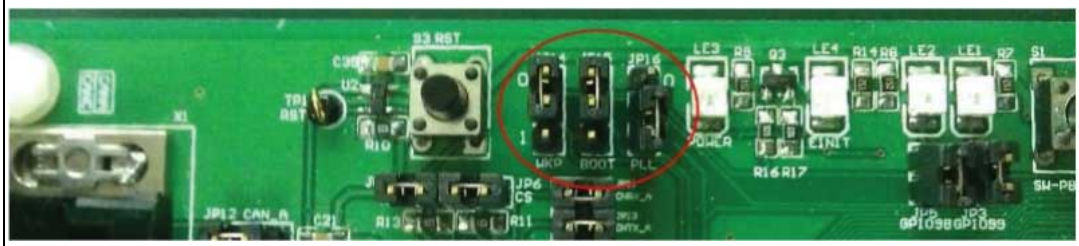
The detailed logic table is as following:

Table 1. SPC563M-DISP – Device startup configuration

	WKPCFG	BOOTCFG1	PLLREF
0 - Low	Weak pull down	Boot from internal flash	Clock from external reference
1 - High	Weak pull up	Serial boot from FlexCAN/eSC	Clock from external oscillator

The evaluation board provides three jumpers, JP14, JP15 & JP16, which can be used for user to configure the device in different working conditions. Figure below shows a typical connection of the evaluation board which only has external crystal oscillator.

Figure 4. Device start-up configuration



2.3 User LEDs

The board provides four LEDs for device status and monitoring GPIO 98 and GPIO99 outputs. The detailed information is given in User LEDs here below:

Table 2. User LEDs

Item	Mark	Color	Function
LE1	-	Green	GPIO99 switching high/low test; ON: LOW, OFF: HIGH
LE2	-	Green	GPIO98 switching high/low test; ON: LOW, OFF: HIGH

Table 2. User LEDs

Item	Mark	Color	Function
LE3	Power	Red	Turn on when 5V supply is ON and it is plugged into the socket (X4)
LE4	EINIT	Green	Indication for internal / external RESET; OFF: RESET, ON: normal.

Figure 5. User LEDs

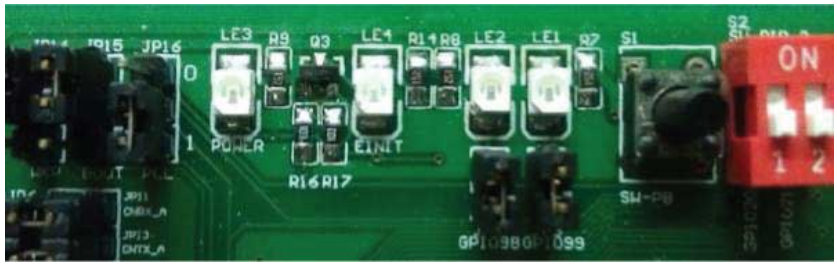


Figure 6. User LEDs- LE1/LE2(schematic diagram)

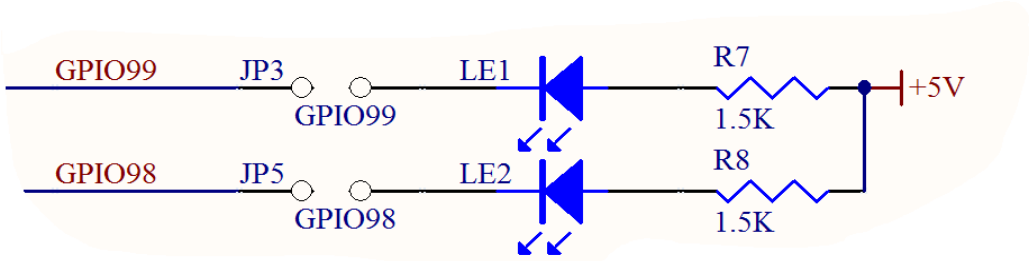
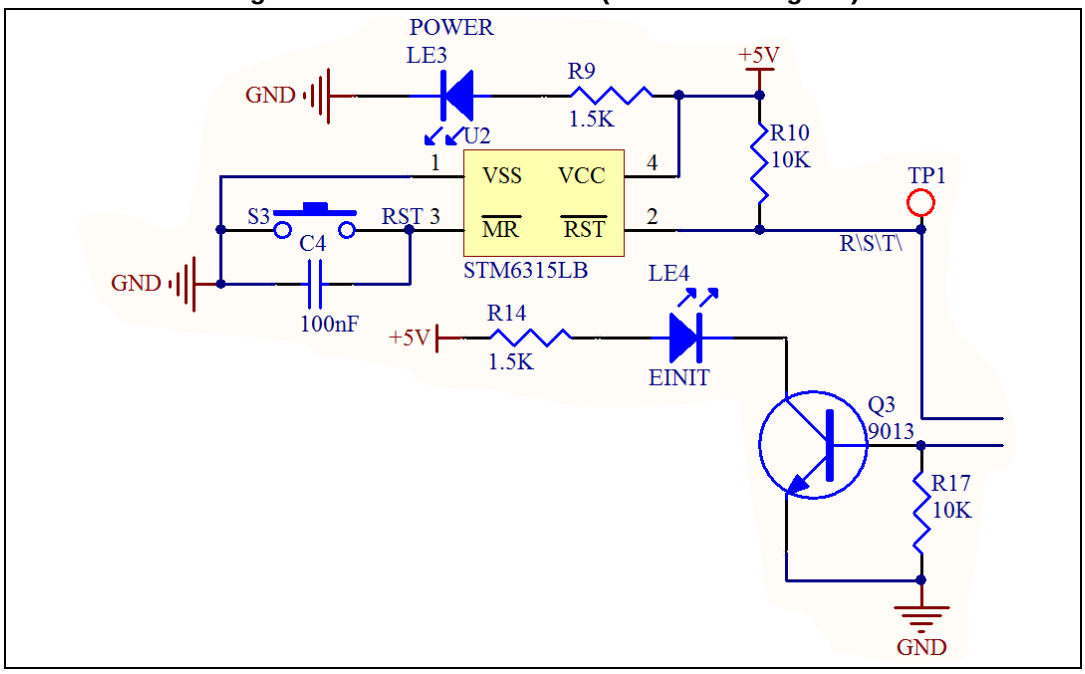


Figure 7. User LEDs- LE3/LE4(schematic diagram)



2.4 JTAG / Nexus debug connection

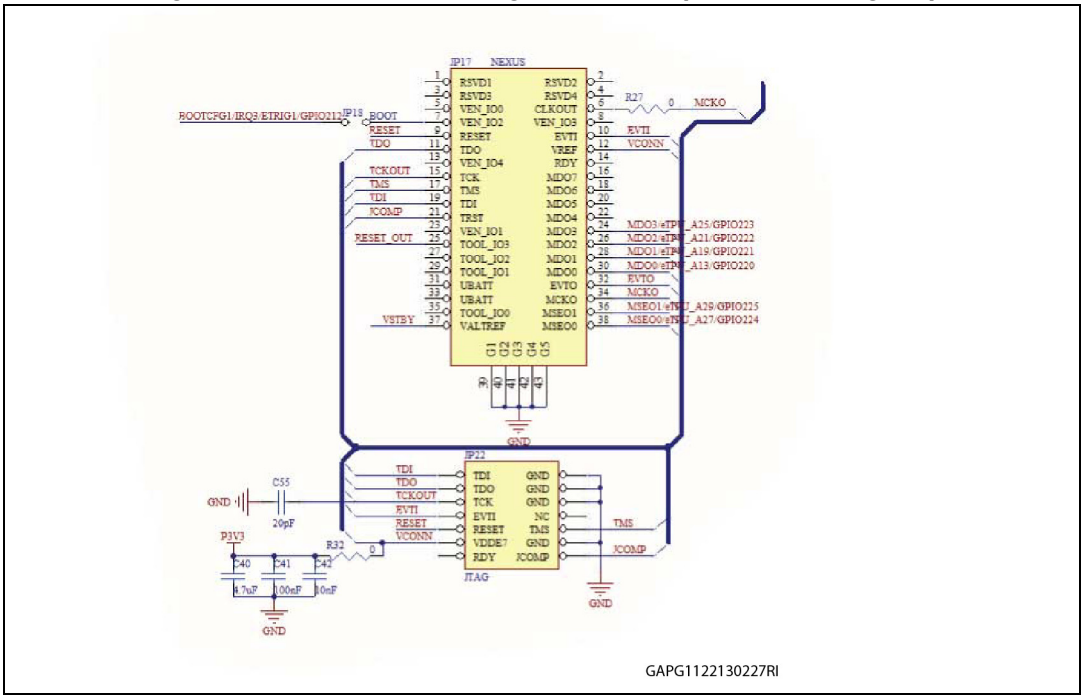
Two kinds of debug interface are utilized in the evaluation board:

- the standard 14-pin JTAG connector of PPC for low-cost/end tools,
- 3MTM Mictor 38-pin connector for Nexus interface in high-end development tools.

Before connecting the development tools to the debug interface, it is highly recommended to switch off the power supply of the board and make sure the pin 1 of the tools' ribbon cable lines up with the pin 1 of onboard connector.

Figure 8. JTAG / Nexus debug connection

Figure 9. JTAG / Nexus debug connection (schematic diagram)



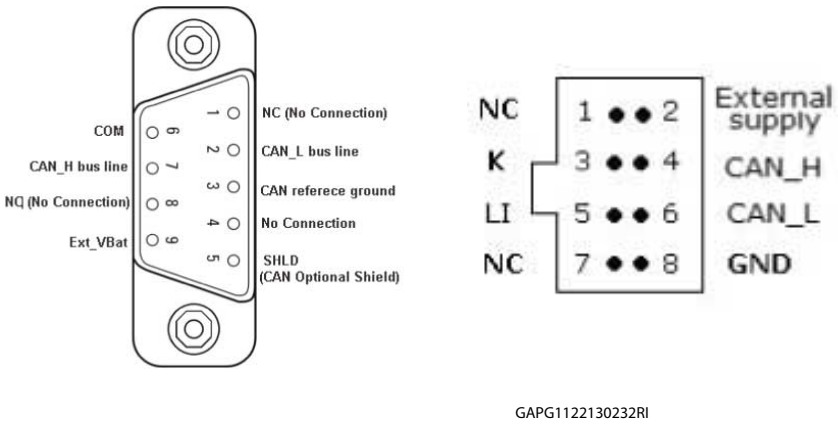
2.5 High speed CAN interface

The whole CAN interface circuit usually includes the CAN module in microcontroller, CAN transceiver & CAN connector.

In the evaluation board, CAN module is integrated and the transceiver is L9616 which support high-speed CAN.

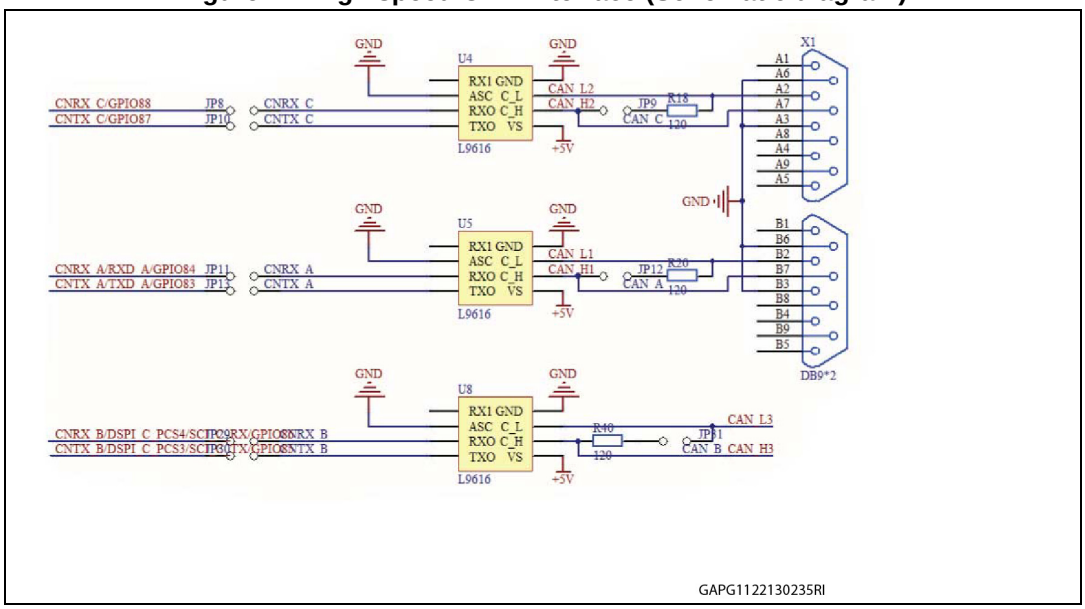
Regarding the CAN connectors, the two basic CAN channels of SPC563M64L7, CANA and CANC, are located in two DB9 male connectors

Figure 10. High speed CAN interface



As the CAN TX/RX IO of microcontroller is multiplexed with other functions, several jumpers are placed between L9616 and the MCU, it avoids unwanted connections to L9616 if the CAN TX/RX has been configured to GPIO; detailed information is reported in the following *Figure 11: High speed CAN interface (Schematic diagram)*.

Figure 11. High speed CAN interface (Schematic diagram)



Note: jumpers JP9, JP12 & JP31 are used to set proper 120Ω termination resistor for CAN bus. Please disconnect the jumper if unnecessary.

2.6 eSCI / K-LINE

eSCI stands for enhanced serial communication interface, as it enhances the conventional asynchronous RX/TX with DMA and LIN support. High speed CAN interface, HW configurations show the hardware connection on evaluation board:

ST232 is the bridge between RS232 DB9 female interface and TX/RX signal of microcontroller.

L9637 is the ISO9141 interface chip. In the microcontroller side, user can set the jumper 20, 21, 23, 26 to choose two SCI interfaces, 1xSCI + 1x K-Line or 1x SCI/K-Line.

Figure 12. High speed CAN interface (Schematic diagram)

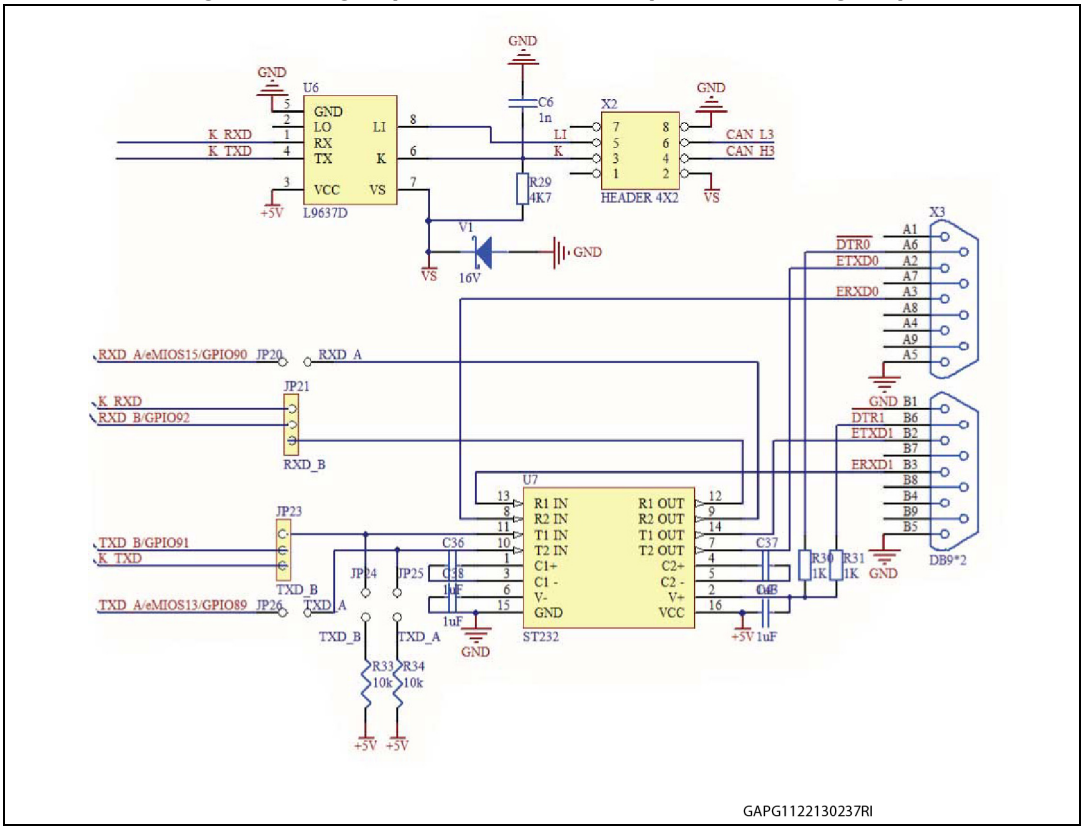


Figure 13. High speed CAN interface, HW configurations

2x SCI, SCIA, SCIB	SCIA + K-Line on T/RXD_B	SCIB + K-Line on T/RXD_A	SCIA	SCIB	K-Line on T/RXD_A	K-Line on T/RXD_B
						

GAPG1122130240RI

2.7 I/O header

All GPIOs/DSPI/eMIOS/eTPU of the MCU can be accessed through the 4x36 I/O headers.

Table 3. I/O header: pin out table

Pin number	A	B	C	D
1	GND	GND	GND	5V
2	AN10/ AN39/ ANY	AN9/ ANX	AN37	AN36
3	AN11/ ANZ	AN16	AN22	AN24
4	AN18	PCS_B1/ GPIO106	AN27	AN30
5	PCS_B5/ PCS_C0 GPIO110	eTPU_A12/ PCS_B1 GPIO126	AN32	AN34
6	PCS_B0 GPIO105	eTPU_A17 GPIO131	AN17	eTPU_A29 AN15/ FCK
7	eTPU_A10/ eTPU_A22 GPIO124	eTPU_A9/ eTPU_A21 GPIO123	MCKO GPIO219	MDO0/ eTPU_A13 GPIO220
8	eTPU_A11/ eTPU_A23 GPIO125	TDI18/ eMIOS5 GPIO232	MDO1/ eTPU_A19 GPIO221	MDO2/ eTPU_A21 GPIO222
9	eTPU_A16 GPIO130	eTPU_A27_O	MDO3/ eTPU_A25 GPIO223	GPIO219
10	eTPU_A18 GPIO132	eTPU_A21 IRQ9 GPIO135	GPIO206	eTPU_A24/ IRQ12 SCK_C_LVDS- GPIO138
11	eTPU_A19 GPIO133	eTPU_A23/ IRQ11 eTPU_A21 GPIO137	TXD_A eMIOS13 GPIO89	RXD_A eMIOS15 GPIO90
12	RESET	eTPU_A13_O	RESET_OUT	PLLREF/ IRQ4/ ETRIG0 GPIO208
13	GPIO207	EVTI eTPU_A2 GPIO231	BOOTCFG1/ IRQ3 ETRIG11 GPIO212	VSTBY
14	GPIO99	MSEO0/ eTPU_A27 GPIO224	WKPCFG/ NMI GPIO213	eTPU_A29_O
15	eMIOS1/ eTPU_A1 GPIO180	PCS_B4/ SCK_C GPIO109	CNRX_A/ RXD_A GPIO84	eTPU_A2_O
16	PCS_B2/ SOUT_C GPIO107	PCS_B3/ SIN_C GPIO108	CNRX_C GPIO88	eTPU_A4_O
17	CNTX_A TXD_A GPIO83	CNTX_C GPIO87	eMIOS8/ eTPU_A8 TXDB GPIO187	MSEO1 eTPU_A29 GPIO225
18	eMIOS14/ IRQ0 eTPU_A29 GPIO193	eTPU_A27 AN14 MA2/SDI	eMIOS9/ eTPU_A9 RXDB GPIO188	eTPU_A28 PCS_C1 GPIO142
19	eTPU_A19 AN12 MA0/SDS	eMIOS13 GPIO192	eTPU_A27/ IRQ15 SOUT_C_LVDS+ SOUTB/ GPIO141	eTPU_A26/ IRQ14 SOUT_C_LVDS- GPIO140

Table 3. I/O header: pin out table (continued)

Pin number	A	B	C	D
20	eTPU_A29 PCS_C2 GPIO143	eTPU_A21 AN13 MA1/SDO	GPIO98	eTPU_A14/ PCS_B4 eTPU_A9 GPIO128
21	RXD_B GPIO92	TXD_B GPIO91	eMIOS11 GPIO190	eTPU_A15/ PCS_B5 GPIO129
22	eMIOS4 eTPU_A4 GPIO183	eMIOS12/ DSPI_C_SOUT eTPU_A27 GPIO191	eMIOS15 IRQ1 GPIO194	eTPU_A8/ eTPU_A20 SOUT_B_LVDS+ GPIO122
23	eMIOS2 eTPU_A2 GPIO181	eMIOS23 GPIO202	eTPU_A7/ eTPU_A19 SOUT_B_LVDS- eTPU_A6/ GPIO121	eTPU_A6/ eTPU_A18 SCK_B_LVDS+ GPIO120
24	eTPU_A20 IRQ8 GPIO134	eTPU_A22/ IRQ10 eTPU_A17 GPIO136	eTPU_A5/ eTPU_A17 SCK_B_LVDS- GPIO119	eTPU_A4 eTPU_A16 GPIO118
25	eTPU_A30/ PCS_C3 eTPU_A11 GPIO144	eTPU_A25/ IRQ13 SCK_C_LVDS+ GPIO139	eTPU_A3 eTPU_A15 GPIO117	SCK_B PCS_C1 GPIO102
26	AN21	AN1/ DAN0-	SOUT_B/PSC_C5 GPIO104	SIN_B/PCS_C2 GPIO103
27	AN0/ DAN0+	AN3/ DAN1-	eTPU_A0/ eTPU_A12 eTPU_A19 GPIO114	eMIOS0/ eTPU_A0 eTPU_A25 GPIO179
28	AN2/ DAN1+	AN5/ DAN2-	eMIOS10 GPIO189	eTPU_A1/ eTPU_A13 GPIO115
29	AN4/ DAN2+	AN7/ DAN3-	eTPU_A31/ PCS_C4 eTPU_A13 GPIO145	eTPU_A2 eTPU_A14 GPIO116
30	AN6/ DAN3+	AN25	TDO/ eMIOS6 GPIO228	eTPU_A13/ PCS_B3 GPIO127
31	AN23	AN31	VRH	EVTO/ eTPU_A4G GPIO227
32	AN28	AN35	GND	GND
33	AN33	AN8/ AN38/ ANW	5V	5V
34	GND	GND	GND	5V
35	GND	eTPU_A19_O	eTPU_A21_O	eTPU_A25_O
36	GND	eMIOS3/eTPUA3_O GPIO182	eMIOS6/eTPUA6_O GPIO185	eMIOS7/eTPUA7_O GPIO186

2.8 Jumper setting

Figure 14. Jumper setting

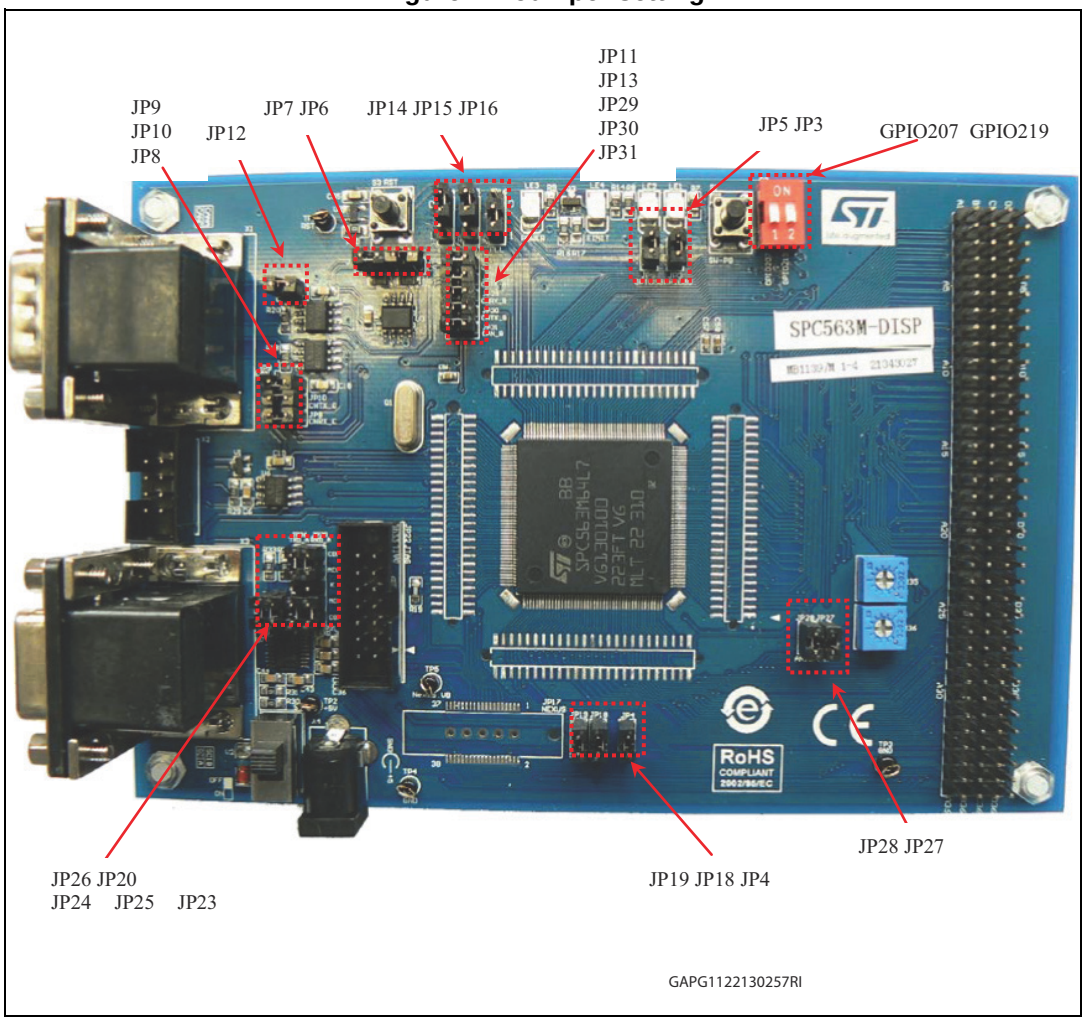


Table 4. Jumper Setting: JP12, JP9, JP10, JP8

JP12	JP9	JP10	JP8
R20, 120Ω	R18, 120Ω	TXO (U4 L9616)	RXO (U4 L9616)
CAN_H1	CAN_H2	CNTX_C	CNRX_C

Table 5. Jumper Setting: JP26, JP20, JP24, JP25, JP23, JP21

JP26	JP20	JP24	JP25	JP23	JP21
T2IN (U7 ST232)	R2OUT (U7 ST232)	5V (10k ohm to Vcc)	5V (10k ohm to Vcc)	TXD_B GPIO91	RXD_B GPIO92
TXD_A GPIO89	RXD_A GPIO90	T1IN (U7 ST232)	T2IN (U7 ST232)	T1IN (U7 ST232)	R1OUT (U7 ST232)

Table 6. Jumper Setting: JP7, JP6

JP7		JP6	
5V	W(M95128)	CS (M95128)	GPIO128

Table 7. Jumper Setting: JP14, JP15, JP16

JP14	JP15	JP16
GND (10kΩ ohm to GND)	GND (10kΩ ohm to GND)	GND (10kΩ ohm to GND)
WKPCFG	BOOTCFG1	PLLREF
5V (10kΩ ohm to Vcc)	5V (10kΩ ohm to Vcc)	5V (10kΩ ohm to Vcc)

Table 8. Jumper Setting: JP11, JP13, JP29, JP30, JP31

JP11	JP13	JP29	JP30	JP31
RXO (U5 L9616)	TXO (U5 L9616)	RXO (U8, L9616)	TXO (U8, L9616)	R40, 120Ω
CNRX_A	CNTX_A	CNRX_B	CNTX_B	CAN_L3
RXD_A	TXD_A	RXD_B	RXD_B	

Table 9. Jumper Setting: JP5, JP3

JP5	JP3
LED2	LED1
GPIO98	GPIO99

Table 10. Jumper Setting: GPIO207, GPIO219

GPIO207	GPIO219
ON(LOW)	ON(LOW)
OFF(HIGH)	OFF(HIGH)

Table 11. Jumper Setting: JP28, JP27

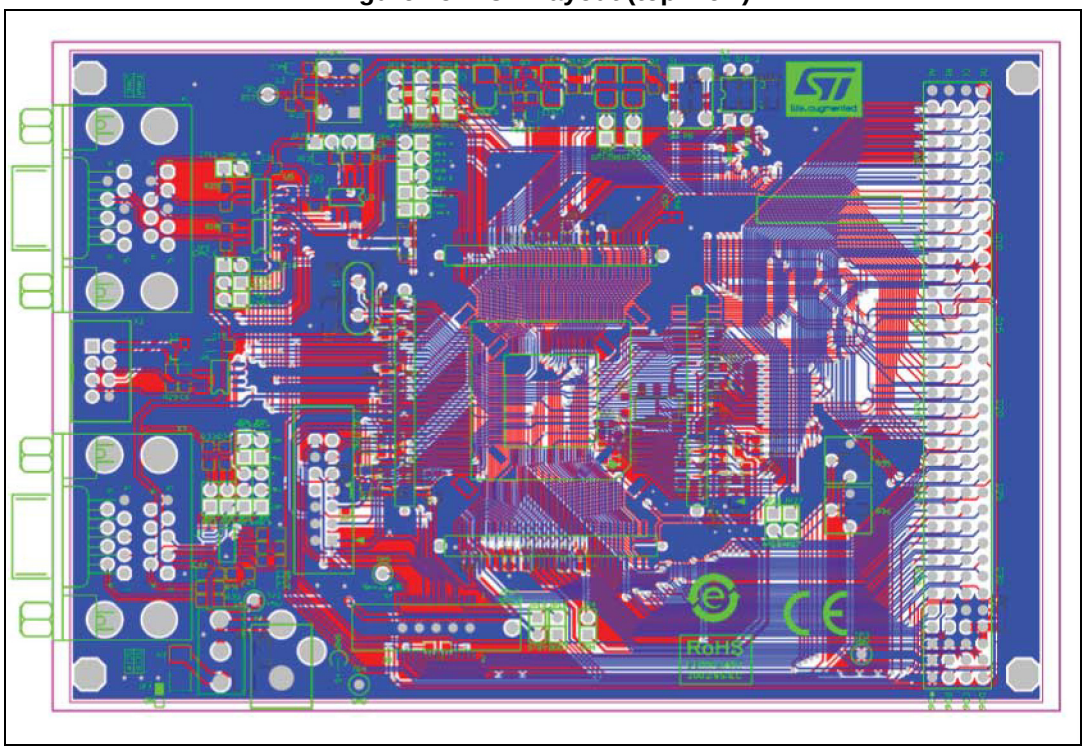
JP28	JP27
AN18	AN17
Potentiometer, R36	Potentiometer, R35

Table 12. Jumper Setting: JP19, JP18, JP4

JP19	JP18	JP4
VSTBY SRAM Standby voltage	VEN_IO2 (NEXUS)	VRH Voltage REF high
5V	BOOTCFG1	5VA

3 PCB layout

Figure 15. PCB Layout (top view)



Appendix A General handling precautions

The following precautions are recommended when using the SPC563M-DIS, discovery board:

- Do not modify or manipulate the board when the external PSU supply is powered and connected to the board.
- Do not open and modify the PSU. Use AC plug adaptor if the main socket is not compatible with the PSU plug.
- Do not supply the board with a DC source higher than 5 V.
- Any equipment or tool used for any manipulation of the semiconductor devices or board modification should be shielded and connected to ground.
- The connectors and cables should be plugged and removed when the board is not supplied.
- It is recommended to use antistatic tools.

Revision history

Table 13. Document revision history

Date	Revision	Changes
02-Dec-2013	1	Initial release.
13-Jul-2015	2	Changed value of DC source from 12 V to 5 V in *Appendix A: General handling precautions*.