SPC56AP60x, SPC56AP54x
SPC560P60x, SPC560P54x

32-bit Power Architecture® based MCU with 1088 KB Flash memory and 80 KB RAM for automotive chassis and safety applications

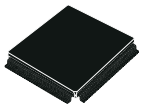
Datasheet – production data

Features

- 64 MHz, dual issue, 32-bit CPU core complex (e200z0h)
  - Compliant with Power Architecture® embedded category
  - Variable Length Encoding (VLE)
- Memory organizazion
  - Up to 1024 KB on-chip code Flash memory with additional 64 KB for EEPROM emulation (data flash), with ECC, with erase/program controller
  - Up to 80 KB on-chip SRAM with ECC
- Fail safe protection
  - ECC protection on system SRAM and Flash
  - Safety port
  - SWT with servicing sequence pseudo-random generator
  - Power management
  - Non-maskable interrupt for both cores
  - Fault collection and control unit (FCCU)
  - Safe mode of system-on-chip (SoC)
  - Register protection scheme
- Nexus® L2+ interface
- Single 3.3 V or 5 V supply for I/Os and ADC
- 2 on-platform peripherals set with 2 INTC
- 16-channel eDMA controller with multiple transfer request sources
- General purpose I/Os (80 GPIO + 26 GPI on LQFP144; 49 GPIO + 16 GPI on LQFP100)
- 2 general purpose eTimer units
  - 6 timers, each with up/down count capabilities
  - 16-bit resolution, cascadable counters
  - Quadrature decode with rotation direction flag
  - Double buffer input capture and output compare



LQFP100
14 x 14 mm



LQFP144
20 x 20 mm

- Communications interfaces
  - 2 LINFlex modules (LIN 2.1, 1 × Master/Slave, 1 × Master Only)
  - 5 DSPI modules with automatic chip select generation
  - 2 FlexCAN interfaces (2.0B Active) with 32 message buffers
  - 1 Safety port based on FlexCAN; usable as third CAN when not used as safety port
  - 1 FlexRay™ module (V2.1) with dual or single channel, 64 message buffers and up to 10 Mbit/s
- 2 CRC units with three contexts and 3 hardwired polynomials(CRC8,CRC32 and CRC-16-CCITT)
- 10-bit A/D converter
  - 27 input channels and pre-sampling feature
  - Conversion time < 1 µs including sampling time at full precision
  - Programmable cross triggering unit (CTU)
  - 4 analog watchdog with interrupt capability
- On-chip CAN/UART Bootstrap loader with boot assist module (BAM)
- Ambient temperature ranges: –40 to 125 °C or –40 to 105 °C

Table 1. Device summary

Package	Part number	
	768 KB Flash	1 MB Flash
LQFP144	SPC560P54L5 SPC56AP54L5	SPC560P60L5 SPC56AP60L5
LQFP100	SPC560P54L3 SPC56AP54L3	SPC560P60L3 SPC56AP60L3

This is information on a product in full production. www.st.com

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56xP54/60 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications specifically the airbag application.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 2 provides a summary of different members of the SPC56xP54/60 family and their features—relative to Full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC56xP54/60 device comparison

Feature	SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Code Flash memory (with ECC)	768 KB	1 MB	768 KB	1 MB
Data Flash / EE (with ECC)	64 KB			
SRAM (with ECC)	64 KB	80 KB	64 KB	80 KB
Processor core	32-bit e200z0h		32-bit Dual e200z0h	
Instruction set	VLE			
CPU performance	0-64 MHz			
FMPLL (frequency-modulated phase-locked loop) modules	1			
INTC (interrupt controller) channels	148			
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)			

Table 2. SPC56xP54/60 device comparison (continued)

Feature		SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Enhanced DMA (direct memory access) channels		16			
FlexRay		Yes (64 message buffer)			
FlexCAN (controller area network)		3(1),(2)			
Safety port		Yes (via third FlexCAN module)			
FCCU (fault collection and control unit)		Yes(3)			
CTU (cross triggering unit)		Yes			
eTimer channels		2 × 6			
FlexPWM (pulse-width modulation) channels		No			
Analog-to-digital converters (ADC)		One (10-bit, 27-channel)(4)			
LINFlex modules		2 (1 × Master/Slave, 1 × Master only)			
DSPI (deserial serial peripheral interface) modules		5(5)			
CRC (cyclic redundancy check) units		2(6)			
JTAG interface		Yes			
Nexus port controller (NPC)		Yes (Level 2+)(7)			
Supply	Digital power supply(8)	3.3 V or 5 V single supply with external transistor			
	Analog power supply	3.3 V or 5 V			
	Internal RC oscillator	16 MHz			
	External crystal oscillator	4–40 MHz			
Packages		LQFP100 LQFP144			LQFP100 LQFP144 LQFP176 (9)
Temperature	Standard ambient temperature	–40 to 125 °C			

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.
3. Enhanced FCCU version
4. Same amount of ADC channels as on SPC560P44/50 not considering the internally connected ones. 26 channels on LQFP144 and 16 channels on LQFP100.
5. Increased number of CS for DSPI_1
6. Upgraded specification with addition of 8-bits polynomial (CRC-8 VDA CAN) support and 3rd context
7. Improved debugging capability with data trace capability and increased Nexus throughput available on emulation package
8. 3.3 V range and 5 V range correspond to different orderable parts.
9. Software development package only. Not available for production.

SPC56xP54/60 is present on the market in two different options enabling different features: Full-featured, and Airbag configuration. *Table 3* shows the main differences between the two versions.

Table 3. SPC56xP54/60 device configuration difference

Feature	Full-featured	Airbag
CTU (cross triggering unit)	Yes	No
FlexRay	Yes (64 message buffer)	No
DSPI (deserial serial peripheral interface) modules	5	4
CRC (cyclic redundancy check) unit	2	1

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC56xP54/60 MCU. *Table 4* summarizes the functions of the blocks.

Figure 1. SPC56xP54/60 block diagram

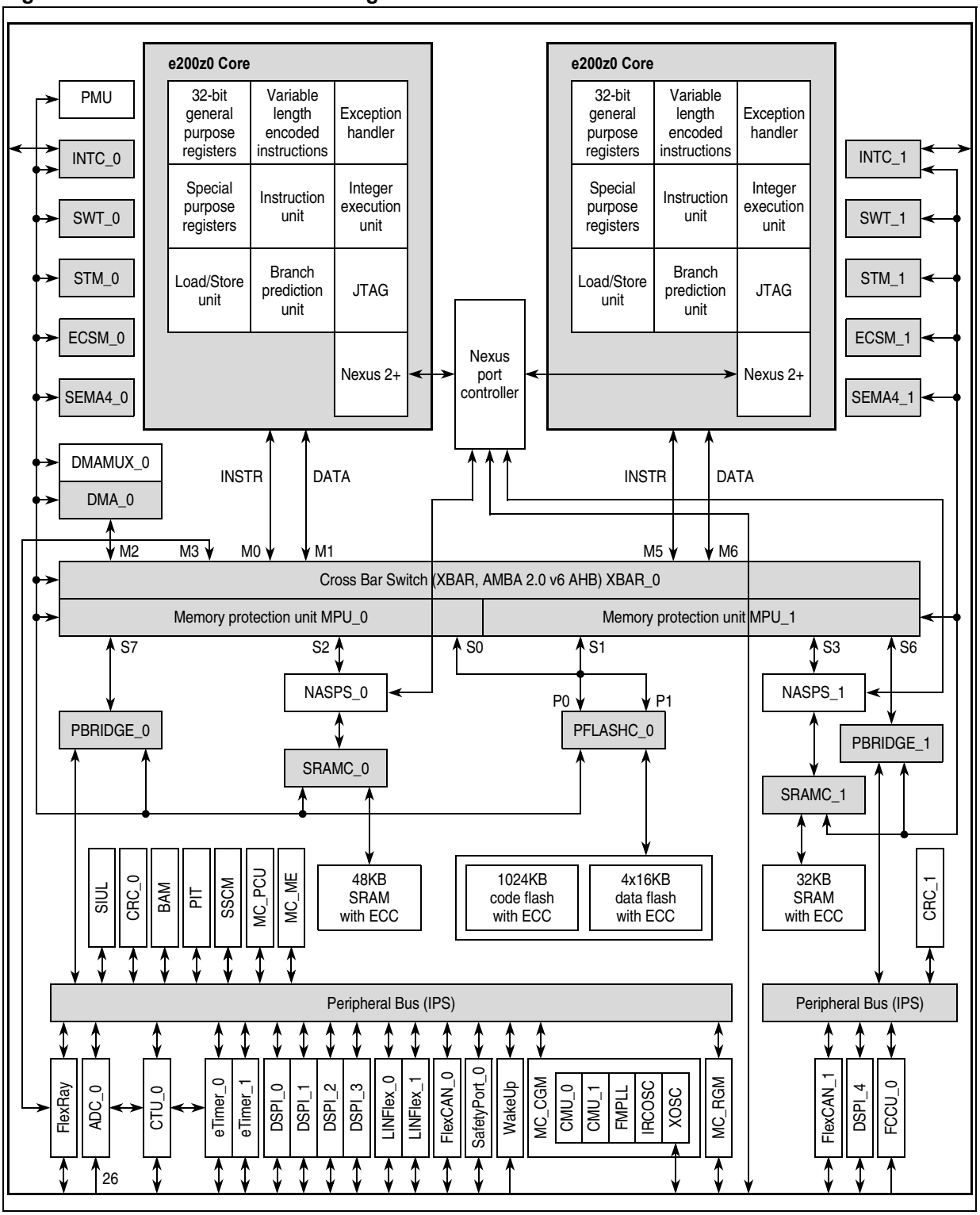


Table 4. SPC56xP54/60 series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.
Cyclic redundancy checker (CRC) unit	Is dedicated to the computation of CRC off-loading the CPU. Each context has a separate CRC computation engine in order to allow the concurrent computation of the CRC of multiple data streams.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection and control unit (FCCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexRay (FlexRay communication controller)	Provides high-speed distributed control for advanced automotive applications
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications

Table 4. SPC56xP54/60 series block summary (continued)

Block	Function
Peripheral bridge (PBRIDGE)	Is the interface between the system bus and on-chip peripherals
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Semaphore unit (SEMA4)	Provides the hardware support needed in multi-core systems for implementing semaphores and provide a simple mechanism to achieve lock/unlock operations via a single write access
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR(1) and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

1. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

1.5 Feature details

1.5.1 High performance e200z0h core processor

The e200z0h Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
  - Results in smaller code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non maskable Interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between six master ports and six slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 6 master ports:
  - 2 e200z0 core complex Instruction ports
  - 2 e200z0 core complex Load/Store Data ports
  - eDMA
  - FlexRay
- 6 slave ports:
  - 2 Flash memory (code flash and data flash)
  - 2 SRAM (48 KB + 32 KB)
  - 2 PBRIDGE
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels support independent 8, 16 or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, eTimer and CTU
- Programmable DMA Channel Multiplexer for assignment of any DMA source to any available DMA channel with up to 30 potential request sources
- eDMA abort operation through software

1.5.4 On-chip flash memory with ECC

The SPC56xP54/60 provides up to 1024 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module interfaces the system bus to a dedicated flash memory array controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 4x128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring 2 wait states.

The flash memory module provides the following features:

- Up to 1024 KB flash memory
  - 14 blocks (2×16 KB + 2×32 KB + 2×16 KB + 2×64 KB + 6×128 KB) code flash
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
  - Full Read While Write (RWW) capability between code and data flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait states for buffer hits, 2 wait states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis.
- Configurable access timing allowing use in a wide range of system frequencies.
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control.
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 On-chip SRAM with ECC

The SPC56xP54/60 SRAM module provides a general-purpose memory of up to 80 KB.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM memory from any master
- Up to 80 KB general purpose RAM
  - 2 blocks (48 KB + 32 KB)
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To

allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority.
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- 2 external high priority interrupts directly accessing the main core and IOP critical interrupt mechanism

The INTC module is replicated for each processor.

1.5.7 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC56xP54/60:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- Programmable output clock divider (÷1, ÷2, ÷3 to ÷256)
- eTimer module running at the same frequency as the e200z0h core
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode
  - Supports frequency trimming by user application

1.5.8 Frequency modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Modulation enabled/disabled through software
- Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency)
  - Programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.9 Main oscillator

The main oscillator provides these features:

- Input frequency range 4 MHz to 40 MHz
- Crystal input mode or Oscillator input mode
- PLL reference

1.5.10 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC Oscillator provides these features:

- Nominal frequency 16 MHz
- ±6% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.11 Periodic interrupt timer (PIT)

The PIT module implements these features:

- Up to four general purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel can be used as trigger for a DMA request

1.5.12 System timer module (STM)

The STM module implements these features:

- 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

The STM module is replicated for each processor.

1.5.13 Software watchdog timer (SWT)

The SWT has the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation

The SWT module is replicated for each processor.

1.5.14 Fault collection and control unit (FCCU)

The FCCU provides an independent fault reporting mechanism even if the CPU is exhibiting unstable behaviors. The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of self-test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, IRQ)
  - External reaction (failure is reported to the external/surrounding system via configurable output pins)

1.5.15 System integration unit (SIUL)

The SPC56xP54/60 SIUL controls MCU pad configuration, external interrupts, general purpose I/O (GPIO) pin configuration, and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIUL provides the following features:

- Centralized general purpose input output (GPIO) control of input/output pins and analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins (except ADC channels) can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIU
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination
  - Up to 4 internal functions can be multiplexed onto one pin

1.5.16 Boot and censorship

Different booting modes are available in the SPC56xP54/60:

- From internal flash memory
- Via a serial link

The default booting scheme is the one which uses the internal flash memory (an internal pull-down is used to select this mode). The alternate option allows the user to boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the contents of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC56xP54/60 devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex.
- BAM can accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory.

1.5.17 Error correction status module (ECSM)

The ECSM on this device features the following:

- Platform configuration and revision
- ECC error reporting for flash memory and SRAM
- ECC error injection for SRAM

The ECSM module is replicated for each processor.

1.5.18 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1 Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a six-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter

1.5.19 Safety port (FlexCAN)

The SPC56xP54/60 MCU has a second CAN controller synthesized to run at high bit rates to be used as a safety port. The CAN module of the safety port provides the following features:

- Identical to the FlexCAN module
- Bit rate as fast as 7.5 Mb at 60 MHz CPU clock using direct connection between CAN modules (no physical transceiver required)
- 32 Message buffers of 0 to 8 bytes data length
- Can be used as a third independent CAN module

1.5.20 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as Tx, Rx or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count and message ID
- Programmable acceptance filters for RxFIFO message buffers

1.5.21 Serial communication interface module (LINFlex)

The LINFlex on the SPC56xP54/60 features the following:

- Supports LIN Master mode (on both modules), LIN Slave mode (on one module) and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 Specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to 8 data bytes
  - Supports message length as long as 64 bytes
  - Detection and flagging of LIN errors: Sync field; Delimiter; ID parity; Bit; Framing; Checksum and Time-out errors
  - Classic or extended checksum calculation
  - Configurable Break duration as long as 36-bit times
  - Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

1.5.22 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC56xP54/60 MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 28 chip select lines available
  - 8 each on DSPI_0 and DSPI_1
  - 4 each on DSPI_2, DSPI_3, and DSPI_4
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.23 eTimer

Two eTimer modules are provided, each with six 16-bit general purpose up/down timer/counter per module. The following features are implemented:

- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0% to 100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock/2 — for external event counting
  - Equals peripheral clock — for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use

1.5.24 Analog-to-digital converter (ADC)

The ADC module provides the following features:

Analog part:

- 1 on-chip analog-to-digital converter
- 10-bit AD resolution
- 1 sample and hold unit per ADC
- Conversion time, including sampling time, less than 1 µs (at full precision)
- Typical sampling time is 150 ns min. (at full precision)
- Differential non-linearity error (DNL) ±1 LSB
- Integral non-linearity error (INL) ±1.5 LSB
- Total unadjusted error (TUE) <3 LSB
- Single-ended input signal range from 0 to 3.3 V / 5.0 V
- ADC and its reference can be supplied with a voltage independent from V_{DDIO}
- ADC supply can be equal or higher than V_{DDIO}
- ADC supply and the ADC reference are not independent from each other (they are internally bonded to the same pad)
- Sample times of 2 (default), 8, 64, or 128 ADC clock cycles

Digital part:

- 27 input channels (26 + 1 internally connected)
- 4 analog watchdogs to compare ADC results against predefined levels (low, high, range) before results are stored
- 2 operating modes: Normal mode and CTU control mode
- Normal mode features
  - Register-based interface with the CPU: control register, status register, 1 result register per channel
  - ADC state machine managing 3 request flows: regular command, hardware injected command, and software injected command
  - Selectable priority between software and hardware injected commands
  - DMA compatible interface
- CTU control mode features
  - Triggered mode only
  - 4 independent result queues (2 × 16 entries, 2 × 4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit part
  - DMA compatible interfaces

1.5.25 Cross triggering unit (CTU)

The Cross Triggering Unit (CTU) allows automatic generation of ADC conversion requests on user selected conditions with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with up to eight independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each Trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with up to 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection

1.5.26 Cyclic redundancy check (CRC)

- 3 contexts for the concurrent CRC computation
- Separate CRC engine for each context
- Zero-wait states during the CRC computation (pipeline scheme)
- 3 hard-wired polynomials (CRC-8 VDA CAN, CRC-32 ethernet and CRC-16-CCITT)
- Support for byte/half-word/word width of the input data stream
- Support for expected and actual CRC comparison

1.5.27 Nexus development interface (NDI)

The NDI block provides real-time development support capabilities for the SPC56xP54/60 Power Architecture based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal buses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
  - DDR
- Auxiliary Output Port
  - 4 MDO (Message Data Out) pins
  - MCKO (Message Clock Out) pin
  - 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - $\overline{\text{EVTI}}$ (Event In) pin

1.5.28 IEEE 1149.1 (JTAG) controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with four pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_CORE0, ACCESS_AUX_TAP_CORE1, ACCESS_AUX_TAP_NASPS_0, ACCESS_AUX_TAP_NASPS_1
- Three test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

1.5.29 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

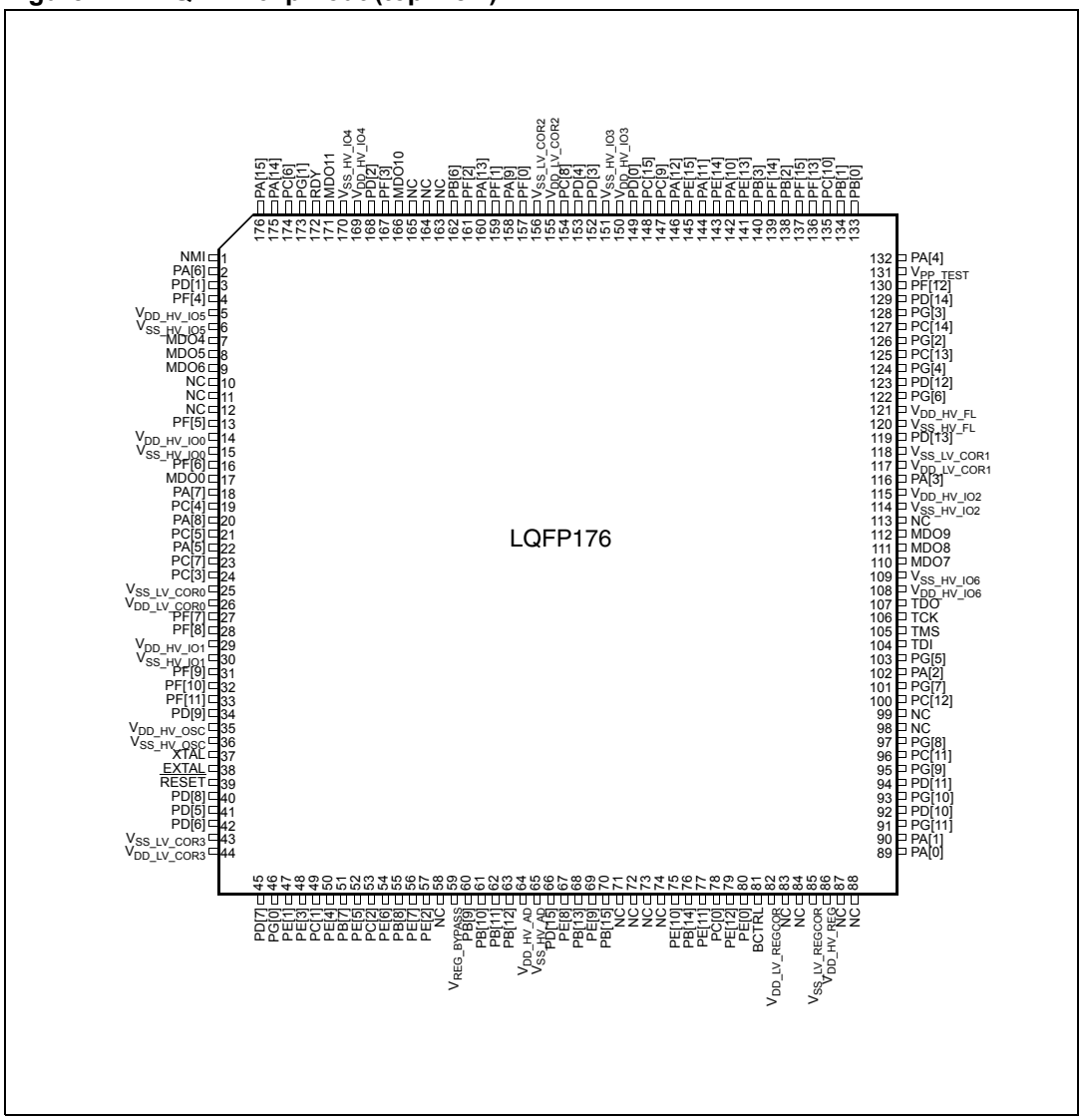
- Uses external NPN transistor
- Regulates external 3.3 V to 5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

2 Package pinouts and signal descriptions

2.1 Package pinouts

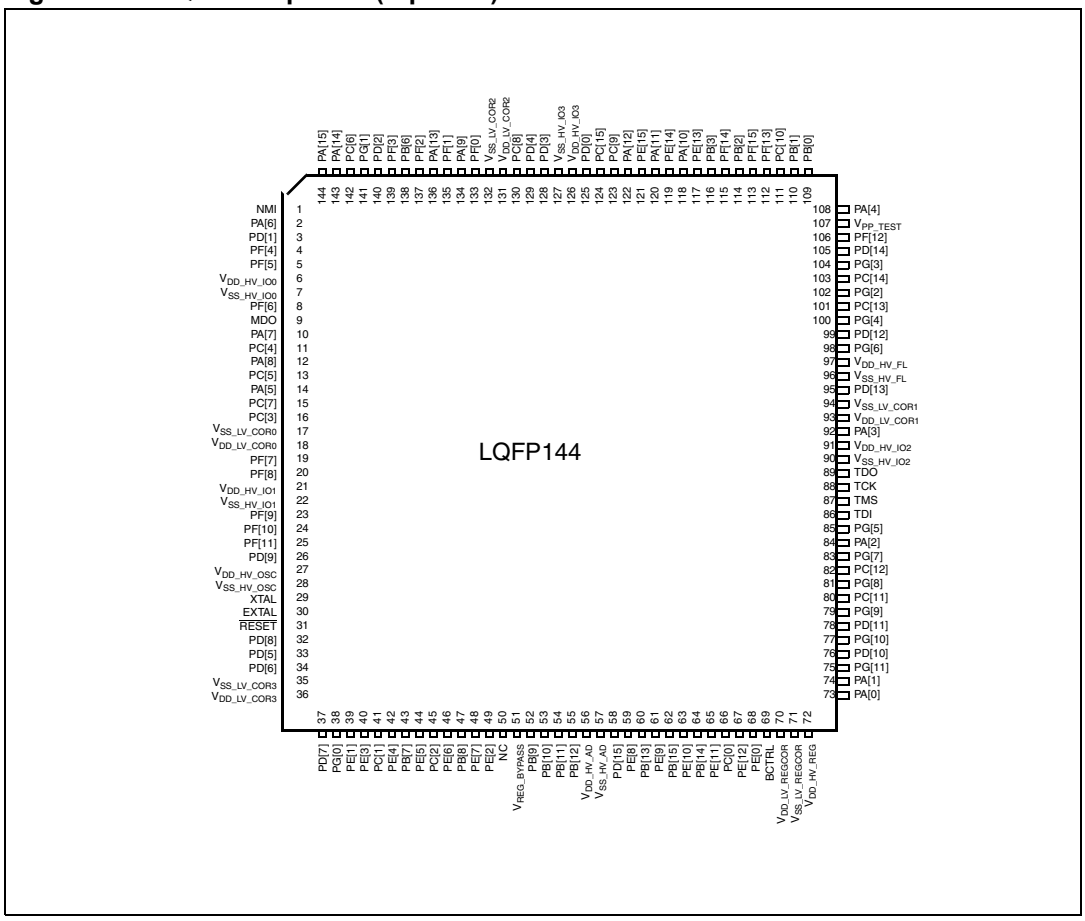
The LQFP pinouts are shown in the following figures.

Figure 2. LQFP176 pinout (top view)[a]



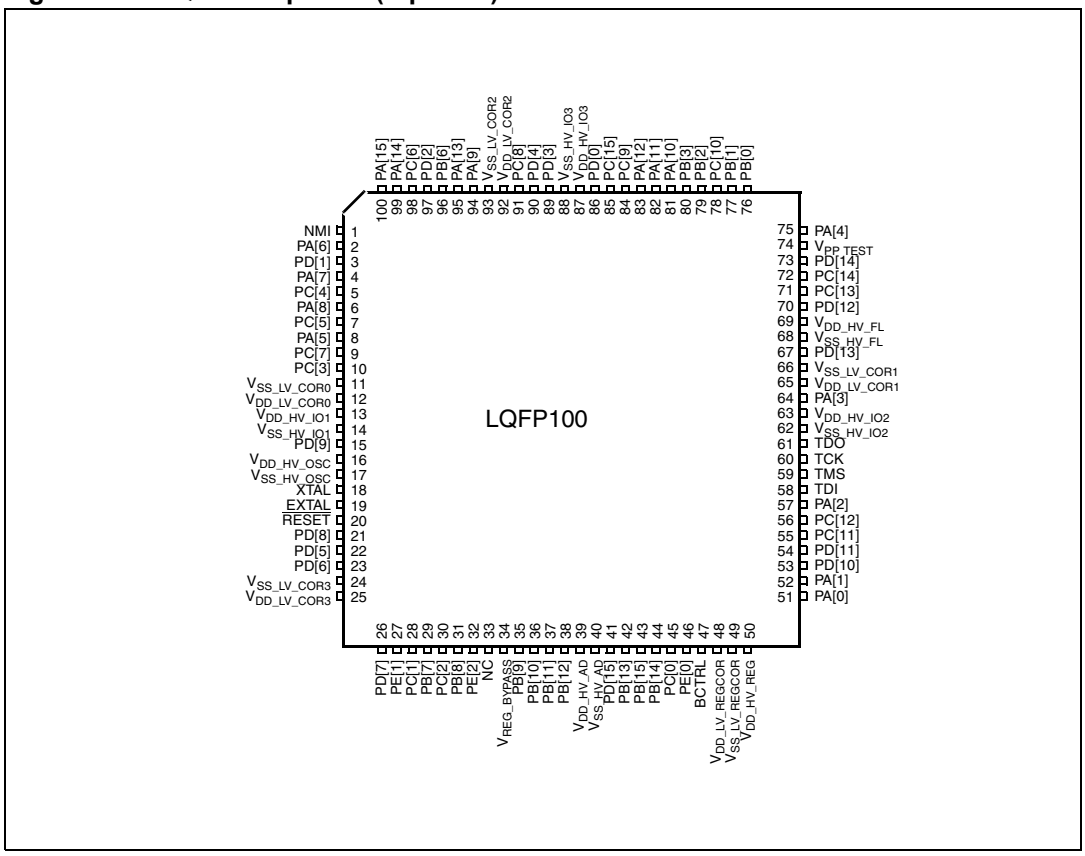
a. Software development package only. Not available for production.

Figure 3. LQFP144 pinout (top view)[(b)]



b. Availability of port pin alternate functions depends on product selection

Figure 4. LQFP100 pinout (top view)(c)



2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC56xP54/60 devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC56xP54/60 devices.

Table 5. Supply pins

Supply		Pin		
Symbol	**Description**	**LQFP 100**	**LQFP 144**	**LQFP 176(1)**
VREG control and power supply pins				
BCTRL	Voltage regulator external NPN Ballast base control pin	47	69	81
$V_{DD_HV_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72	86

c. Availability of port pin alternate functions depends on product selection

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	**Description**	**LQFP 100**	**LQFP 144**	**LQFP 176(1)**
$V_{DD_LV_REGCOR}$	1.2 V decoupling(2) pins for core logic supply and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS_LV_REGCOR}$.	48	70	82
$V_{SS_LV_REGCOR}$	1.2 V decoupling(2) pins for core logic GND and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD_LV_REGCOR}$.	49	71	85
ADC0 reference and supply voltage				
$V_{DD_HV_AD}$	ADC supply and high reference voltage	39	56	64
$V_{SS_HV_AD}$	ADC ground and low reference voltage	40	57	65
Power supply pins (3.3 V or 5.0 V)				
$V_{DD_HV_IO0}$	Input/Output supply voltage	—	6	14
$V_{SS_HV_IO0}$	Input/Output ground	—	7	15
$V_{DD_HV_IO1}$	Input/Output supply voltage	13	21	29
$V_{SS_HV_IO1}$	Input/Output ground	14	22	30
$V_{DD_HV_IO2}$	Input/Output supply voltage	63	91	115
$V_{SS_HV_IO2}$	Input/Output ground	62	90	114
$V_{DD_HV_IO3}$	Input/Output supply voltage	87	126	150
$V_{SS_HV_IO3}$	Input/Output ground	88	127	151
$V_{DD_HV_IO4}$	Input/Output supply voltage	—	—	169
$V_{SS_HV_IO4}$	Input/Output ground	—	—	170
$V_{DD_HV_IO5}$	Input/Output supply voltage	—	—	5
$V_{SS_HV_IO5}$	Input/Output ground	—	—	6
$V_{DD_HV_IO6}$	Input/Output supply voltage	—	—	108
$V_{SS_HV_IO6}$	Input/Output ground	—	—	109
$V_{DD_HV_FL}$	Code and data flash supply voltage	69	97	121
$V_{SS_HV_FL}$	Code and data flash supply ground	68	96	120
$V_{DD_HV_OSC}$	Crystal oscillator amplifier supply voltage	16	27	35
$V_{SS_HV_OSC}$	Crystal oscillator amplifier ground	17	28	36
Power supply pins (1.2 V)				
$V_{DD_LV_COR0}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR0}$ pin.	12	18	26
$V_{SS_LV_COR0}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR0}$ pin.	11	17	25

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	Description	LQFP 100	LQFP 144	LQFP 176[1]
$V_{DD_LV_COR1}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR1}$ pin.	65	93	117
$V_{SS_LV_COR1}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR1}$ pin.	66	94	118
$V_{DD_LV_COR2}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR2}$ pin.	92	131	155
$V_{SS_LV_COR2}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR\ 2}$ pin.	93	132	156
$V_{DD_LV_COR3}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR3}$ pin.	25	36	44
$V_{SS_LV_COR3}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR\ 3}$ pin.	24	35	43

1. LQFP176 available only as development package.
2. See datasheet Voltage Regulator Electrical Characteristics section for more details.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC56xP54/60 devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad Speed[1]		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176[2]
Dedicated pins							
MDO0	Nexus Message Data Output—line 0	Output Only	Fast		—	9	17
MDO4	Nexus Message Data Output—line 4	Output Only	Fast		—	—	7
MDO5	Nexus Message Data Output—line 5	Output Only	Fast		—	—	8
MDO6	Nexus Message Data Output—line 6	Output Only	Fast		—	—	9

Table 6. System pins (continued)

Symbol	Description	Direction	Pad Speed(1)		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176(2)
MDO7	Nexus Message Data Output—line 7	Output Only	Fast		—	—	110
MDO8	Nexus Message Data Output—line 8	Output Only	Fast		—	—	111
MDO9	Nexus Message Data Output—line 9	Output Only	Fast		—	—	112
MDO10	Nexus Message Data Output—line 10	Output Only	Fast		—	—	166
MDO11	Nexus Message Data Output—line 11	Output Only	Fast		—	—	171
RDY	Nexus ready output	Output Only	—	—	—	—	172
NMI	Non-Maskable Interrupt	Input Only	—	—	1	1	1
XTAL	Analog output of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.	—	—	—	18	29	37
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	—	—	—	19	30	38
TMS(3)	JTAG state machine control	Input Only	—	—	59	87	105
TCK(3)	JTAG clock	Input Only	—	—	60	88	106
TDI(3)	JTAG data input	Input Only	—	—	58	86	104
TDO(3)	JTAG data output	Output Only	—	—	61	89	107
Reset pin							
$\overline{\text{RESET}}$(4)	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31	39
Test pin							
$V_{PP\ TEST}$	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107	131
V_{REG_BYPASS}	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	34	51	59

1. SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.
2. LQFP176 available only as development package.
3. In this pin there is an internal pull, refer to JTAGC chapter in the device reference manual for pull direction.
4. Its configuration can be set up by the PCR[108] register inside the SIU module. See SIUL chapter in the device reference manual.

2.2.3 Pin muxing

Table 7 defines the pin list and muxing for the SPC56xP54/60 devices relative to Full-featured version.

Each row of *Table 7* shows all the possible ways of configuring each pin, via “alternate functions”. The default function assigned to each pin after reset is the ALT0 function.

Pins marked as external interrupt capable can also be used to resume from STOP and HALT mode.

SPC56xP54/60 devices provide four main I/O pad types depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

Table 7. Pin muxing(1)

Port pin	PCR register	Alternate function (2),(3)	Functions	Peripheral (4)	I/O direction (5)	Pad speed(6)		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176(7)
Port A										
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK_2 F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCCU SIUL	I/O I/O I/O O I	Slow	Medium	51	73	89
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT_2 F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCCU SIUL	I/O I/O O O I	Slow	Medium	52	74	90
A[2](8)	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] CS3 — SIN_2 ABS[0] EIRQ[2]	SIUL eTimer_0 DSPI_4 — DSPI_2 MC_RGM SIUL	I/O I/O O — I I I	Slow	Medium	57	84	102

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function [2],[3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
A[3][8]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0_2 — ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 — MC_RGM SIUL	I/O I/O I/O — I I	Slow	Medium	64	92	116
A[4][8]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1_2 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108	132
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0_1 ETC[5] CS7_0 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14	22
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK_1 CS2_4 — EIRQ[6]	SIUL DSPI_1 DSPI_4 — SIUL	I/O I/O I/O — I	Slow	Medium	2	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 —	GPIO[7] SOUT_1 CS1_4 — EIRQ[7]	SIUL DSPI_1 DSPI_4 — SIUL	I/O O I/O — I	Slow	Medium	4	10	18
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — CS0_4 — SIN_1 EIRQ[8]	SIUL — DSPI_4 — DSPI_1 SIUL	I/O — I/O — I I	Slow	Medium	6	12	20
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3 —	GPIO[9] CS1_2 — — SIN_4	SIUL DSPI_2 — — DSPI_4	I/O O — — I	Slow	Medium	94	134	158

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function (2),(3)	Functions	Peripheral (4)	I/O direction (5)	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3 —	GPIO[10] CS0_2 — — EIRQ[9]	SIUL DSPI_2 — — SIUL	I/O I/O — — I	Slow	Medium	81	118	142
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK_2 — — EIRQ[10]	SIUL DSPI_2 — — SIUL	I/O I/O — — I	Slow	Medium	82	120	144
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT_2 — — EIRQ[11]	SIUL DSPI_2 — — SIUL	I/O O — — I	Slow	Medium	83	122	146
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[13] CS4_1 — — SIN_2 EIRQ[12]	SIUL DSPI_1 — — DSPI_2 SIUL	I/O — — — I I	Slow	Medium	95	136	160
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD ETC[4] CS5_1 EIRQ[13]	SIUL Safety Port eTimer_1 DSPI_1 SIUL	I/O O I/O O I	Slow	Medium	99	143	175
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] CS6_1 ETC[5] — RXD EIRQ[14]	SIUL DSPI_1 eTimer_1 — Safety Port SIUL	I/O O I/O — I I	Slow	Medium	100	144	176
Port B										
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD ETC[2] DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 eTimer_1 SSCM SIUL	I/O O I/O — I	Slow	Medium	76	109	133

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function [2],[3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] CS7_1 ETC[3] DEBUG[1] RXD EIRQ[16]	SIUL DSPI_1 eTimer_1 SSCM FlexCAN_0 SIUL	I/O O I/O — I I	Slow	Medium	77	110	134
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD SOUT_4 DEBUG[2] EIRQ[17]	SIUL LINFlex_0 DSPI_4 SSCM SIUL	I/O O I/O — I	Slow	Medium	79	114	138
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — SCK_4 DEBUG[3] RXD	SIUL — DSPI_4 SSCM LINFlex_0	I/O — I/O — I	Slow	Medium	80	116	140
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] clk_out CS2_2 clk_out_div256 EIRQ[18]	SIUL MC_CGL DSPI_2 MC_CGL SIUL	I/O O O O I	Slow	Medium	96	138	162
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LINFlex_0	Input Only	—	—	29	43	51
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input Only	—	—	31	47	55
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIUL — — — ADC_0	Input Only	—	—	35	52	60

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function[2],[3]	Functions	Peripheral[4]	I/O direction[5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIUL — — — ADC_0	Input Only	—	—	36	53	61
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3 —	GPIO[27] — — — AN[13]	SIUL — — — ADC_0	Input Only	—	—	37	54	62
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — — — AN[14]	SIUL — — — ADC_0	Input Only	—	—	38	55	63
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[29] — — — AN[16] RXD	SIUL — — — ADC_0 LINFlex_1	Input Only	—	—	42	60	68
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[30] — — — AN[17] ETC[4] EIRQ[19]	SIUL — — — ADC_0 eTimer_0 SIUL	Input Only	—	—	44	64	76
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[31] — — — AN[18] EIRQ[20]	SIUL — — — ADC_0 SIUL	Input Only	—	—	43	62	70
Port C										
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3 —	GPIO[32] — — — AN[19]	SIUL — — — ADC_0	Input Only	—	—	45	66	78

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function[2],[3]	Functions	Peripheral[4]	I/O direction[5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 —	GPIO[33] — — — AN[2]	SIUL — — — ADC_0	Input Only	—	—	28	41	49
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 —	GPIO[34] — — — AN[3]	SIUL — — — ADC_0	Input Only	—	—	30	45	53
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 —	GPIO[35] CS1_0 ETC[4] TXD EIRQ[21]	SIUL DSPI_0 eTimer_1 LINFlex_1 SIUL	I/O O I/O O I	Slow	Medium	10	16	24
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 —	GPIO[36] CS0_0 — DEBUG[4] EIRQ[22]	SIUL DSPI_0 — SSCM SIUL	I/O I/O — — I	Slow	Medium	5	11	19
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 —	GPIO[37] SCK_0 SCK_4 DEBUG[5] EIRQ[23]	SIUL DSPI_0 DSPI_4 SSCM SIUL	I/O I/O I/O — I	Slow	Medium	7	13	21
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT_0 — DEBUG[6] EIRQ[24]	SIUL DSPI_0 — SSCM SIUL	I/O O — — I	Slow	Medium	98	142	174
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[39] — — DEBUG[7] SIN_0 SIN_4	SIUL — — SSCM DSPI_0 DSPI_4	I/O — — — I I	Slow	Medium	9	15	23
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3	GPIO[40] CS1_1 CS1_4 CS6_0	SIUL DSPI_1 DSPI_4 DSPI_0	I/O O O O	Slow	Medium	91	130	154

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function[2],[3]	Functions	Peripheral[4]	I/O direction[5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3	GPIO[41] CS3_2 CS0_4 —	SIUL DSPI_2 DSPI_4 —	I/O O I/O —	Slow	Medium	84	123	147
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3	GPIO[42] CS2_2 CS2_4 —	SIUL DSPI_2 DSPI_4 —	I/O O O —	Slow	Medium	78	111	135
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[4] CS2_2 CS0_3	SIUL eTimer_0 DSPI_2 DSPI_3	I/O I/O O I/O	Slow	Medium	55	80	96
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	GPIO[44] ETC[5] CS3_2 CS1_3	SIUL eTimer_0 DSPI_2 DSPI_3	I/O I/O O O	Slow	Medium	56	82	100
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[45] ETC[1] — — EXT_IN RXD	SIUL eTimer_1 — — CTU_0 FlexCAN_1	I/O I/O — — I I	Slow	Medium	71	101	125
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3	GPIO[46] ETC[2] EXT_TGR TXD	SIUL eTimer_1 CTU_0 FlexCAN_1	I/O I/O O O	Slow	Medium	72	103	127
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 —	GPIO[47] CA_TR_EN ETC[0] — EXT_IN	SIUL FlexRay_0 eTimer_1 — CTU_0	I/O O I/O — I	Slow	Symmet-ric	85	124	148
Port D										
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] CA_TX ETC[1] —	SIUL FlexRay_0 eTimer_1 —	I/O O I/O —	Slow	Symmet-ric	86	125	149

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function[2],[3]	Functions	Peripheral[4]	I/O direction[5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3 —	GPIO[49] CS4_1 ETC[2] EXT_TRG CA_RX	SIUL DSPI_1 eTimer_1 CTU_0 FlexRay_0	I/O O I/O O I	Slow	Medium	3	3	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3 —	GPIO[50] CS5_1 ETC[3] — CB_RX	SIUL DSPI_1 eTimer_1 — FlexRay_0	I/O O I/O — I	Slow	Medium	97	140	168
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] CB_TX ETC[4] —	SIUL FlexRay_0 eTimer_1 —	I/O O I/O —	Slow	Symmet-ric	89	128	152
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] CB_TR_EN ETC[5] —	SIUL FlexRay_0 eTimer_1 —	I/O O I/O —	Slow	Symmet-ric	90	129	153
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3_0 — SOUT_3	SIUL DSPI_0 — DSPI_3	I/O O — O	Slow	Medium	22	33	41
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3	GPIO[54] CS2_0 SCK_3 SOUT_4	SIUL DSPI_0 DSPI_3 DSPI_4	I/O O I/O O	Slow	Medium	23	34	42
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3_1 — CS4_0 SIN_3	SIUL DSPI_1 — DSPI_0 DSPI_3	I/O O — O I	Slow	Medium	26	37	45
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2_1 RDY CS5_0	SIUL DSPI_1 nexus_0 DSPI_0	I/O O O O	Slow	Medium	21	32	40
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] — TXD CS6_1	SIUL — LINFlex_1 DSPI_1	I/O — O O	Slow	Medium	15	26	34

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function [2],[3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] — CS0_3 —	SIUL — DSPI_3 —	I/O — I/O —	Slow	Medium	53	76	92
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] — CS1_3 SCK_3	SIUL — DSPI_3 DSPI_3	I/O — O I/O	Slow	Medium	54	78	94
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] — — DS7_1 RXD	SIUL — — DSPI_1 LINFlex_1	I/O — — O I	Slow	Medium	70	99	123
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] — CS2_3 SOUT_3	SIUL — DSPI_3 DSPI_3	I/O — O O	Slow	Medium	67	95	119
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] — CS3_3 — SIN_3	SIUL — DSPI_3 — DSPI_3	I/O — O — I	Slow	Medium	73	105	129
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[20]	SIUL — — — ADC_0	Input Only	—	—	41	58	66
Port E										
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[21]	SIUL — — — ADC_0	Input Only	—	—	46	68	80
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input Only	—	—	27	39	47

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function [2],[3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input Only	—	—	32	49	57
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input Only	—	—	—	40	48
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input Only	—	—	—	42	50
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input Only	—	—	—	44	52
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input Only	—	—	—	46	54
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input Only	—	—	—	48	56
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3 —	GPIO[72] — — — AN[22]	SIUL — — — ADC_0	Input Only	—	—	—	59	67
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3 —	GPIO[73] — — — AN[23]	SIUL — — — ADC_0	Input Only	—	—	—	61	69

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function [2],[3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3 —	GPIO[74] — — — AN[24]	SIUL — — — ADC_0	Input Only	—	—	—	63	75
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3 —	GPIO[75] — — — AN[25]	SIUL — — — ADC_0	Input Only	—	—	—	65	77
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3 —	GPIO[76] — — — AN[26]	SIUL — — — ADC_0	Input Only	—	—	—	67	79
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3 —	GPIO[77] SCK_3 — — EIRQ[25]	SIUL DSPI_3 — — SIUL	I/O I/O — — I	Slow	Medium	—	117	141
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3 —	GPIO[78] SOUT_3 — — EIRQ[26]	SIUL DSPI_3 — — SIUL	I/O O — — I	Slow	Medium	—	119	143
E[15]	PCR[79]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[79] — — — SIN_3 EIRQ[27]	SIUL — — — DSPI_3 SIUL	I/O — — — I I	Slow	Medium	—	121	145
Port F										
F[0]	PCR[80]	ALT0 ALT1 ALT2 ALT3 —	GPIO[80] DBG_0 CS3_3 — EIRQ[28]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	133	157

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function (2),(3)	Functions	Peripheral (4)	I/O direction (5)	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
F[1]	PCR[81]	ALT0 ALT1 ALT2 ALT3 —	GPIO[81] DBG_1 CS2_3 — EIRQ[29]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	135	159
F[2]	PCR[82]	ALT0 ALT1 ALT2 ALT3	GPIO[82] DBG_2 CS1_3 —	SIUL FlexRay_0 DSPI_3 —	I/O O O —	Slow	Medium	—	137	161
F[3]	PCR[83]	ALT0 ALT1 ALT2 ALT3	GPIO[83] DBG_3 CS0_3 —	SIUL FlexRay_0 DSPI_3 —	I/O O I/O —	Slow	Medium	—	139	167
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	— — MDO[3] —	— — nexus_0 —	— — O —	Slow	Fast	—	4	4
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	— — MDO[2] —	— — nexus_0 —	— — O —	Slow	Fast	—	5	13
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] — MDO[1] —	SIUL — nexus_0 —	I/O — O —	Slow	Fast	—	8	16
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	GPIO[87] — MCKO —	SIUL — nexus_0 —	I/O — O —	Slow	Fast	—	19	27
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	GPIO[88] — MSEO1 —	SIUL — nexus_0 —	I/O — O —	Slow	Fast	—	20	28
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	GPIO[89] — MSEO0 —	SIUL — nexus_0 —	I/O — O —	Slow	Fast	—	23	31

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function (2),(3)	Functions	Peripheral (4)	I/O direction (5)	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	GPIO[90] — EVTO —	SIUL — nexus_0 —	I/O — O —	Slow	Fast	—	24	32
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3	GPIO[91] EVTI — —	SIUL nexus_0 — —	I/O I — —	Slow	Medium	—	25	33
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[3] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	106	130
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3	GPIO[93] ETC[4] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	112	136
F[14]	PCR[94]	ALT0 ALT1 ALT2 ALT3	GPIO[94] TXD — —	SIUL LINFlex_1 — —	I/O O — —	Slow	Medium	—	115	139
F[15]	PCR[95]	ALT0 ALT1 ALT2 ALT3 —	GPIO[95] — — — RXD	SIUL — — — LINFlex_1	I/O — — — I	Slow	Medium	—	113	137
Port G										
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3 —	GPIO[96] F[0] — — EIRQ[30]	SIUL FCCU — — SIUL	I/O O — — I	Slow	Medium	—	38	46
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIUL FCCU — — SIUL	I/O O — — I	Slow	Medium	—	141	173

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function [2],[3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3 —	GPIO[98] — — — SIN_4	SIUL — — — DSPI_4	I/O — — — I	Slow	Medium	—	102	126
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] — SOUT_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	104	128
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] — SCK_4 —	SIUL — DSPI_4 —	I/O — I/O —	Slow	Medium	—	100	124
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] — CS0_4 —	SIUL — DSPI_4 —	I/O — I/O —	Slow	Medium	—	85	103
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] — CS1_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	98	122
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	GPIO[103] — CS2_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	83	101
G[8]	PCR[104]	ALT0 ALT1 ALT2 ALT3 —	GPIO[104] — CS3_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	81	97
G[9]	PCR[105]	ALT0 ALT1 ALT2 ALT3 —	GPIO[105] — — — RXD	SIUL — — — FlexCAN_1	I/O — — — I	Slow	Medium	—	79	95

Table 7. Pin muxing[1] (continued)

Port pin	PCR register	Alternate function (2),(3)	Functions	Peripheral (4)	I/O direction (5)	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
G[10]	PCR[106]	ALT0 ALT1 ALT2 ALT3	GPIO[106] — TXD —	SIUL — FlexCAN_1 —	I/O — O —	Slow	Medium	—	77	93
G[11]	PCR[107]	ALT0 ALT1 ALT2 ALT3	GPIO[107] — — —	SIUL — — —	I/O — — —	Slow	Medium	—	75	91

1. This table concerns Full-featured version. Please refer to “SPC56xP54/60 device configuration difference” table for difference between Full-featured, and Airbag configuration.
2. ALT0 is the primary (default) function for each port after reset.
3. Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIU module. PCR[PA] = 00 → ALT0; PCR[PA] = 01 → ALT1; PCR[PA] = 10 → ALT2; PCR[PA] = 11 → ALT3. This is intended to select the output functions; to use one of the input-only functions, the PCR[IBE] bit must be written to ‘1’, regardless of the values selected in the PCR[PA] bitfields. For this reason, the value corresponding to an input only function is reported as “—”.
4. Module included on the MCU.
5. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMI[PADSEL*x*] bitfields inside the SIUL module.
6. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
7. LQFP176 available only as development package.
8. Weak pull down during reset.

3 Electrical characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All of the following parameter values can vary depending on the application and must be confirmed during silicon validation, silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Min	Max[2]	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD_HV_IOx}$[3]	SR	3.3 V / 5.0 V input/output supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD_HV_FL}$	SR	3.3 V / 5.0 V code and data flash memory supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD_HV_IOx}$	–0.3	$V_{DD_HV_IOx}$ + 0.3	
$V_{SS_HV_FL}$	SR	Code and data flash memory ground with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD_HV_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD_HV_IOx}$	–0.3	$V_{DD_HV_IOx}$ + 0.3	
$V_{SS_HV_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD_HV_REG}$	SR	3.3 V / 5.0 V voltage regulator supply voltage with respect to ground (V_{SS_HV})	—	– 0.3	6.0	V
			Relative to $V_{DD_HV_IOx}$	– 0.3	$V_{DD_HV_IOx}$ + 0.3	
$V_{DD_HV_AD}$	SR	3.3 V / 5.0 V ADC supply and high reference voltage with respect to ground (V_{SS_HV})	$V_{DD_HV_REG}$ < 2.7 V	– 0.3	$V_{DD_HV_REG}$ + 0.3	V
			$V_{DD_HV_REG}$ > 2.7 V	– 0.3	6.0	
$V_{SS_HV_AD}$	SR	ADC ground and low reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
TV_{DD}[4]	SR	Slope characteristics on all V_{DD} during power up[5] with respect to ground (V_{SS_HV})	—	0.25	250	V/ms
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS_HV_IOx}$) with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD_HV_IOx}$	–0.3	$V_{DD_HV_IOx}$ + 0.3	
V_{INAN}	SR	Analog input voltage	$V_{DD_HV_REG}$ < 2.7 V	$V_{SS_HV_AD}$ – 0.3	$V_{DD_HV_AD}$ + 0.3	V
			$V_{DD_HV_REG}$ > 2.7 V	$V_{SS_HV_AD}$	$V_{DD_HV_AD}$	V
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA

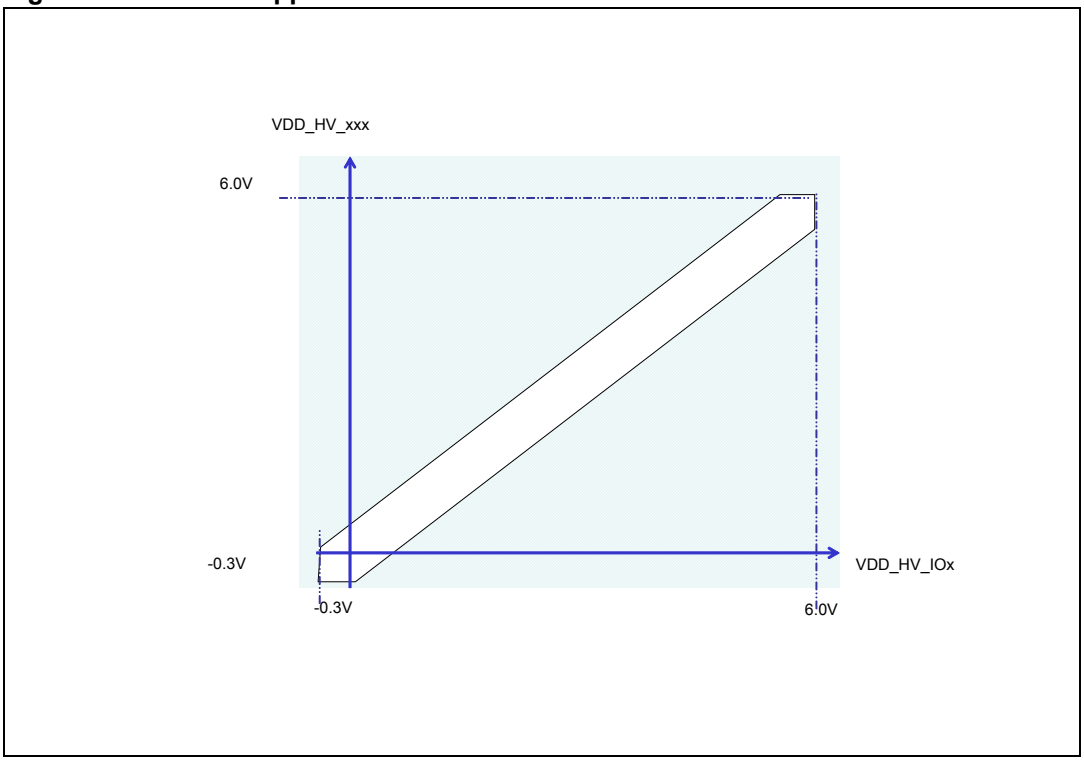
Table 9. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Min	Max(2)	Unit
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
I_{VDD_LV}	SR	Low voltage static current sink through V_{DD_LV}	—	—	155	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
3. The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 300$ mV.
4. Ensure a monotonic supply ramp starting at ground level
5. Guaranteed by device validation

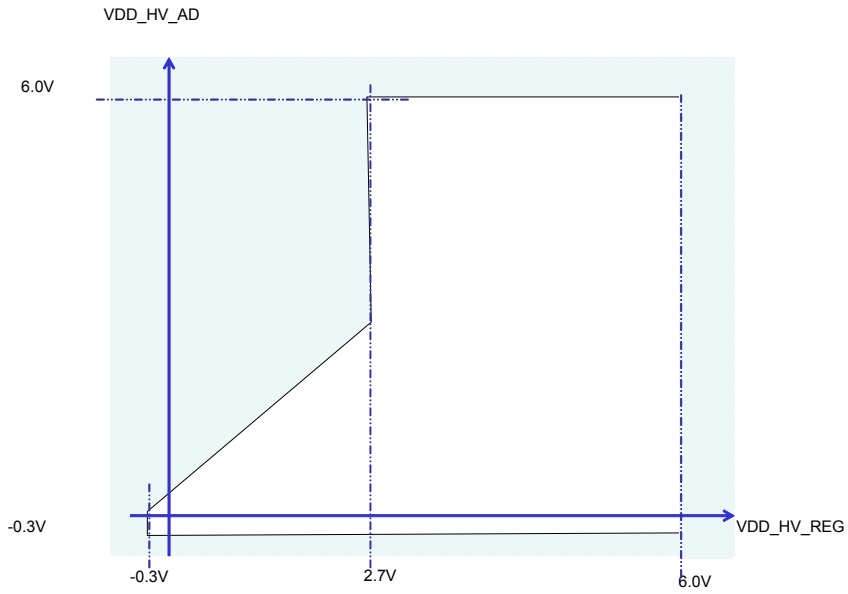
Figure 5 shows the constraints of the different power supplies.

Figure 5. Power supplies constraints



The SPC56xP54/60 supply architecture provides an ADC supply that is managed independently of standard V_{DD_HV} supply. *Figure 6* shows the constraints of the ADC power supply.

Figure 6. Independent ADC supply[d]



3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD_HV_IOx}$[2]	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD_HV_FL}$	SR	5.0 V code and data flash memory supply voltage	—	4.5	5.5	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx}$ – 0.1	$V_{DD_HV_IOx}$ + 0.1	
$V_{SS_HV_FL}$	SR	Code and data flash memory ground	—	0	0	V
$V_{DD_HV_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx}$ – 0.1	$V_{DD_HV_IOx}$ + 0.1	
$V_{SS_HV_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V

d. Device design targets the removal of this conditions. To be confirmed by design during device validation.

Table 10. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Min	Max(1)	Unit
$V_{DD_HV_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx}$ – 0.1	$V_{DD_HV_IOx}$ + 0.1	
$V_{DD_HV_AD}$	SR	5.0 V ADC supply and high reference voltage	—	4.5	5.5	V
			Relative to $V_{DD_HV_REG}$	$V_{DD_HV_REG}$ – 0.1	—	
$V_{SS_HV_AD}$	SR	ADC ground and low reference voltage	—	0	0	V
$V_{DD_LV_REGCOR}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_REGCOR}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_CORx}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	—	–40	125	°C

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 100$ mV.
3. To be connected to emitter of external NPN. Low voltage supplies are not under user control—these are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS_LV_xxx}$) must be shorted to high voltage grounds ($V_{SS_HV_xxx}$) and the low voltage supply pins ($V_{DD_LV_xxx}$) must be connected to the external ballast emitter.
4. The low voltage supplies ($V_{DD_LV_xxx}$) are not all independent. $V_{DD_LV_COR1}$ and $V_{DD_LV_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS_LV_COR1}$ and $V_{SS_LV_COR2}$ are internally shorted. $V_{DD_LV_REGCOR}$ and $V_{DD_LV_REGCORx}$ are physically shorted internally, as are $V_{SS_LV_REGCOR}$ and $V_{SS_LV_CORx}$.

Table 11. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min	Max(1)	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD_HV_IOx}$(2)	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD_HV_FL}$	SR	3.3 V code and data flash memory supply voltage	—	3.0	3.6	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx}$ – 0.1	$V_{DD_HV_IOx}$ + 0.1	
$V_{SS_HV_FL}$	SR	Code and data flash memory ground	—	0	0	V
$V_{DD_HV_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx}$ – 0.1	$V_{DD_HV_IOx}$ + 0.1	
$V_{SS_HV_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V

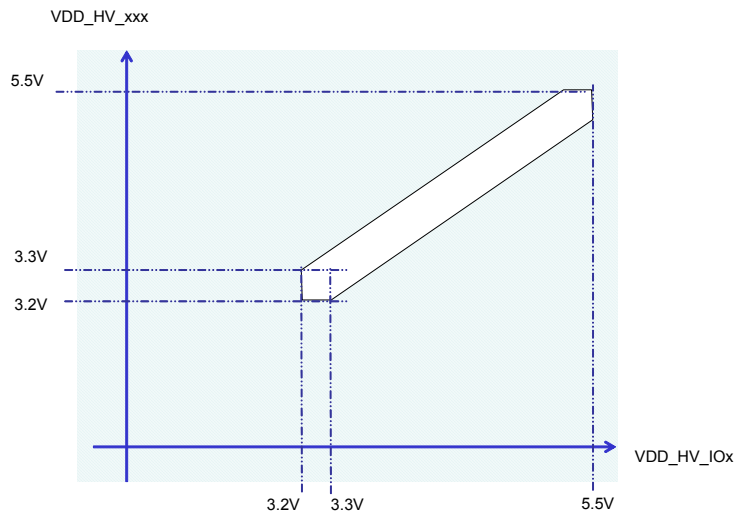
Table 11. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min	Max(1)	Unit
$V_{DD_HV_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx}$ – 0.1	$V_{DD_HV_IOx}$ + 0.1	
$V_{DD_HV_AD}$	SR	3.3 V ADC supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD_HV_REG}$	$V_{DD_HV_REG}$ – 0.1	5.5	
$V_{SS_HV_AD}$	SR	ADC ground and low reference voltage	—	0	0	V
$V_{DD_LV_REGCOR}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_REGCOR}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_CORx}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	—	–40	125	°C

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 100$ mV.
3. To be connected to emitter of external NPN. Low voltage supplies are not under user control—these are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS_LV_xxx}$) must be shorted to high voltage grounds ($V_{SS_HV_xxx}$) and the low voltage supply pins ($V_{DD_LV_xxx}$) must be connected to the external ballast emitter.
4. The low voltage supplies ($V_{DD_LV_xxx}$) are not all independent.
$V_{DD_LV_COR1}$ and $V_{DD_LV_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS_LV_COR1}$ and $V_{SS_LV_COR2}$ are internally shorted. $V_{DD_LV_REGCOR}$ and $V_{DD_LV_REGCORx}$ are physically shorted internally, as are $V_{SS_LV_REGCOR}$ and $V_{SS_LV_CORx}$.

Figure 7 shows the constraints of the different power supplies.

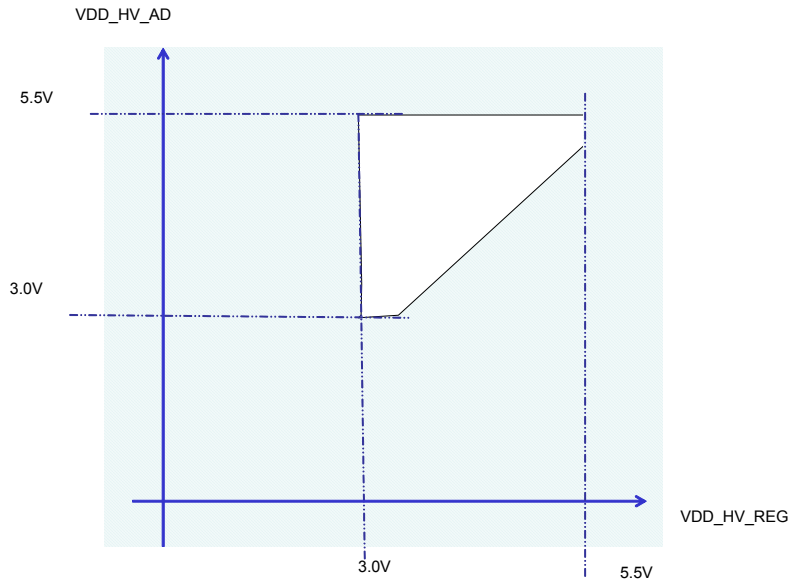
Figure 7. Power supplies constraints[e]



The SPC56xP54/60 supply architecture provides an ADC supply that is managed independently of standard V_{DD_HV} supply. *Figure 8* shows the constraints of the ADC power supply.

e. IO AC and DC characteristics are guaranteed only in the range 3.0V–3.6V when PAD3V5V is low, and in the range 4.5V–5.5V when PAD3V5V is high.

Figure 8. Independent ADC supply



3.5 Thermal characteristics

Table 12. Thermal characteristics for 144-pin LQFP

Symbol		Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	53.4	°C/W
	D		Four layer board—2s2p	43.9	°C/W
$R_{\theta JB}$	D	Thermal resistance junction-to-board(2)	Four layer board—2s2p	29.6	°C/W
$R_{\theta JCtop}$	D	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.3	°C/W
Ψ_{JB}	D	Junction-to-board, natural convection(4)	Operating conditions	29.8	°C/W
Ψ_{JC}	D	Junction-to-case, natural convection(5)	Operating conditions	1.3	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

Table 13. Thermal characteristics for 100-pin LQFP

Symbol		Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	47.3	°C/W
	D		Four layer board—2s2p	35.6	°C/W
$R_{\theta JB}$	D	Thermal resistance junction-to-board(2)	Four layer board—2s2p	19.1	°C/W
$R_{\theta JCtop}$	D	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.1	°C/W
Ψ_{JB}	D	Junction-to-board, natural convection(4)	Operating conditions	19.1	°C/W
Ψ_{JC}	D	Junction-to-case, natural convection(5)	Operating conditions	1.1	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1 $$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

Equation 2 $$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3 $$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 U.S.A.
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53-58, March 1998.

3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.6 Electromagnetic interference (EMI) characteristics

Table 14. EMI testing specifications

Parameter	Symbol	Conditions	f_{OSC}/f_{BUS}	Frequency	Level (Max)	Unit
V_{RE_TEM}	Radiated emissions, electric field	V_{DD} = 5 V; T_A = 25 °C 150 kHz–30 MHz RBW 9 kHz, Step Size 5 kHz 30 MHz–1 GHz RBW 120 kHz, Step Size 80 kHz	8 MHz crystal 64 MHz bus No PLL frequency modulation	150 kHz–150 MHz	18	dBµV
				150–1000 MHz	12	
				IEC Level	M	—
			8 MHz crystal 64 MHz bus ±2% PLL frequency modulation	150 kHz–150 MHz	18	dBµV
				150–1000 MHz	12	
				IEC Level	M	—

3.7 Electrostatic discharge (ESD) characteristics

Table 15. ESD ratings(1),(2)

Symbol		Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	—	2000	V
$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	—	750 (corners)	V
				500 (other)	

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The internal voltage regulator requires an external NPN ballast to be connected as shown in *Figure 9*. *Table 16* contains all approved NPN ballast components. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the $V_{DD_HV_REG}$, BCTRL and $V_{DD_LV_CORx}$ pins to less than L_{Reg}, see *Table 17*.

Note: The voltage regulator output cannot be used to drive external circuits. Output pins are used only for decoupling capacitances.

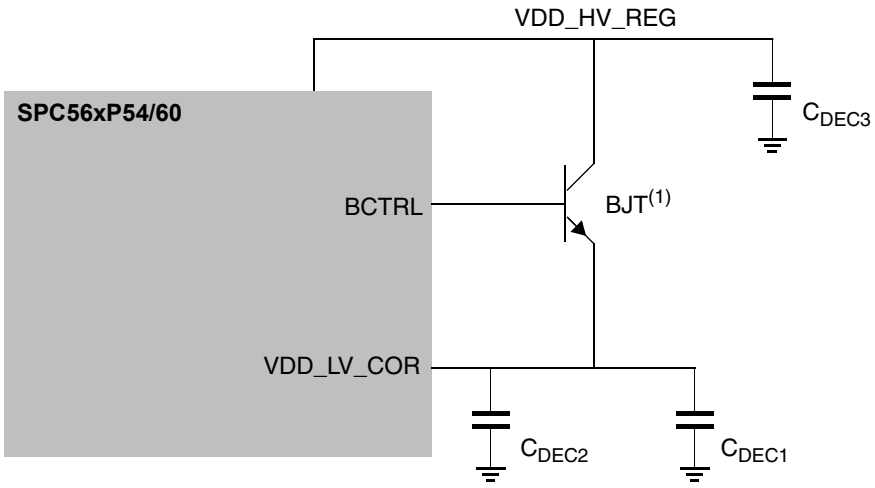
$V_{DD_LV_COR}$ must be generated using internal regulator and external NPN transistor. It is not possible to provide $V_{DD_LV_COR}$ through external regulator.

For the SPC56xP54/60 microcontroller, capacitors, with total values not below C_{DEC1}, should be placed between $V_{DD_LV_CORx}/V_{SS_LV_CORx}$ close to external ballast transistor emitter. 4 capacitors, with total values not below C_{DEC2}, should be placed close to microcontroller pins between each $V_{DD_LV_CORx}/V_{SS_LV_CORx}$ supply pairs and the

$V_{DD_LV_REGCOR}/V_{SS_LV_REGCOR}$ pair . Additionally, capacitors with total values not below C_{DEC3}, should be placed between the $V_{DD_HV_REG}/V_{SS_HV_REG}$ pins close to ballast collector. Capacitors values have to take into account capacitor accuracy, aging and variation versus temperature.

All reported information are valid for voltage and temperature ranges described in recommended operating condition, *Table 10* and *Table 11*.

Figure 9. Voltage regulator configuration



1. Refer to *Table 16*.

Table 16. Approved NPN ballast components

Part	Manufacturer	Approved derivatives(1)
BCP68	ON Semi	BCP68
	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10;BCX68-16;BCX68-25
BC868	NXP	BC868
BC817	Infineon	BC817-16;BC817-25;BC817SU;
	NXP	BC817-16;BC817-25
BCP56	ST	BCP56-16
	Infineon	BCP56-10;BCP56-16
	ON Semi	BCP56-10
	NXP	BCP56-10;BCP56-16

1. For automotive applications please check with the appropriate transistor vendor for automotive grade certification

Table 17. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD_LV_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	BJT from *Table 16*. 3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	—	µF
				BJT BC817, one capacitance of 22 µF	14.3	22		µF
R_{REG}	SR	—	Resulting ESR of all three capacitors of C_{DEC1}	BJT from *Table 16*. 3x10 µF. Absolute maximum value between 100 kHz and 10 MHz	—	—	50	mΩ
			Resulting ESR of the unique capacitor C_{DEC1}	BJT BC817, 1x 22 µF. Absolute maximum value between 100 kHz and 10 MHz	10	—	40	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances (i.e. X7R or X8R capacitors) with nominal value of 440 nF	1200	1760	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on $V_{DD_HV_REG}$	3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF; C_{DEC3} has to be equal or greater than C_{DEC1}	19.5	30	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD_HV_REG}$, BCTRL and $V_{DD_LV_CORx}$ pins	—	—	—	15	nH

3.8.2 Voltage monitor electrical characteristics

The device implements a Power On Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0V ± 10% range
- LVDLVCOR monitors low voltage digital power domain

Table 18. Low voltage monitor electrical characteristics

Symbol		Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25°C	1.0	—	V
$V_{REGLVDMOK_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK_H}$	P	Flash memory low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK_L}$	P	Flash memory low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK_H}$	P	I/O 5V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK_L}$	P	I/O 5V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK_H}$	P	Digital supply low voltage detector high	—	—	1.15	V
$V_{MLVDDOK_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power Up/Down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC56xP54/60 implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

1. A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5V. Associated POWER_ON (or POR) signal is active low.
   - Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
   - A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash memory and RC16 oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated modules are set into a safe state.

Figure 10. Power-up typical sequence

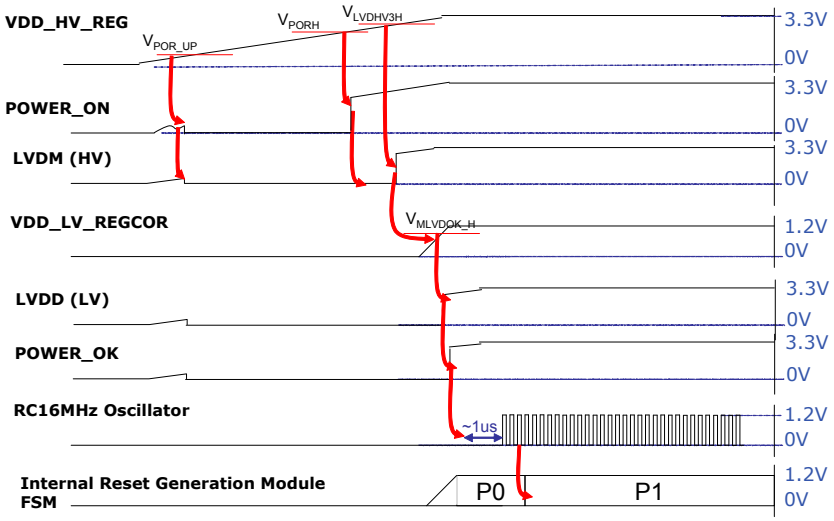


Figure 11. Power-down typical sequence

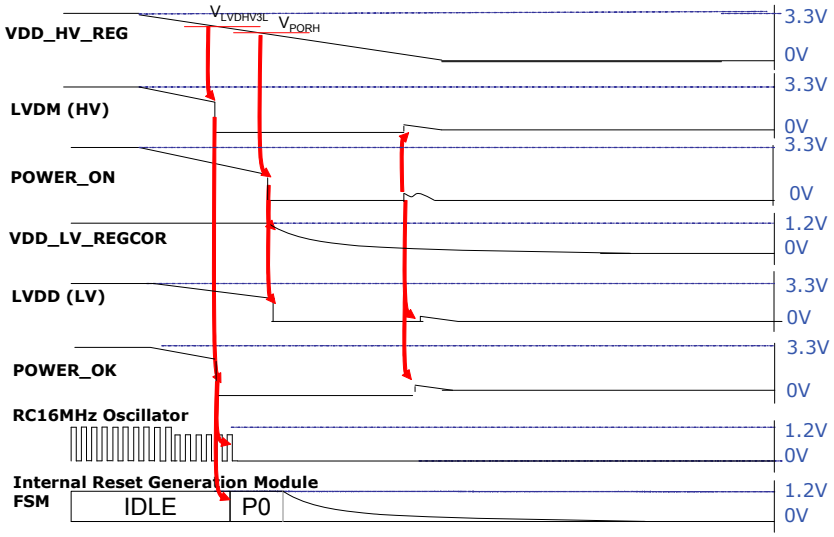
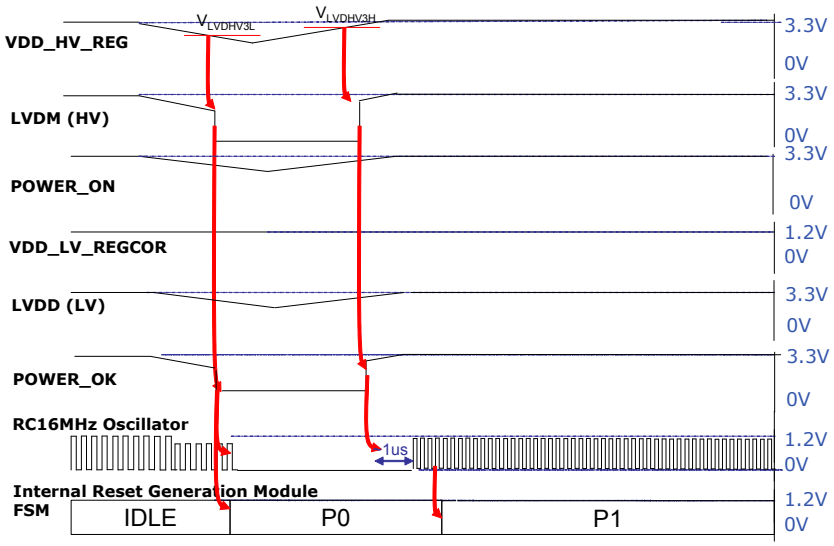


Figure 12. Brown-out typical sequence



3.10 NVUSRO register

Portions of the device configuration, such as high voltage supply, and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options register (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

3.10.1 NVUSRO[PAD3V5V] field description

Table 19 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 19. PAD3V5V field description(1)

Value(2)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. See the device reference manual for more information on the NVUSRO register.
2. '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.11 DC electrical characteristics

3.11.1 DC electrical characteristics (5 V)

Table 20 gives the DC electrical characteristics at 5 V (4.5 V < $V_{DD_HV_IOx}$ < 5.5 V, NVUSRO[PAD3V5V]=0) as described in *Figure 13*.

Figure 13. I/O input DC electrical characteristics definition

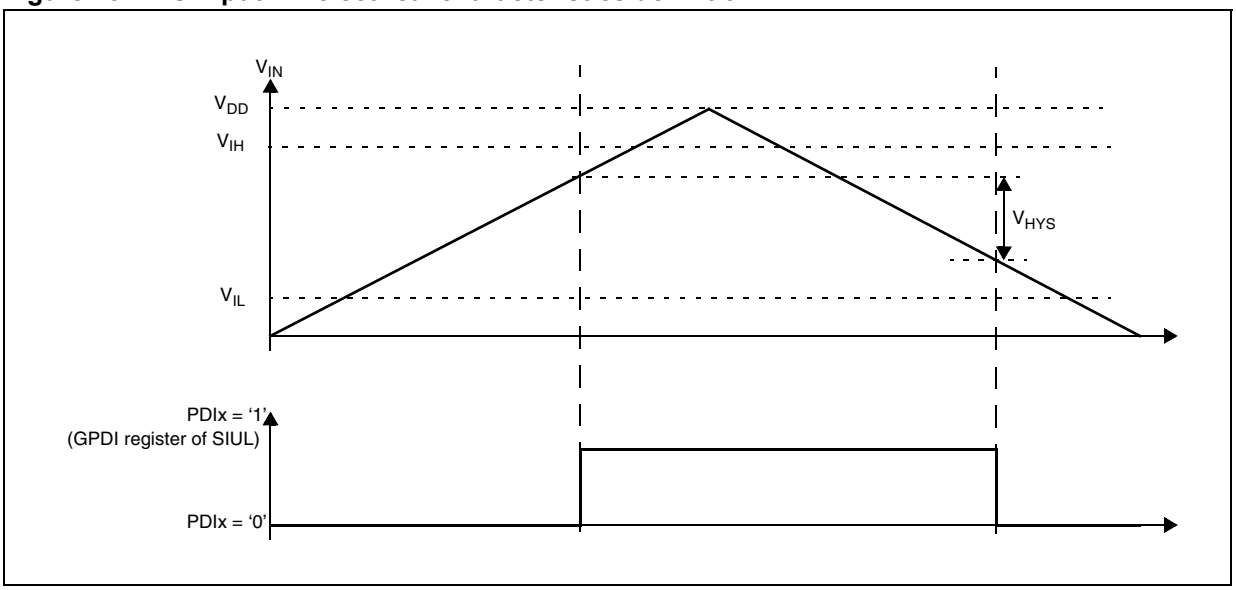


Table 20. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1(1)	—	V
V_{IL}	P	Maximum level input voltage	—	—	0.35 $V_{DD_HV_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD_HV_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD_HV_IOx}$ + 0.1(1)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD_HV_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD_HV_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8$V_{DD_HV_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD_HV_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD_HV_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD_HV_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD_HV_IOx}$	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD_HV_IOx}$	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD_HV_IOx}$	—	V

Table 20. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 21. Supply current (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter		Conditions		Value		Unit
						Typ	Max	
$I_{DD_LV_CORE}$	T	Supply current	RUN — Maximum Mode(1)	$V_{DD_LV_CORE}$ externally forced at 1.3 V ADC Freq = 32 MHz PLL Freq = 64 MHz	64 MHz	90	120	mA
			RUN - Platform consumption, single core(2)	VDD_LV_CORE externally forced to 1.3V	16 MHz	21	37	
					40 MHz	35	55	
					64 MHz	48	72	
			RUN - Platform consumption, dual core(3)		16 MHz	24	41	
					40 MHz	42	64	
					64 MHz	58	85	
	P		RUN — Maximum Mode(4)	$V_{DD_LV_CORE}$ externally forced at 1.3 V	64 MHz	85	113	
			HALT Mode(5)	$V_{DD_LV_CORE}$ externally forced at 1.3 V	—	5.5	15	
			STOP Mode(6)	$V_{DD_LV_CORE}$ externally forced at 1.3 V	—	4.5	13	
I_{DD_FLASH}	T		Flash memory supply current during read	$V_{DD_HV_FL}$ at 5.0 V	—	—	14	
			Flash memory supply current during erase operation on 1 flash memory module	$V_{DD_HV_FL}$ at 5.0 V	—	—	42	
I_{DD_ADC}	T		ADC supply current — Maximum Mode	$V_{DD_HV_AD}$ at 5.0 V ADC Freq = 16 MHz	—	3	4	
I_{DD_OSC}	T		OSC supply current	V_{DD_OSC} at 5.0 V	8 MHz	2.6	3.2	

1. Maximum mode configuration: Code fetched from Flash executed by dual core, SIUL, PIT, ADC_0, eTimer_0/1, LINFlex_0/1, STM, INTC_0/1, DSPI_0/1/2/3/4, FlexCAN_0/1, FlexRay (static consumption), CRC_0/1, FCCU, SRAM enabled. I/O supply current excluded.
2. RAM, Code and Data Flash powered, code fetched from Flash executed by single core, all peripherals gated; IRC16MHz on, PLL64MHz OFF(except for code running at 64MHz).
Code is performing continous data transfet from Flash to RAM.
3. RAM, Code and Data Flash powered, code fetched from Flash executed by dual core, all peripherals gated; IRC16MHz on, PLL64MHz OFF(except for code running at 64MHz).
Code is performing continous data transfet from Flash to RAM.
4. Maximum mode configuration: Code fetched from RAM executed by dual core, SIUL, PIT, ADC_0, eTimer_0/1, LINFlex_0/1, STM, INTC_0/1, DSPI_0/1/2/3/4, FlexCAN_0/1, FlexRay (static consumption), CRC_0/1, FCCU, SRAM enabled. I/O supply current excluded.
5. HALT mode configuration, only for the “P” classification: Code Flash memory in low power mode, data Flash memory in power down mode, OSC/PLL are OFF, FIRC is ON, Core clock gated, all peripherals are disabled.
6. STOP mode configuration, only for the “P” classification: Code and data Flash memories in power down mode, OSC/PLL are OFF, FIRC is ON, Core clock gated, all peripherals are disabled.

3.11.2 DC electrical characteristics (3.3 V)

Table 22 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD_HV_IOx}$ < 3.6 V, NVUSRO[PAD3V5V]=1) as described in *Figure 14*.

Figure 14. I/O input DC electrical characteristics definition

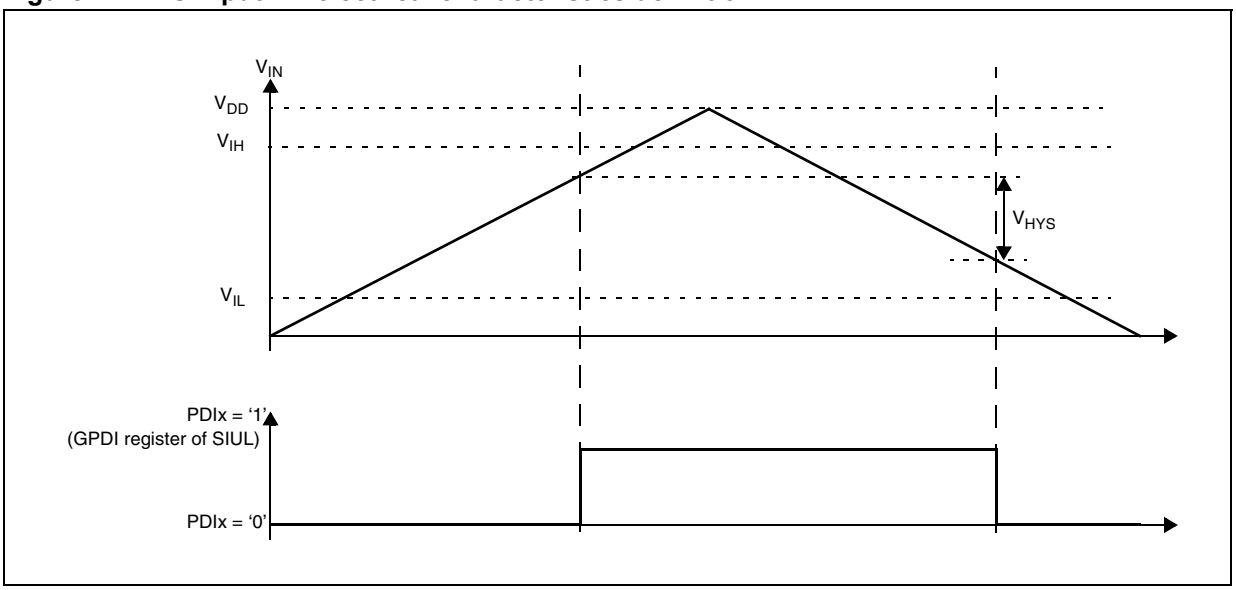


Table 22. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)(1)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1(2)	—	V
V_{IL}	P	Maximum low level input voltage	—	—	0.35 $V_{DD_HV_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD_HV_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD_HV_IOx}$ + 0.1(2)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD_HV_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD_HV_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD_HV_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –1.5 mA	$V_{DD_HV_IOx}$ – 0.8	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD_HV_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

Table 22. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)(1) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	

1. These specifications are design targets and subject to change per device characterization.
2. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 23. Supply current (3.3 V, NVUSRO[PAD3V5V]=1)

Symbol		Parameter		Conditions		Value		Unit
						Typ	Max	
$I_{DD_LV_CORE}$	T	Supply current	RUN — Maximum Mode(1)	$V_{DD_LV_CORE}$ externally forced at 1.3 V ADC Freq = 32 MHz PLL Freq = 64 MHz	64 MHz	90	120	mA
			RUN - Platform consumption, single core(2)	VDD_LV_CORE externally forced to 1.3V	16 MHz	21	37	
					40 MHz	35	55	
					64 MHz	48	72	
			RUN - Platform consumption, dual core(3)		16 MHz	24	41	
					40 MHz	42	64	
					64 MHz	58	85	
	P		RUN — Maximum Mode(4)	$V_{DD_LV_CORE}$ externally forced at 1.3 V	64 MHz	85	113	
			HALT Mode(5)	$V_{DD_LV_CORE}$ externally forced at 1.3 V	—	5.5	15	
			STOP Mode(6)	$V_{DD_LV_CORE}$ externally forced at 1.3 V	—	4.5	13	
I_{DD_FLASH}	D		Flash memory supply current during read	$V_{DD_HV_FL}$ at 3.3 V	—	—	14	
			Flash memory supply current during erase operation on 1 flash memory module	$V_{DD_HV_FL}$ at 3.3 V	—	—	42	
I_{DD_ADC}	T		ADC supply current — Maximum Mode	$V_{DD_HV_AD}$ at 3.3 V ADC Freq = 16 MHz	—	3	4	
I_{DD_OSC}	T		OSC supply current	V_{DD_OSC} at 3.3 V	8 MHz	2.4	3	

1. Maximum mode configuration: Code fetched from Flash executed by dual core, SIUL, PIT, ADC_0, eTimer_0/1, LINFlex_0/1, STM, INTC_0/1, DSPI_0/1/2/3/4, FlexCAN_0/1, FlexRay (static consumption), CRC_0/1, FCCU, SRAM enabled. I/O supply current excluded.
2. RAM, Code and Data Flash powered, code fetched from Flash executed by single core, all peripherals gated; IRC16MHz on, PLL64MHz OFF(except for code running at 64MHz).
Code is performing continous data transfet from Flash to RAM.
3. RAM, Code and Data Flash powered, code fetched from Flash executed by dual core, all peripherals gated; IRC16MHz on, PLL64MHz OFF(except for code running at 64MHz).
Code is performing continous data transfet from Flash to RAM.
4. Maximum mode configuration: Code fetched from RAM executed by dual core, SIUL, PIT, ADC_0, eTimer_0/1, LINFlex_0/1, STM, INTC_0/1, DSPI_0/1/2/3/4, FlexCAN_0/1, FlexRay (static consumption), CRC_0/1, FCCU, SRAM enabled. I/O supply current excluded.
5. HALT mode configuration, only for the “P” classification: Code Flash memory in low power mode, data Flash memory in power down mode, OSC/PLL are OFF, FIRC is ON, Core clock gated, all peripherals are disabled.
6. STOP mode configuration, only for the “P” classification: Code and data Flash memories in power down mode, OSC/PLL are OFF, FIRC is ON, Core clock gated, all peripherals are disabled.

Table 24. Peripherals supply current (5 V and 3.3 V)[1]

Symbol		Parameter	Conditions		Value		Unit
					Typ	Max	
$I_{DD_BV(CAN)}$	T	CAN (FlexCAN) supply current on VDD_BV	500 Kbyte/s	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL@ 8 MHz used as CAN engine clock source • Message sending period is 580 µs	21.6 * f_{periph}	28.1* f_{periph}	µA
$I_{DD_BV(SCI)}$	T	SCI (LINFlex) supply current on VDD_BV	Total (static + dynamic) consumption: • LIN mode • Baudrate: 115.2 Kbyte/s		10.8 * f_{periph}	14.1 * f_{periph}	
$I_{DD_BV(SPI)}$	T	SPI (DSPI) supply current on VDD_BV	Ballast dynamic consumption (continuous communication): • Baudrate: 2 Mbit/s • Transmission every 8 µs • Frame: 16 bits		4.8 * f_{periph}	6.3 * f_{periph}	
$I_{DD_BV(ADC)}$	T	ADC supply current on VDD_BV	VDD = 5.5 V	Ballast dynamic consumption (continuous conversion)	120 * f_{periph}	156 * f_{periph}	
$I_{DD_HV_ADC(ADC)}$	T	ADC supply current on VDD_HV_ADC	VDD = 5.5 V	Analog dynamic consumption (continuous conversion)	0.005 * f_{periph} + 2.8	0.007 * f_{periph} + 3.4	mA
$I_{DD_BV(eTimer)}$	T	eTimer supply current on VDD_BV	PWM signals generation on all 1 channel @10kHz	Dynamic consumption does not change varying the frequency	1.8	2.4	mA
$I_{DD_BV(FlexRay)}$	T	FlexRay supply current on VDD_BV	Static consumption		4.2 * f_{periph}	5.5 * f_{periph}	µA

1. Operating conditions: f_{periph} = 8 MHz to 64 MHz

3.11.3 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 25*.

Table 25. I/O supply segment

Package	Supply segment						
	1	2	3	4	5	6	7
LQFP144	pin8 – pin20	pin23 – pin38	pin39 – pin55	pin58 – pin68	pin73 – pin89	pin92 – pin125	pin128 – pin5
LQFP100	pin15 – pin26	pin27 – pin38	pin41 – pin46	pin51 – pin61	pin64 – pin86	pin89 – pin10	—

Table 26. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	

Table 26. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.12 Main oscillator electrical characteristics

The SPC56xP54/60 provides an oscillator/resonator driver.

Table 27. Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	6.5	25	mA/V
V_{OSC}	T	Oscillation amplitude on EXTAL pin	1	—	V
t_{OSCSU}	T	Start-up time[1],[2]	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of EXTAL

Table 28. Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	4	20	mA/V
V_{OSC}	T	Oscillation amplitude on EXTAL pin	1	—	V
t_{OSCSU}	T	Start-up time[1],[2]	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of EXTAL

Table 29. Input clock characteristics

Symbol		Parameter	Min	Typ	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	64	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.13 FMPLL electrical characteristics

Table 30. PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		Parameter		Conditions	Value		Unit
					min	max	
$f_{ref_crystal}$ f_{ref_ext}	D	PLL reference frequency range(1)		Crystal reference	4	40	MHz
f_{pll_in}	D	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode		—	4	120	MHz
f_{FREE}	P	Free running frequency		Measured using clock division — typically /16	20	150	MHz
f_{sys}	D	On-chip PLL frequency		—	16	64	MHz
t_{CYC}	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window(2)		Lower limit	1.6	3.7	MHz
				Upper limit	24	56	
f_{SCM}	D	Self-clocked mode frequency(3),(4)		—	20	150	MHz
C_{JITTER}	T	CLKOUT period jitter(5),(6),(7),(8)	Short-term jitter(9)	f_{SYS} maximum	–4	4	% f_{CLKOUT}
			Long-term jitter (avg. over 2 ms interval)	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 64 MHz, 4000 cycles	—	10	ns
t_{lpll}	D	PLL lock time (10), (11)		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	–6	6	% f_{sys}
f_{UL}	D	Frequency un-LOCK range		—	–18	18	% f_{sys}
f_{CS} f_{DS}	D	Modulation Depth		Center spread	±0.25	±4.0(12)	%f_{sys}
				Down Spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency(13)		—	—	70	kHz

1. Considering operation with PLL not bypassed.

2. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
3. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
4. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
5. This value is determined by the crystal manufacturer and board design.
6. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
7. Proper PC board layout procedures must be followed to achieve specifications.
8. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
9. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
10. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
11. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
12. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
13. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.14 16 MHz RC oscillator electrical characteristics

Table 31. 16 MHz RC oscillator electrical characteristics

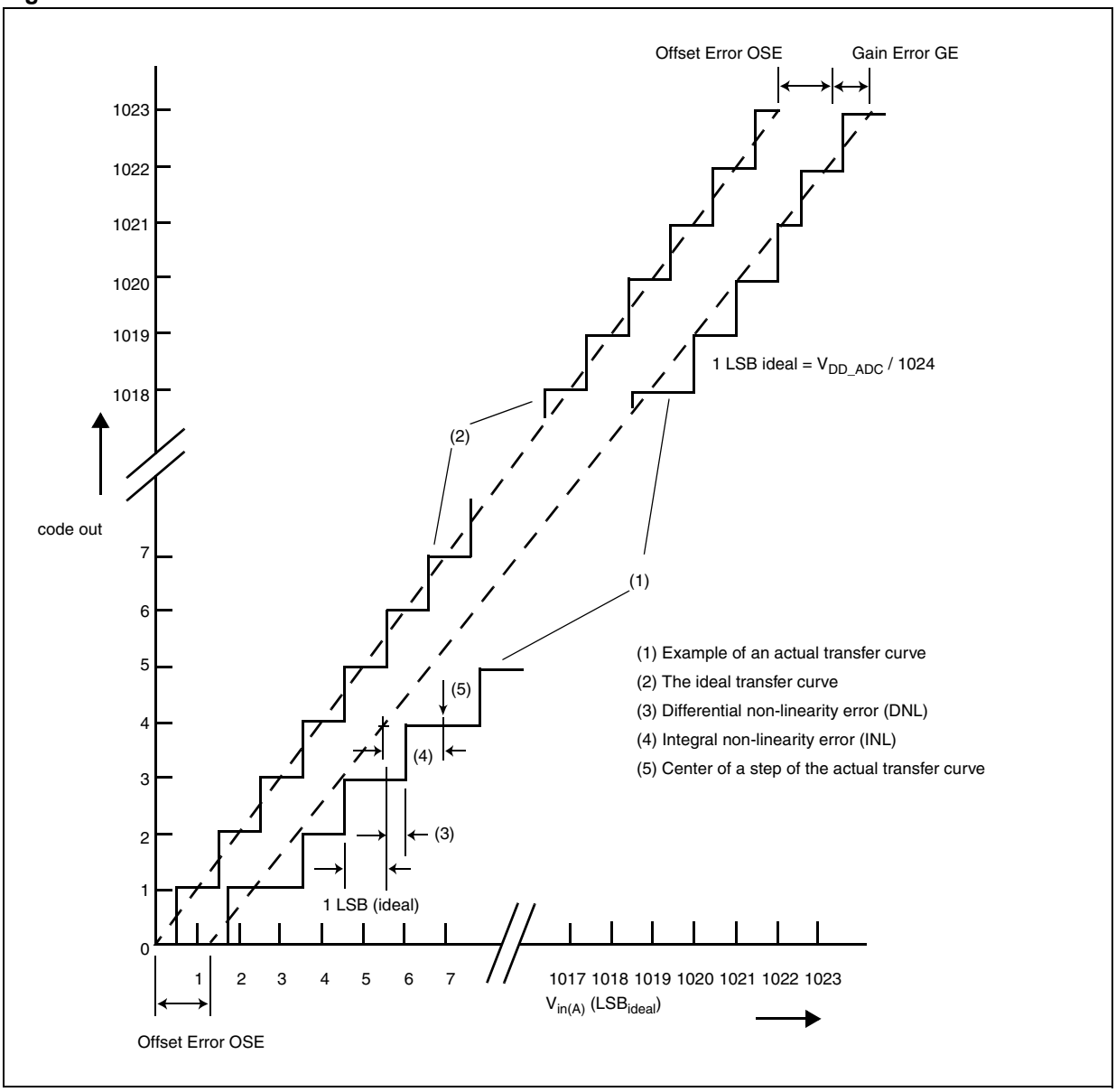
Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–6	—	6	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF(1) from the 16 MHz	T_A = 25 °C	–1	—	1	%
$\Delta_{RCMSTEP}$	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

1. PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.15 Analog-to-Digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Figure 15. ADC characteristics and error definitions



3.15.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high-frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuate the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured.

The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{P2} substantially two switched capacitances, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with $C_S + C_{P2}$ equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (fc \times (C_S + C_{P2}))$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S + C_{P2}$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \times \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

Figure 16. Input equivalent circuit (precise channels)

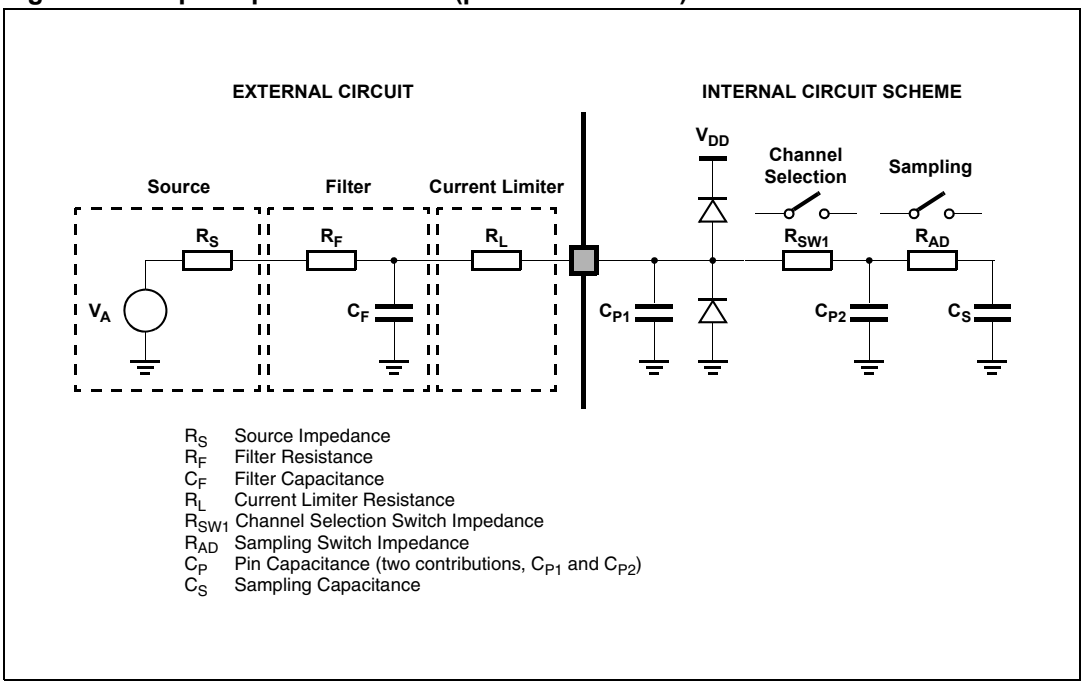
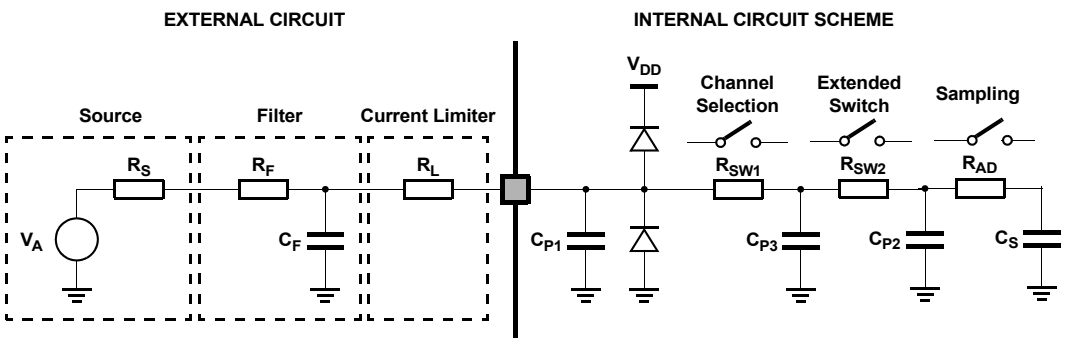


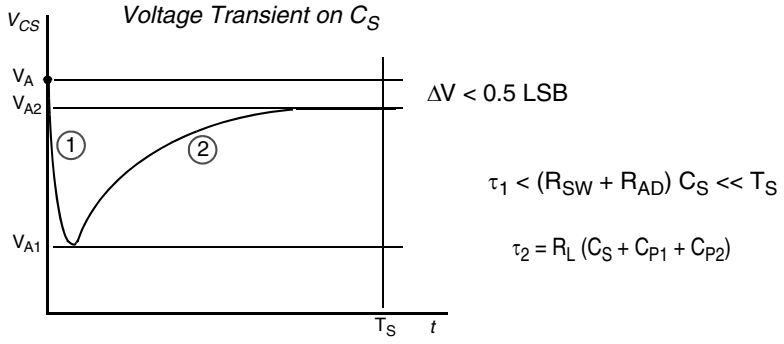
Figure 17. Input equivalent circuit (extended channels)



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance (two contributions, R_{SW1} and R_{SW2})
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1}, C_{P2} and C_{P3})
C_S: Sampling capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 18. Transient behavior during sampling phase



In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \times \frac{C_P \times C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \times C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \times (C_S + C_{P1} + C_{P2}) = V_A \times (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \times (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraint on R_L sizing is obtained:

Equation 9

$$8.5 \times \tau_2 = 8.5 \times R_L \times (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

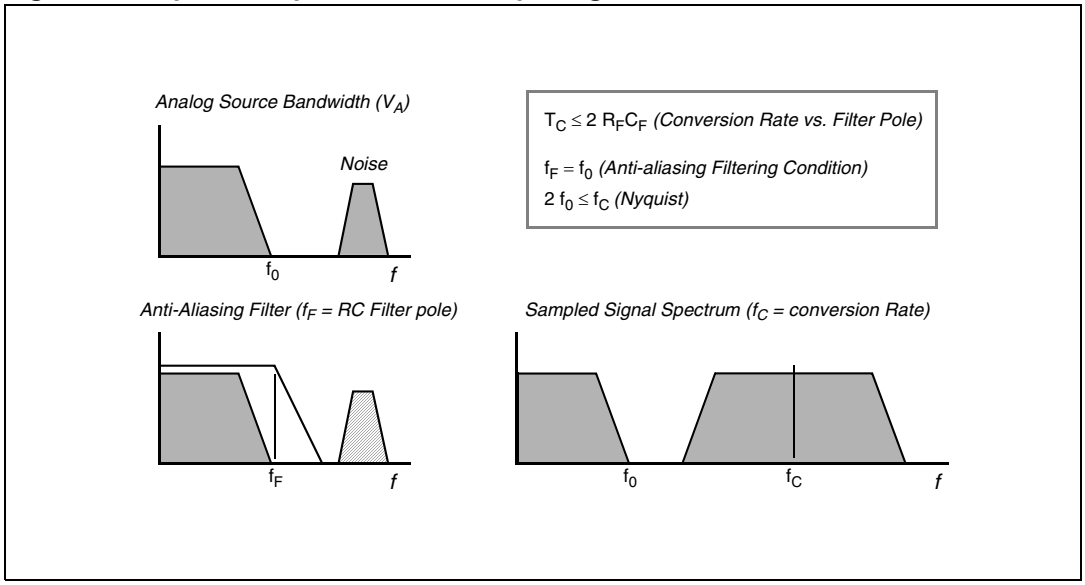
Equation 10

$$V_{A2} \times (C_S + C_{P1} + C_{P2} + C_F) = V_A \times C_F + V_{A1} \times (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on

C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

Figure 19. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 2048 \times C_S$$

3.15.2 ADC conversion characteristics

Table 32. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
V_{INAN}	SR	Analog input voltage[2]	—	$V_{SS_HV_AD}$ – 0.3	—	$V_{SS_HV_AD}$ + 0.3	V
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk[3] frequency)	—	3[4]	—	60	MHz
f_s	SR	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	D	Sample time[5]	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
			f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_{ADC_C}	P	Conversion time[6]	f_{ADC} = 20 MHz[7], INPCMP = 1	0.650	—	—	µs
C_S[8]	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[8]	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}[8]	D	ADC input pin capacitance 2	—	—	—	1	pF
C_{P3}[8]	D	ADC input pin capacitance 3	—	—	—	1	pF
R_{SW1}[8]	D	Internal resistance of analog source	$V_{DD_HV_AD}$ = 5 V ±10%	—	—	0.6	kΩ
			$V_{DD_HV_AD}$ = 3.3 V ±10%	—	—	3	kΩ
R_{SW2}[8]	D	Internal resistance of analog source	$V_{DD_HV_AD}$ = 5 V ±10%	—	—	2.15	kΩ
			$V_{DD_HV_AD}$ = 3.3 V ±10%	—	—	3.6	kΩ
R_{AD}[8]	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	–5	—	5	mA
INL	P	Integral Non Linearity	No overload	—	±1.5	—	LSB
DNL	P	Differential Non Linearity	No overload	–1.0	—	1.0	LSB
OFS	T	Offset error	—	—	±1	—	LSB
GNE	T	Gain error	—	—	±1	—	LSB
TUE	P	Total unadjusted error without current injection	16 precision channels	–2.5	—	2.5	LSB

Table 32. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
TUE	T	Total unadjusted error with current injection	16 precision channels	–3	—	3	LSB
TUE	T	Total unadjusted error with current injection	10 standard channels	–4	—	4	LSB

1. V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS_HV_AD}$ to $V_{DD_HV_AD}$.
2. V_{INAN} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
3. AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
4. When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.
5. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.
6. This parameter includes the sample time t_{ADC_S}.
7. 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.
8. See *Figure 16*.

3.16 Flash memory electrical characteristics

Table 33. Program and erase specifications

Symbol		Parameter	Conditions	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{wprogram}$	P	Word Program (32 bits) Time[4]	Data Flash	—	30	70	500	µs
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	Code Flash	—	18	50	500	µs
T_{BKPRG}	P	Bank Program (64 KB)[4, 5]	Data Flash	—	0.49	1.2	4.1	s
	P	Bank Program (1056 KB)[4, 5]	Code Flash	—	2.6	6.6	66	s
T_{MDPRG}	P	Module Program (512 KB)[4]	Code Flash	—	1.3	1.65	33	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	Code Flash	—	200	500	5000	ms
			Data Flash		700	800		
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	Code Flash	—	300	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	Code Flash	—	400	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	Code Flash	—	600	1300	5000	ms
t_{ESRT}	P	Erase Suspend Request Rate[6]	Code Flash	20	—	—	—	ms
			Data Flash	10				

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. Typical bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).
6. Time between erase suspend resume and next erase suspend.

Table 34. Flash memory module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	100000	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 64 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0 – 1000 P/E cycles	20	—	years
			Blocks with 10000 P/E cycles	10	—	years
			Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 35. Flash read access timing

Symbol	C	Parameter	Conditions(1)	Max	Unit
Fmax	C	Maximum working frequency for Code Flash at given number of WS in worst conditions	2 wait states	66	MHz
			0 wait states	22	
Fmax	C	Maximum working frequency for Data Flash at given number of WS in worst conditions	8 wait states	66	MHz

1. VDD = 3.3 V ± 10% / 5.0 V ± 10%, TA = –40 to 125 °C, unless otherwise specified

3.17 AC specifications

3.17.1 Pad AC specifications

Table 36. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
T_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
T_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	
T_{sim}[3]	CC	T	Symmetric, same drive strength between N and P transistor	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	4	ns
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).
3. Transition timing of both positive and negative slopes will differ maximum 50%

3.18 AC timing characteristics

3.18.1 $\overline{\text{RESET}}$ pin characteristics

The SPC56xP54/60 implements a dedicated bidirectional RESET pin.

Figure 20. Start-up reset requirements(f)

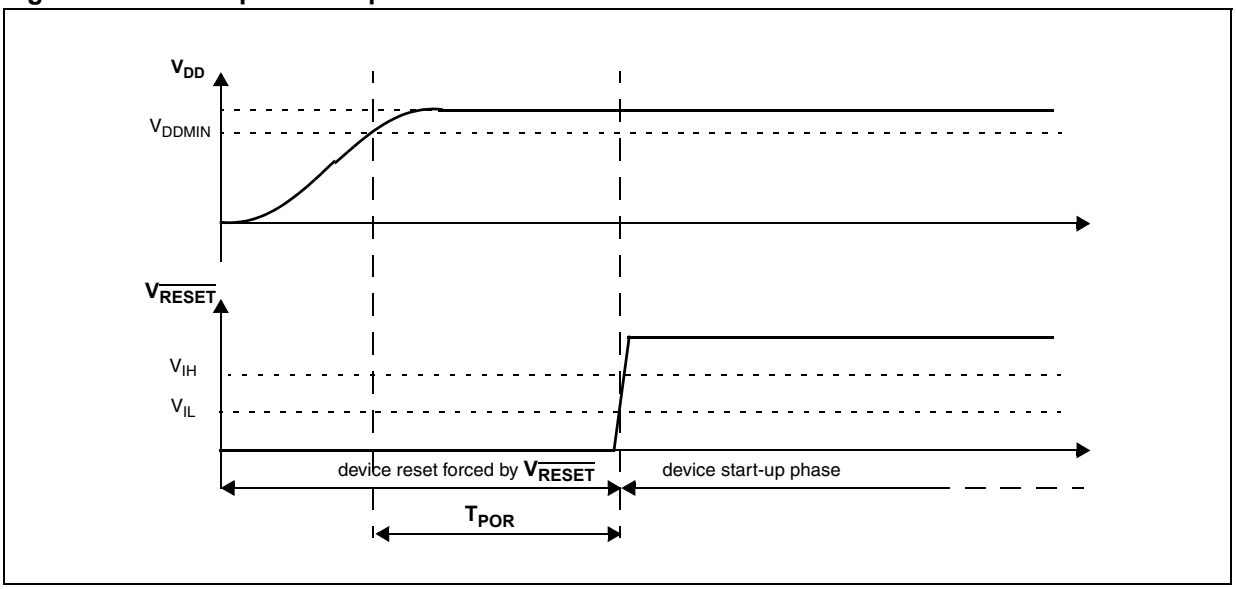
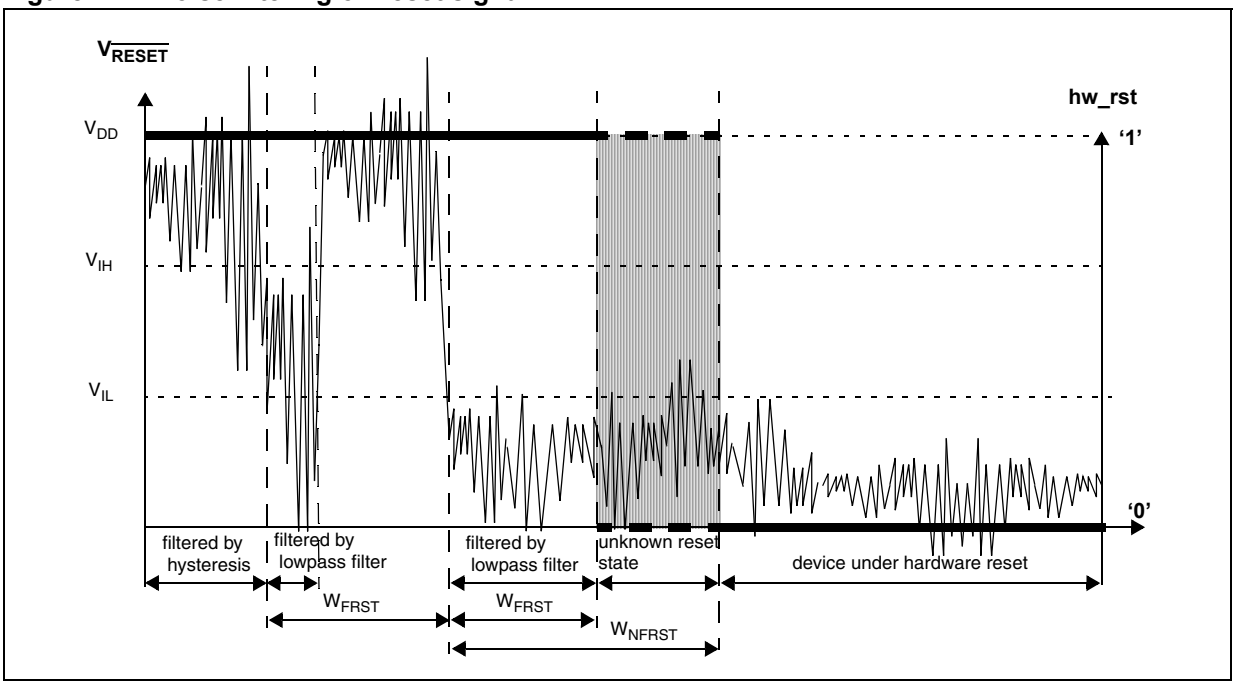


Figure 21. Noise filtering on reset signal



f. The output drive provided is open drain and hence must be terminated by an external resistor of value 1 kΩ.

Table 37. $\overline{\text{RESET}}$ electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
T_{POR}	CC	D	maximum delay before internal reset is released after all VDD_HV reach nominal supply	Monotonic VDD_HV supply ramp	—	—	1	ms
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).
4. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.18.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD_HV_IOx}/2$)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing

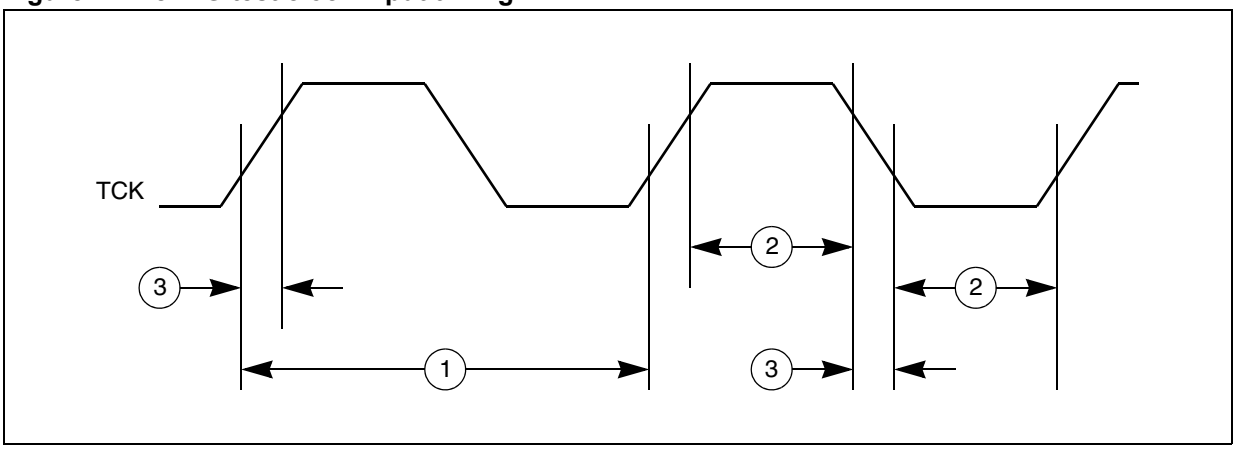


Figure 23. JTAG test access port timing

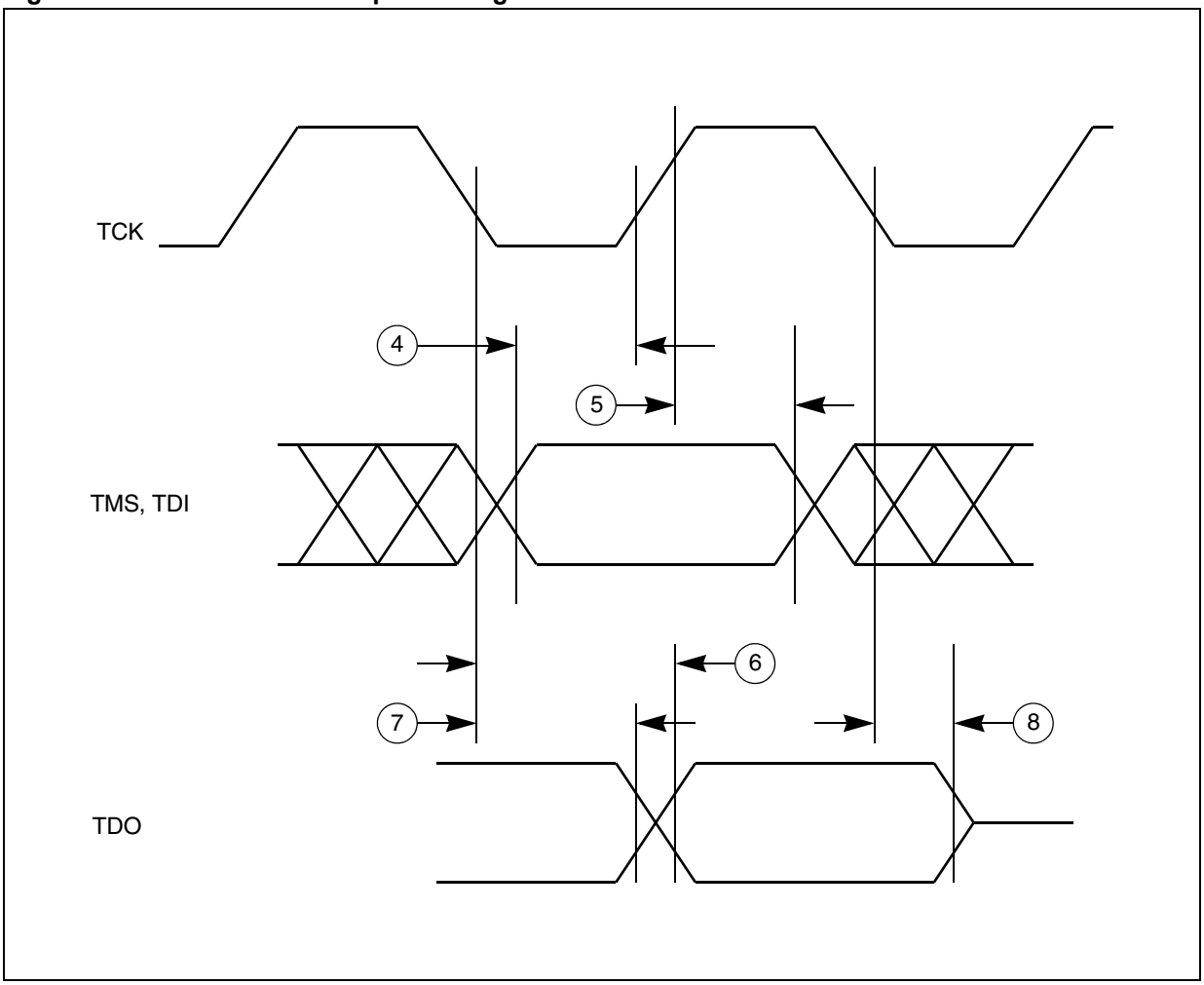
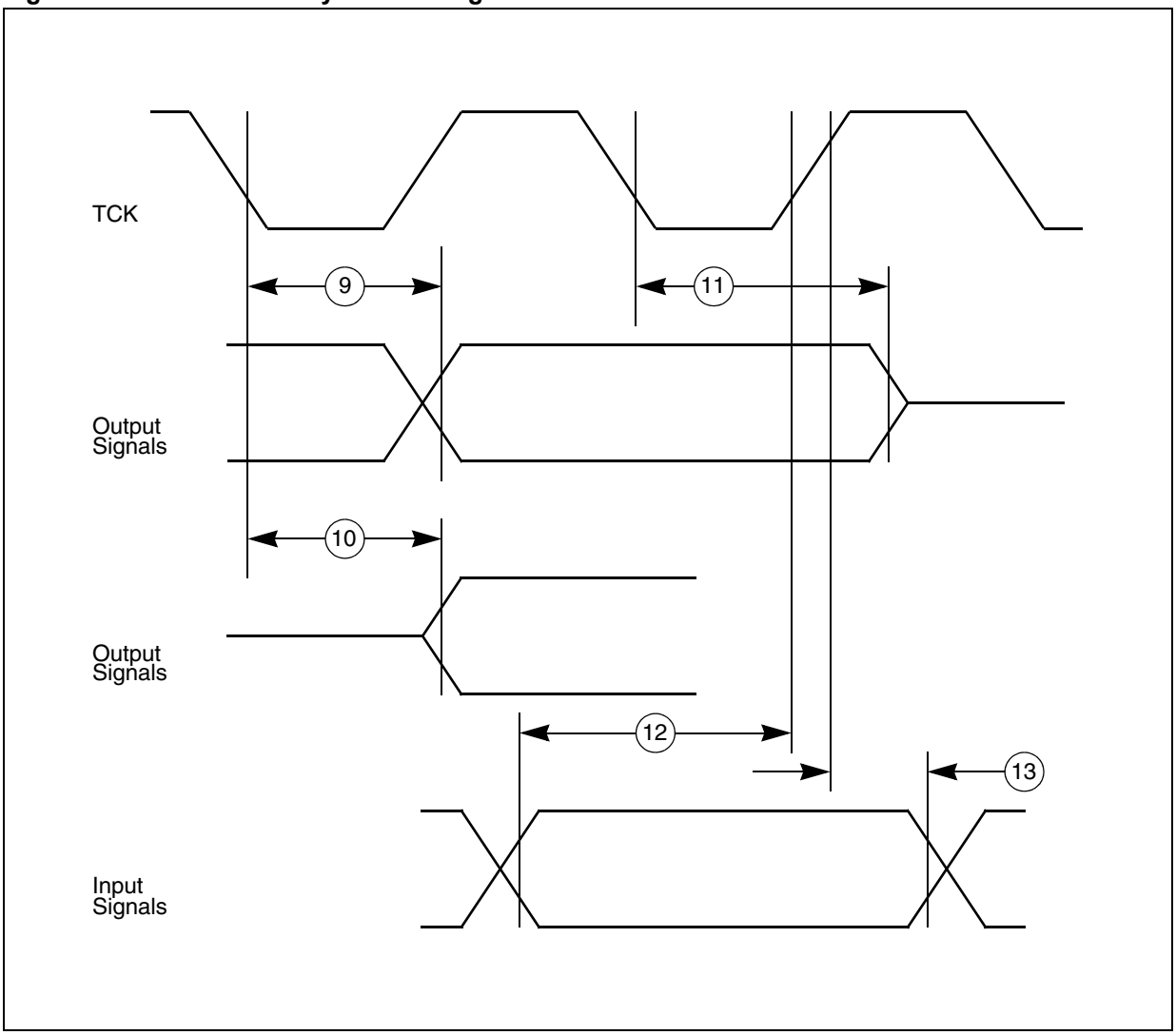


Figure 24. JTAG boundary scan timing



3.18.3 Nexus timing

Table 39. Nexus debug port timing(1)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
2	t_{MDOV}	CC	D	MCKO edge to MDO data valid	$-0.1 \times t_{MCYC}$	—	$0.25 \times t_{MCYC}$	ns
3	t_{MSEOV}	CC	D	MCKO edge to $\overline{\text{MSEO}}$ data valid	$-0.1 \times t_{MCYC}$	—	$0.25 \times t_{MCYC}$	ns
4	t_{EVTOV}	CC	D	MCKO edge to $\overline{\text{EVTO}}$ data valid	$-0.1 \times t_{MCYC}$	—	$0.25 \times t_{MCYC}$	ns
5	t_{TCYC}	CC	D	TCK cycle time	64(2)	—	—	ns

Table 39. Nexus debug port timing(1) (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t_{NTDIS}	CC	D	TDI data setup time	6	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	6	—	—	ns
7	t_{NTDIH}	CC	D	TDI data hold time	10	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	10	—	—	ns
8	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	35	ns
9	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

1. All values need to be confirmed during device validation.
2. Lower frequency is required to be fully compliant to standard.

Figure 25. Nexus output timing

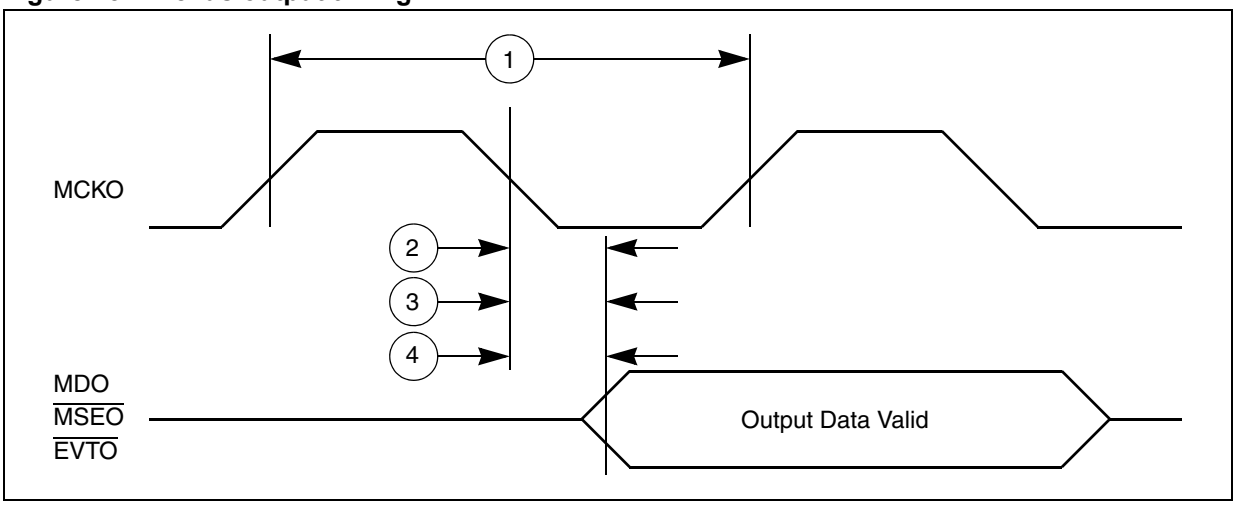


Figure 26. Nexus event trigger and test clock timings

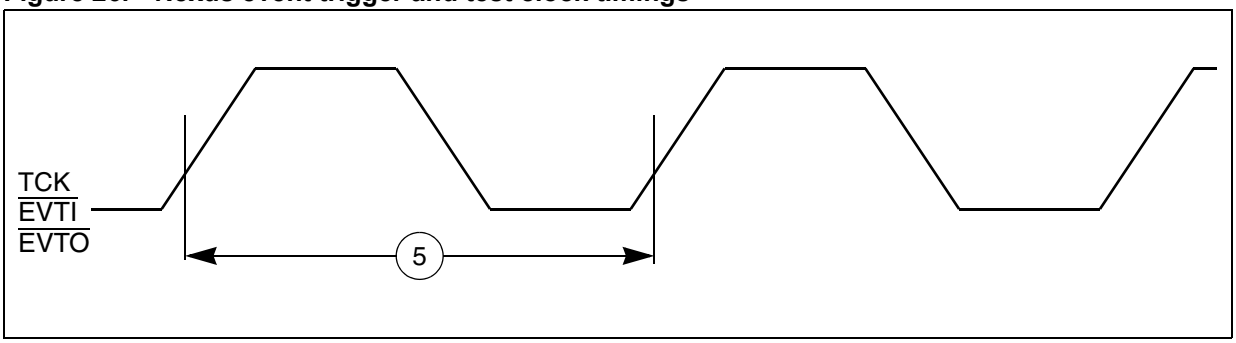
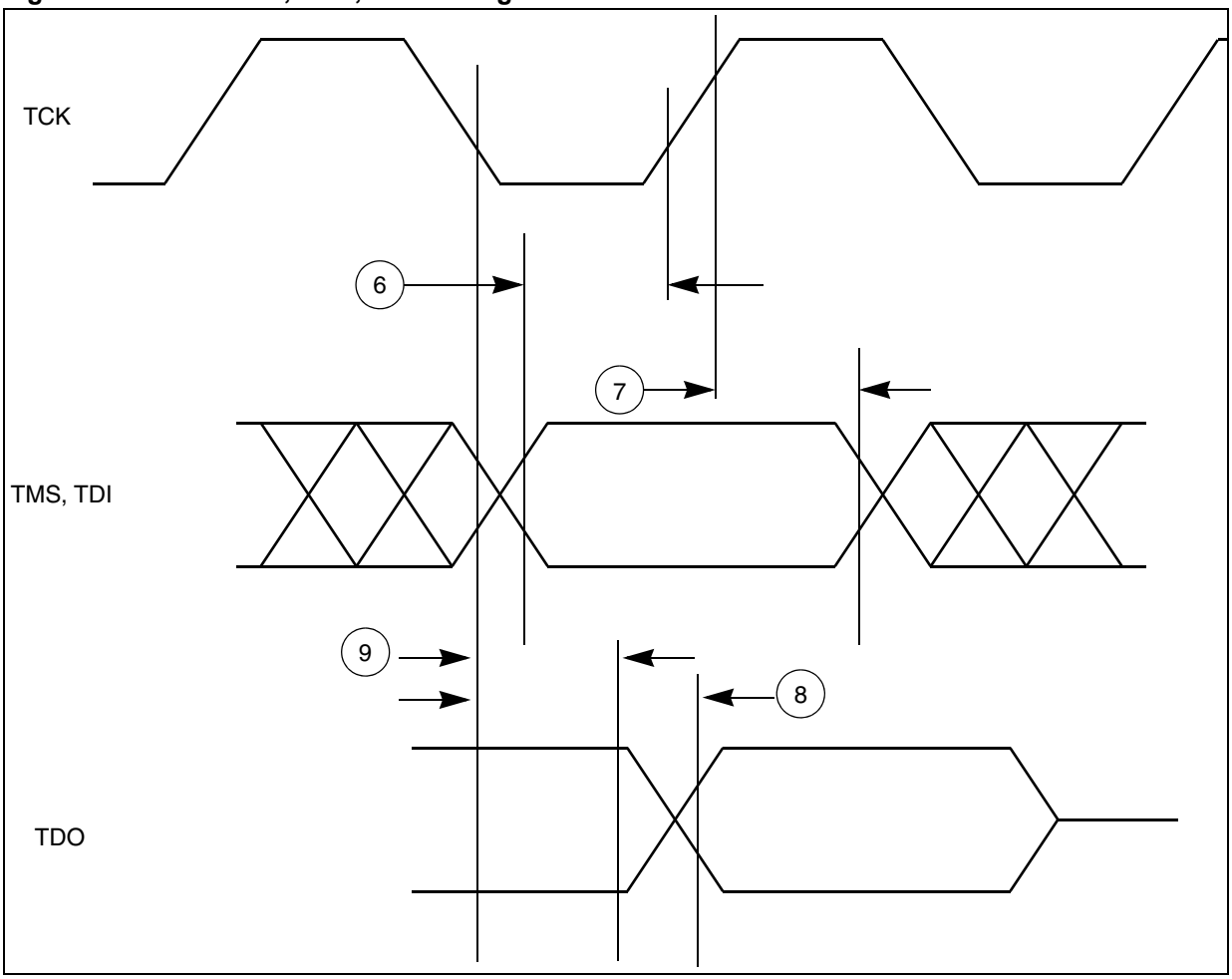


Figure 27. Nexus TDI, TMS, TDO timing



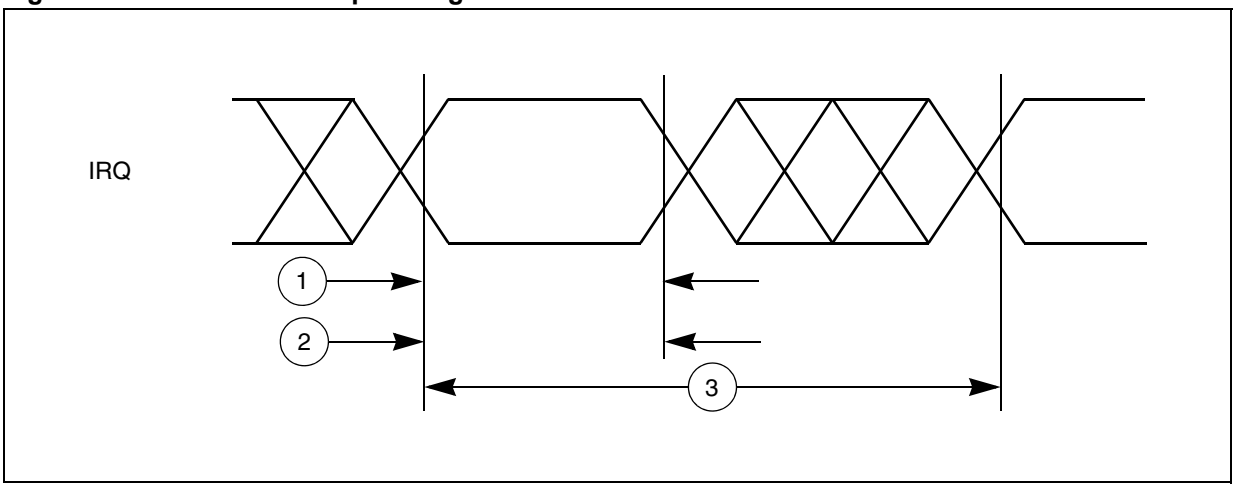
3.18.4 External interrupt timing (IRQ pin)

Table 40. External interrupt timing(1)

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	CC	D	IRQ pulse width low	—	4	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	4	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time(2)	—	4 + N (3)	—	t_{CYC}

1. IRQ timing specified at f_{SYS} = 64 MHz and $V_{DD_HV_IOx}$ = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and CL = 200pF with SRC = 0b00.
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.
3. N= ISR time to clear the flag.

Figure 28. External interrupt timing



3.18.5 DSPI timing

Table 41. DSPI timing(1)

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	60	—	ns
					Slave (MTFE = 0)	60	—	
2	t_{CSC}	CC	D	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	26	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 × t_{SCK}	0.6 × t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	30	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	16	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	35	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	35	—	
					Master (MTFE = 1, CPHA = 1)	35	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	

Table 41. DSPI timing(1) (continued)

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

1. All timing are provided with 50pF capacitance on output, 1ns transition time on input signal

Figure 29. DSPI classic SPI timing — master, CPHA = 0

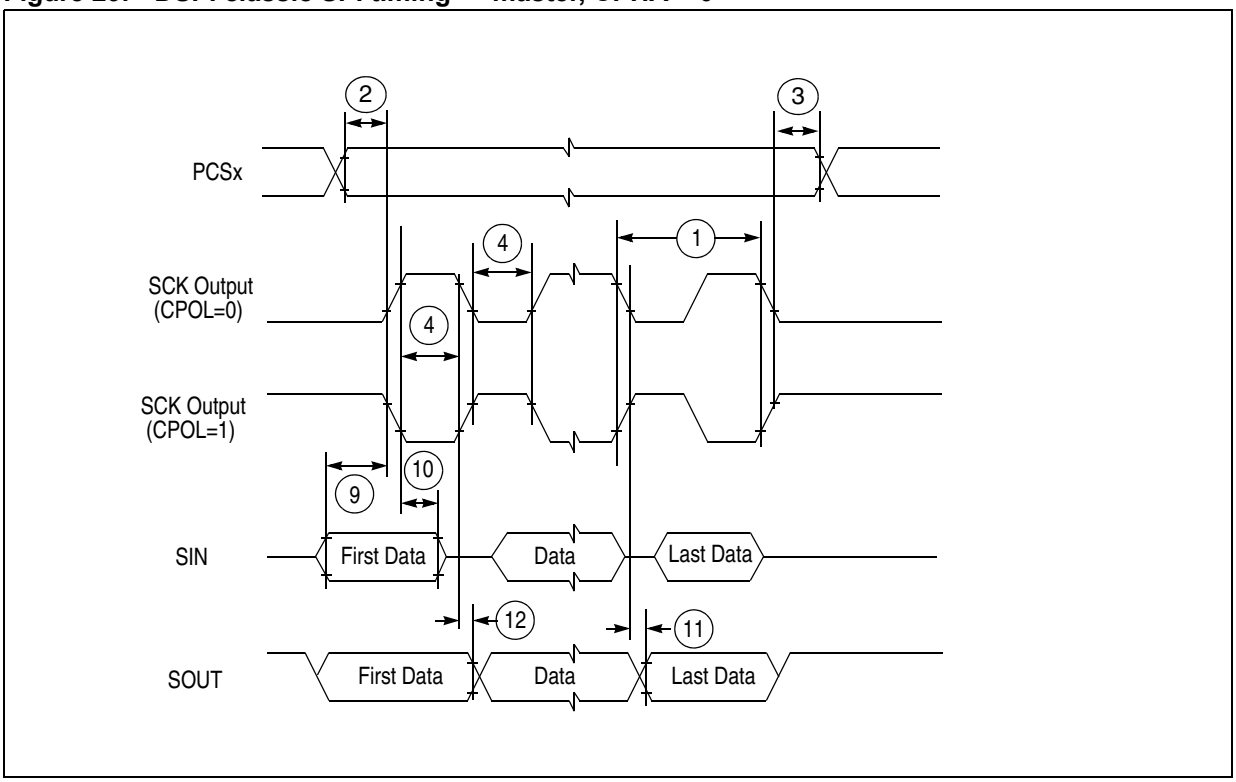


Figure 30. DSPI classic SPI timing — master, CPHA = 1

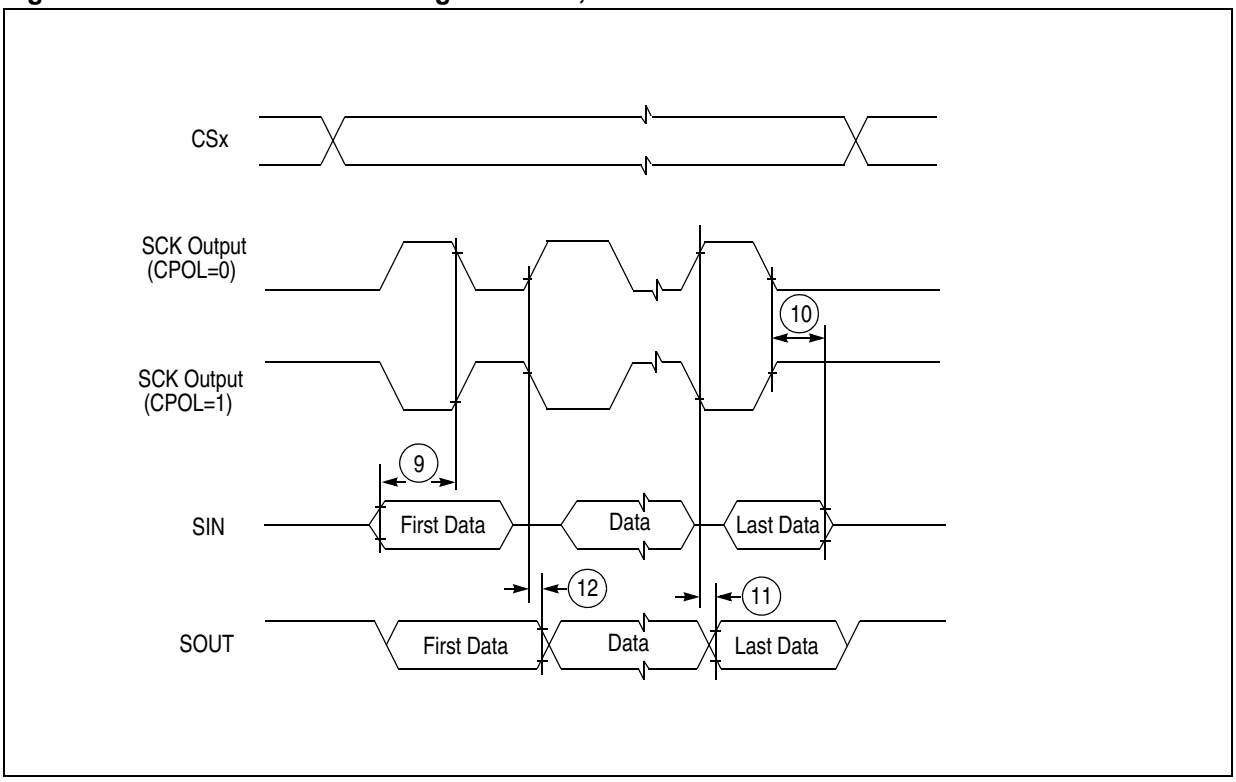


Figure 31. DSPI classic SPI timing — slave, CPHA = 0

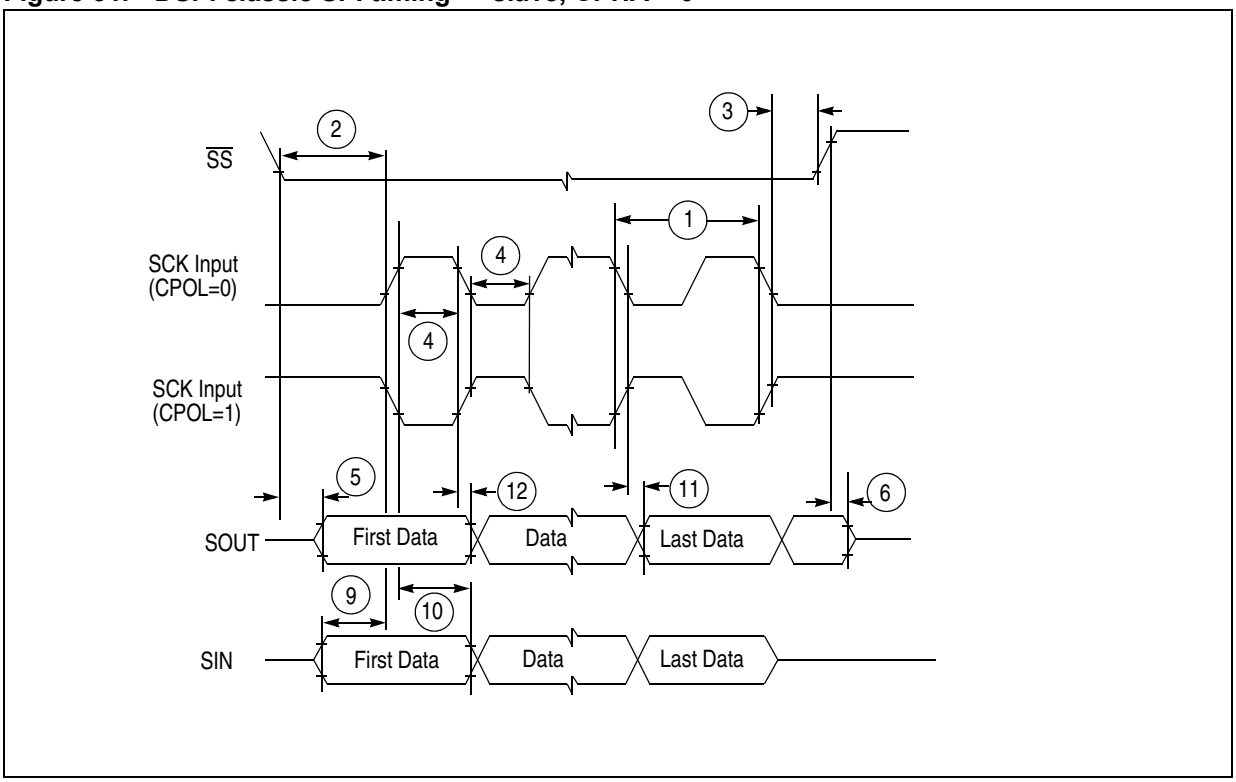


Figure 32. DSPI classic SPI timing — slave, CPHA = 1

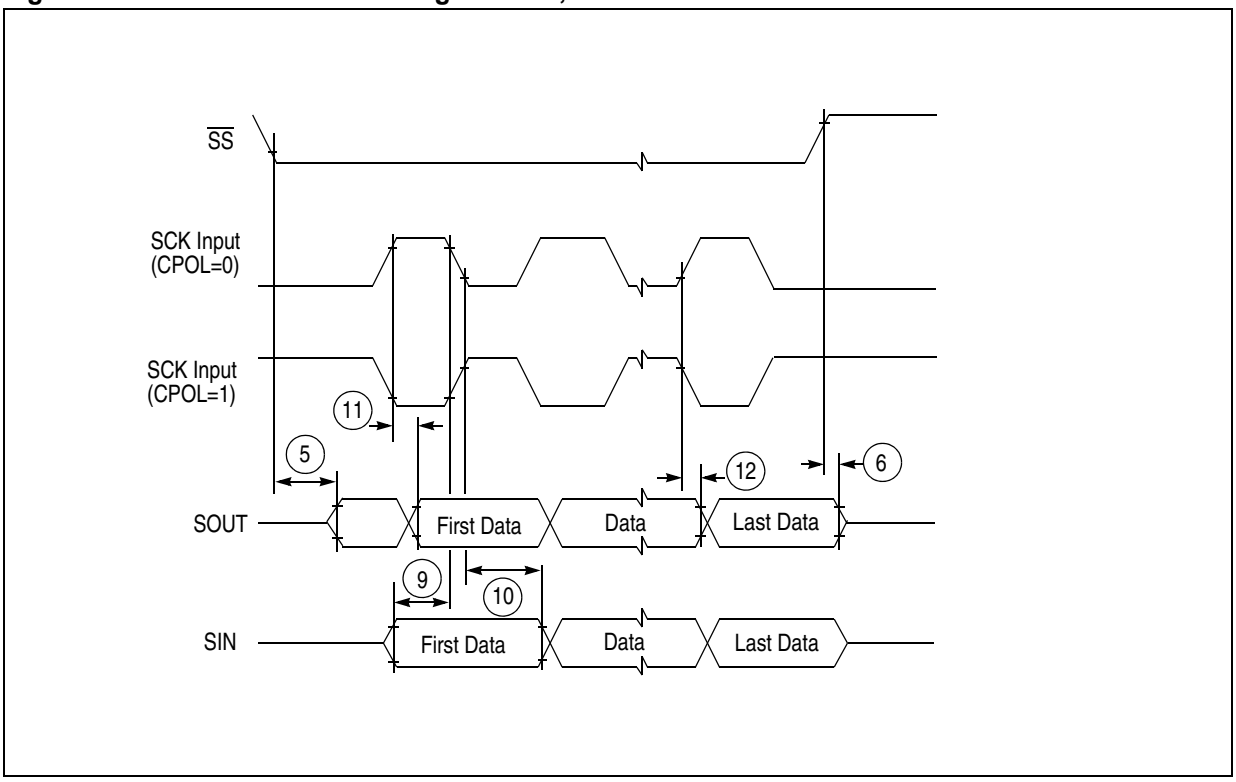


Figure 33. DSPI modified transfer format timing — master, CPHA = 0

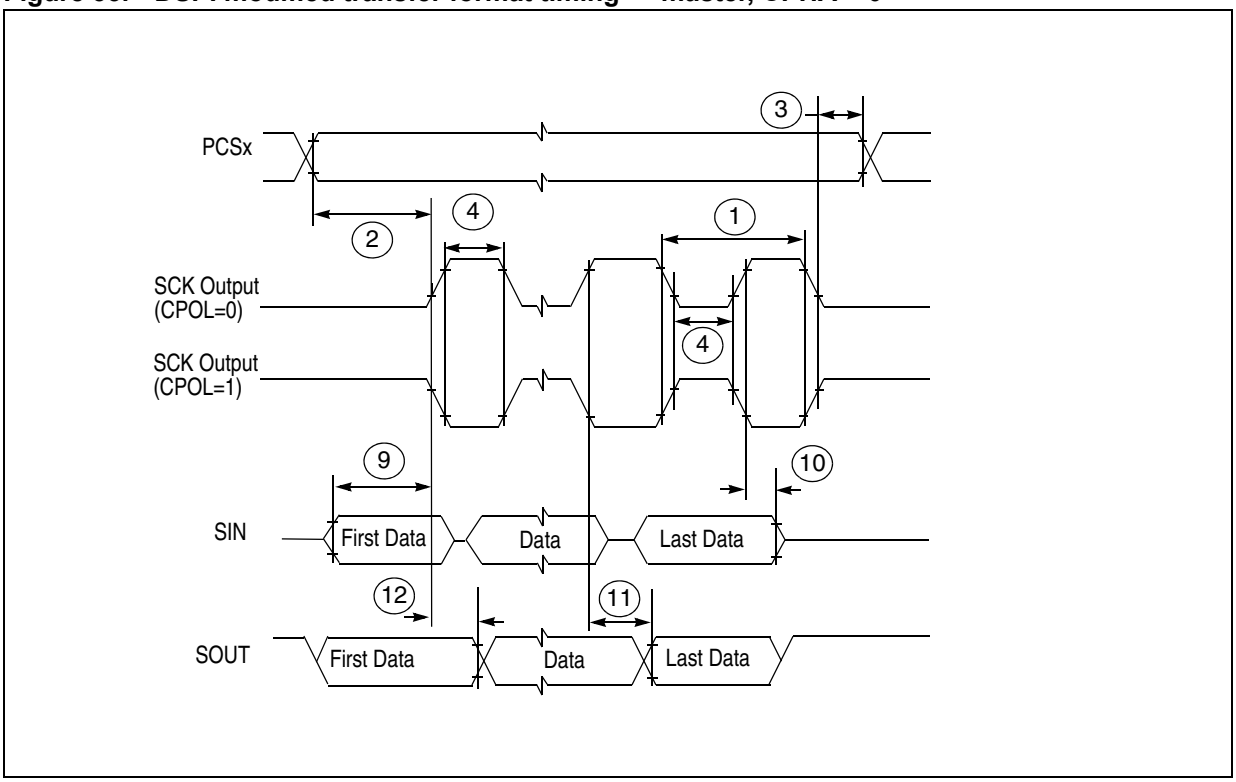


Figure 34. DSPI modified transfer format timing — master, CPHA = 1

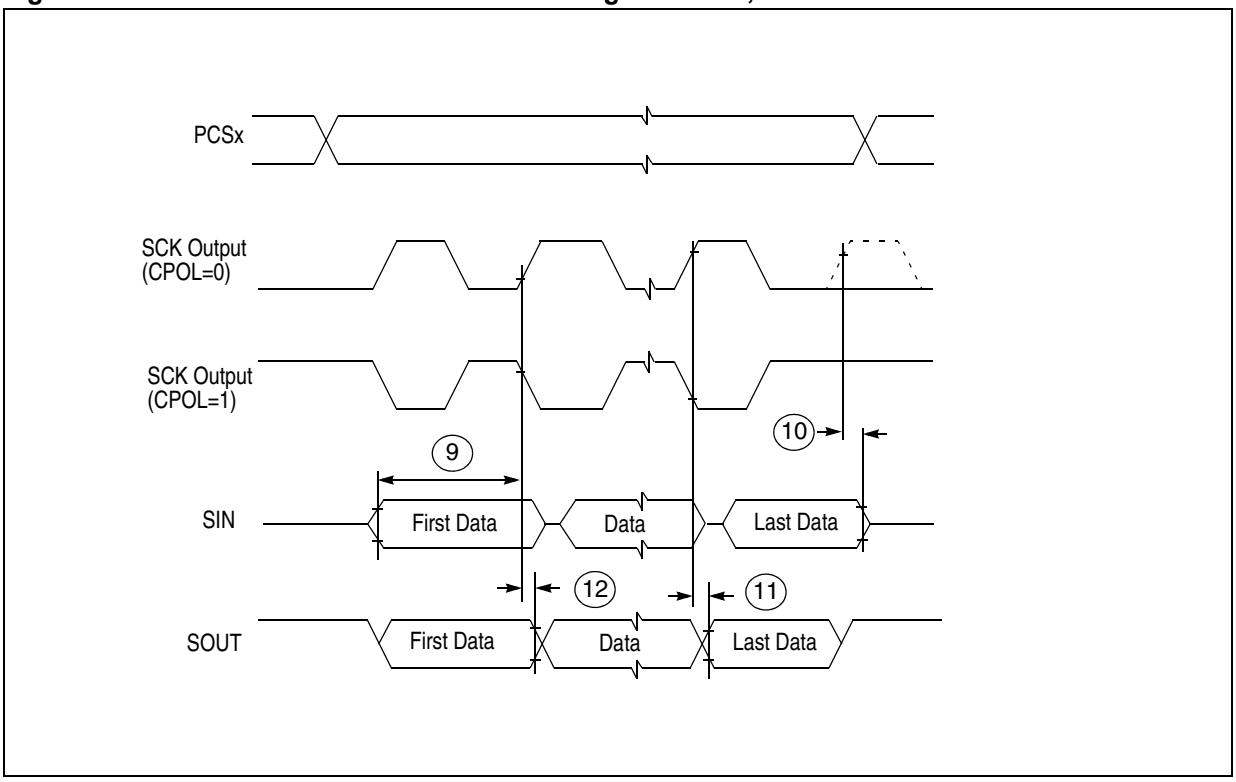


Figure 35. DSPI modified transfer format timing — slave, CPHA = 0

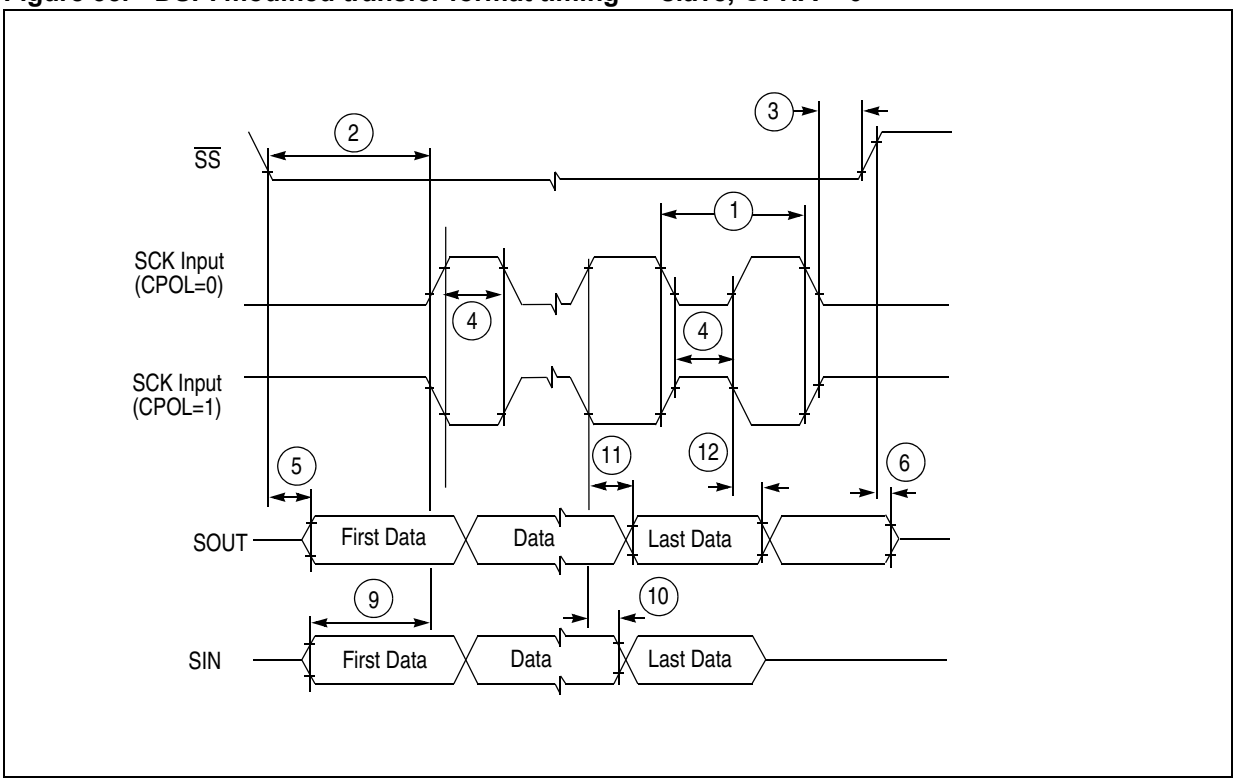


Figure 36. DSPI modified transfer format timing — slave, CPHA = 1

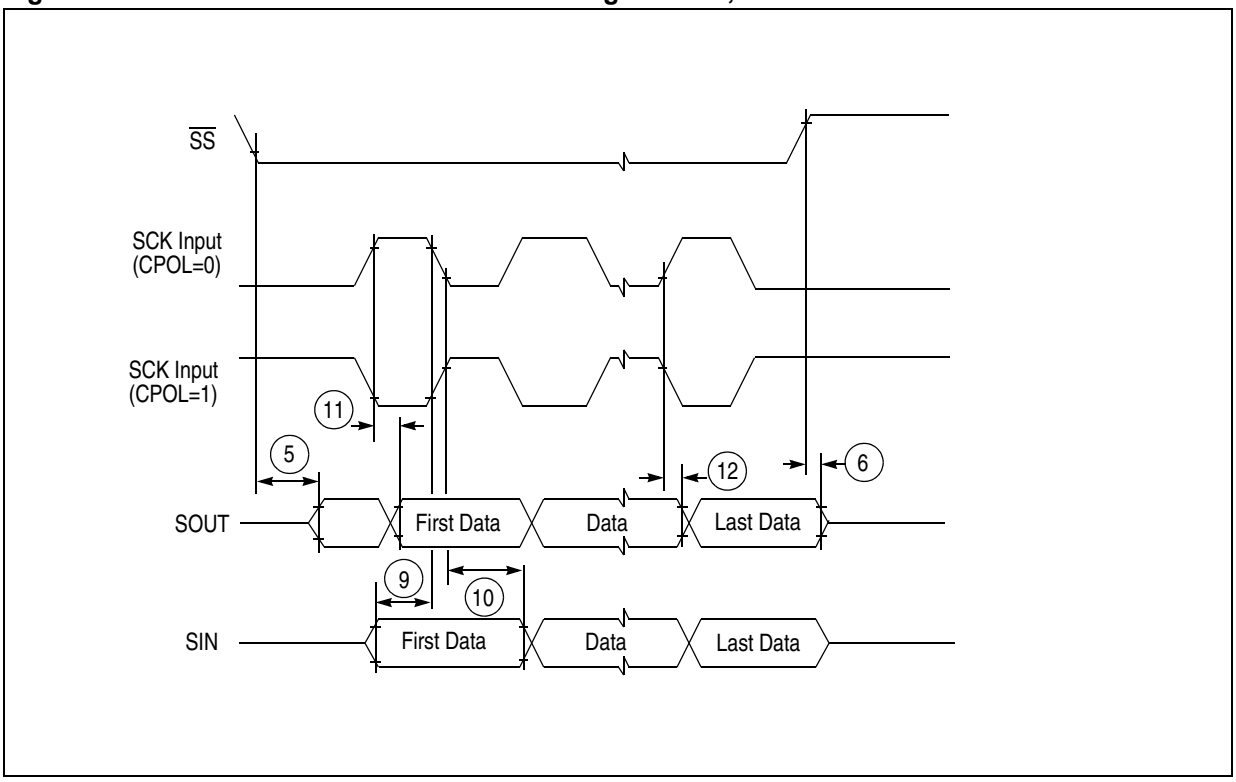
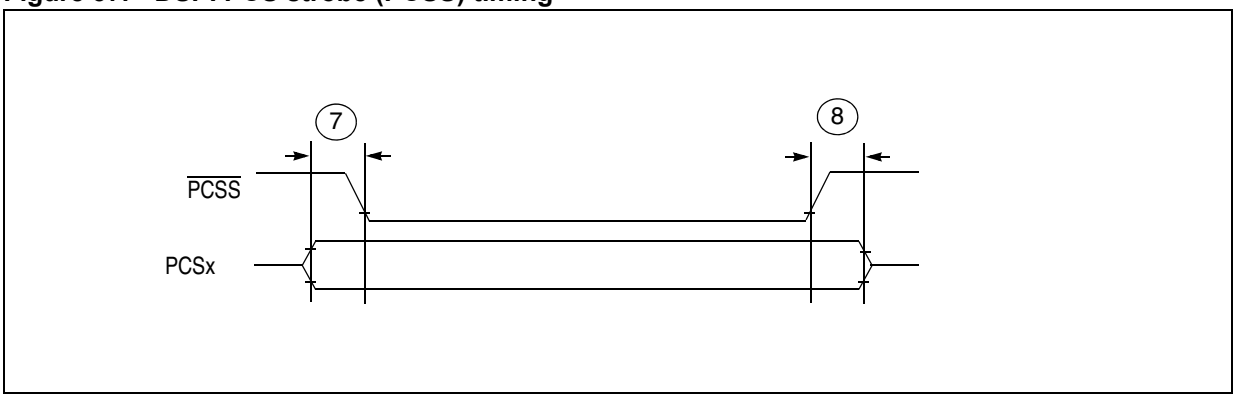


Figure 37. DSPI PCS strobe (PCSS) timing



4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP144 mechanical outline drawing

Figure 38. LQFP144 package mechanical drawing

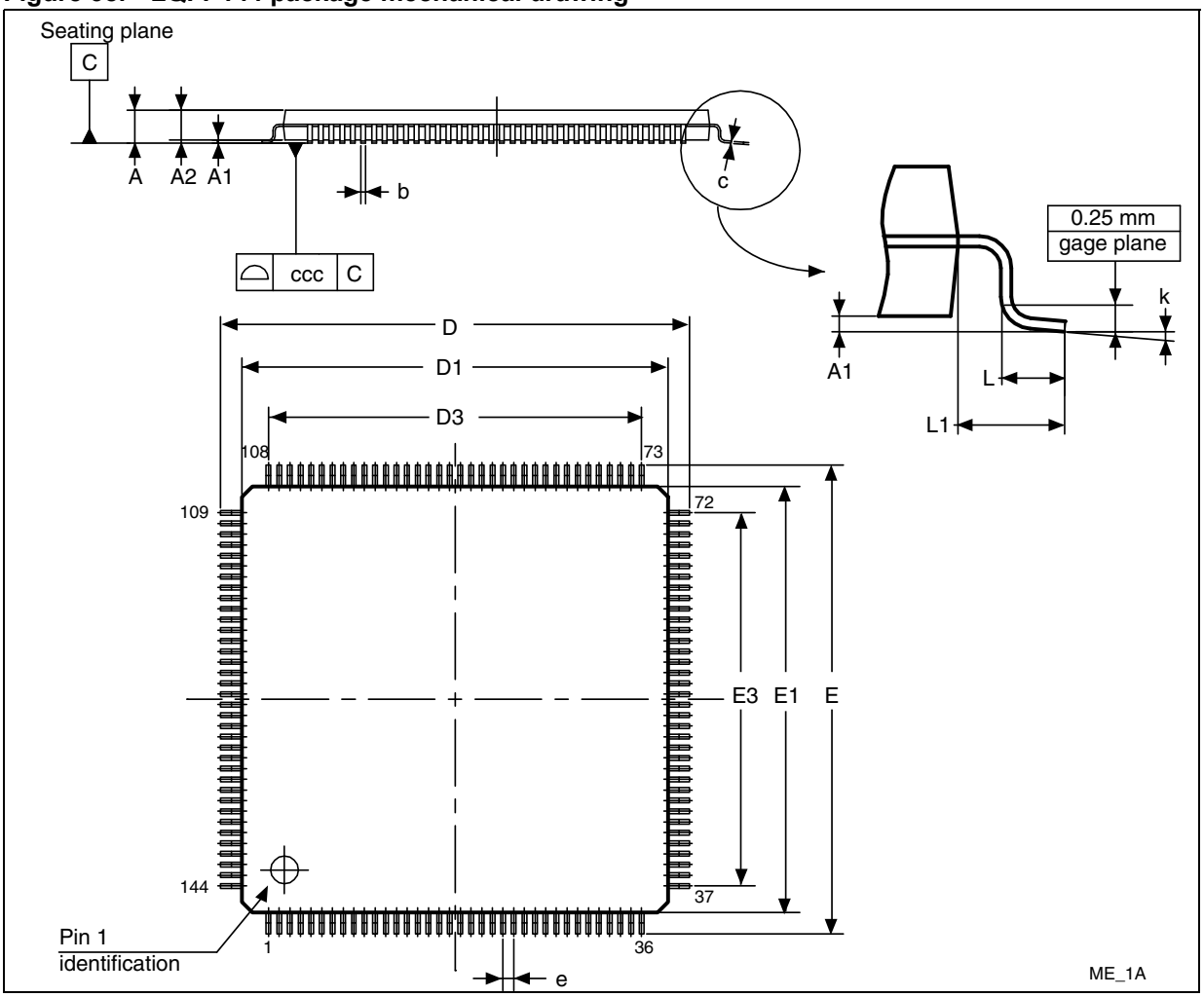


Table 42. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance

4.2.2 LQFP100 mechanical outline drawing

Figure 39. LQFP100 package mechanical drawing

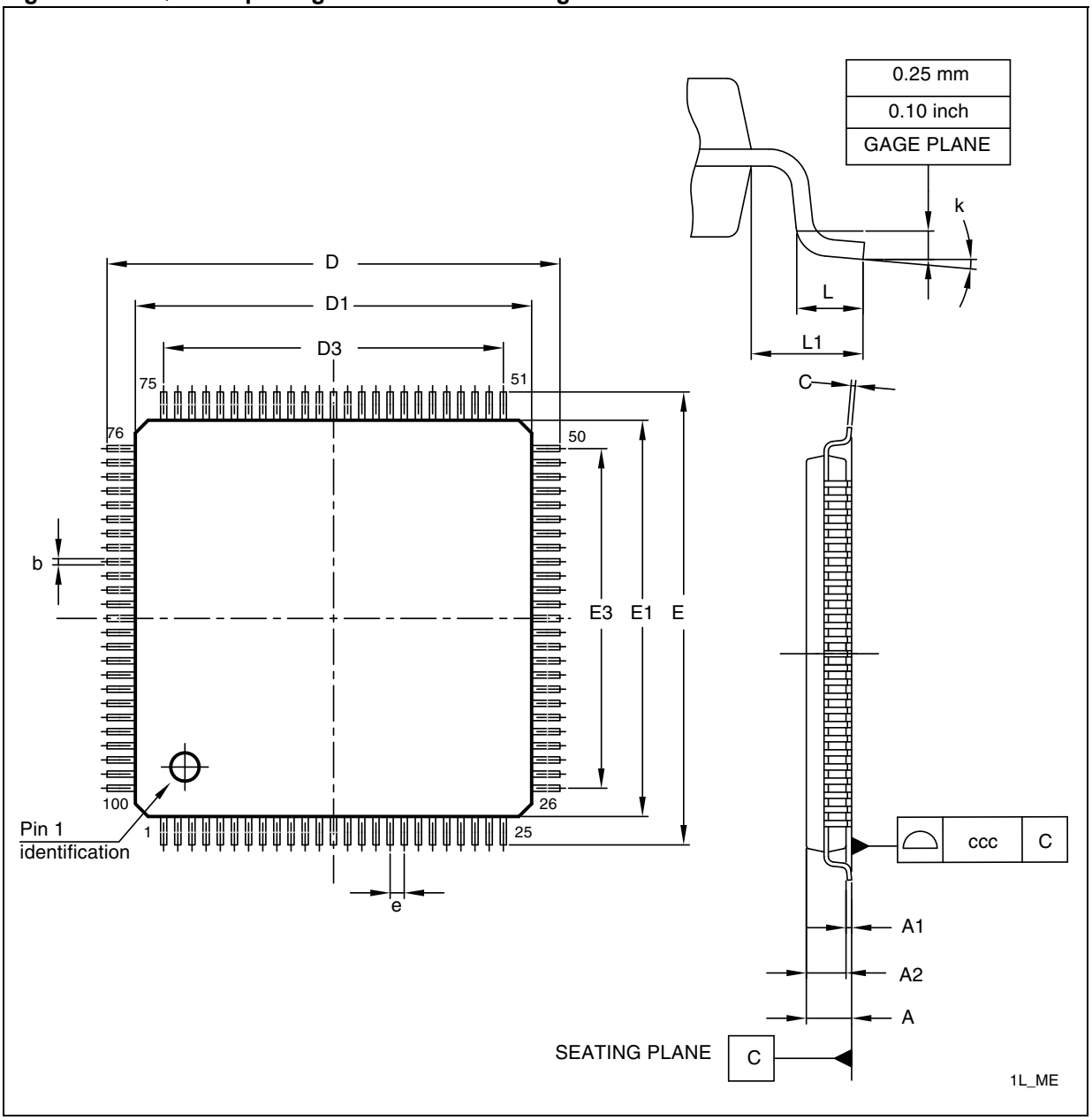


Table 43. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 43. LQFP100 mechanical data (continued)

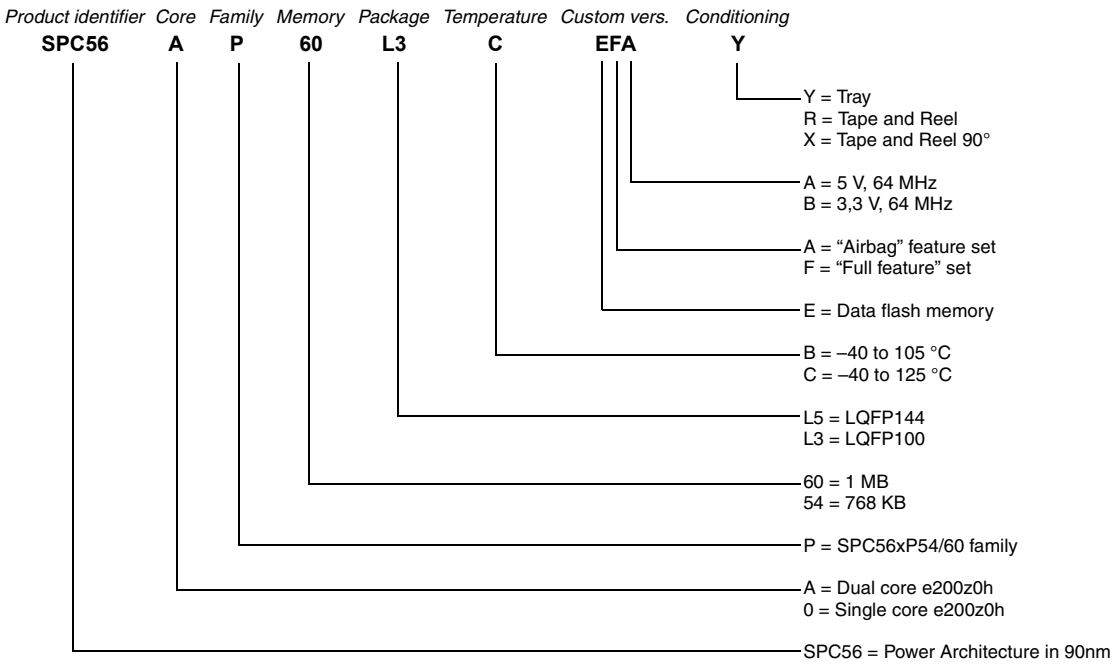
Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance

5 Ordering information

Figure 40. Ordering information scheme[g]

Example code:



g. Not all configurations are available on the market. Please contact your ST Sales Rappresentative to get the list of orderable commercial part number.

6 Revision history

Table 44 summarizes revisions to this document.

Table 44. Document revision history

Date	Revision	Substantive changes
21-Dec-2010	1	Initial release
18-Oct-2011	2	In the Feature list: Revised the first bullet. Changed “Up to 82 GPIO” to “Up to 80 GPIO” Changed “and 82 GPIO” to “and 49 GPIO” Changed “FlexRay module“ to “1 FlexRay™ module”. Added *Section 1.5, Feature details* *Table 4: SPC56xP54/60 series block summary*, added FlexRay entry. In the “LQFP176 pinout (top view)” figure: – Pin 104 now is TDI, was PB[5] – Pin 107 now is TDO, was PB[4] – Pin 71 now is NC, was OKOUT – Pin 72 now is NC, was OKOUT_B – Pin 87 now is NC, was NBYPASS_HV – Pin 88 now is NC, was IPP_LIVI_B_VDDIO *Table 7: Pin muxing*: PB[6] was clk_out_div5, is now clk_out_div256 Removed PB[4] and PB[5] rows In the A[3] row, changed ABS[2] to ABS[1] *Section 3.11, DC electrical characteristics*, added “Peripherals supply current (5 V and 3.3 V)” table *Table 14: EMI testing specifications*, removed all references to SAE Replaced both *Table 12: Thermal characteristics for 144-pin LQFP* and *Table 13: Thermal characteristics for 100-pin LQFP* *Table 30: PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, TA = TL to TH)*, changed the max value of f_{SYS} from 120 to 64 *Table 33: Program and erase specifications*: Removed all TBC changed the initial max value of T_{BKPRG} (Code Flash) from 3.3 to 6.6 s changed the max value of T_{BKPRG} (Data Flash) from 1.9 to 4.1 s changed the max value of $T_{wprogram}$ (Data Flash) from 300 to 500 µs Added t_{ESRT} row *Table 17: Voltage regulator electrical characteristics*, updated $V_{DD_LV_REGCOR}$ values Updated *Table 18: Low voltage monitor electrical characteristics* Updated *Table 21: Supply current (5.0 V, NVUSRO[PAD3V5V]=0)* and *Table 23: Supply current (3.3 V, NVUSRO[PAD3V5V]=1)* Removed “NVUSRO[OSCILLATOR_MARGIN] field description” section. Removed ordarable parts tables.

Table 44. Document revision history (continued)

Date	Revision	Substantive changes
15-May-2012	3	Removed “Enhanced Full-featured” version. In the cover page, added “(1 × Master/Slave, 1 × Master Only)“ at the end of the bullet “2 LINFlex modules (LIN 2.1)” *Table 2: SPC56xP54/60 device comparison*, updated the value of “LINFLEX module” to “2 (1 × Master/Slave, 1 × Master only)” *Section 1.5.4: On-chip flash memory with ECC* replaced two occurrences of “3 wait states” to “2 wait states” replaced 60 MHz to 64 MHz *Section 1.5.21: Serial communication interface module (LINFlex)*, updated first bullet to “Supports LIN Master mode (on both modules), LIN Slave mode (on one module) and UART mode” *Section 1.5.24: Analog-to-digital converter (ADC)*, removed bullet concerning the analog watchdogs from Normal mode features. *Table 5: Supply pins*, removed V_{REG_BYPASS} row. *Table 6: System pins*: added V_{REG_BYPASS} row added a footnote about $\overline{RESET}$ *Table 9: Absolute maximum ratings*: changed typical value of TV_{DD} to 0.25 and added a footnote added V_{INAN} entry Updated *Section 3.8.1: Voltage regulator electrical characteristics* Updated *Table 14: EMI testing specifications* *Table 18: Low voltage monitor electrical characteristics*, changed maximum value of $V_{MLVDDOK_H}$ to 1.15 *Table 20: DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)*, added IPU and IPD rows for $\overline{RESET}$ pin. *Table 21: Supply current (5.0 V, NVUSRO[PAD3V5V]=0)*: added maximum values of $I_{DD_LV_CORE}$ for: RUN, HALT, and STOP mode updated values and parameter classification of I_{DD_FLASH} *Table 22: DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)*, added IPU and IPD rows for $\overline{RESET}$ pin. *Table 23: Supply current (3.3 V, NVUSRO[PAD3V5V]=1)*: added maximum values of $I_{DD_LV_CORE}$ for: RUN, HALT, and STOP mode updated values and parameter classification of I_{DD_FLASH} Added *Table 26: I/O consumption* *Table 31: 16 MHz RC oscillator electrical characteristics*, changed minimum and maximum values of Δ_{RCMVAR} respectively to -6 and 6. Renamed *Figure 16: Input equivalent circuit (precise channels)* (was “Input equivalent circuit”) Added *Figure 17: Input equivalent circuit (extended channels)* *Section 3.15.1: Input impedance and ADC accuracy*, updated *Equation 4* and *Equation 10* *Table 32: ADC conversion characteristics*, added V_{INAN}, C_{P3} and R_{SW2} rows

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