PLESSEY
Solid State

SP8906

500MHz 4-MODULUS DIVIDER

The SP8906 is a 4-modulus (÷256/255/240/239) divider for use in frequency synthesisers operating to 500MHz. Designed to interface directly to the NJ8811 synthesiser control circuit, the SP8906 simplifies synthesiser designs at UHF.

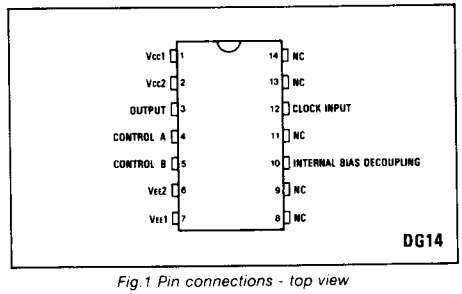


Fig.1 Pin connections - top view

FEATURES

- AC Coupled Input (Internal Bias)
- TTL/MOS Compatible Inputs and Outputs
- Wide Frequency Range: 20 to 500MHz

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 500mW
- Temperature Range: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +150°C
- Max. Clock Input Voltage: 2.5V p-p

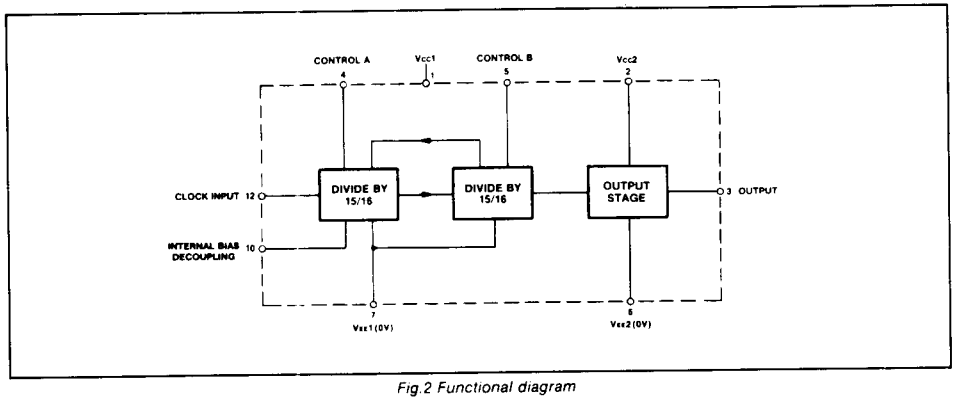


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC1}, V_{CC2} = 5.0V ± 0.25V
Temperature: T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency(sinewave input)	f_{max}	500		MHz	Input 400-1000mV p-p
Miminim frequency(sinewave input)	f_{min}		20	MHz	Input 600-1000mV p-p
Output high voltage	V_{OH}	2.5		V	I_{OH} = -1mA
Output low voltage	V_{OL}		0.5	V	I_{OL} = 2mA
Power supply current	I_{CC}		100	mA	Inputs and output O/C
Input low level	V_{IL}		1.3	V	
Input high level	V_{IH}	2.3		V	
Input current	I_{IL}		-1.2	mA	V_{IN} = 0.5V
Clock to output delay	t_p		60	ns	
Set-up and release time	t_s,t_r	5		ns	Control A I/P
Set-up and release time	t_s,t_r	8		ns	Control B I/P

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig. 6

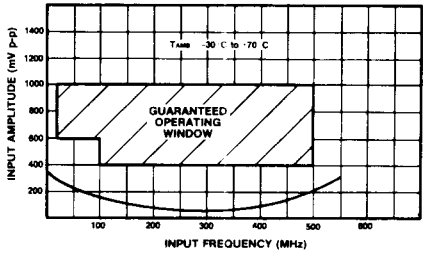


Fig.3 Typical characteristics SP8906

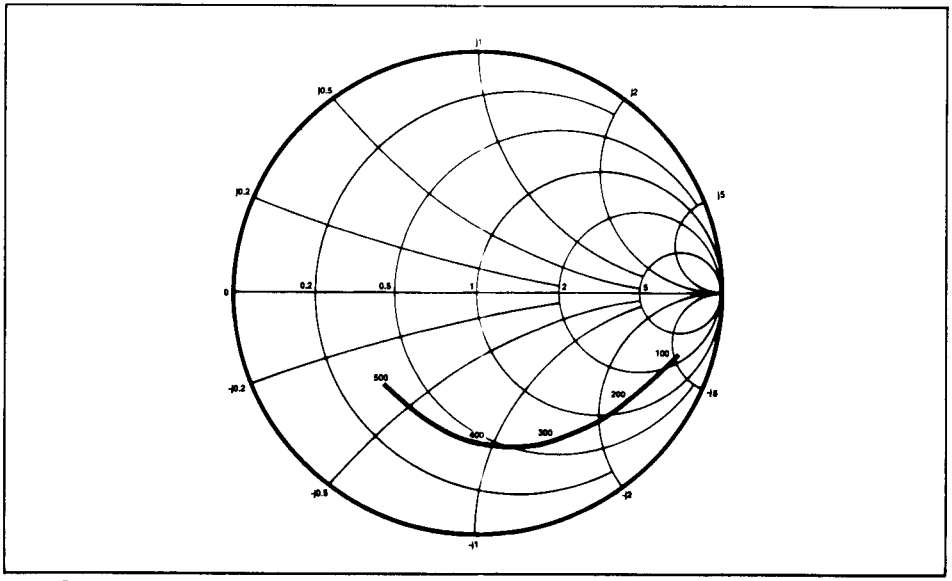


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input should be capacitively coupled to the signal source. The input signal path is completed by connecting a decoupling capacitor from the internal bias decoupling, pin 10, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 33k or greater between pin 10 and ground (pin 7), see Fig. 5 .
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The output is TTL/CMOS compatible and is current limited to 3mA sink in the low state and 5mA source in the high state.
5. The control inputs have internal 5k pull-up resistors which can be directly coupled to open collector outputs.
6. There are separate supply lines for the output stage ($V_{CC}2$, $V_{EE}2$) to reduce input to output and output to input coupling.
7. The minimum input sinewave frequency can be improved by adding hysteresis (See Fig. 5) to reference inputs. Care must be taken not to apply to much hysteresis as this will reduce input sensitivity. A maximum value of 50mV (R1 = 33k) should not be exceeded.
8. Under certain conditions, when the device is dynamically locked, an oscillation occurs which can be prevented by insertion of a 1µH RF choke in series with $V_{CC}1$ and $V_{CC}2$. Under these conditions $V_{CC}1$ and $V_{CC}2$ pins should not be decoupled. See Fig. 5.
9. The input impedance of SP8906 is a function of frequency. See Fig. 4.
10. See Table II for different ratios obtained.

Control A	Control B	Division Ratio
1	1	256
0	1	255
1	0	240
0	0	239

Table 2

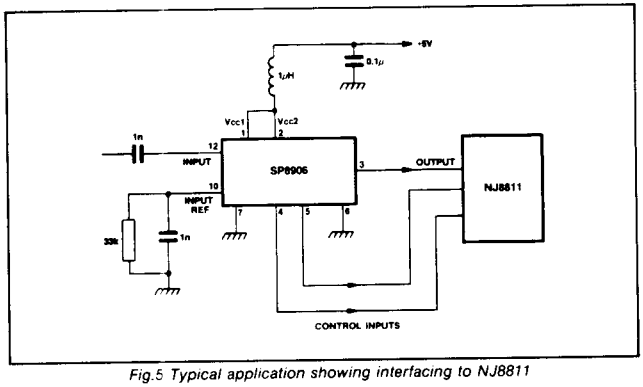


Fig.5 Typical application showing interfacing to NJ8811

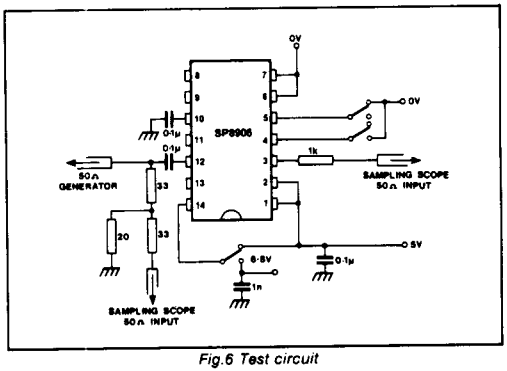


Fig.6 Test circuit