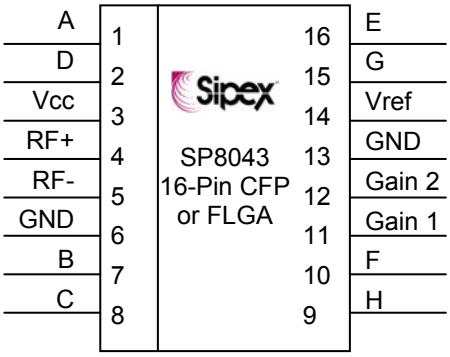
SP8043

10 Channel Photo Detector IC

FEATURES

- Dual wavelength 650 and 780nm
- 55MHz Data channel bandwidth (-1db point)
- Selectable gain and Power Down Mode
- Available in wafer form,
  16-pin Clear-mold FlatPack (CFP) package,
  or 16-pin Flexible Land Grid Array (FLGA)



APPLICATION

- x4 DVD + R Read and write
- x2.4 DVD Dual layer write
- x4 DVD + RW Write
- x8 CD Read

GENERAL DESCRIPTION

The SP8043 is a ten-channel photo detector IC (PDIC) designed for DVD and CD applications and can operate at wavelength of 650 and 780 nm. The device contains three photo diode (sensor) arrays, one of them with four identical sensors A – D and others with two sensors (E, F and G, H respectively). The ten channels consist of four high speed channels (A, B, C, and D), four slow channels (E, F, G, and H), and two RF channel with paraphase output (RF+ and RF-). The high speed channel output provides a signal from one of the sensors A – D. The E, F, G, and H channels output is used for servo control. The RF channels output is the sum of A + B + C + D channels with identical weights given to all channels.

Two gain select inputs allow the setting of four gain modes and a Power Down mode with low power consumption if Gain 2 input left floating.

The SP8043 is manufactured with an advanced 10GHz BICMOS technology.

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PIN ASSIGNMENTS

Pin #	Pin Name	Pin Function
1	A	Output of A channel
2	D	Output of D channel
3	Vcc	Supply voltage. Bypass to GND with ceramic capacitor 0.1uF
4	RF+	Output of RF+ channel. RF+ = 0.375 (A + B + C + D)
5	RF-	Output of RF- channel. RF- = -0.375 (A + B + C + D)
6	GND	Ground pin
7	B	Output of B channel
8	C	Output of C channel
9	H	Output of H channel
10	F	Output of F channel
11	Gain 1	Mode switch input.
12	Gain 2	Mode switch input.
13	GND	Ground pin
14	Vref	Reference voltage. Bypass to GND with ceramic capacitor 0.1uF
15	G	Output of G channel
16	E	Output of E channel

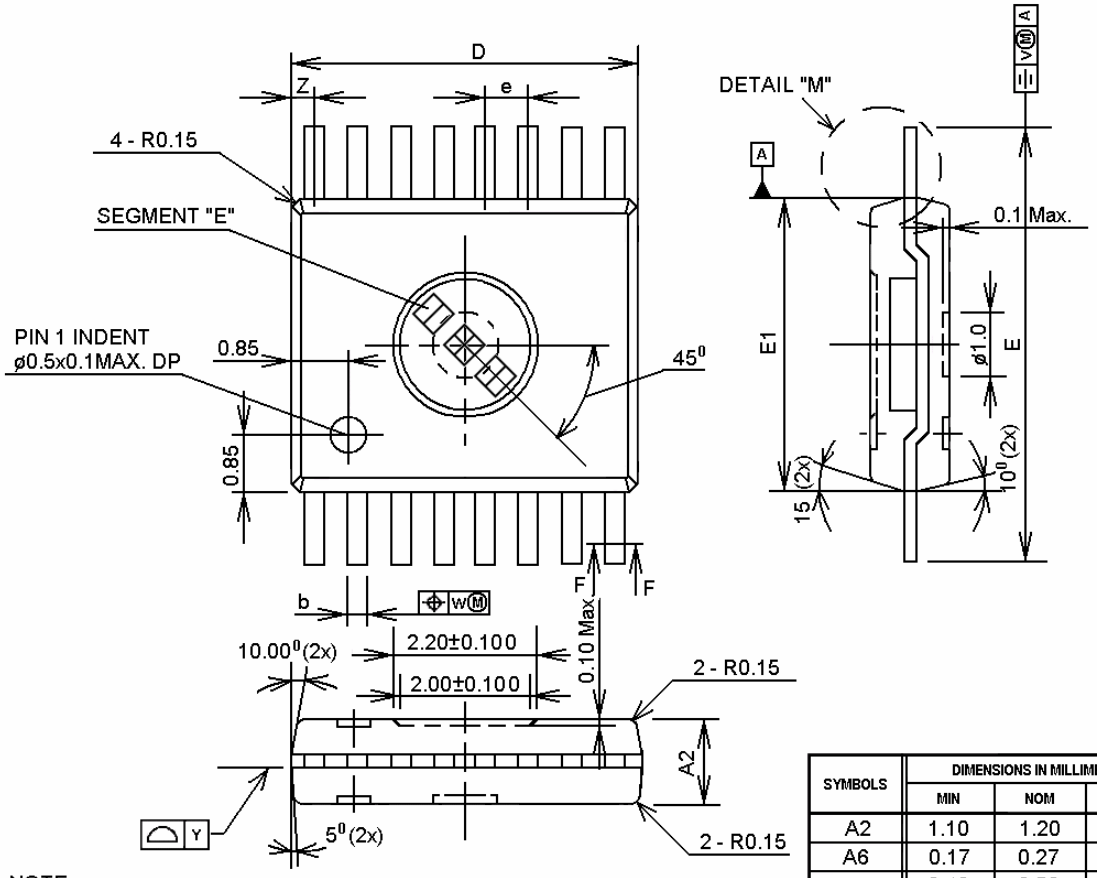
BOARD LAYOUT AND GROUNDING

To obtain the best performance from the SP8043, a printed circuit board with ground plane is required. Both ground pins (pins #6 and #13) should be connected to the ground plane. High quality, low series resistance ceramic 0.1uF bypass capacitors should be used at the Vcc and Vref pins (pins #3 and #14). These capacitors must be located as close to the pins as possible. The traces connecting the pins to the ground plane, Vcc, Vref, and bypassing capacitors must be kept short and should be made as wide as possible.

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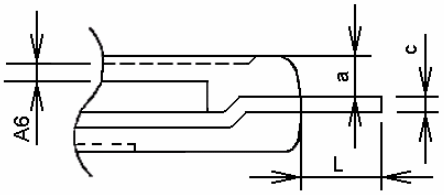
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16LD CLEAR MOLD FLATPACK (CFP) PACKAGE DIMENSIONS

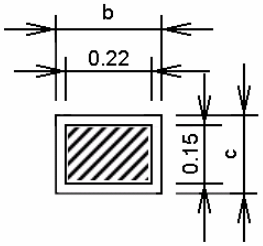


SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A2	1.10	1.20	1.30
A6	0.17	0.27	0.37
a	0.40	0.50	0.60
b	0.20	0.26	0.32
c	0.13	0.20	0.25
D	5.10	5.20	5.30
E	6.50	6.60	6.70
E1	4.30	4.40	4.50
e	–	0.65	–
L	–	1.10	–
V	–	0.20	–
W	–	0.13	–
Z	0.18	0.33	0.48
y	0.00	–	0.10

NOTE:
1. CONTROLLING DIMENSION: mm
2. LEAD FRAME METAL: C194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS, AND GATE BURRS. MOLD FLASH, TIE BAR BURRS, AND GATE BURRS SHALL NOT EXCEED 0.008" (0.20mm) PER END DIMENSION. "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.008" (0.20mm) PER SIDE
4. TOLERANCE: ±0.008" (0.20mm) UNLESS OTHERWISE SPECIFIED
5. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC
6. LEAD FRAME DOWNSET IS 0.200mm±0.025
7. WAFER THICKNESS IS: 380±20um



DETAIL "M"

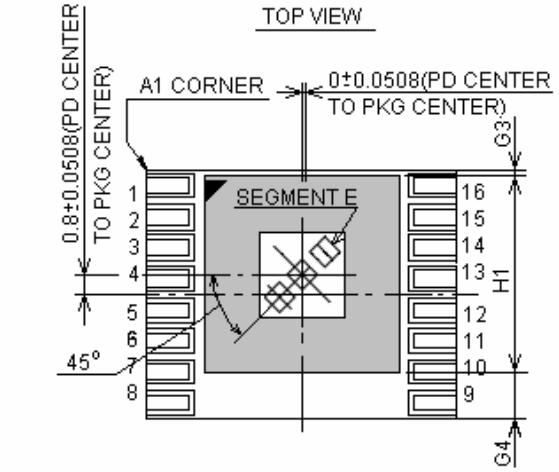


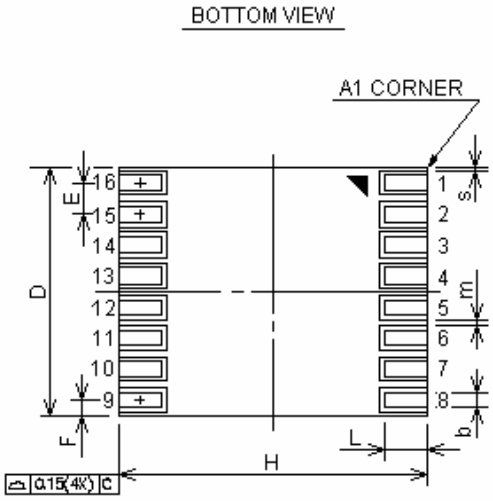
"SECTION F-F"

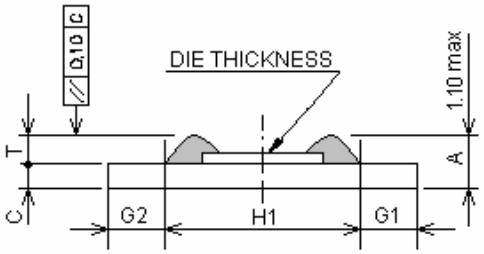
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16LD FLEXIBLE LAND GRID ARRAY (FLGA) PACKAGE DIMENSIONS







NOTE: CROSS SECTION (CENTER PD AREA)
DIE THICKNESS 0.2 mm (8mil)

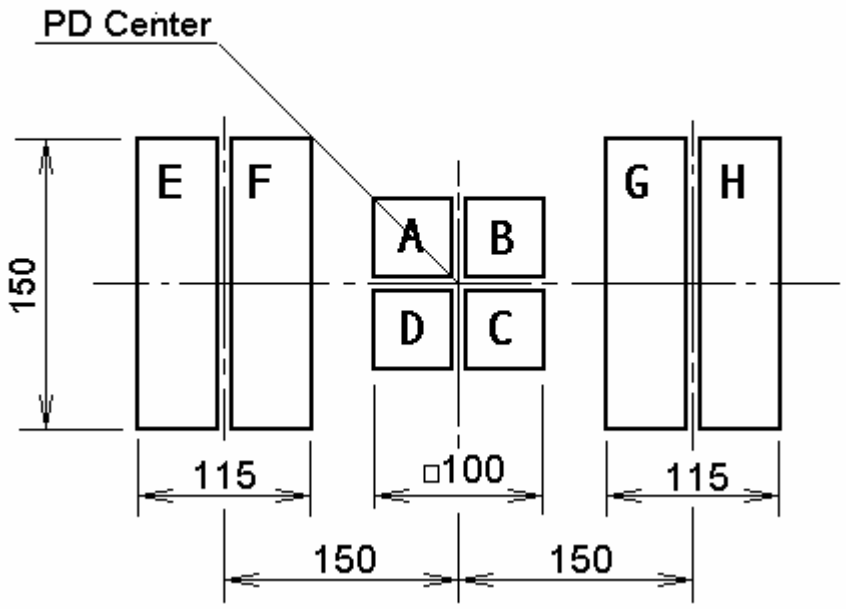
SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	–	–	1.10
b	0.23	0.28	0.33
C	–	0.36	–
D	5.10	5.20	5.30
H	6.50	6.60	6.70
H1	–	4.20	–
G1	–	1.20	–
G2	–	1.20	–
G3	–	0.15	–
G4	–	0.85	–
E	–	0.65	–
F	0.24	0.32	0.40
L	0.50	0.60	0.70
T	–	0.50	–
s	0.135	–	–
m	0.27	–	–

Note: Dimensions are subject to changes but will be fixed once this package is fully developed

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PHOTO DETECTOR PATTERN



Note: 1. Detector size units: µm
2. Separation between segments < 5 µm
3. PD array is rotated clockwise by 45º in CFP package (as shown on page 3) and by 135º in FLGA package (as shown on page 4)

ORDERING INFORMATION

Part number	Temperature range	Package Type
SP8043DC	-30 + 80^{0}C	16-pin Clear Mold Flatpack (CFP)
SP8043DG1	-30 + 80^{0}C	16-pin Flexible Land Grid Array (FLGA)
SP8043W	-30 + 80^{0}C	Wafer

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