SP706R/S/T - SP708R/S/T

3.0V/3.3V Low Power Microprocessor Supervisory Circuits

June 2010 Rev. 2.0.0

GENERAL DESCRIPTION

The SP706R/S/T and SP708R/S/T series is a family of microprocessor (µP) supervisory circuits that integrate myriad components involved in discrete solutions which monitor power-supply and battery in µP and digital systems.

The SP706R/S/T and SP708R/S/T series will significantly improve system reliability and operational efficiency when compared to solutions obtained with discrete components. The features of the SP706R/S/T and SP708R/S/T series include a watchdog timer, a µP reset, a Power Fail Comparator, and a manual-reset input.

The SP706R/S/T and SP708R/S/T series is ideal for 3.0V or 3.3V applications in automotive systems, computers, controllers, and intelligent instruments. The SP706R/S/T and SP708R/S/T series is an ideal solution for systems in which critical monitoring of the power supply to the µP and related digital components is demanded.

APPLICATIONS

- **Processors & DSPs Based Systems**
- **Industrial & Medical Instruments**

FEATURES

- **Precision Low Voltage Monitor**
  - SP706R/SP708R: +2.63V
  - SP706S/SP708S: +2.93V
  - SP706T/SP708T: +3.08V
- **200ms RESET Pulse Width**
  - SP706R/S/T: Active Low
  - SP708R/S/T: Active High and Active Low
- **Independent Watchdog Timer**
  - 1.6s Timeout (SP706R/S/T)
  - Enable/Disable Function
- **40µA Maximum Supply Current**
- **Debounced TTL/CMOS Manual Reset Input**
- **$\overline{\text{RESET}}$ Asserted Down to V_{CC}=1V**
- **V_{CC} Glitch Immunity**
- **Voltage Monitor for Power Failure or Low Battery Warning**
- **8-Pin NSOIC and MSOP Packages**
- **Pin Compatible with Industry Standards 706R/S/T and 708R/S/T**

Part Number	RESET Threshold	RESET Active	Manual RESET	Watchdog	PFI Accuracy
SP706R	2.63V	Low	Yes	Yes	4%
SP706S	2.93V	Low	Yes	Yes	4%
SP706T	3.08V	Low	Yes	Yes	4%
SP708R	2.63V	Low and High	Yes	No	4%
SP708S	2.93V	Low and High	Yes	No	4%
SP708T	3.08V	Low and High	Yes	No	4%

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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} .....-0.3V to 6.0V
All Other Inputs (Note 1).....-0.3V to (V_{CC}+0.3V)
Input Current
  VCC.....20mA
  GND 20mA
  Output Current (All outputs) 20mA
ESD Rating (HBM - Human Body Model) 2kV
Continuous Power Dissipation
  SO (derate 5.88mW/°C above +70°C).....471mW
  Mini SO (derate 4.10mW/°C above +70°C) 330mW
Storage Temperature .....-65°C to 160°C
Lead Temperature (Soldering, 10 sec) .....300°C

ELECTRICAL SPECIFICATIONS

Unless otherwise indicated, V_{CC} = 2.7V to 5.5V (SP70xR), V_{CC} = 3.15V to 5.5V (SP70xS), V_{CC} = 3.0V to 5.5V (SP70xT), T_A= T_{MIN} to T_{MAX}, typical at 25°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
Operating Voltage Range V_{CC}	1.0		5.5	V		
Supply Current I_{SUPPLY}		25	40	µA		$\overline{MR}$=V_{CC} or floating, WDI floating
Reset Threshold	2.55	2.63	2.70	V		SP706R. SP708R
	2.85	2.93	3.00			SP706S. SP708S
	3.00	3.08	3.15			SP706T. SP708T
Reset Threshold Hysteresis		20		mV		Note 2
Reset Pulse Width t_{RS}	140	200	280	ms		Note 2
$\overline{RESET}$ Output Voltage				V		
V_{OH}	0.8xV_{CC}					$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SOURCE}=500µA
V_{OL}			0.3			$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SINK}=1.2mA
V_{OH}	V_{CC}-1.5					4.5V<V_{CC}<5.5V, I_{SOURCE}=800µA
V_{OL}			0.4			4.5V<V_{CC}<5.5V, I_{SINK}=3.2mA
RESET Output Voltage				V		
V_{OH}	V_{CC}-0.6					$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SOURCE}=215µA
V_{OL}			0.3			$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SOURCE}=1.2mA
V_{OH}	V_{CC}-1.5					4.5V<V_{CC}<5.5V, I_{SOURCE}=800µA
V_{OL}			0.4			4.5V<V_{CC}<5.5V, I_{SOURCE}=3.2mA
Watchdog Timeout Period t_{WD}	1.00	1.60	2.25	s		V_{CC}<3.6V
WDI Pulse Width t_{WP} (note 1)	50			ns		V_{IL}=0.4V, V_{IH}=0.8xV_{CC}
WDI Input Threshold				V		
V_{IL}			0.6			$V_{RST(MAX)}$<V_{CC}<3.6V
V_{IH}	0.7xV_{CC}					$V_{RST(MAX)}$<V_{CC}<3.6V
V_{IL}			0.8			V_{CC}=5V
V_{IH}	3.5					V_{CC}=5V
WDI Input Current	-1	0.02	1	µA		WDI=0V or WDI=V_{CC}
$\overline{WDO}$ Output Voltage				V		
V_{IL}	0.8xV_{CC}					$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SOURCE}=500µA
V_{IH}			0.3			$V_{RST(MAX)}$<V_{CC}<3.6V, I_{SINK}=1.2mA
V_{IL}	V_{CC}-1.5					4.5V<V_{CC}<5.5V, I_{SOURCE}=800µA
V_{IH}			0.4			4.5V<V_{CC}<5.5V, I_{SINK}=3.2mA
$\overline{MR}$ Pull-up Current	25	70	250	µA		$\overline{MR}$ = 0V, $V_{RST(MAX)}$<V_{CC}<3.6V
	100	250	600			$\overline{MR}$ = 0V, 4.5V<V_{CC}<5.5V

Parameter	Min.	Typ.	Max.	Units		Conditions
$\overline{MR}$ Pulse Width t_{MR}	500			ns		$V_{RST(MAX)}<V_{CC}<3.6V$
	150					$4.5V<V_{CC}<5.5V$
$\overline{MR}$ Input Threshold				V		
V_{IL}			0.6			$V_{RST(MAX)}<V_{CC}<3.6V$
V_{IH}	$0.7xV_{CC}$					$V_{RST(MAX)}<V_{CC}<3.6V$
V_{IL}			0.8			$4.5V<V_{CC}<5.5V$
V_{IH}	2.0					$4.5V<V_{CC}<5.5V$
$\overline{MR}$ to Reset Out Delay t_{MD}			750	ns		$V_{RST(MAX)}<V_{CC}<3.6V$
			250			$4.5V<V_{CC}<5.5V$
PFI Input Threshold	1.20	1.25	1.30	V		V_{CC}=3.0V - SP70xR, PFI falling V_{CC}=3.3V - SP70xS/T, PFI falling
PFI Input Current	-25.00	0.01	25.00	nA		
$\overline{PFO}$ Output Voltage				V		
V_{IL}	$0.8xV_{CC}$					$V_{RST(MAX)}<V_{CC}<3.6V$, I_{SOURCE}=500µA
V_{IH}			0.3			$V_{RST(MAX)}<V_{CC}<3.6V$, I_{SINK}=1.2mA
V_{IL}	V_{CC}-1.5					$4.5V<V_{CC}<5.5V$, I_{SOURCE}=800µA
V_{IH}			0.4			$4.5V<V_{CC}<5.5V$, I_{SINK}=3.2mA

Note 1:WDI minimum rise /fall time is 1µs.

BLOCK DIAGRAM

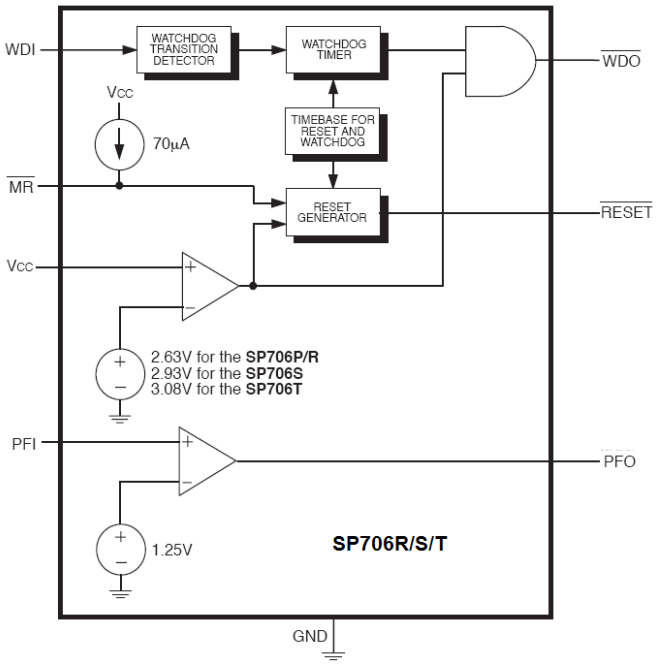


Fig. 1: SP706R/S/T Block Diagram

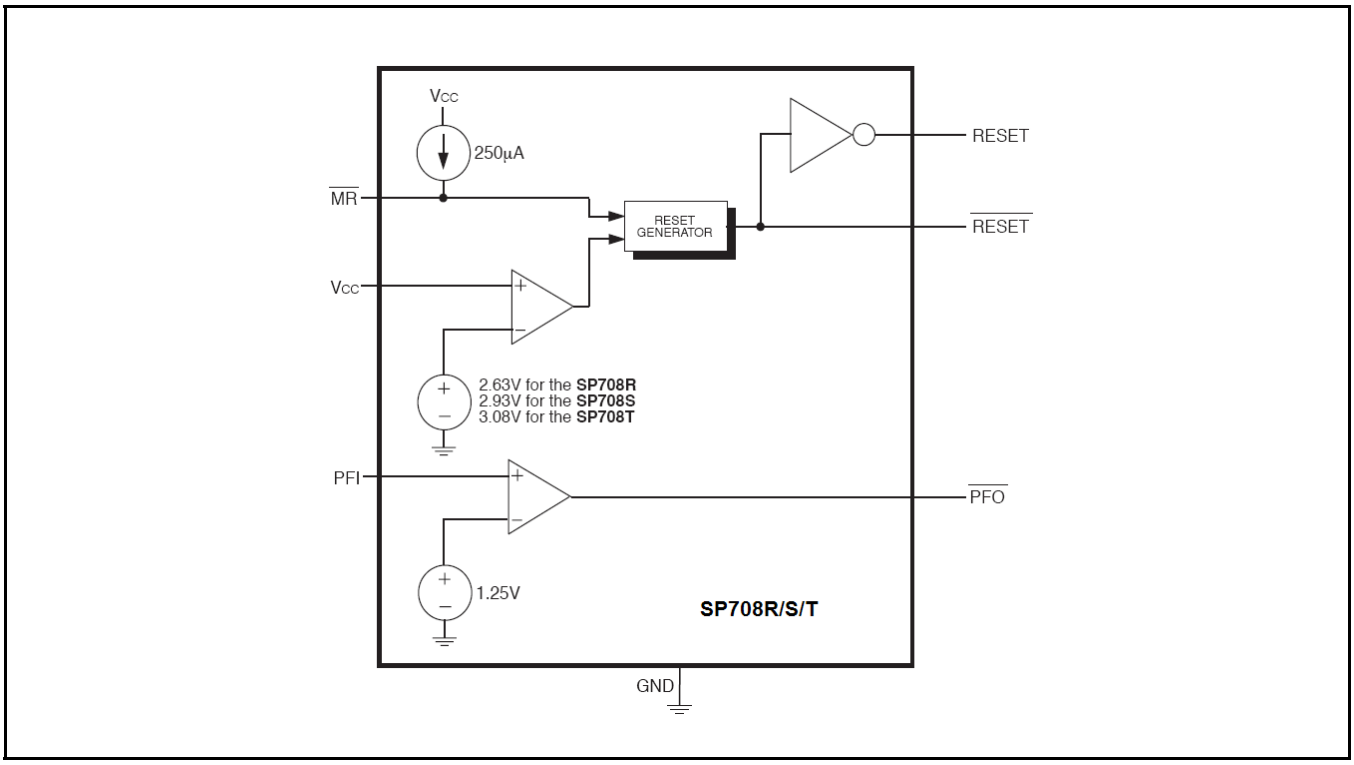


Fig. 2: SP708R/S/T Block Diagram

PIN ASSIGNMENT

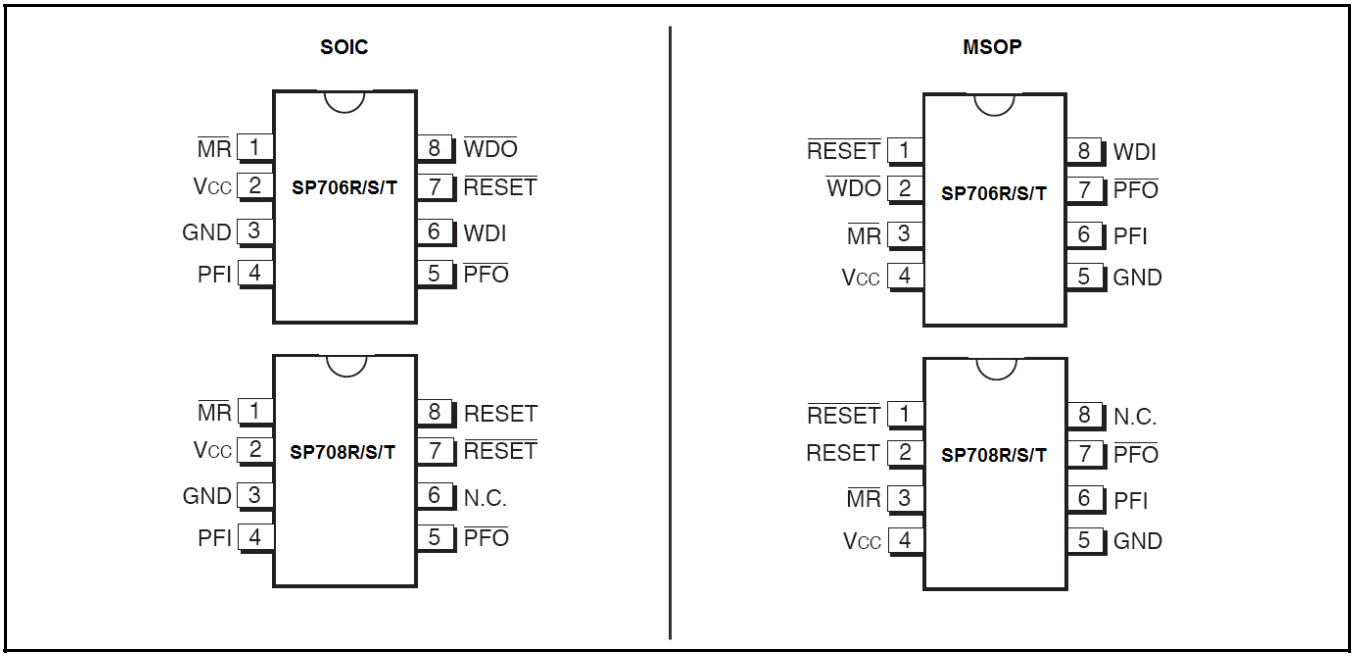


Fig. 3: Pin Assignment

PIN DESCRIPTION

Name	Pin Number				Description
	SP706R/S/T		SP708R/S/T		
	SOIC	MSOP	SOIC	MSOP	
$\overline{MR}$	1	3	1	3	Manual Reset This input triggers a reset pulse when pulled below 0.8V. This active LOW input has an internal 70µA pull-up current. It can be driven from a TTL or CMOS logic line or shorted to ground with a switch.
V_{CC}	2	4	2	4	Voltage Input
GND	3	5	3	5	Ground reference for all signals
PFI	4	6	4	6	Power-Fail Input When this voltage monitor input is less than 1.25V, $\overline{PFO}$ goes LOW. Connect PFI to ground or V_{CC} when not in use.
$\overline{PFO}$	5	7	5	7	Power-Fail Output This output is LOW until PFI is less then 1.25V
WDI	6	8	-	-	Watchdog Input If this input remains HIGH or LOW for 1.6s, the internal watchdog timer times out and $\overline{WDO}$ goes LOW. Floating WDI or connecting WDI to a high-impedance tri-state buffer disables the watchdog feature. The internal watchdog timer clears whenever $\overline{RESET}$ is asserted, WDI is tri-stated, or whenever WDI sees a rising or falling edge.
N.C.	-	-	6	8	No Connect
$\overline{RESET}$	7	1	7	1	Active-LOW $\overline{RESET}$ Output This output pulses LOW for 200ms when triggered and stays LOW whenever V_{CC} is below the reset threshold. It remains LOW for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
$\overline{WDO}$	8	2	-	-	Watchdog Output This output pulls LOW when the internal watchdog timer finishes its 1.6s count and does not go HIGH again until the watchdog is cleared. $\overline{WDO}$ also goes LOW during low-line conditions. Whenever V_{CC} is below the reset threshold, WDO stays LOW. However, unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} is above the reset threshold, $\overline{WDO}$ goes HIGH with no delay.
RESET	-	-	8	2	Active-HIGH RESET Output This output is the complement of $\overline{RESET}$. Whenever RESET is HIGH, $\overline{RESET}$ is LOW and vice-versa. Note that the SP708R/S/T has a reset output only.

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SP706RCN-L	0°C≤T_A≤+70°C	SP706RC YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP706RCN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP706RCU-L	0°C≤T_A≤+70°C	706R CXXX YWW	8-pin MSOP	Bulk	Lead Free	
SP706RCU-L/TR	0°C≤T_A≤+70°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	
SP706REN-L	-40°C≤T_A≤+85°C	SP706RE YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP706REN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP706REU-L	-40°C≤T_A≤+85°C	706R EXXX YWW	8-pin MSOP	Bulk	Lead Free	
SP706REU-L/TR	-40°C≤T_A≤+85°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	
SP706SCN-L	0°C≤T_A≤+70°C	SP706SC YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP706SCN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP706SCU-L	0°C≤T_A≤+70°C	706S CXXX YWW	8-pin MSOP	Bulk	Lead Free	
SP706SCU-L/TR	0°C≤T_A≤+70°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SP706SEN-L	-40°C≤T_A≤+85°C	SP706SE YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP706SEN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP706SEU-L	-40°C≤T_A≤+85°C	706S EXXX YWW	8-pin MSOP	Bulk	Lead Free	
SP706SEU-L/TR	-40°C≤T_A≤+85°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	
SP706TCN-L	0°C≤T_A≤+70°C	SP706TC YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP706TCN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP706TCU-L	0°C≤T_A≤+70°C	706T CXXX YWW	8-pin MSOP	Bulk	Lead Free	
SP706TCU-L/TR	0°C≤T_A≤+70°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	
SP706TEN-L	-40°C≤T_A≤+85°C	SP706TE YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP706TEN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP706TEU-L	-40°C≤T_A≤+85°C	706T EXXX YWW	8-pin MSOP	Bulk	Lead Free	
SP706TEU-L/TR	-40°C≤T_A≤+85°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	
SP708REN-L	-40°C≤T_A≤+85°C	SP708RE YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP708REN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP708SCN-L	0°C≤T_A≤+70°C	SP708SC YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP708SCN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP708SCU-L	0°C≤T_A≤+70°C	708S UXXX YWW	8-pin MSOP	Bulk	Lead Free	
SP708SCU-L/TR	0°C≤T_A≤+70°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	
SP708SEN-L	-40°C≤T_A≤+85°C	SP708SE YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP708SEN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP708TCN-L	0°C≤T_A≤+70°C	SP708TC YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP708TCN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP708TEN-L	-40°C≤T_A≤+85°C	SP706TE YYWWL X	8-pin NSOIC	Bulk	Lead Free	
SP708TEN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	

"YY" = Year – "WW" = Work Week – "X" = Lot Number

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{CC} = 2.7V to 5.5V (SP70xR), V_{CC} = 3.15V to 5.5V (SP70xS), V_{CC} = 3.0V to 5.5V (SP70xT), T_A= 25°C, unless otherwise indicated.

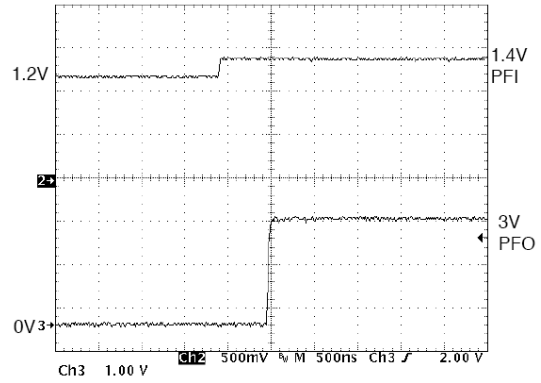


Fig. 4: Power-Fail Comparator De-Assertion Response Time

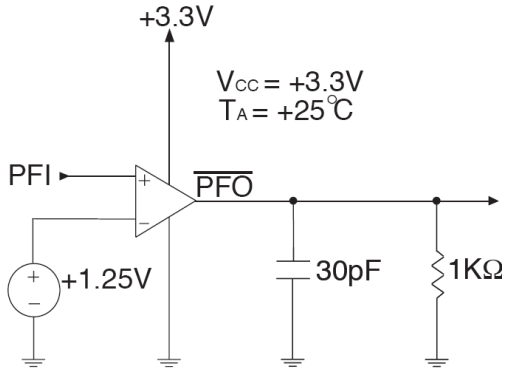


Fig. 5: Power-Fail Comparator De-Assertion Response Time Circuit

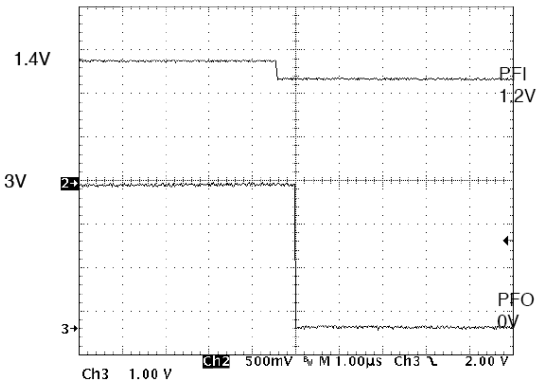


Fig. 6: Power-Fail Comparator Assertion Response Time

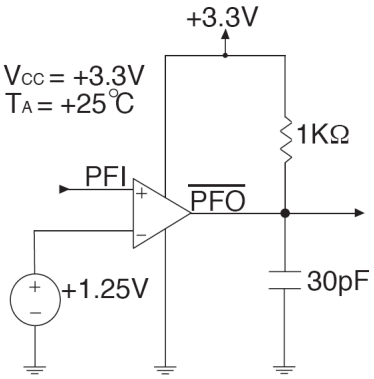


Fig. 7: Power-Fail Comparator Assertion Response Time Circuit

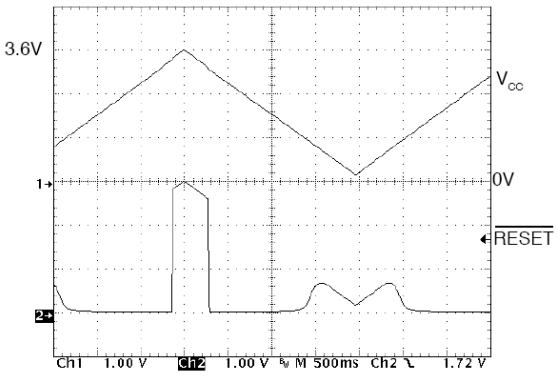


Fig. 8: SP706 $\overline{\text{RESET}}$ Output Voltage vs. Supply Voltage

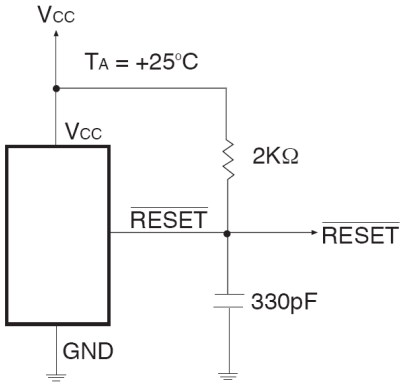


Fig. 9: SP706 $\overline{\text{RESET}}$ Output Voltage vs. Supply Voltage Circuit

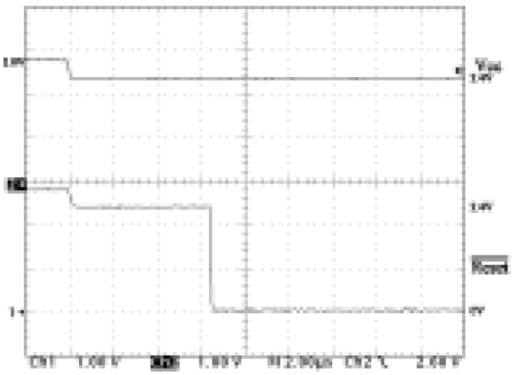


Fig. 10: SP706 $\overline{\text{RESET}}$ Response Time

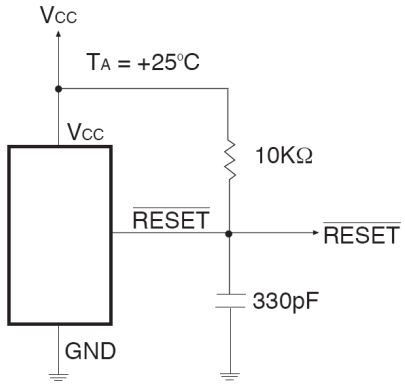


Fig. 11: SP706 $\overline{\text{RESET}}$ Response Time Circuit

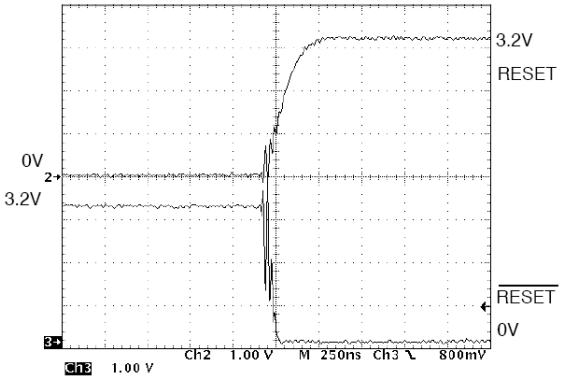


Fig. 12: SP708 RESET and $\overline{\text{RESET}}$ Assertion

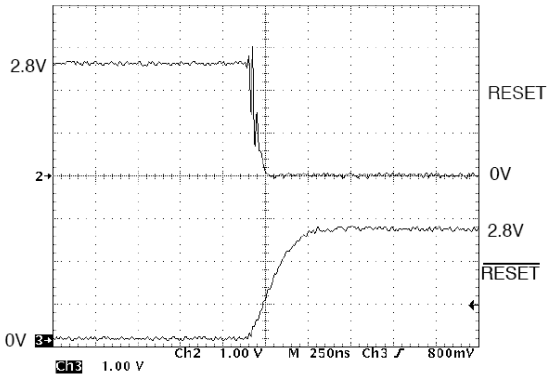


Fig. 13: SP708 RESET and $\overline{\text{RESET}}$ De-Assertion

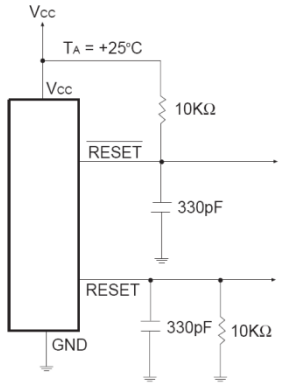


Fig. 14: SP708 RESET and $\overline{\text{RESET}}$ Assertion and De-Assertion Circuit

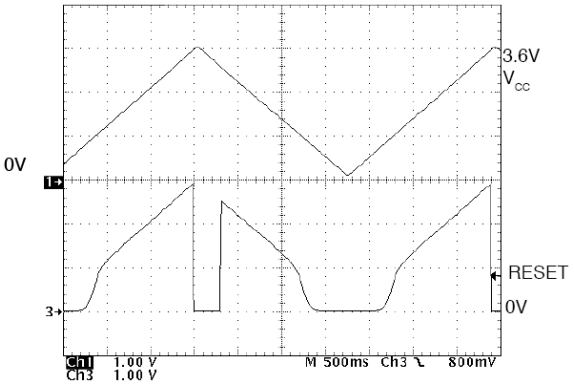


Fig. 15: SP708 RESET Output Voltage vs. Supply Voltage

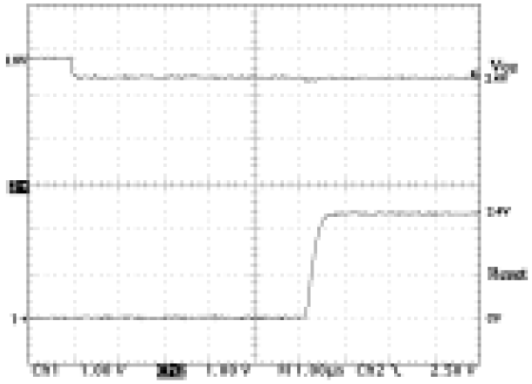


Fig. 16: SP708 RESET Response Time

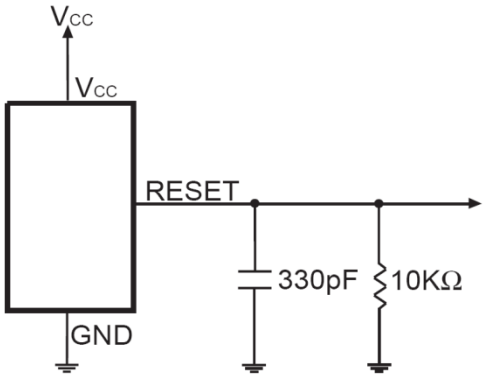


Fig. 17: SP708 RESET Output Voltage vs. Supply Voltage and SP813L RESET Response Time Circuit

FEATURES

The SP706R/S/T and SP708R/S/T series provides four key functions:

1. A reset output during power-up, power-down and brownout conditions.

2. An independent watchdog output that goes LOW if the watchdog input has not been toggled within 1.6 seconds.

3. A 1.25V threshold detector for power-fail warning, low battery detection, or monitoring a power supply other than +3.3V/+3.0V.

4. An active-LOW manual-reset that allows RESET to be triggered by a pushbutton switch.

The SP706R/S/T devices are the same as the SP708R/S/T devices except for the active-HIGH RESET substitution of the watchdog timer.

THEORY OF OPERATION

The SP706R/S/T-SP708R/S/T series is a microprocessor (µP) supervisory circuit that monitors the power supplied to digital circuits such as microprocessors, microcontrollers, or memory. The series is an ideal solution for portable, battery-powered equipment that requires power supply monitoring. Implementing this series will reduce the number of components and overall complexity. The watchdog functions of this product family will continuously oversee the operational status of a system. The operational features and benefits of the SP706R/S/T-SP708R/S/T series are described in more detail below.

RESET OUTPUT

A microprocessor's reset input starts the µP in a known state. The SP706R/S/T-SP708R/S/T series asserts reset during power-up and prevents code execution errors during power down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is a guaranteed logic LOW of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays LOW. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{RESET}$ after 200ms. $\overline{RESET}$ pulses LOW whenever V_{CC} dips below the reset threshold, such as in a brownout condition. When a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays LOW and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The active-HIGH RESET output is simply the complement of the $\overline{RESET}$ output and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-HIGH reset pulse.

WATCHDOG TIMER

The SP706R/S/T-SP708R/S/T watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6 seconds and WDI is not tri-stated, $\overline{WDO}$ goes LOW. As long as $\overline{RESET}$ is asserted or the WDI input is tri-stated, the watchdog timer will stay cleared and will not count. As soon as $\overline{RESET}$ is released and WDI is driven HIGH or LOW, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ will go LOW whether or not the watchdog timer had timed out. Normally this would trigger an NMI but $\overline{RESET}$ goes LOW simultaneously and thus overrides the NMI.

If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes LOW only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

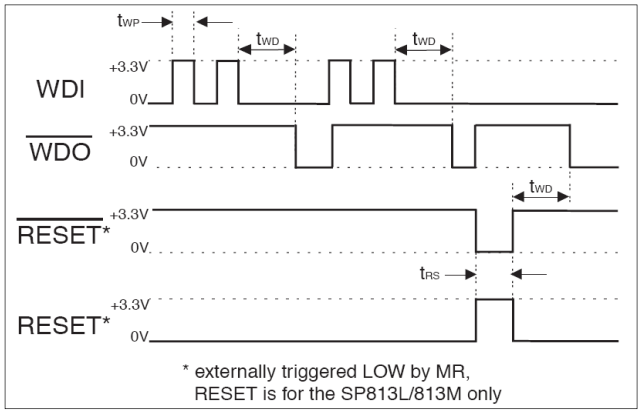


Fig. 18: Watchdog Timing Waveforms

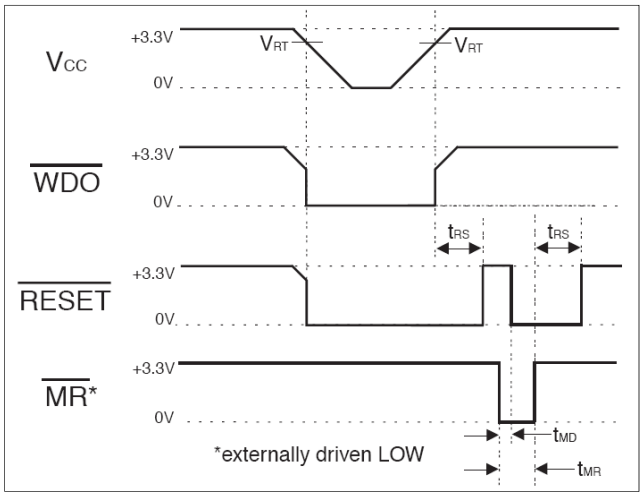


Fig. 19: Timing Diagrams with WDI tri-stated.

POWER-FAIL COMPARATOR

The power-fail comparator can be used for various purposes because its output and non inverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider as shown in Figure 20. Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use $\overline{PFO}$ to interrupt the µP so it can prepare for an orderly power-down.

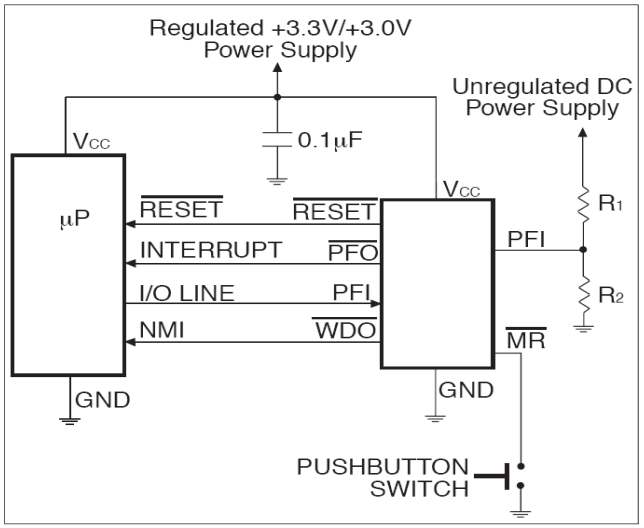


Fig. 20: Typical Operating Circuit

MANUAL RESET

The manual-reset input ($\overline{MR}$) allows RESET to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum RESET pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a RESET pulse in the SP706R/S/T-SP708R/S/T. Simply connect WDO to $\overline{MR}$.

Ensuring a Valid Reset Output Down to V_{CC}=0V

When V_{CC} falls below 1V, the $\overline{RESET}$ output no longer sinks current, it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the $\overline{RESET}$ pin, any stray charge or leakage currents will be shunted to ground, holding $\overline{RESET}$ LOW. The resistor value is not critical. It should be about 100KΩ, large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

MONITORING VOLTAGES OTHER THAN THE UNREGULATED DC INPUT

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{RESET}$ can be used to monitor voltages other than the +3.3V/+3.0V V_{CC} line. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a $\overline{RESET}$ pulse when PFI drops below 1.25V. Figure 21 shows the SP706R/S/T-SP708R/S/T series configured to assert $\overline{RESET}$ when the +3.3V/3.0V supply falls below the RESET threshold, or when the +12V supply falls below approximately 11V.

MONITORING A NEGATIVE VOLTAGE SUPPLY

The power-fail comparator can also monitor a negative supply rail, shown in Figure 22. When the negative rail is good (a negative voltage of large magnitude), $\overline{PFO}$ is LOW. By adding the

resistors and transistor as shown, a HIGH $\overline{PFO}$ triggers RESET. As long as $\overline{PFO}$ remains HIGH, the SP706R/S/T-SP708R/S/T series will keep RESET asserted (where $\overline{RESET}$ = LOW and RESET = HIGH). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

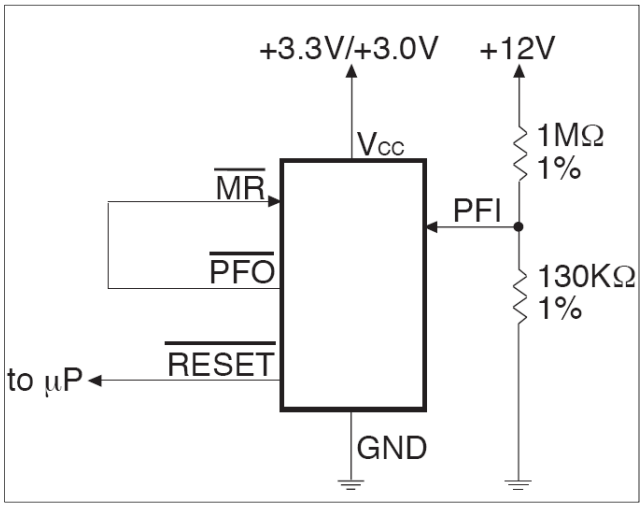


Fig. 21: Monitoring +3.3V/+3.0V and +12V Power Supplies

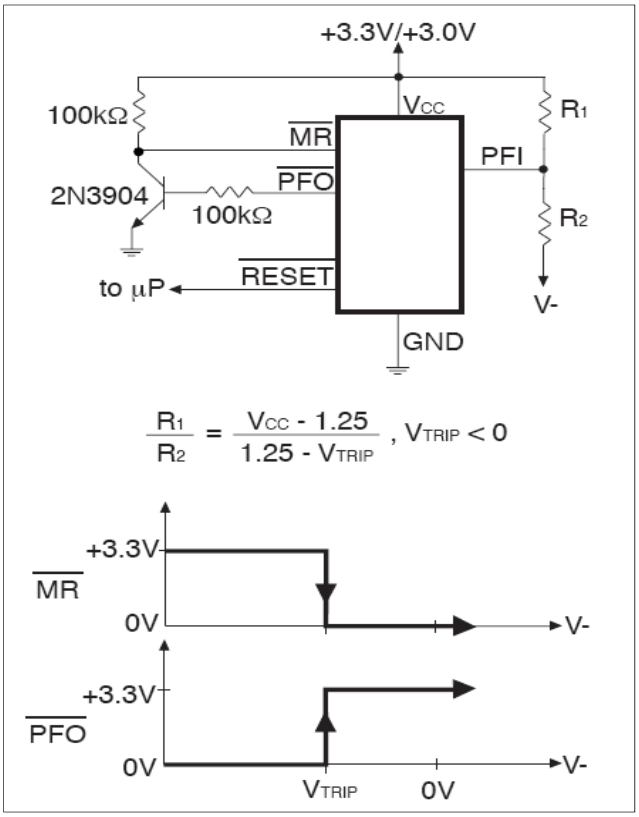


Fig. 22: Monitoring a Negative Voltage Supply

Interfacing to µPs with Bidirectional RESET Pins

µPs with bidirectional RESET pins, such as the Motorola 68HC11 series, can contend with the SP705/706/707/708 $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven HIGH and the µP wants to pull it LOW, indeterminate logic levels may result. To correct this, connect a 4.7KΩ resistor between the $\overline{RESET}$ output and the µP reset I/O, as shown if Figure 23. Buffer the $\overline{RESET}$ output to other system components.

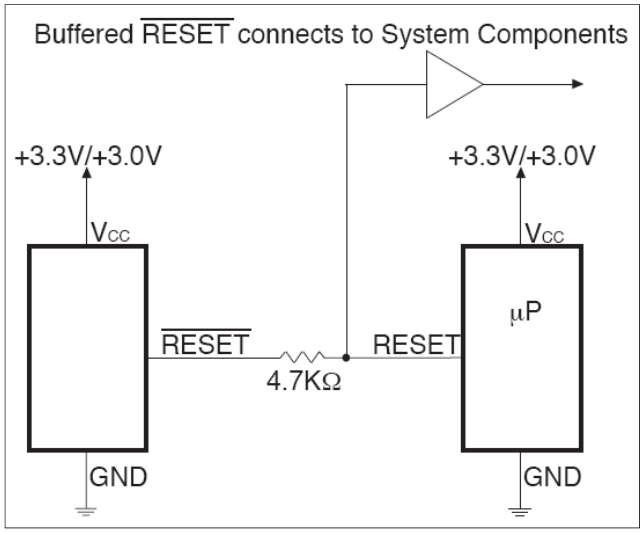


Fig. 23: Interfacing to Microprocessors with Bidirectional RESET I/O (SP706)

Negative-Going V_{CC} Transient

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short duration negative-going VCC transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

Figure 24 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are not generated. The data was generated using negative-going V_{CC} pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e. goes farther below

the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued. A 100nF bypass capacitor mounted close to the VCC pin provides additional transient immunity.

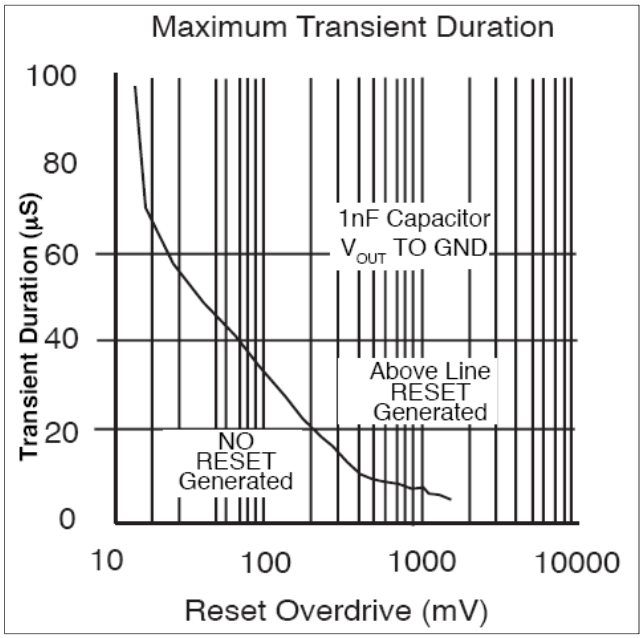


Fig. 24: Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

APPLICATIONS

The SP706P/R/S/T-SP708R/S/T series offers unmatched performance and the lowest power consumption for these industry standard devices. Refer to Figures 25 and 26 for supply current performance characteristics rated against temperature and supply voltages.

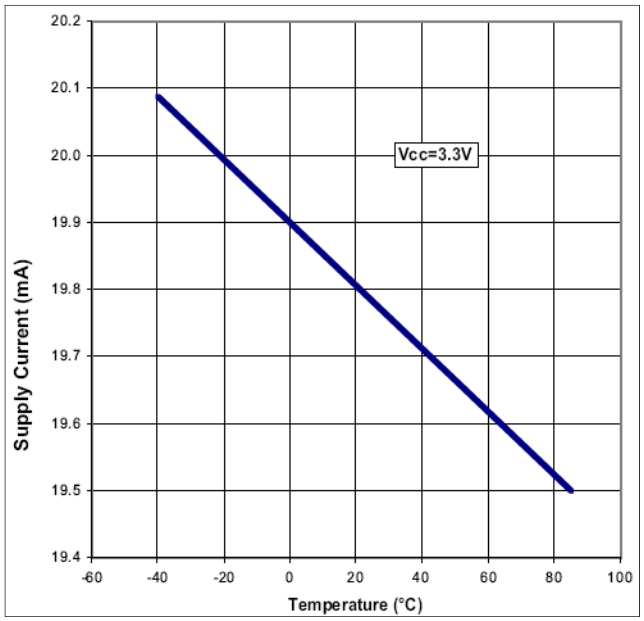


Fig. 25: Supply Current vs. Temperature

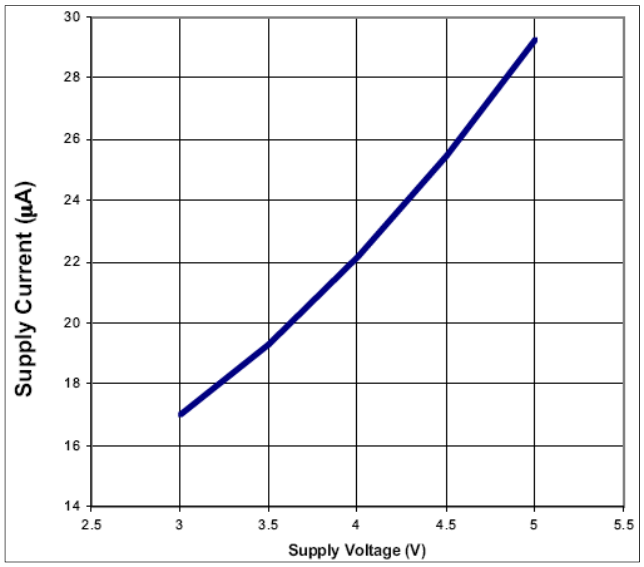
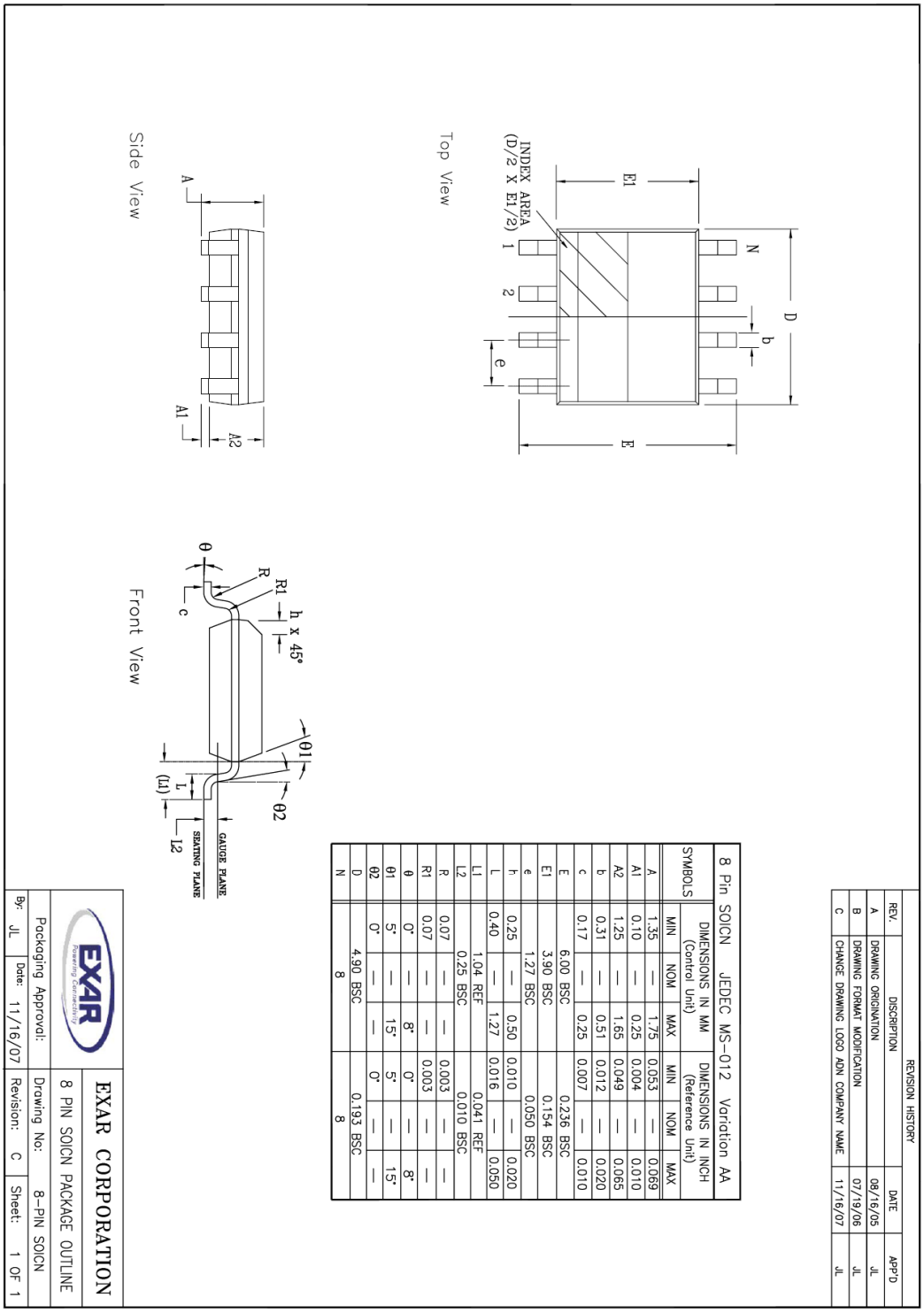


Fig. 26: Supply Current vs. Supply Voltage

PACKAGE SPECIFICATION

8-PIN NSOIC

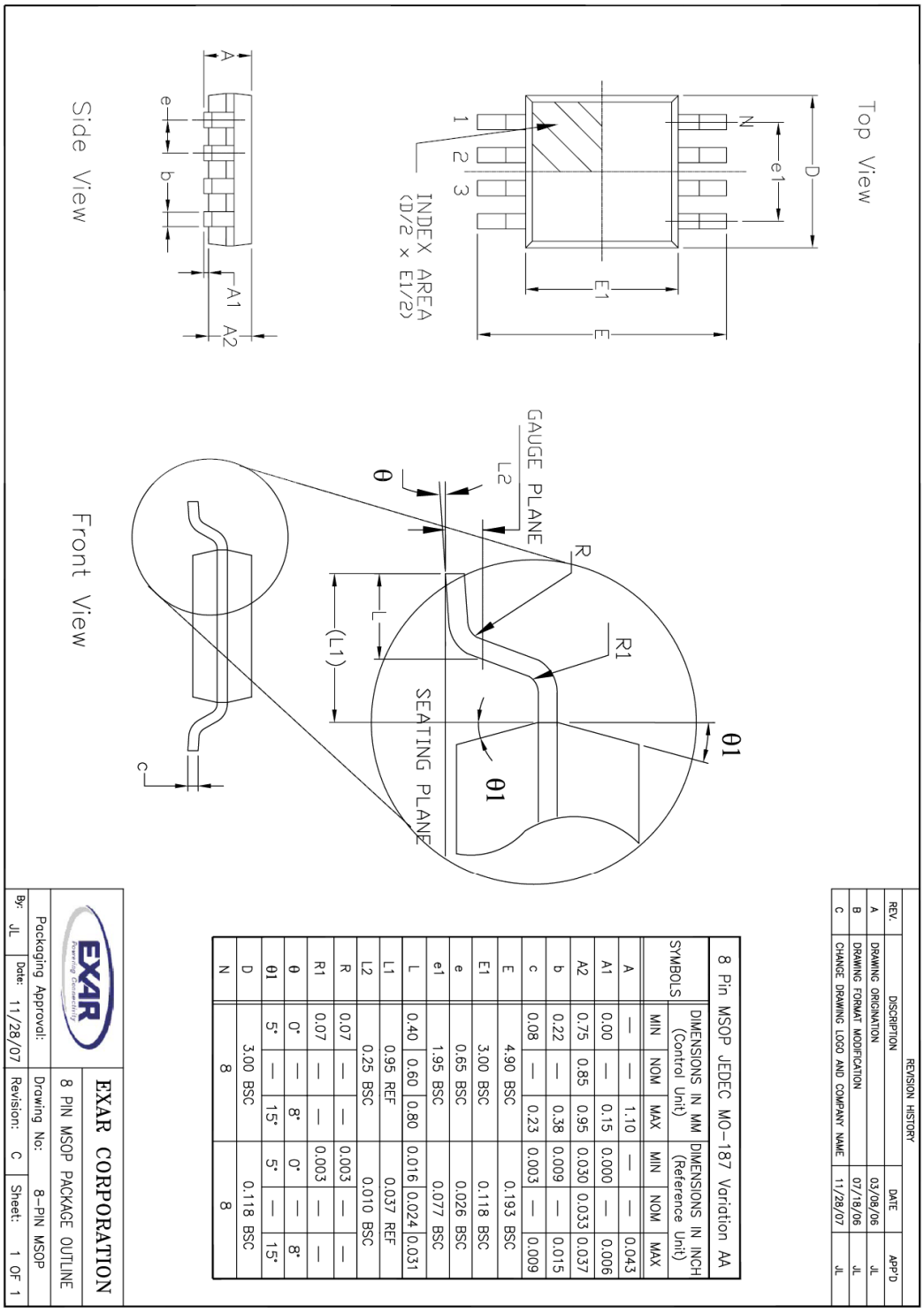


REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO ADN COMPANY NAME	11/16/07	JL

8 Pin SOICN JEDEC MS-012 Variation AA								
	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)				
SYMBOLS	MIN	NOM	MAX	MIN	NOM	MAX		
A	1.35	—	1.75	0.053	—	0.069		
A1	0.10	—	0.25	0.004	—	0.010		
A2	1.25	—	1.65	0.049	—	0.065		
b	0.31	—	0.51	0.012	—	0.020		
c	0.17	—	0.25	0.007	—	0.010		
E	6.00 BSC			0.236 BSC				
E1	3.90 BSC			0.154 BSC				
e	1.27 BSC			0.050 BSC				
h	0.25	—	0.50	0.010	—	0.020		
L	0.40	—	1.27	0.016	—	0.050		
L1	1.04 REF			0.041 REF				
L2	0.25 BSC			0.010 BSC				
R	0.07	—	—	0.003	—	—		
R1	0.07	—	—	0.003	—	—		
θ	0°	—	8°	0°	—	8°		
θ1	5°	—	15°	5°	—	15°		
θ2	0°	—	—	0°	—	—		
D	4.90 BSC			0.193 BSC				
N	8			8				

EXAR CORPORATION			
8 PIN SOICN PACKAGE OUTLINE			
Packaging Approval:	Drawing No: 8-PIN SOICN	Revision: C	Sheet: 1 OF 1
By: JL	Date: 11/16/07		

8-PIN MSOP


Top View
Side View
Front View
INDEX AREA
(D/2 x E1/2)
GAUGE PLANE
SEATING PLANE
REVISION HISTORY
REV. DESCRIPTION DATE APP'D
A DRAWING ORIGINATION 03/08/06 JL
B DRAWING FORMAT MODIFICATION 07/18/06 JL
C CHANGE DRAWING LOGO AND COMPANY NAME 11/28/07 JL
8 Pin MSOP JEDEC MO-187 Variation AA
SYMBOLS
DIMENSIONS IN MM (Control Unit)
DIMENSIONS IN INCH (Reference Unit)
MIN NOM MAX MIN NOM MAX
A — — 1.10 — — 0.043
A1 0.00 — 0.15 0.000 — 0.006
A2 0.75 0.85 0.95 0.030 0.033 0.037
b 0.22 — 0.38 0.009 — 0.015
c 0.08 — 0.23 0.003 — 0.009
E 4.90 BSC 0.193 BSC
E1 3.00 BSC 0.118 BSC
e 0.65 BSC 0.026 BSC
e1 1.95 BSC 0.077 BSC
L 0.40 0.60 0.80 0.016 0.024 0.031
L1 0.95 REF 0.037 REF
L2 0.25 BSC 0.010 BSC
R 0.07 — — 0.003 — —
R1 0.07 — — 0.003 — —
θ 0° — 8° 0° — 8°
θ1 5° — 15° 5° — 15°
D 3.00 BSC 0.118 BSC
N 8 8
EXAR CORPORATION
8 PIN MSOP PACKAGE OUTLINE
Packaging Approval: Drawing No: 8-PIN MSOP
By: JL Date: 11/28/07 Revision: C Sheet: 1 OF 1

REVISION HISTORY

Revision	Date	Description
2.0.0	06/04/2010	Reformat of datasheet

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