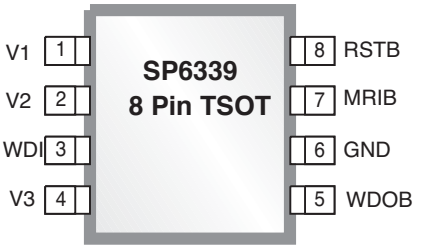
SP6339, SP6341

Triple μPower Supervisory Circuit with Manual Reset and Watchdog

FEATURES

- Low operating voltage of 1.6V
- Low operating current of 20μA typical
- Monitors up to 3 supplies simultaneously
- Adjustable input monitors down to 0.5V
- Reset asserted down to 0.9V
- 2% accuracy over temperature range
- Open Drain (OD) or CMOS RSTB output
- 4 Reset Timeout Periods: 50mS, 100mS, 200mS, and 400mS
- Watch Dog Timer Function -- WDI
- Independent OD or CMOS Watchdog Output (Active Low) -- WDOB
- Manual Reset Input (Active Low) -- MRIB
- 8 Pin TSOT package



Open Drain $\overline{\text{RESET}}$

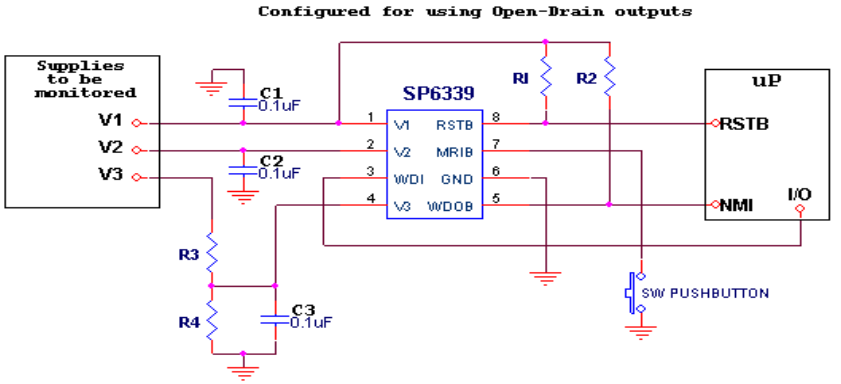
SEE PAGE 2 FOR OTHER AVAILABLE PINOUTS

Now Available in Lead Free Packaging

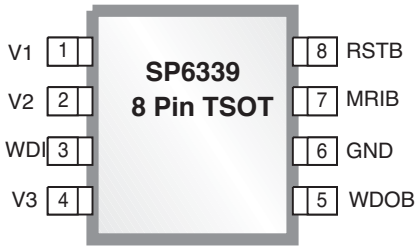
DESCRIPTION

SP6339-SP6341 Triple μPower Supervisory Circuit Family is a family of microprocessor reset supervisory circuits with multiple reset voltages. The family provides low voltage monitoring ability for up to three supplies with two precision factory-set thresholds and one user defined custom threshold. These circuits perform a single function: if any of the input supply voltages drops below its associated threshold, reset outputs are asserted. Products in the family offer manual reset and watchdog functionalities. SP6339 and SP6341 are packaged in an 8-pin TSOT package. All devices are fully specified over -40°C to +85°C temperature range.

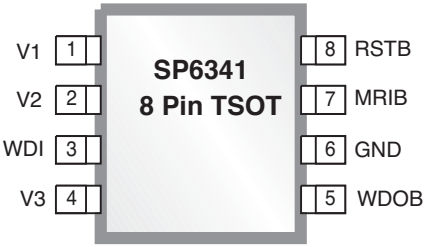
TYPICAL APPLICATION CIRCUIT



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Open Drain $\overline{\text{RESET}}$



CMOS $\overline{\text{RESET}}$

PART NUMBER	V1	V2	V3	Reset	MRIB	WDI	WDOB
SP6339	√	√	√	OD Active Low	√	√	OD Active Low
SP6341	√	√	√	CMOS Active Low	√	√	CMOS Active Low

Feature and Pinout Diagram

Representative Samples Available

Sipex Product	Product Description	Package	V1 (Volts)	V2 (Volts)	V3 (Volts)	V4 (Volts)	Reset (ms)	Ordering #
SP6339	Triple Supervisor Open Drain low	8 Pin TSOT	4.625	2.313	0.5	N/A	200	SP6339EK1-L-Z-J-C

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

Terminal Voltage (with respect to GND)
V1, V2..... -0.3 to +6V

Open-Drain RSTB,
WDOB.....-0.3 to +6V

CMOS RST, RSTB,
WDOB..... -0.3 to (V1+0.3V)

Input Current/Output
Current.....,,.....20mA

V3, MRIB, WDI.....-0.3 to (V1+0.3V)

Operating Temperature
Range.....-40°C to +85°C

Storage Temperature
Range.....-65°C to 150°C

Thermal Resistance Θ_{JA}.....134°C/W

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PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 = 1.6V to 5.5V; TA = -40ºC to +85ºC; unless otherwise noted. Typical values are at TA =+25ºC					
Operating Voltage Range	0.9		5.5	V	T_A = -40ºC to +85ºC
Supply Current		20	30	uA	V1 < 5.5V, V2 < 3.60V, all I/O pins open
		15	25		V1 < 3.6V, V2 < 2.75V, all I/O pins open
V1 Reset Threshold	4.532	4.625	4.718	V	Z (valid for V1 falling)
	4.287	4.375	4.463		Y (valid for V1 falling)
	3.013	3.075	3.137		X (valid for V1 falling)
	2.866	2.925	2.984		W (valid for V1 falling)
	2.572	2.625	2.678		V (valid for V1 falling)
	2.273	2.320	2.367		U (valid for V1 falling)
	2.146	2.190	2.234		T (valid for V1 falling)
	1.636	1.670	1.704		S (valid for V1 falling)
	1.548	1.580	1.612		R (valid for V1 falling)
V2 Reset Threshold	2.266	2.313	2.360	V	J (valid for V2 falling)
	2.144	2.188	2.232		I (valid for V2 falling)
	1.631	1.665	1.698		H (valid for V2 falling)
	1.543	1.575	1.607		G (valid for V2 falling)
	1.360	1.388	1.416		F (valid for V2 falling)
	1.286	1.313	1.340		E (valid for V2 falling)
	1.087	1.110	1.133		D (valid for V2 falling)
	1.029	1.050	1.071		C (valid for V2 falling)
	0.816	0.833	0.850		B (valid for V2 falling)
	0.772	0.788	0.804		A (valid for V2 falling)
Threshold 1 Tempco		0.06		mV/ºC	
Threshold 2 Tempco		0.04		mV/ºC	
Threshold 1 Hysteresis		0.65		%	reference to Vth1 typical
Threshold 2 Hysteresis		0.5		%	reference to Vth2 typical
V1 to RST/RSTB Delay		50		us	V1 = Vth1 to (Vth1-0.1V), Vth1 = 3.075
V2 to RST/RSTB Delay		50		us	V2 = Vth2 to (Vth2-0.1V), Vth2 = 1.575
Reset Timeout Period (T1)	37	50	63	ms	TOPT-1
Reset Timeout Period (T2)	74	100	126	ms	TOPT-2
Reset Timeout Period (T3)	148	200	252	ms	TOPT-3
Reset Timeout Period (T4)	296	400	504	ms	TOPT-4

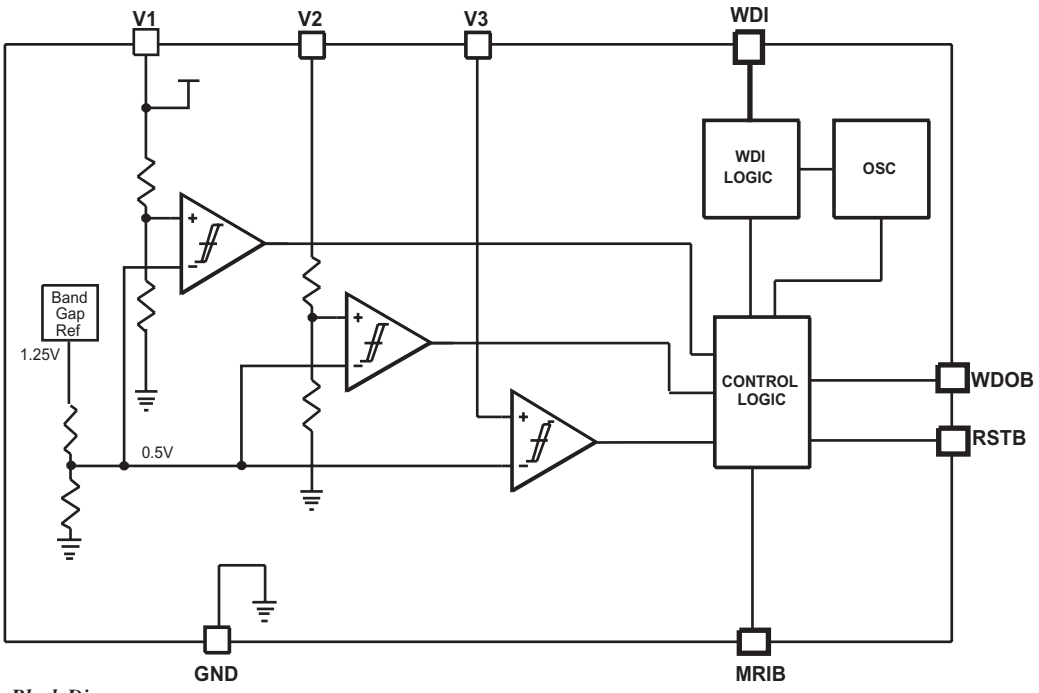
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PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 = 1.6V to 5.5V; T_A = -40ºC to +85ºC; unless otherwise noted. Typical values are at T_A =+25ºC					
V3 RESET COMPARATOR INPUT					
V3 Input Threshold	490	500	510	mV	
V3 Input Current	-50		50	nA	T_A = +25ºC
V3 Threshold Hysteresis		1.5		mV	
MRIB - MANUAL RESET INPUT					
MRIB Input Threshold			0.4	V	Vil
MRIB Input Threshold	0.8*V1			V	Vih
MRIB Minimum Input Pulse Width	1			us	
MRIB Glitch Rejection		150		ns	
MRIB to RST/RSTB Delay		100		ns	
MRIB Pull-Up Resistance	30	55	85	kΩ	
WDI - WATCHDOG INPUT					
Watchdog Timeout Period	1.2	1.6	2	sec	
WDI Pulse Width	0.1			us	
WDI Input Threshold			0.4	V	Vil
WDI Input Threshold	0.8*V1			V	Vih
WDI Input Current	-500		500	nA	WDI = 0.0V or V1
RESET / WATCHDOG OUTPUTS		**RSTB / WDOB**			
RSTB (CMOS or OD)			0.4	V	V1 = Vth1 - 0.1V, Isink = 1mA, output asserted
RSTB (CMOS)	0.8*V1			V	V1 = Vth1 + 0.1V, Isource = 1mA, output not asserted
WDOB (CMOS or OD)			0.4	V	WDI = 0.0V or V1, V1 > Vth1, V2 > Vth2, V3 > 0.5, MRIB float, Isink = 1mA, WDOB output asserted
WDOB (CMOS)	0.8*V1			V	V1 > Vth1, V2 > Vth2, V3 > 0.5, MRIB float, WDOB not asserted, Isource = 1mA
RSTB / WDOB Output OD Leakage Current		2		nA	T_A = +25ºC

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Pin #	Name	Description
1	V1	First supply voltage input. Also powers internal circuitry. Trip threshold voltage internally set.
2	V2	Second supply voltage input. Trip threshold voltage internally set.
3	WDI	Watch-Dog Input pin. When no transition is detected at the WDI pin for the duration of WDI timeout period, reset is asserted. RSTB output is used to signal watchdog timeout overflow -- RSTB output pulses high/low (depending on the active reset polarity) for the reset timeout period after each watchdog timeout overflow. WDOB remains at “LOW” logic level after watchdog timeout period is expired and it remains “LOW” until WDI makes a transition. RSTB output is not affected by the watchdog functionality. The watchdog timer clears whenever the reset is asserted or manual reset is asserted or a transition is observed at WDI pin.
4	V3	Input for the third supply voltage. Trip threshold is 0.5V.
5	WDOB	Watch Dog Output. Open-Drain or CMOS, active LOW. If WDI remains at “HIGH” or “LOW” logic level for longer than the watchdog timeout period, the internal watchdog timer overflows and WDOB is asserted. WDOB does not de-assert until the watchdog is cleared via transition at the WDI pin. Another scenario for WDOB to assert is when the reset output is asserted due to an under-voltage V1, V2, V3 condition. WDO de-asserts without a reset timeout period. Floating WDI will not disable watchdog timer in devices with dedicated WDOB output. Open-drain WDOB outputs require an external pull-up resistor. CMOS outputs are referenced to V1.
6	GND	Common ground reference pin.
7	MRIB	Manual Reset Input pin. Active low. It has an internal pull-up resistor. Reset asserted when MRIB is pulled low and is kept asserted for 200ms after MRIB is released or pulled high. Leave open if not used.
8	RSTB	Reset output. Open-Drain or CMOS, active low. Reset is asserted when any of the three supply inputs is below its trip threshold. It stays asserted for 200 ms (typical / default) after the last supply input traverses its trip threshold. Reset is guaranteed to be in the correct state for V1>0.9V. RSTB asserts when V1 or V2 or V3 drop below their corresponding reset thresholds, or MRIB is pulled “LOW”. RSTB remains asserted for the reset timeout period after V1 and V2 and V3 exceed their corresponding reset thresholds or MRIB goes “LOW” to “HIGH”. Open-drain outputs require an external pull-up resistor. CMOS outputs are referenced to V1.

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Block Diagram

The SP6339 and SP6341 include a low-voltage precision bandgap reference, three precision comparators, an oscillator, a digital counter chain, a logic control block, trimmed resistor divider chains and additional supporting circuitry. The family is designed to supervise up to 3 independent supply voltages. V1 and V2 supply inputs have their resistor dividers on the chip. Their trip thresholds are factory trimmed. The V3 input allows users to customize an additional supply threshold to be monitored by means of an external resistor divider. The parts are furnished with manual reset and watchdog output functionalities. The watchdog functionality cannot be disabled.

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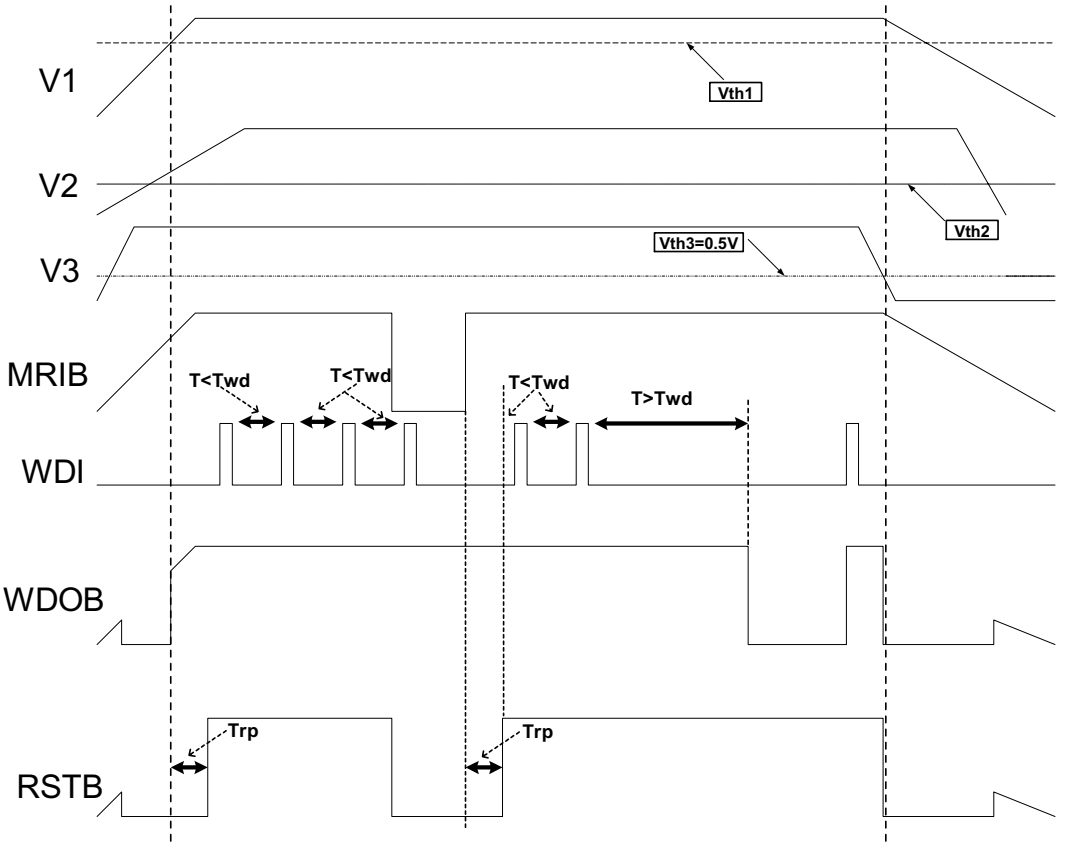
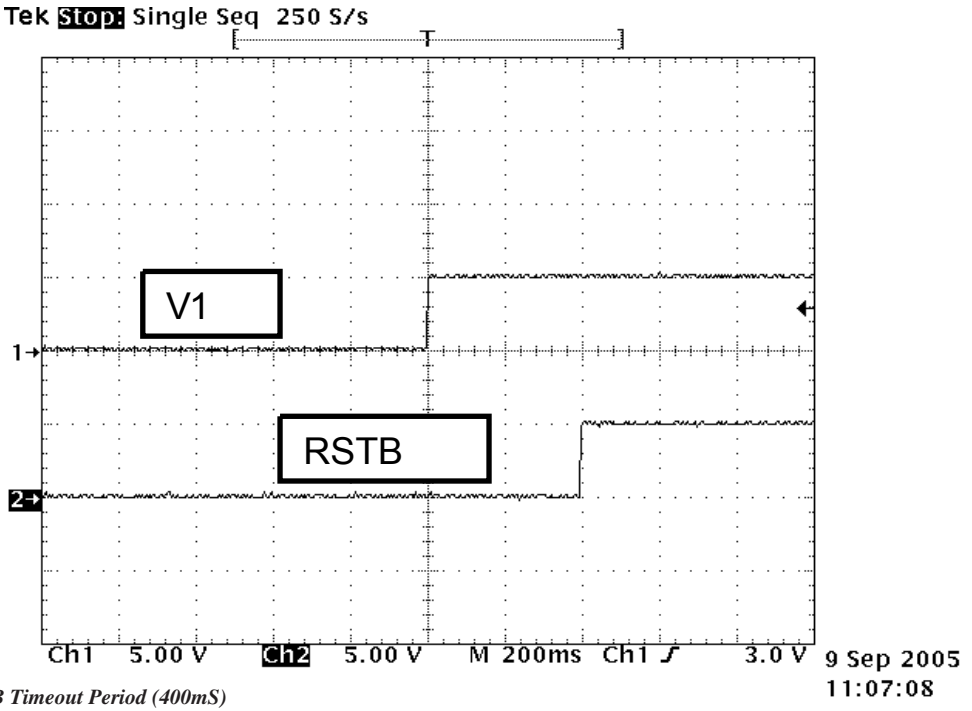


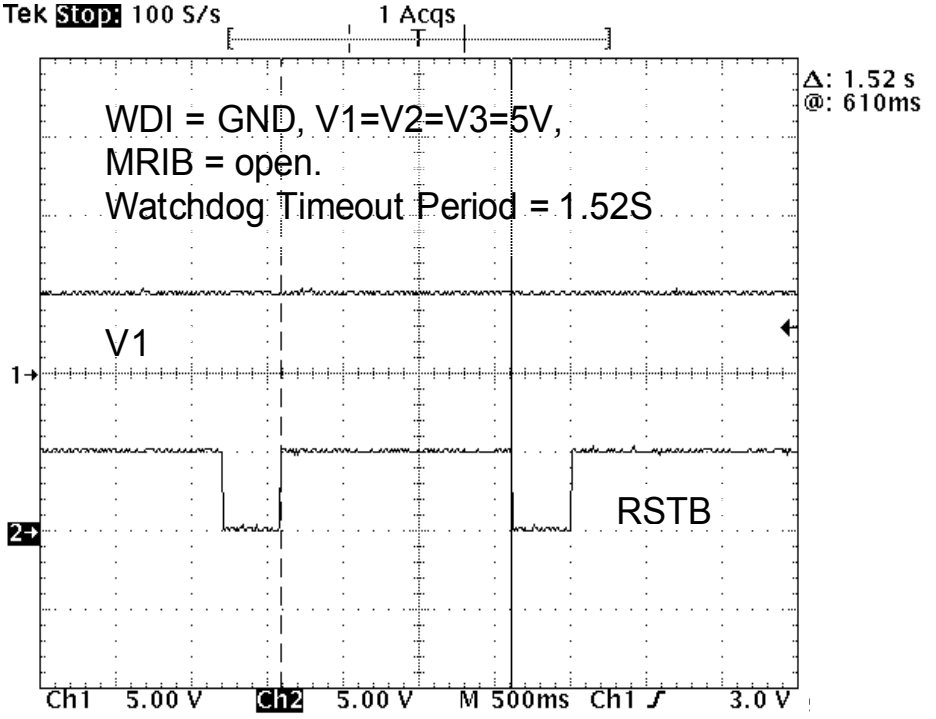
Figure 1: functionality of the SP6339 and SP6341.

- V1 > Vth1, V2 > Vth2 , and V3 > Vth3 (all supplies over their corresponding thresholds)----> RSTB is de-asserted after reset timeout period (Trp) & WDOB de-asserts immediately without waiting for reset timeout period.
- MRIB goes to “LOW” to force “Reset” ----> RSTB is asserted immediately & WDOB is not affected by MRIB and is not asserted.
- WDI keeps making transitions within watchdog timeout period (t<Twd) ----> neither RSTB nor WDOB changes state.
- One of the supplies drops below its corresponding threshold (in this case V3) ----> RSTB is asserted immediately & WDOB is asserted immediately too. Whenever V1, V2, V3 are below their specified thresholds WDOB is asserted.

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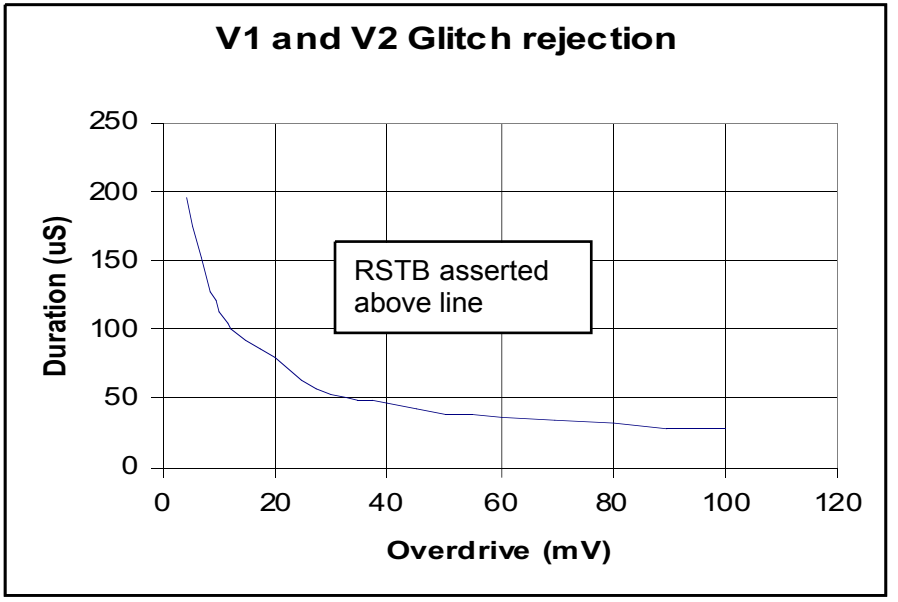


RESETB Timeout Period (400mS)

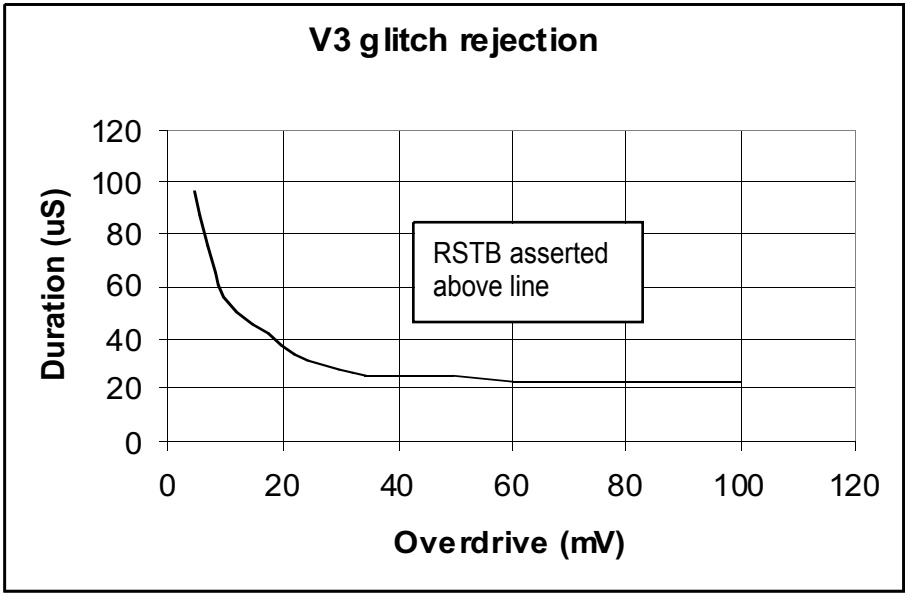


SP6339Watchdog Timeout Period

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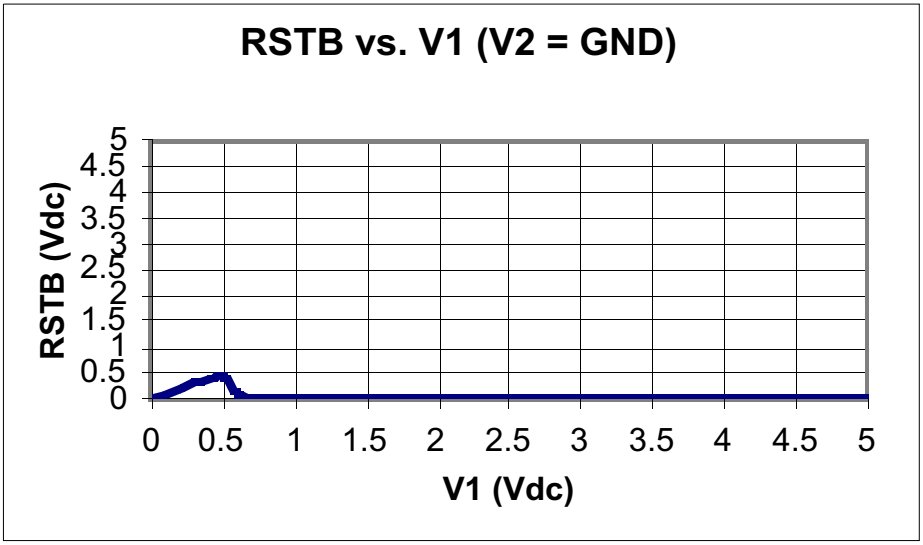


V1 and V2 Glitch Rejection

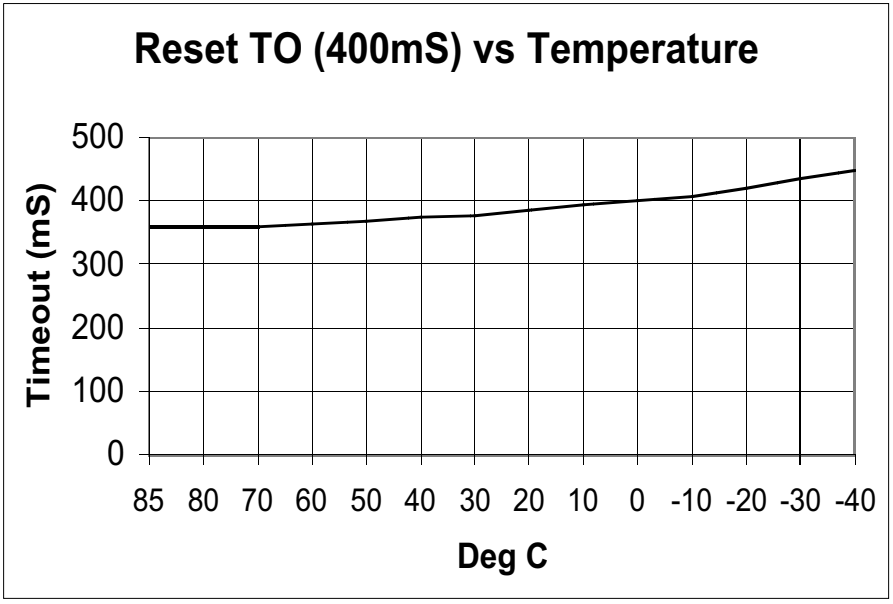


V3Glitch Rejection

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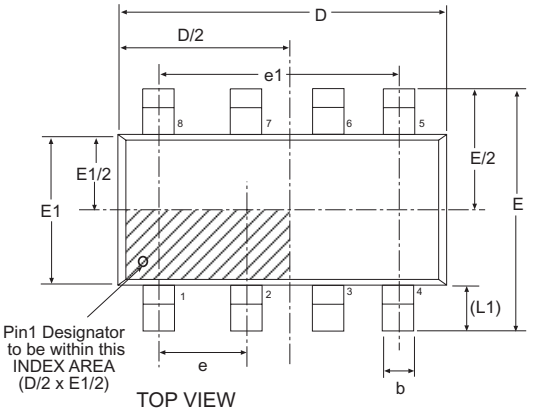


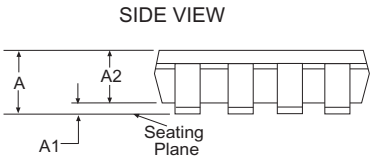
Reset Good

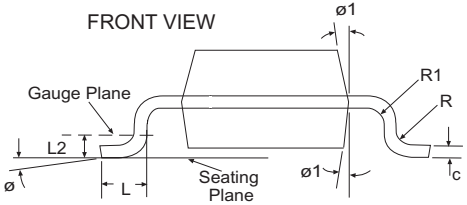


Reset Timeout vs. Temperature

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8 Pin TSOT JEDEC MO-193 Variation BA						
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.10	-	-	0.043
A1	0.00	-	0.10	0.000	-	0.004
A2	0.70	0.90	1.00	0.028	0.036	0.039
c	0.08	-	0.20	0.003	-	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
Ø	0˚	4º	8º	0º	4º	8º
Ø1	4˚	10º	12º	4º	10º	12º
R	0.10	-	-	0.004	-	-
R1	0.10	-	0.25	0.004	-	0.010
b	0.22	-	0.38	0.009	-	0.015
e	0.65 BSC			0.026 BSC		
e1	1.95 BSC			0.077 BSC		
SIPEX Pkg Signoff Date/Rev:				JL Oct3-05 / Rev A		

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Part Naming Nomenclature

SP63N - Th1 - Th2 - TOPT

TOPT

- A -- 50 ms
- B -- 100 ms
- C -- 200 ms
- D -- 400 ms

Th2

- A -- 0.788 V
- B -- 0.833 V
- C -- 1.050 V
- D -- 1.110 V
- E -- 1.313 V
- F -- 1.388 V
- G -- 1.575 V
- H -- 1.665 V
- I -- 2.188 V
- J -- 2.313 V

Example:
JZJD means:
SP6339 in TSOT-8 lead package
V1 Threshold is 4.625V
V2 Threshold is 2.313V
Reset Timeout is 400ms



Th1

- Z -- 4.625 V
- Y -- 4.375 V
- X -- 3.075 V
- W -- 2.925 V
- V -- 2.625 V
- U -- 2.320 V
- T -- 2.190 V
- S -- 1.670 V
- R -- 1.580 V

SP63N

- A 30 -- Quad Sp, MR, WDI, OD RSTB
- B 31 -- Quad Sp, OD RSTB
- C 32 -- Quad Sp, MR, WDI, CMOS RSTB
- D 33 -- Quad Sp, CMOS RSTB
- E 34 -- Quad Sp, MR, WDI, CMOS RST
- F 35 -- Quad Sp, CMOS RST
- G 36 -- Triple Sp, WDI, PF, OD RSTB
- H 37 -- Triple Sp, WDI, PF, CMOS RSTB
- I 38 -- Triple Sp, WDI, PF, CMOS RST
- J 39 -- Triple Sp, MR, WDI, OD RSTB - WDOB
- K 40 -- Dual Sp, WDI, OD RSTB - WDOB
- L 41 -- Triple Sp, WDI, PF, CMOS RSTB - WDOB
- M 42 -- Dual Sp, WDI, CMOS RSTB - WDOB

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Model	Temperature Range	Package Type
SP6339EK1-L-X-X-X	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6339EK1-L-X-X-X/TR	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6341EK1-L-X-X-X	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6341EK1-L-X-X-X/TR	-40°C to +85°C	Lead Free 8-Pin TSOT

Available in lead free packaging only.

/TR = Tape and Reel

Pack quantity 2,500 for TSOT.

Contact Factory for availability of particular voltage threshold and reset timeout options. Note that the Ordering Information denoting those options corresponds to the Part Naming Nomenclature shown on the previous page.

Ordering example: SP6339EK1-L-W-G-C/TR == W -- 2.925V for Voltage Threshold 1; G -- 1.575V for Voltage Threshold 2; and C -- 200ms reset timeout.

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