

# **SP623 IBERT Getting Started Guide (ISE 12.3)**

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## Revision History

The following table shows the revision history for this document.

| Date     | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 06/22/10 | 1.0     | Initial Xilinx release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 12/20/10 | 2.0     | Revised content to support ISE software, v12.1. Removed explicit instructions describing setup and operation on Duals 245 and 267. Added text and <a href="#">Appendix A</a> to generalize instructions to apply to either Duals 101 and 123 or Duals 245 and 267. Revised Superclock-2 information in <a href="#">Connecting the GTP Transceivers and Reference Clocks, page 7</a> . Revised <a href="#">Figure 1-1, page 6</a> . Included Si570 initialization instructions in <a href="#">Starting the Clock Module, page 14</a> . Added <a href="#">Figure 1-12, page 15</a> . Added <a href="#">Regenerating IBERT Designs, page 20 through page 33</a> . |
| 01/19/11 | 3.0     | Revised document to reflect ChipScope™ Pro software v12.3.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 01/26/11 | 3.0.1   | Revised cover title. Was: “SP623 IBERT Getting Started Guide.” Is: “SP623 IBERT Getting Started Guide (ISE 12.3).”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

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# SP623 IBERT Getting Started Guide

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## Overview

This document provides a procedure for setting up the SP623 Spartan®-6 FPGA GTP Transceiver Characterization Board to run the Integrated Bit Error Ratio Test (IBERT) demonstration. The designs that are required to run the IBERT demonstration are stored in the CompactFlash memory card that is provided with the SP623 board. The demonstration shows the capabilities of the Spartan-6 XC6SLX150T FPGA GTP transceivers.

The IBERT demonstration is divided into two designs included on the CompactFlash memory card. The first design tests the transceivers located on the top half of the FPGA (GTP Duals 101 and 123), the second design tests the transceivers on the bottom half of the FPGA (GTP Duals 245 and 267). This procedure describes the steps to test the top design. The bottom design is tested following the same series of steps with the changes described in [Appendix A](#). The procedure consists of:

1. [Extracting the IBERT Demonstration Files.](#)
2. [Setting Up the SP623 Board.](#)
3. [Connecting the GTP Transceivers and Reference Clocks.](#)
4. [Configuring the FPGA.](#)
5. [Setting Up the ChipScope Pro Analyzer Tool.](#)
6. [Viewing the GTP Transceiver Operation.](#)

The SP623 board is described in detail in [UG751](#), *SP623 Spartan-6 FPGA GTP Transceiver Characterization Board User Guide*.

## Requirements

The equipment and software required to run the demonstration are:

- SP623 Spartan-6 FPGA GTP Transceiver Characterization Board including:
  - 12V DC power adapter
  - CompactFlash memory card containing the IBERT demonstration designs
  - GTP transceiver power supply module (installed on SP623 board)
  - SuperClock-2 module (installed on SP623 board)
  - 12 SMA to SMA cables
- One of these JTAG cables:
  - Platform Cable USB-II (DLC10)
  - Parallel IV Cable (PC4)
- Host PC or Linux system, with USB ports

- Xilinx® ChipScope™ Pro software, version 12.3 or higher.  
Software is available at: <http://www.xilinx.com/chipscopepro>

The additional equipment and software required to regenerate the designs are:

- Linux system with Xilinx ISE® Design Suite v12.3 already installed
- SP623 IBERT design source files (provided online as collection rdf0100\_12-3.zip) at:  
[http://www.xilinx.com/products/boards/sp623/reference\\_designs.htm](http://www.xilinx.com/products/boards/sp623/reference_designs.htm)

## Running the IBERT Demonstration

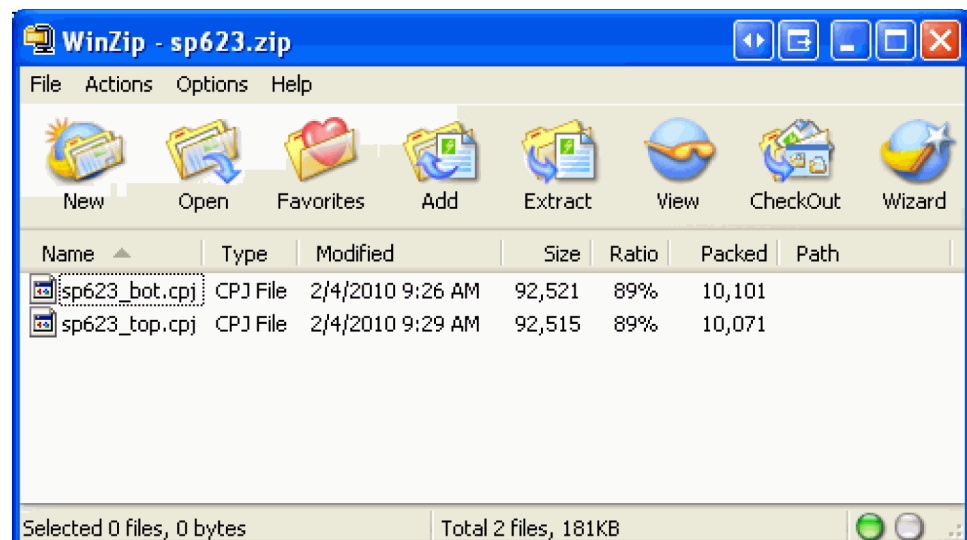
### Extracting the IBERT Demonstration Files

The ChipScope Pro Software .cpj project files for the IBERT demonstration are located on the CompactFlash memory card that is provided with the SP623 board. They are also located online along with .bit files for both designs (as collection rdf0098\_12-3.zip) at:

[http://www.xilinx.com/products/boards/sp623/reference\\_designs.htm](http://www.xilinx.com/products/boards/sp623/reference_designs.htm)

The .cpj files are used to load pre-saved MGT/IBERT and clock module control settings for the demonstration. These files must be copied to a working directory on the host computer. To copy the files from the CompactFlash memory card:

1. Connect the CompactFlash memory card to the host computer.  
**Note:** The CompactFlash memory card can be plugged into a host PC's PCMCIA interface using a PCMCIA adapter card.
2. Locate the file sp623.zip on the Compact Flash memory card. The ZIP file content is similar to the files shown in Figure 1-1.



UG752\_c1\_01\_121510

Figure 1-1: ChipScope Software Project Files Included in the sp623.zip File

3. Unzip the files to a working directory on the host computer.

## Setting Up the SP623 Board

**Caution!** The SP623 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

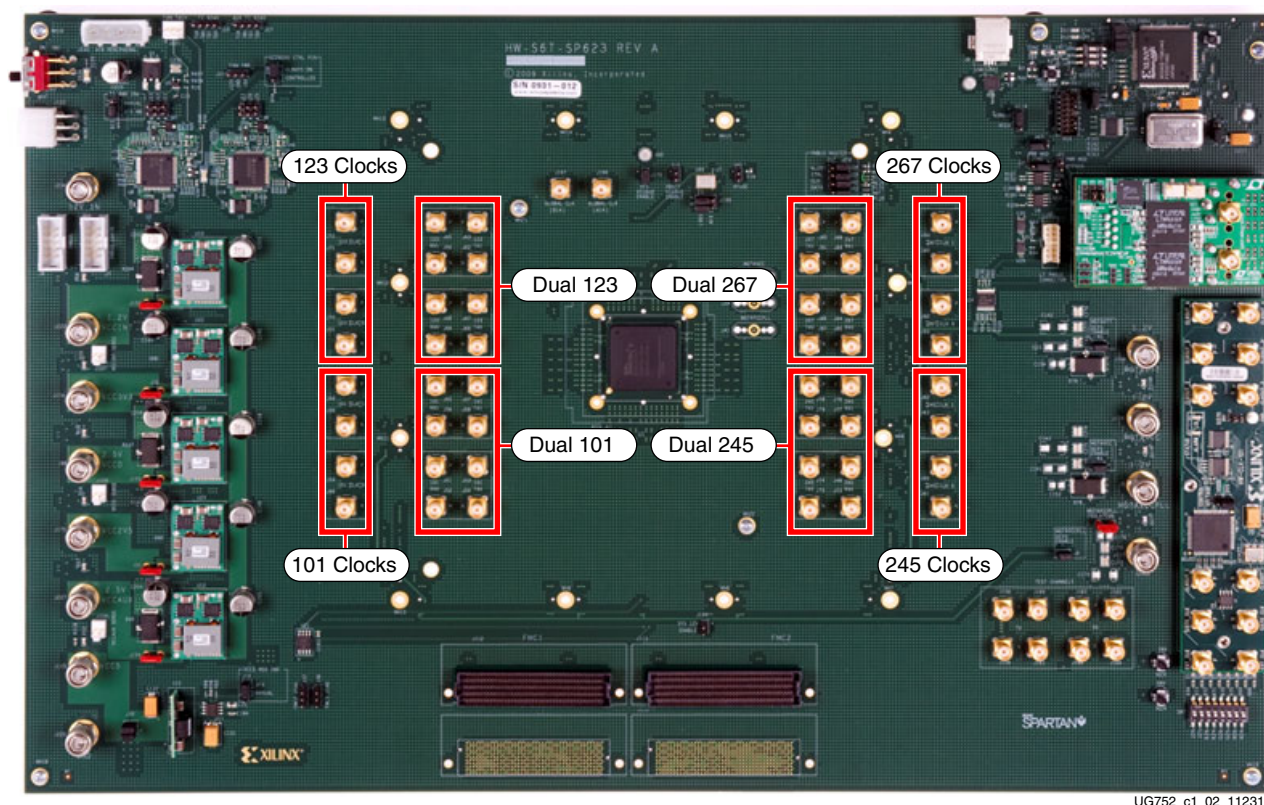
To set up the SP623 board:

1. Install the GTP transceiver power module:
  - a. Plug the module into connectors J34 and J179.
  - b. Remove DCPS ENABLE jumpers at J184 and J185 located on the SP623 board.
2. Verify the four SYSACE JTAG ENABLE jumpers are installed at locations J22, J23, J195, and J196 on the SP623 board.
3. Place a jumper across pins 1–2 of the JTAG FMC BYPASS header at J162.
4. Enable the 200 MHz LVDS system clock by placing two jumpers (P, N) across pins 1–3 and pins 2–4 of J188.
5. Verify there is a 30 MHz oscillator in the SYSTEM ACE CLK oscillator socket at location X1 on the SP623 board.
6. Enable the System ACE™ controller clock by placing the jumper on J4 to the ON position.
7. Insert the CompactFlash memory card into the CF card connector (U24) located on the underside of the SP623 board.
8. Install the SuperClock-2 module:
  - a. Align the three metal standoffs on the bottom side of the module with the three mounting holes in the CLOCK MODULE interface of the SP623 board.
  - b. Using three 4-40 x 0.25 inch screws, firmly screw down the module from the bottom of the SP623 board.
  - c. On the SuperClock-2 module, place a jumper across pins 1–2 (VCCO) of the CONTROL VOLTAGE header, J18.

## Connecting the GTP Transceivers and Reference Clocks

All GTP transceiver pins are connected to differential SMA connector pairs. The GTP transceivers are grouped into four sets of two (referred to as Duals) which share two differential reference clock pin-pairs. [Figure 1-2](#) shows the SMA locations for the GTP transceiver Duals (Dual 101, Dual 123, Dual 245, and Dual 267) and their associated reference clocks (101 Clocks, 123 Clocks, 245 Clocks, and 267 Clocks).



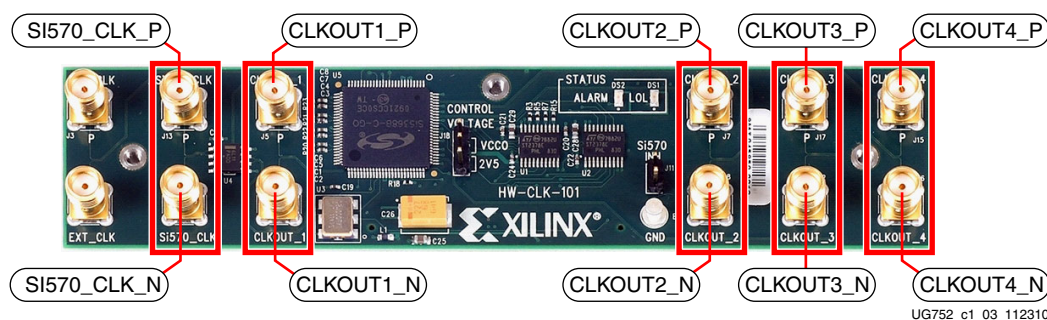


UG752\_c1\_02\_112310

Figure 1-2: GTP Transceiver and Reference Clock SMA Locations

**Note:** The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

The SuperClock-2 module provides LVDS clock outputs for the GTP transceiver reference clocks in the IBERT demonstration. Figure 1-3 shows the location of the differential clock SMA connectors on the clock module which can be connected to the GTP transceiver reference clock SMAs on the SP623 board. The four SMA pairs labeled “CLKOUT” provide LVDS clock outputs from the Si5378 clock multiplier/jitter attenuator device on the clock module. The SMA pair labeled “Si570\_CLK” provides LVDS clock output from the Si570 programmable oscillator on the clock module. For the IBERT demonstration, the output clock frequencies from both devices are preset to 156.25 MHz. For more information regarding the SuperClock-2 module, refer to [UG770](#), *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide*.



UG752\_c1\_03\_112310

Figure 1-3: SuperClock-2 Module Output Clock SMA Locations



**Note:** The image in [Figure 1-3](#) is for reference only and might not reflect the current revision of the board.

## Running the IBERT Demonstration

This section describes running the IBERT demonstration on Duals 101 and 123.

For running the IBERT demonstration on Duals 245 and 267 refer to [Repeating the IBERT Demonstration for the Remaining GTP Duals](#), page 18.

### GTP Transceiver Clock Connections

Refer to [Table 1-1](#) and use four SMA cables to connect the output clock SMAs from the SuperClock-2 module to the reference clock SMAs of GTP Duals 101 and 123 on the SP623 board. In other words, for each row in [Table 1-1](#), connect the source SMA with its corresponding destination SMA. For example, connect CKOUT1\_P (J5) to 101\_REFCLK0\_P (J59).

**Note:** Any one of the five differential output SMA clocks from the clock module can be used to source either REFCLK0\_P|N or REFCLK1\_P|N on the SP623 board. Output clocks from the Si5368 device, specifically CKOUT1\_P|N and CKOUT2\_P|N, are described here and throughout this document as an example.

**Table 1-1: Reference Clock Connections for Duals 101 and 123**

| Source              |               | Destination   |               |
|---------------------|---------------|---------------|---------------|
| SuperClock-2 Module |               | SP623 Board   |               |
| Net Name            | SMA Connector | Net Name      | SMA Connector |
| CKOUT1_P            | J5            | 101_REFCLK0_P | J59           |
| CKOUT1_N            | J6            | 101_REFCLK0_N | J60           |
| CKOUT2_P            | J7            | 123_REFCLK0_P | J70           |
| CKOUT2_N            | J8            | 123_REFCLK0_N | J61           |

**Notes:**

1. See [Table A-1](#), page 35 for a listing of reference clock SMA connections for Duals 245 and 267.

### GTP TX/RX Connections

Refer to [Table 1-2](#) and use eight SMA cables to connect the transmitter SMAs to the receiver SMAs in GTP Duals 101 and 123. In other words, for each row in [Table 1-2](#), connect the transmitter SMA with its corresponding receiver SMA. For example, connect 101\_TX0\_P (J53) to 101\_RX0\_P (J51) on the SP623 board.

**Table 1-2: TX/RX Connections for Duals 101 and 123**

| Transmitter |               | Receiver  |               |
|-------------|---------------|-----------|---------------|
| Net Name    | SMA Connector | Net Name  | SMA Connector |
| 101_TX0_P   | J53           | 101_RX0_P | J51           |
| 101_TX0_N   | J54           | 101_RX0_N | J52           |
| 101_TX1_P   | J57           | 101_RX1_P | J55           |
| 101_TX1_N   | J58           | 101_RX1_N | J56           |

Table 1-2: TX/RX Connections for Duals 101 and 123 (Cont'd)

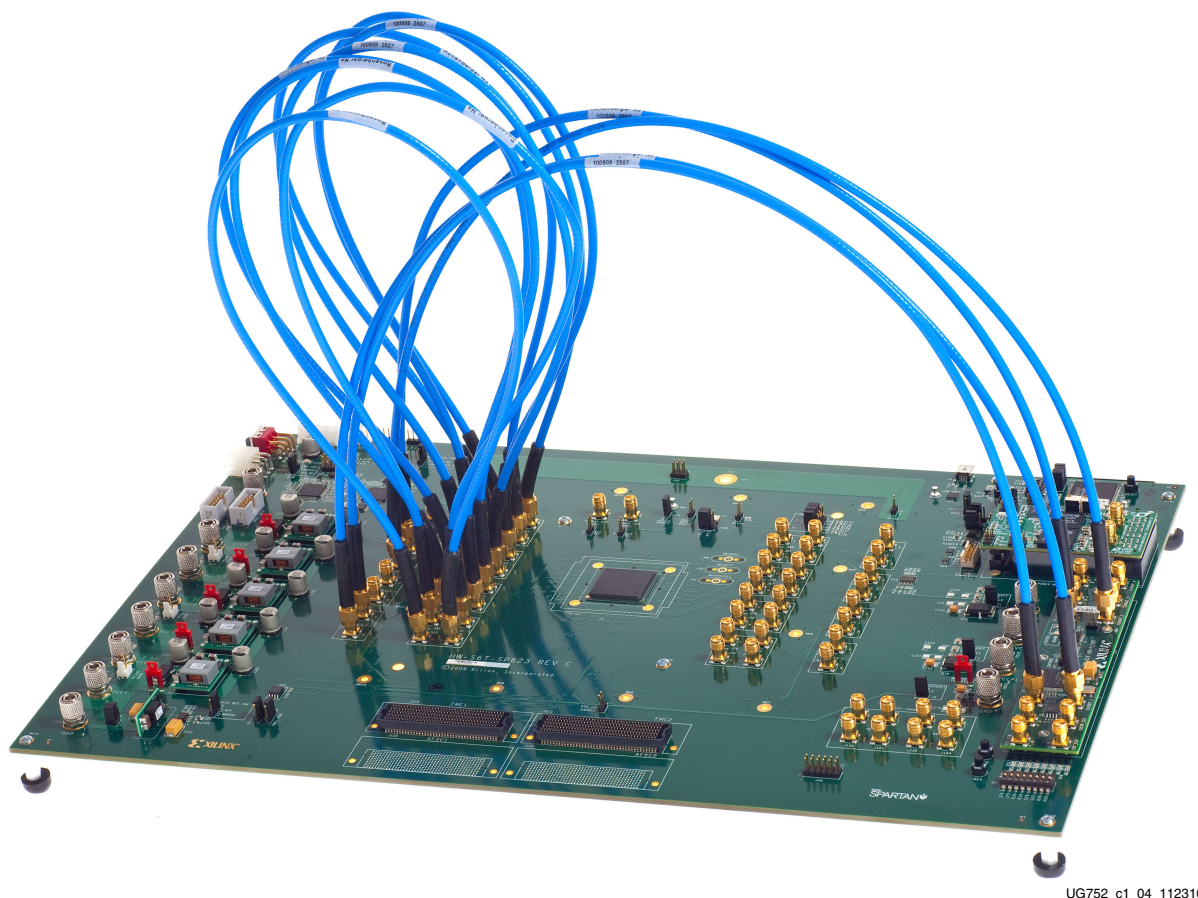
| Transmitter |               | Receiver  |               |
|-------------|---------------|-----------|---------------|
| Net Name    | SMA Connector | Net Name  | SMA Connector |
| 123_TX0_P   | J67           | 123_RX0_P | J68           |
| 123_TX0_N   | J66           | 123_RX0_N | J69           |
| 123_TX1_P   | J63           | 123_RX1_P | J65           |
| 123_TX1_N   | J62           | 123_RX1_N | J64           |

**Notes:**

1. See [Table A-2, page 35](#) for a listing of TX/RX connections for Duals 245 and 267.

The final SMA cable connections for Duals 101 and 123 are shown in [Figure 1-4](#).

**Note:** The final SMA cable connections for Duals 245 and 267 are shown in [Figure A-1, page 36](#).



UG752\_c1\_04\_112310

Figure 1-4: SMA Cable Connections for Dual 101 and 123 Transceivers and Clocks

## Configuring the FPGA

The following set of instructions describe how to configure the FPGA using the CompactFlash memory card included with the board. The FPGA may also be configured through ChipScope analyzer or iMPACT using the .bit files located online (as collection rdf0098\_12-3.zip) at:

[http://www.xilinx.com/products/boards/sp623/reference\\_designs.htm](http://www.xilinx.com/products/boards/sp623/reference_designs.htm)

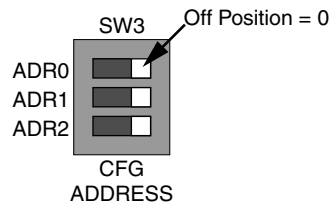
To configure from the CompactFlash memory card:

1. Plug the 12V output from the power supply into connector J122.
2. Connect the SP623 board to the host computer. Either of these cables may be used for this connection:
  - Platform Cable USB-II (DLC10)
  - Parallel IV Cable (PC4)

Connect one end of the cable to the host computer. Connect the other end to the download cable connector (J1) on the SP623 board.

- To run the IBERT demonstration on Duals 101 and 123, set the System Ace Controller Configuration Address switch SW3 to 000 as shown in Figure 1-5. The setting on SW3 determines which of the two bitstreams stored in the CompactFlash card configures the FPGA.

Configuration Address for Dual 101 and Dual 123 (000)



UG752\_c1\_05\_112310

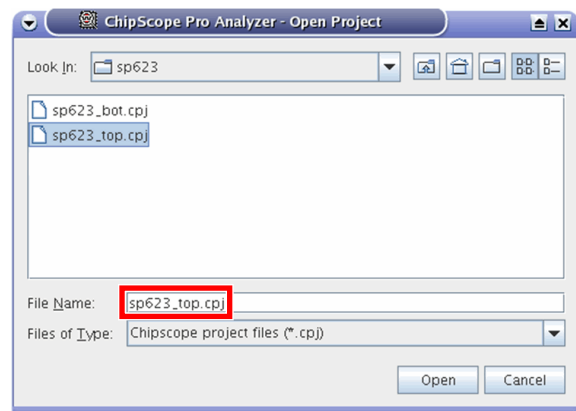
Figure 1-5: DIP Switch SW3 Settings For Duals 101 and 123

**Note:** Set SW3 to 001 as shown in Figure A-2, page 37 if running the IBERT demonstration on Duals 245 and 267.

- Apply power to the board by placing SW1 in the ON position. After a few seconds, the FPGA is configured and the Done LED (DS6) lights.

## Setting Up the ChipScope Pro Analyzer Tool

- Open the ChipScope Pro Analyzer tool and select **File → Open Project**.
- When the Open Project window appears, navigate to the location on the host computer where the .cpj project files were extracted, select sp623\_top.cpj (Duals 101 and 123) and click **Open** (Figure 1-6).



UG752\_c1\_07\_060110

Figure 1-6: Open Project Window

**Note:** The .cpj file loads pre-saved project settings for the demonstration including MGT/IBERT and clock module control parameters. For more information regarding MGT/IBERT settings, refer to UG029, *ChipScope Pro Software and Cores User Guide*.

- Click the **Open Cable** button (Figure 1-7).

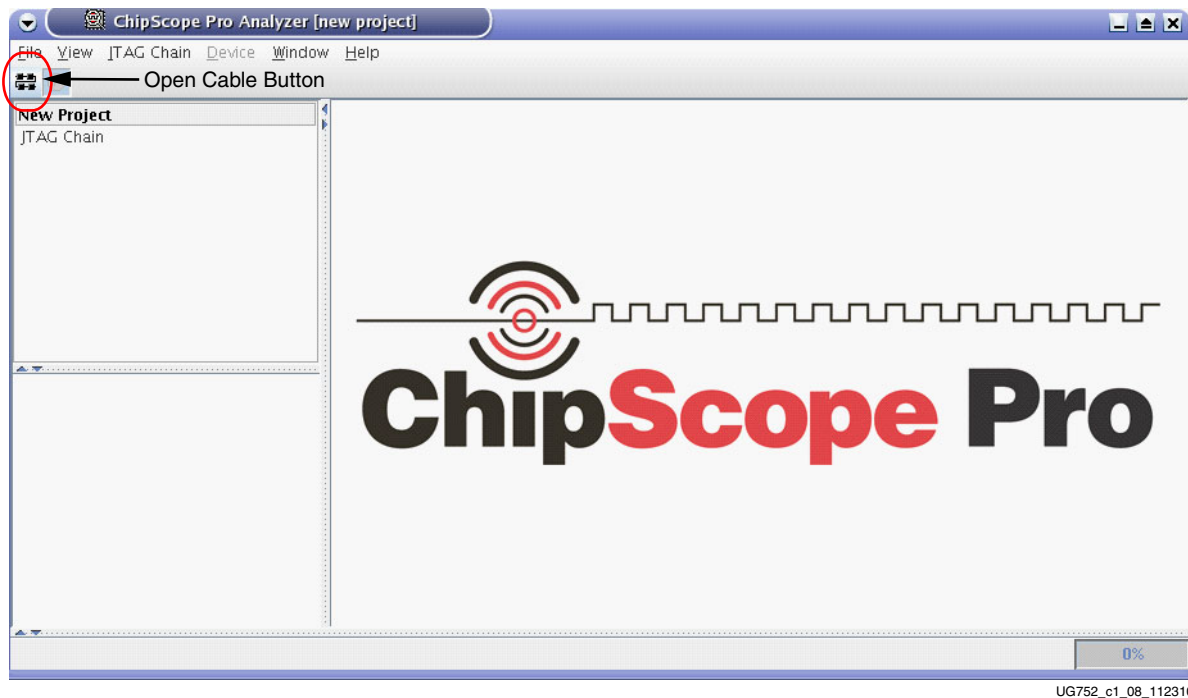


Figure 1-7: Open Cable Button

- When the dialog box opens asking to set up the core with settings from the current project, click **Yes** (Figure 1-8).

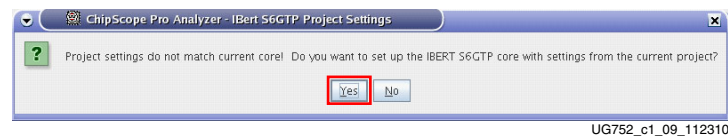


Figure 1-8: Core Settings Dialog Box

- When the project panel opens, verify the JTAG chain shows the devices listed in Figure 1-9.

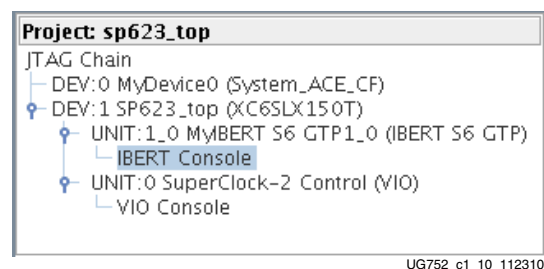


Figure 1-9: Project Panel

## Starting the Clock Module

The IBERT demonstration design uses a ChipScope VIO core to control the clocks on the SuperClock-2 module. The SuperClock-2 module features two clock-source components: An always-on Si570 crystal oscillator and an Si5368 jitter-attenuating clock multiplier. The IBERT demonstration uses the output from either device to clock the GTP transceivers.

1. In the project panel, double-click **VIO Console** (Figure 1-10).

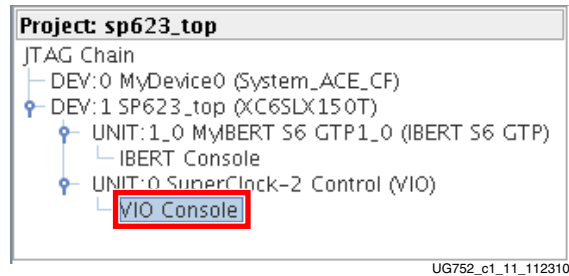


Figure 1-10: VIO Console Selection

2. Having selected the VIO Console, the clock source(s) for the GTP transceivers can be initialized. Do one or both of the following:
  - a. If using the Si5368 device to source the GTP transceiver clocks (e.g. as described in Table 1-1, page 9), initialize the Si5368 device. Click the **Si5368 Start** button (Figure 1-11). A transition arrow flashes ON/OFF to the right of **Si5368 Done** when the command is complete.

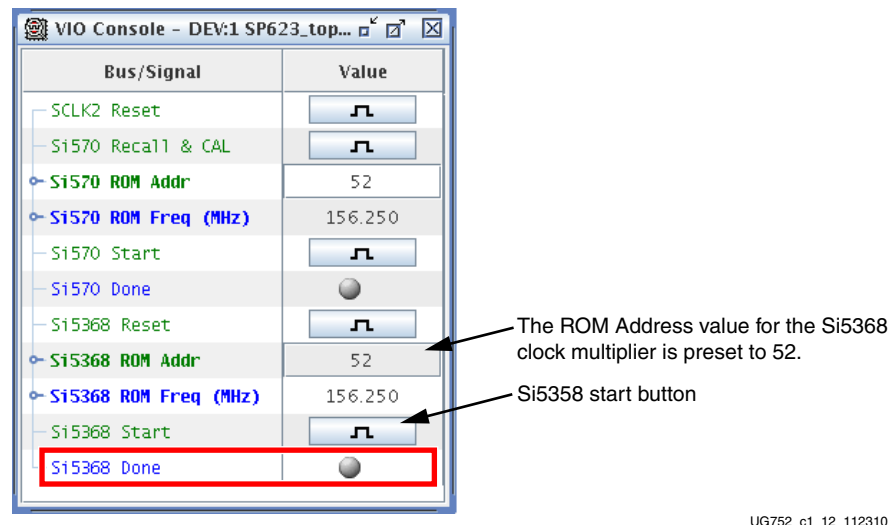


Figure 1-11: VIO Console, Si5368 Initialization

- b. If using the Si570 crystal to source the GTP transceiver clocks, click the Si570 Start button (Figure 1-12). A transition arrow flashes ON/OFF to the right of **Si570 Done** when the command is complete.

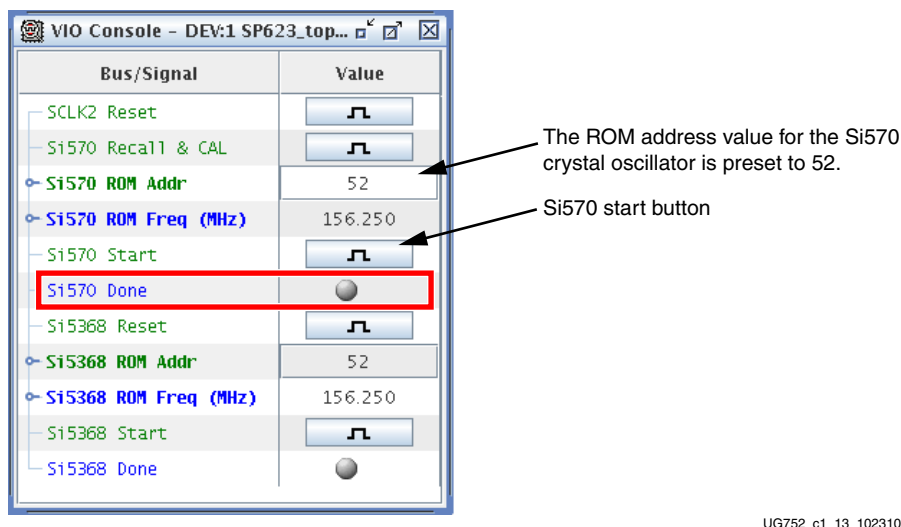


Figure 1-12: VIO Console, Si570 Initialization

**Note:** The ROM address value for the Si5368 is preset to 52 to produce an output frequency of 156.25 MHz. Typing in a different address changes the frequency of the GTP transceiver reference clocks. A complete list of frequency options and their associated ROM addresses is provided in [Table 2, page 19](#).

3. In the project panel, double-click **IBERT Console** ([Figure 1-13](#)).

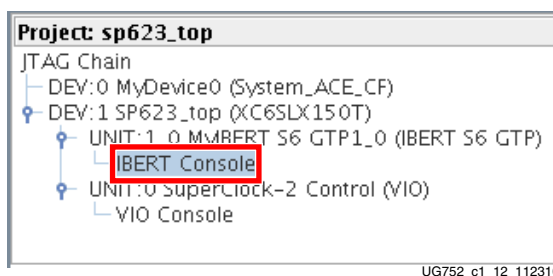


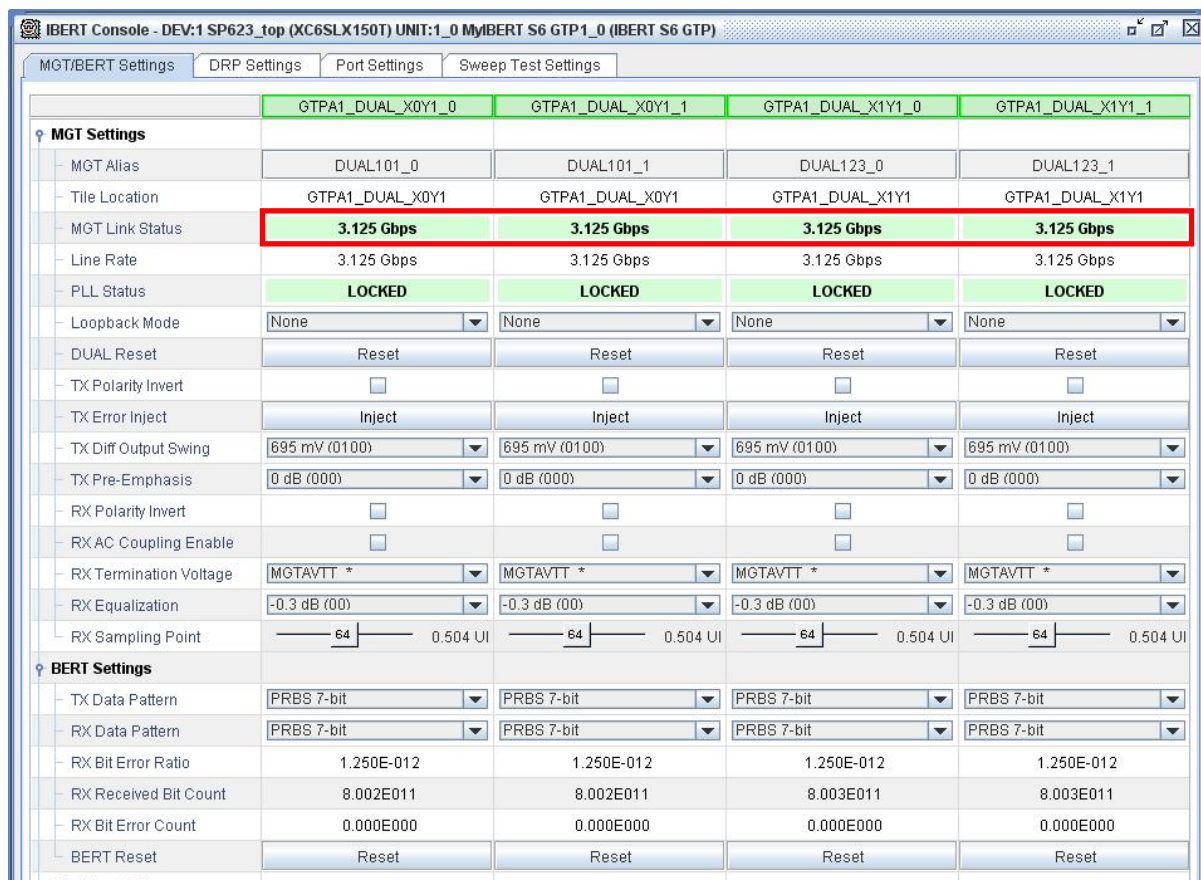
Figure 1-13: IBERT Console Selection

## Viewing the GTP Transceiver Operation

After completing [step 3](#) in [Starting the Clock Module](#), the IBERT demonstration is configured and running as indicated by the **MGT/IBERT Settings** tab within the IBERT Console.



- Note the line rate is 3.125 Gb/s for all four GTP transceivers (MGT Link Status in Figure 1-14).



|                          | GTPA1_DUAL_X0Y1_0        | GTPA1_DUAL_X0Y1_1        | GTPA1_DUAL_X1Y1_0        | GTPA1_DUAL_X1Y1_1        |
|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| <b>MGT Settings</b>      |                          |                          |                          |                          |
| - MGT Alias              | DUAL101_0                | DUAL101_1                | DUAL123_0                | DUAL123_1                |
| - Tile Location          | GTPA1_DUAL_X0Y1          | GTPA1_DUAL_X0Y1          | GTPA1_DUAL_X1Y1          | GTPA1_DUAL_X1Y1          |
| - MGT Link Status        | <b>3.125 Gbps</b>        | <b>3.125 Gbps</b>        | <b>3.125 Gbps</b>        | <b>3.125 Gbps</b>        |
| - Line Rate              | 3.125 Gbps               | 3.125 Gbps               | 3.125 Gbps               | 3.125 Gbps               |
| - PLL Status             | <b>LOCKED</b>            | <b>LOCKED</b>            | <b>LOCKED</b>            | <b>LOCKED</b>            |
| - Loopback Mode          | None                     | None                     | None                     | None                     |
| - DUAL Reset             | Reset                    | Reset                    | Reset                    | Reset                    |
| - TX Polarity Invert     | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| - TX Error Inject        | Inject                   | Inject                   | Inject                   | Inject                   |
| - TX Diff Output Swing   | 695 mV (0100)            | 695 mV (0100)            | 695 mV (0100)            | 695 mV (0100)            |
| - TX Pre-Emphasis        | 0 dB (000)               | 0 dB (000)               | 0 dB (000)               | 0 dB (000)               |
| - RX Polarity Invert     | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| - RX AC Coupling Enable  | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| - RX Termination Voltage | MGTAVTT *                | MGTAVTT *                | MGTAVTT *                | MGTAVTT *                |
| - RX Equalization        | -0.3 dB (00)             | -0.3 dB (00)             | -0.3 dB (00)             | -0.3 dB (00)             |
| - RX Sampling Point      | 64 0.504 UI              | 64 0.504 UI              | 64 0.504 UI              | 64 0.504 UI              |
| <b>BERT Settings</b>     |                          |                          |                          |                          |
| - TX Data Pattern        | PRBS 7-bit               | PRBS 7-bit               | PRBS 7-bit               | PRBS 7-bit               |
| - RX Data Pattern        | PRBS 7-bit               | PRBS 7-bit               | PRBS 7-bit               | PRBS 7-bit               |
| - RX Bit Error Ratio     | 1.250E-012               | 1.250E-012               | 1.250E-012               | 1.250E-012               |
| - RX Received Bit Count  | 8.002E011                | 8.002E011                | 8.003E011                | 8.003E011                |
| - RX Bit Error Count     | 0.000E000                | 0.000E000                | 0.000E000                | 0.000E000                |
| - BERT Reset             | Reset                    | Reset                    | Reset                    | Reset                    |

UG752\_c1\_17\_112310

Figure 1-14: GTP Transceiver Link Status

- Note the GTP transmitter differential output swing is preset to 695 mV (0100) as shown in Figure 1-15.

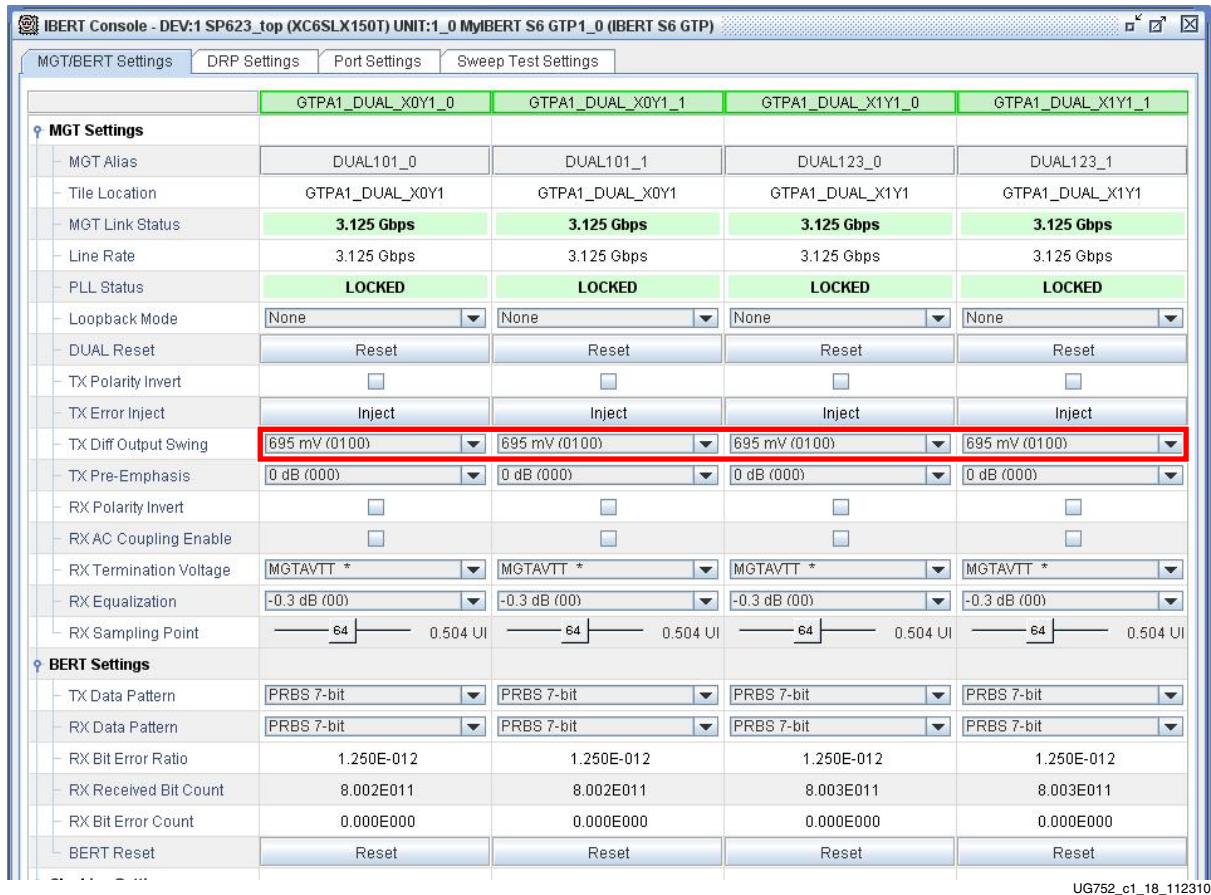
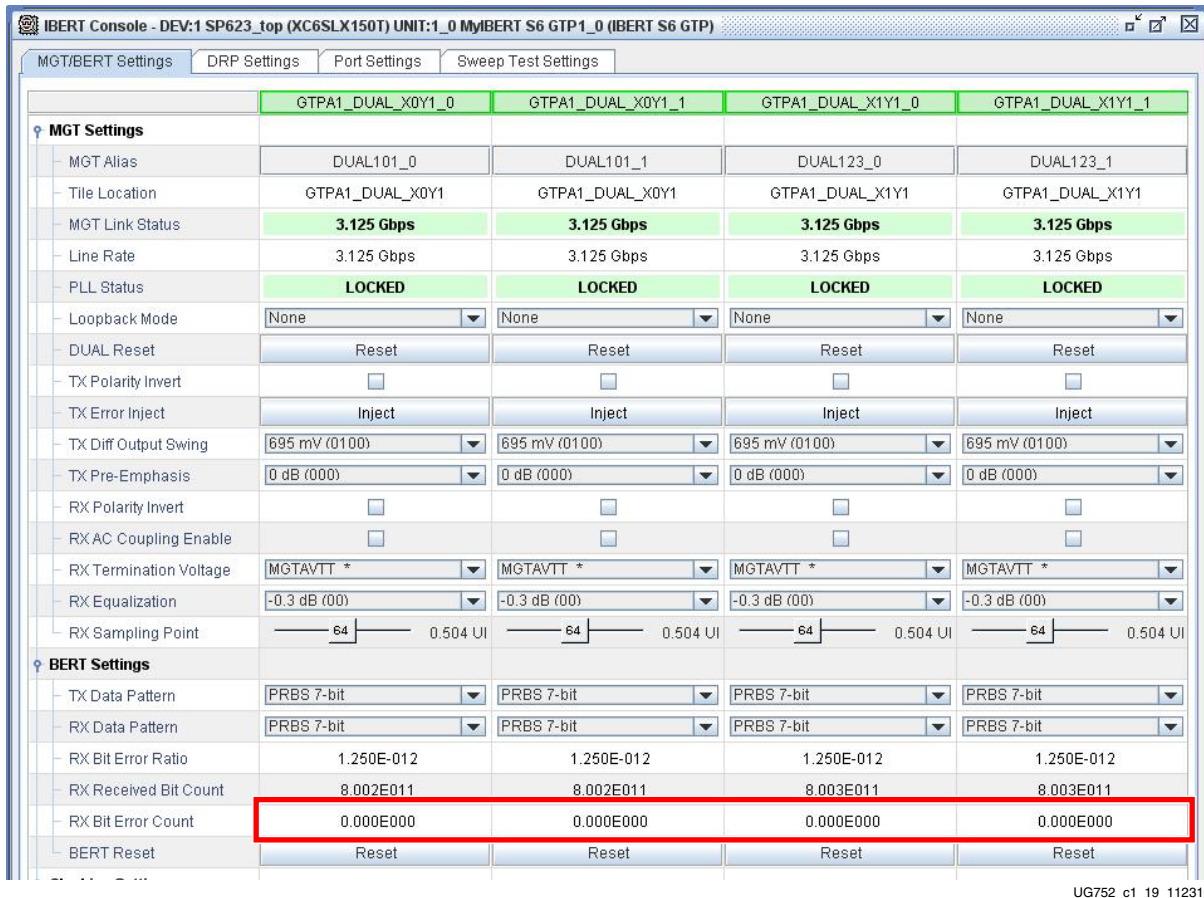


Figure 1-15: GTP Transceiver TX Differential Output Swing

- Note the RX Bit Error Count as shown in [Figure 1-16](#). For any channel that doesn't automatically reset to 0.000E000, click the Reset button immediately below the RX Bit Error Count for that particular channel.



UG752\_c1\_19\_112310

Figure 1-16: RX Bit Error Count

## Stopping the IBERT Demonstration

To stop the IBERT demonstration:

- Close the ChipScope Pro Analyzer tool.  
**Note:** Do not save changes to the project.
- Remove power to the SP623 board by placing SW1 in the OFF position.
- Remove the SMA cables from the SP623 board.

## Repeating the IBERT Demonstration for the Remaining GTP Duals

To run the demonstration on Duals 245 and 267, follow the procedure described in [Running the IBERT Demonstration, page 6](#), with the changes described here:

- Substitute the connections for Duals 245 and 267 listed in [Table A-1](#) and [Table A-2](#)
- Set dip switch SW3 to 001 for Duals 245 and 267 ([Figure A-2](#))
- Run the IBERT demonstration with `sp623_bot.cpj` ([Figure A-3](#))

The final SMA cable connections for Duals 245 and 267 are shown in [Figure A-1](#).

# Frequency Table

Table 2 lists the addresses of the output frequencies of the Si570 and Si5360 programmable clock sources.

Table 2: Si570 and Si5368 Frequency Table

| Address | Protocol         | Frequency | Address | Protocol  | Frequency | Address | Protocol | Frequency |
|---------|------------------|-----------|---------|-----------|-----------|---------|----------|-----------|
| 0       | Aurora           | 81.250    | 30      | OC-48     | 77.760    | 60      | Generic  | 533.333   |
| 1       | Aurora           | 162.500   | 31      | OC-48     | 155.520   | 61      | Generic  | 644.000   |
| 2       | Aurora           | 325.000   | 32      | OC-48     | 311.040   | 62      | Generic  | 666.667   |
| 3       | Aurora           | 650.000   | 33      | OC-48     | 622.080   | 63      | Generic  | 205.000   |
| 4       | CPRI             | 61.440    | 34      | OTU-1     | 166.629   | 64      | Generic  | 210.000   |
| 5       | CPRI             | 122.880   | 35      | OTU-1     | 333.257   | 65      | Generic  | 215.000   |
| 6       | CPRI             | 245.760   | 36      | OTU-1     | 666.514   | 66      | Generic  | 220.000   |
| 7       | CPRI             | 491.520   | 37      | PCIe      | 100.000   | 67      | Generic  | 225.000   |
| 8       | Display Port     | 67.500    | 38      | PCIe      | 125.000   | 68      | Generic  | 230.000   |
| 9       | Display Port     | 81.000    | 39      | PCIe      | 250.000   | 69      | Generic  | 235.000   |
| 10      | Display Port     | 135.000   | 40      | SATA      | 75.000    | 70      | Generic  | 240.000   |
| 11      | Display Port     | 162.000   | 41      | SATA      | 150.000   | 71      | Generic  | 245.000   |
| 12      | Fibre channel    | 106.250   | 42      | SATA      | 300.000   | 72      | Generic  | 250.000   |
| 13      | Fibre channel    | 212.500   | 43      | SATA      | 600.000   | 73      | Generic  | 255.000   |
| 14      | Fibre channel    | 425.000   | 44      | SDI       | 74.250    | 74      | Generic  | 260.000   |
| 15      | Gigabit Ethernet | 62.500    | 45      | SDI       | 148.500   | 75      | Generic  | 265.000   |
| 16      | Gigabit Ethernet | 125.000   | 46      | SDI       | 297.000   | 76      | Generic  | 270.000   |
| 17      | Gigabit Ethernet | 250.000   | 47      | SDI       | 594.000   | 77      | Generic  | 275.000   |
| 18      | Gigabit Ethernet | 500.000   | 48      | SMPTE435M | 167.063   | 78      | Generic  | 280.000   |
| 19      | GPON             | 187.500   | 49      | SMPTE435M | 334.125   | 79      | Generic  | 285.000   |
| 20      | Interlaken       | 132.813   | 50      | SMPTE435M | 668.250   | 80      | Generic  | 290.000   |
| 21      | Interlaken       | 195.313   | 51      | XAUI      | 78.125    | 81      | Generic  | 295.000   |
| 22      | Interlaken       | 265.625   | 52      | XAUI      | 156.250   | 82      | Generic  | 300.000   |
| 23      | Interlaken       | 390.625   | 53      | XAUI      | 312.500   | 83      | Generic  | 305.000   |
| 24      | Interlaken       | 531.250   | 54      | XAUI      | 625.000   | 84      | Generic  | 310.000   |
| 25      | OBSAI            | 76.800    | 55      | Generic   | 66.667    | 85      | Generic  | 315.000   |
| 26      | OBSAI            | 153.600   | 56      | Generic   | 133.333   | 86      | Generic  | 320.000   |
| 27      | OBSAI            | 307.200   | 57      | Generic   | 166.667   | 87      | Generic  | 325.000   |
| 28      | OBSAI            | 614.400   | 58      | Generic   | 266.667   | 88      | Generic  | 330.000   |
| 29      | OC-48            | 19.440    | 59      | Generic   | 333.333   | 89      | Generic  | 335.000   |

Table 2: Si570 and Si5368 Frequency Table (Cont'd)

| Address | Protocol | Frequency | Address | Protocol | Frequency | Address | Protocol | Frequency |
|---------|----------|-----------|---------|----------|-----------|---------|----------|-----------|
| 90      | Generic  | 340.000   | 103     | Generic  | 405.000   | 116     | Generic  | 470.000   |
| 91      | Generic  | 345.000   | 104     | Generic  | 410.000   | 117     | Generic  | 475.000   |
| 92      | Generic  | 350.000   | 105     | Generic  | 415.000   | 118     | Generic  | 480.000   |
| 93      | Generic  | 355.000   | 106     | Generic  | 420.000   | 119     | Generic  | 485.000   |
| 94      | Generic  | 360.000   | 107     | Generic  | 425.000   | 120     | Generic  | 490.000   |
| 95      | Generic  | 365.000   | 108     | Generic  | 430.000   | 121     | Generic  | 495.000   |
| 96      | Generic  | 370.000   | 109     | Generic  | 435.000   | 122     | Generic  | 500.000   |
| 97      | Generic  | 375.000   | 110     | Generic  | 440.000   | 123     | Generic  | 505.000   |
| 98      | Generic  | 380.000   | 111     | Generic  | 445.000   | 124     | Generic  | 510.000   |
| 99      | Generic  | 385.000   | 112     | Generic  | 450.000   | 125     | Generic  | 515.000   |
| 100     | Generic  | 390.000   | 113     | Generic  | 455.000   | 126     | Generic  | 520.000   |
| 101     | Generic  | 395.000   | 114     | Generic  | 460.000   | 127     | Generic  | 525.000   |
| 102     | Generic  | 400.000   | 115     | Generic  | 465.000   |         |          |           |

## Regenerating IBERT Designs

### Source File Overview

The file `rdf0100_12-3.zip` contains the source files for both designs (`SP623_top` and `SP623_bot`). The `.zip` file is located at:

[http://www.xilinx.com/products/boards/sp623/reference\\_designs.htm](http://www.xilinx.com/products/boards/sp623/reference_designs.htm)

In addition to the two project directories containing the source files, a `scripts` folder containing the `run_simple` script is included. This script is required to recompile the design through the ISE tool chain.

To set up the source files:

1. Download `rdf0100_12-3.zip` to a working directory on the Linux System.
2. Unzip the files to the working directory.

The files for both designs are organized in the same project directory structure. The `SP623_top` content is shown as an example:

```
SP623_top/
  par/
    ibert_s6_top.ngc
    ibert_s6_top.ncf
    icon_s6_1.ngc
    i2c_sclk2_control.ngc
    top_par.ncd
    top.ngc
    top.ucf
    vio_s6_si84_so78.ngc
  src/
    chipscope.v
```

```
i2c_sclk2_control_bb.v
ibert_s6_top_bb.v
top.v
top.xst
top.prj
vio_sclk2_control.v
```

## IBERT Design IP Components

The IBERT design IP consists of three main components:

- **ibert\_s6\_xxx**  
A four-channel IBERT core utilizing two reference clocks.
  - `ibert_s6_top` tests GTP Duals 101 and 123 located on the top half of the FPGA
  - `ibert_s6_bot` tests GTP Duals 245 and 267 located on the bottom half of the FPGA
- **vio\_sclk2\_control**  
A ChipScope Pro virtual I/O controller core for the SuperClock-2 module.
- **icon\_s6\_1**  
Single-channel Integrated Controller (ICON) core for Spartan-6 devices.

**Note:** `ibert_s6_xxx` use the BSCAN USER1 scan chain, `icon_s6_1` uses the BSCAN USER2 scan chain.

An example design hierarchy is:

```
top.v
  icon_s6_1.ngc
  ibert_s6_top.v
  vio_sclk2_control.v
    i2c_sclk2_control.v
```

### ibert\_s6\_xxx Module

Both `ibert_s6_top` and `ibert_s6_bot` designs have their own individual module generated by the Xilinx CORE Generator™ v12.3 (using the Spartan-6 IBERT GTP core, v2.01.a) without the **Implement Design** option selected. The module features four GTP lanes (one lane equals: TXP, TXN, RXP, RXN), two reference clock inputs (REFCLK0, REFCLK1), and a 25 MHz system clock.

The example `top.v` file includes an IBUF and BUFG network, as well as an ODDR2 and OBUF to drive out and back into the design.

### vio\_sclk2\_control Module

The `vio_sclk2_control.v` module provides a VIO core for controlling the SuperClock-2 module through the ChipScope Pro software. The `vio_sclk2_control.v` module features 84 synchronous inputs (14 free) and 78 synchronous outputs (12 free). No logic exists in this level because `vio_sclk2_control.v` is only a wrapper. The `i2c_sclk2_control` module instantiated at this level is a black-box HDL module and is provided as an ISE software v11.4 NGC file.

## CLK50

The IBERT design uses a 25 MHz system clock to match the IBERT requirements. Using the same clock, the I<sup>2</sup>C interface runs at half its target clock frequency of 50 MHz with no impact on the functionality or performance of the design.

## Design Notes

All files are built using ISE Design Suite, v12.3. The SP623 IBERT design uses a new methodology to combine an IBERT from the CORE Generator software with user logic.

The `vio_sclk2_control` module is configured with fixed values to reduce user error:

- **`sclk_out [3] - Si5368 RESET_B pin`**  
Connected to Logic 1 to avoid accidental reset of the Si5368 jitter-attenuating clock multiplier on the SuperClock-2 module.
- **`pca0_ctrl [5:0]`**  
Set to 0x05. Enables the SuperClock-2 module on the I<sup>2</sup>C bus only.
- **`si570_idcode`**  
Set to the idcode of the Si570 crystal oscillator on the SuperClock-2 module (0x55).

## Recreating IBERT Module with CORE Generator

This procedure describes the steps to recreate the IBERT module for GTP transceiver Duals 101 and 123 (`SP623_top`) which are located on the top half of the FPGA. The IBERT module for GTP Duals 245 and 267 (`SP623_bot`) can be recreated following the same series of steps.

To recreate the IBERT module from CORE Generator, follow these steps on a Linux system on which ISE Design Suite v12.3 is installed.

1. Open a command window.
2. In the command window, navigate to the top-level directory where the IBERT source files are located. [Source File Overview](#) is described on [page 20](#).
3. Open up CORE Generator by executing the following command:  

```
% coregen
```
4. When the Core Generator window appears on screen, click the **New Project** icon (highlighted in [Figure 1-17](#)).



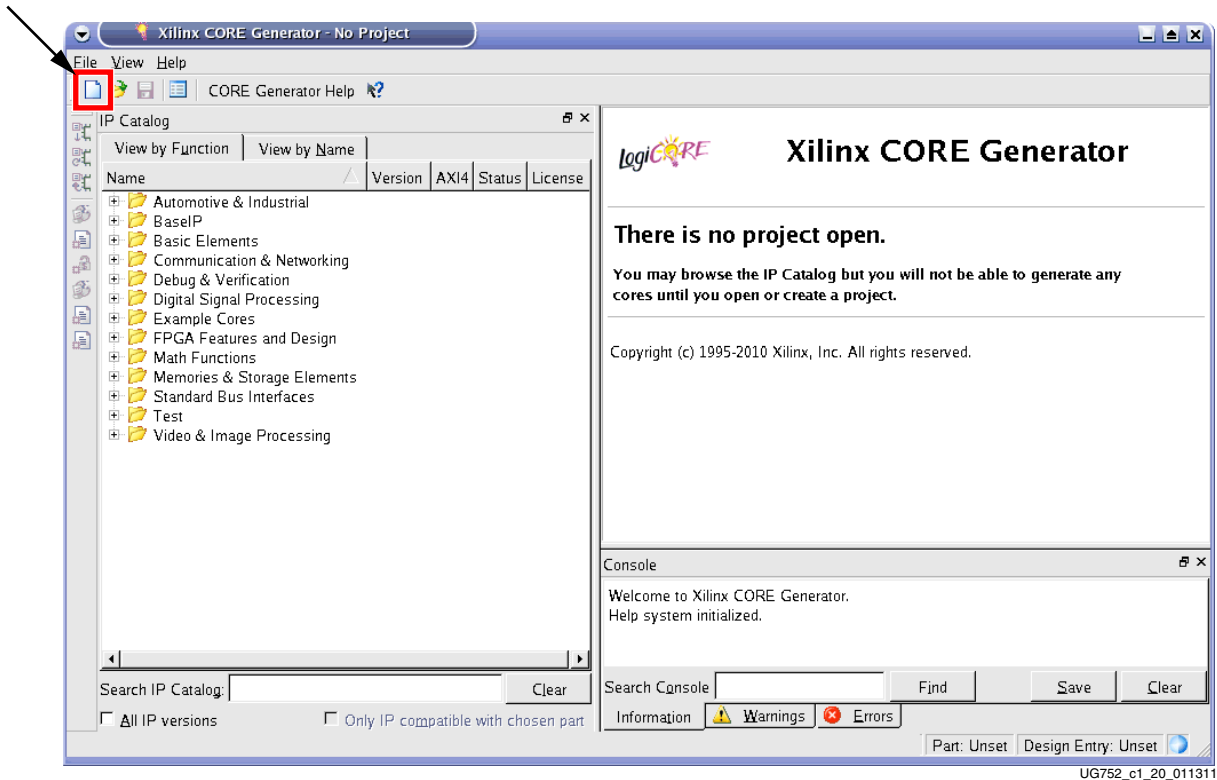


Figure 1-17: Open New Project

5. Name the project `coregen_top.cgp` and click **Save** (Figure 1-18). Note that for the "SP623\_bot" design, the project will be named `coregen_bot.cgp`.

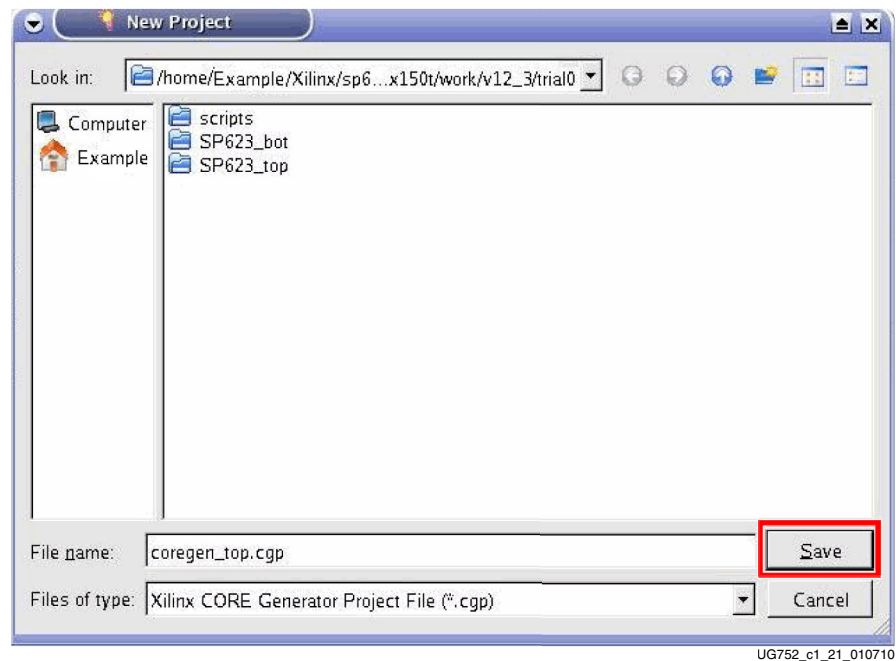


Figure 1-18: Save New Project



6. In the Project Options window, under **Part**, select the parameters listed here:

- Family: **Spartan6**
- Device: **xc6slx150t**
- Package: **fgg676**
- Speed Grade: **-3**

Figure 1-19 shows the correct settings.

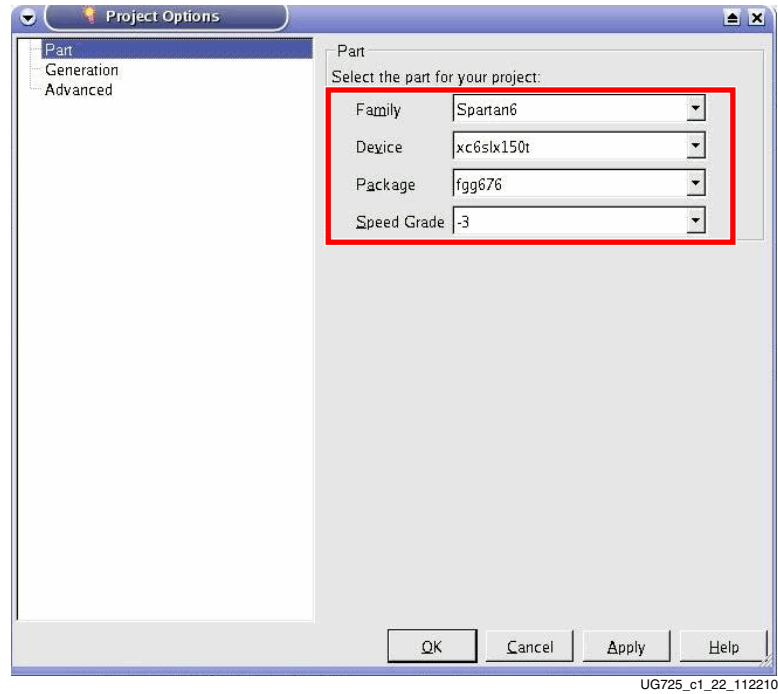


Figure 1-19: Part Options

7. In the Project Options window, click **Generation** and select **Verilog** for **Design Entry**, select **Structural** for **Preferred Simulation Model**, and uncheck the box for **ASY Symbol File**. Leave the other settings unchanged. Figure 1-20 shows the correct settings.

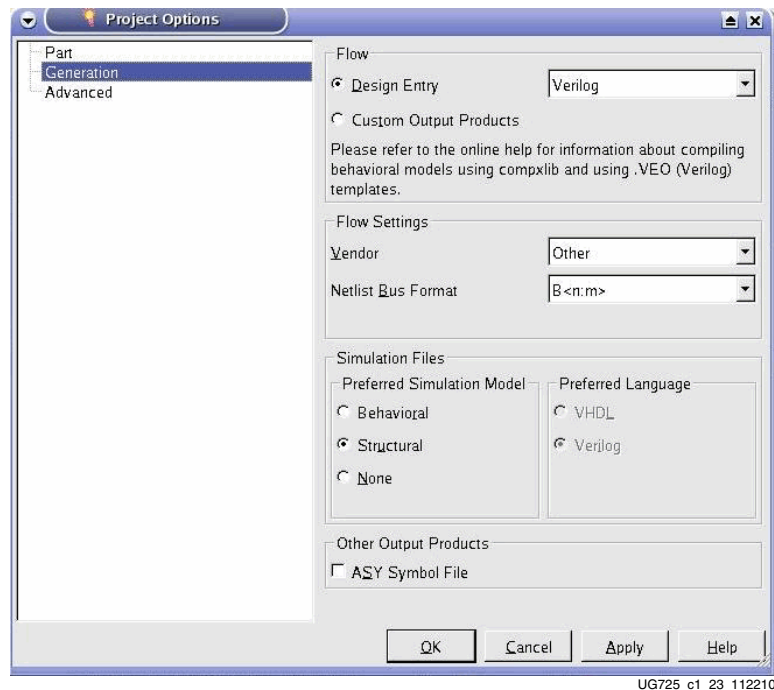


Figure 1-20: Generation Options

8. In the Project Options window, under **Advanced**, leave all settings unchanged. Figure 1-21 shows the correct settings.

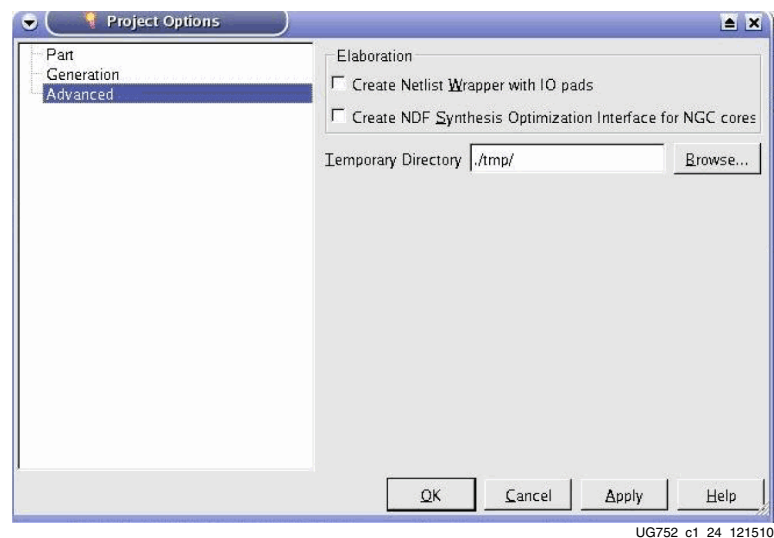


Figure 1-21: Advanced Options

9. Click **OK** to close the Project Options window.

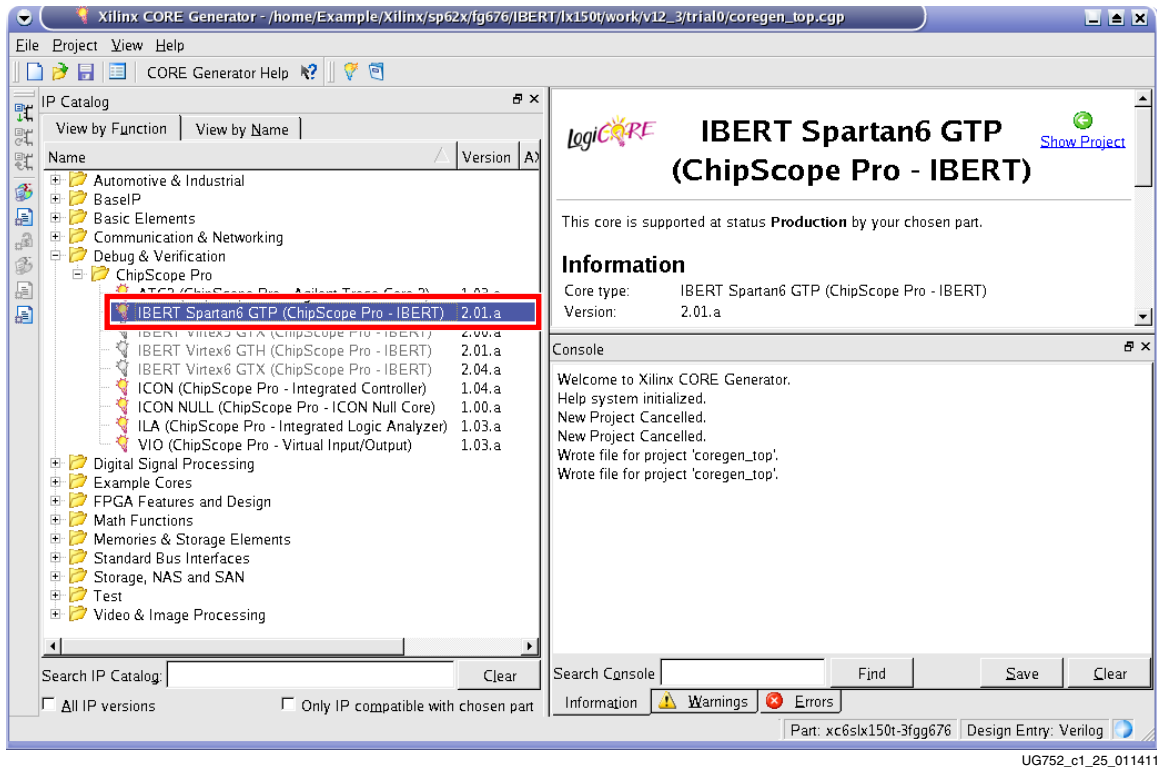
10. In the Xilinx Core Generator window under **IP Catalog** select:

**Debug & Verification** →

**ChipScope Pro** →

**IBERT Spartan6 GTP (ChipScope Pro - IBERT) 2.01.a**

Double-click the selected core as shown in [Figure 1-22](#).



*Figure 1-22: Select IP Core*

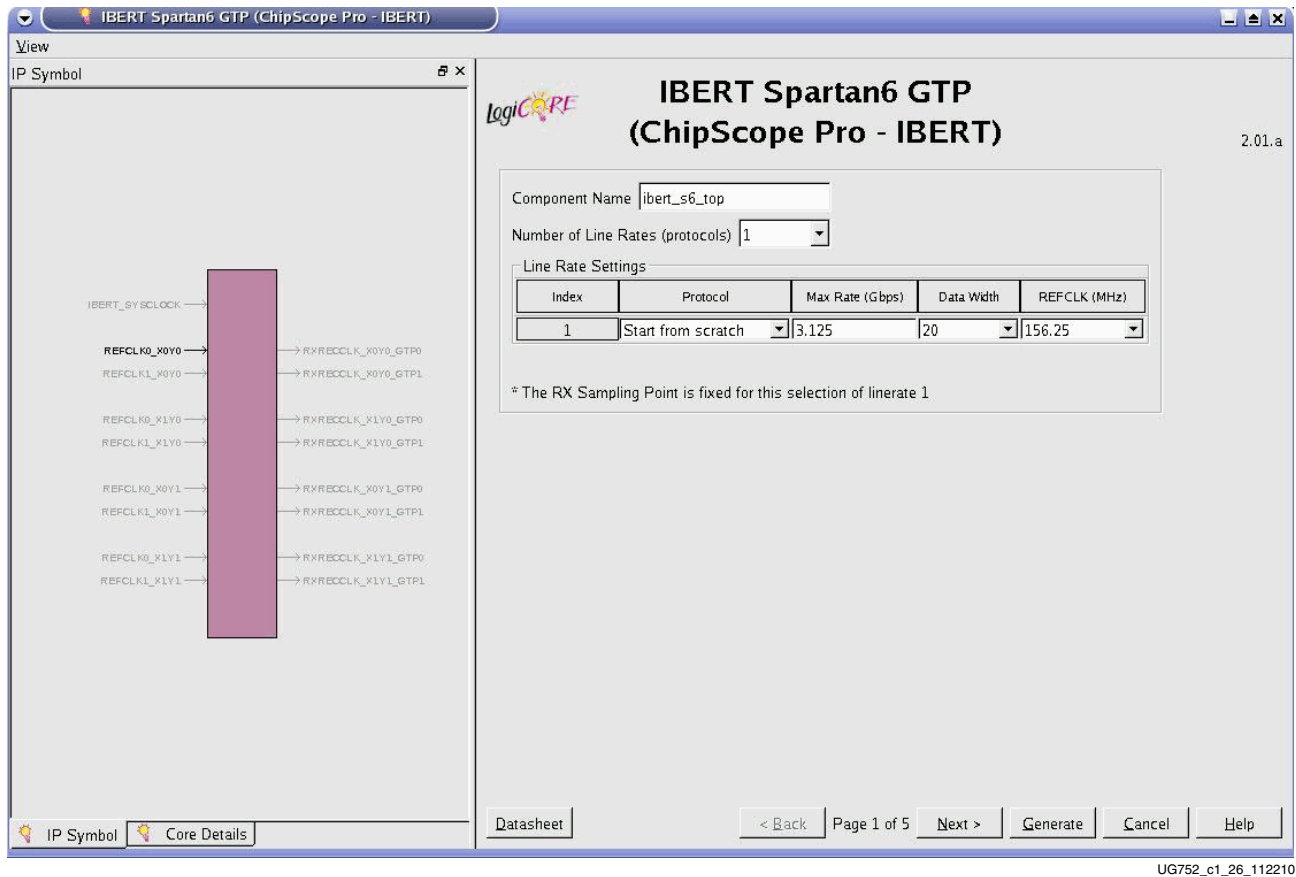
11. After page 1 of the IP customization window appears, edit the fields using the values listed here:

- Component Name: **ibert\_s6\_top**
- Max Rate (Gbps): **3.125**
- REFCLK (MHz): **156.25**

Note the name for the “SP623\_bot” design would be “ibert\_s6\_bot.”

[Figure 1-23](#) shows the correct settings.

After entering the changes to page 1, click **Next >** to continue to page 2.



UG752\_c1\_26\_112210

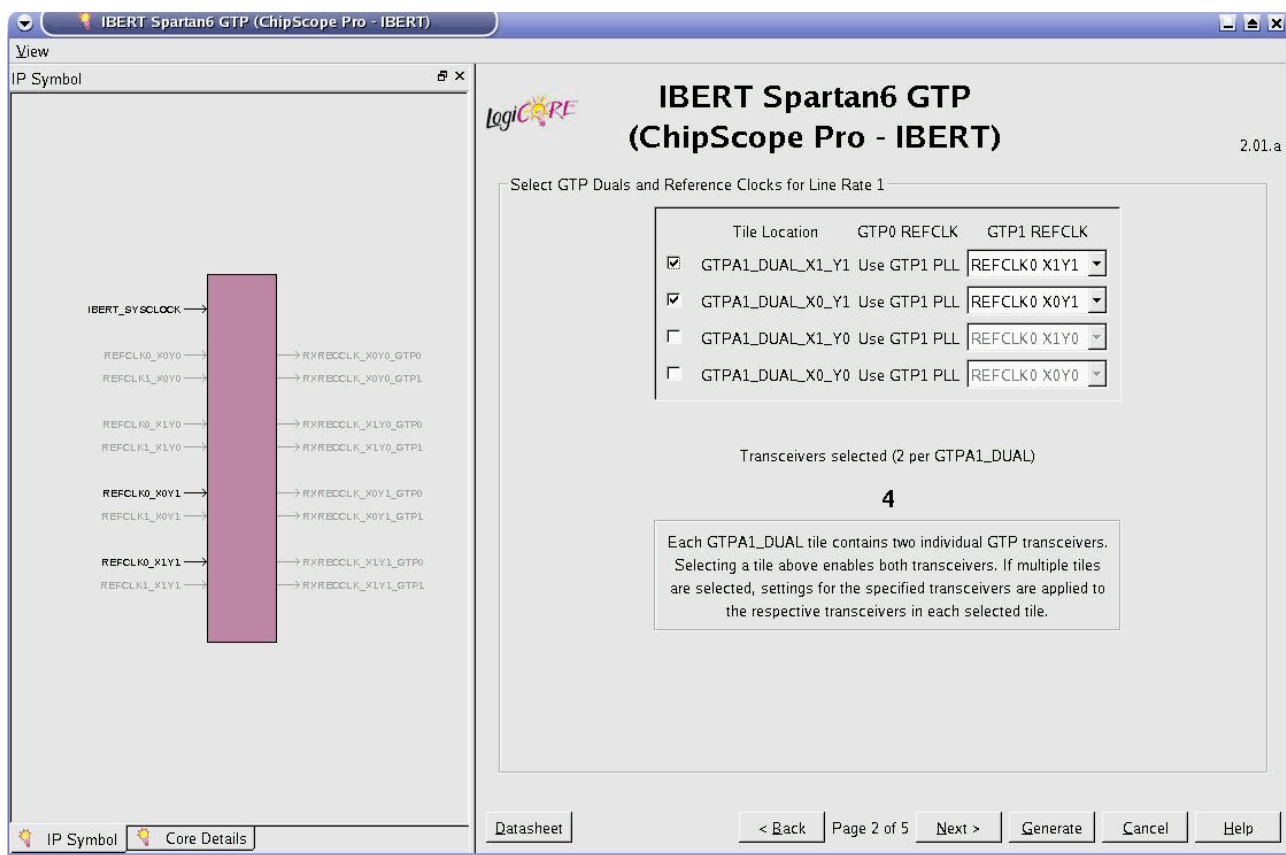
Figure 1-23: IP Customization, Page 1

12. After page 2 of the IP customization window appears, refer to [Table 1-1](#) and select (check) the tile locations associated with GTP duals 101 and 123 shown in [Figure 1-24](#). In the GTP1 REFCLK column, refer to [Table 1-1](#) and choose the appropriate REFCLK0 associated with the tile location selected in the GUI ([Figure 1-24](#)). Note: The default settings in the GUI should already match the values listed in [Table 1-1](#).

**Note:** To set up page 2 for GTP duals 245 and 267, refer to [Table 1-1](#) for the appropriate dedicated reference clock pair associated with the GTP Dual of interest.

Table 1-1: GTP Dual Tile Locations and REFCLK Selections

| GTP Dual | Tile Location    | GTP1 REFCLK  |
|----------|------------------|--------------|
| 101      | GTPA1_DUAL_X0_Y1 | REFCLK0 X0Y1 |
| 123      | GTPA1_DUAL_X1_Y1 | REFCLK0 X1Y1 |
| 245      | GTPA1_DUAL_X0_Y0 | REFCLK0 X0Y0 |
| 267      | GTPA1_DUAL_X1_Y0 | REFCLK0 X1Y0 |



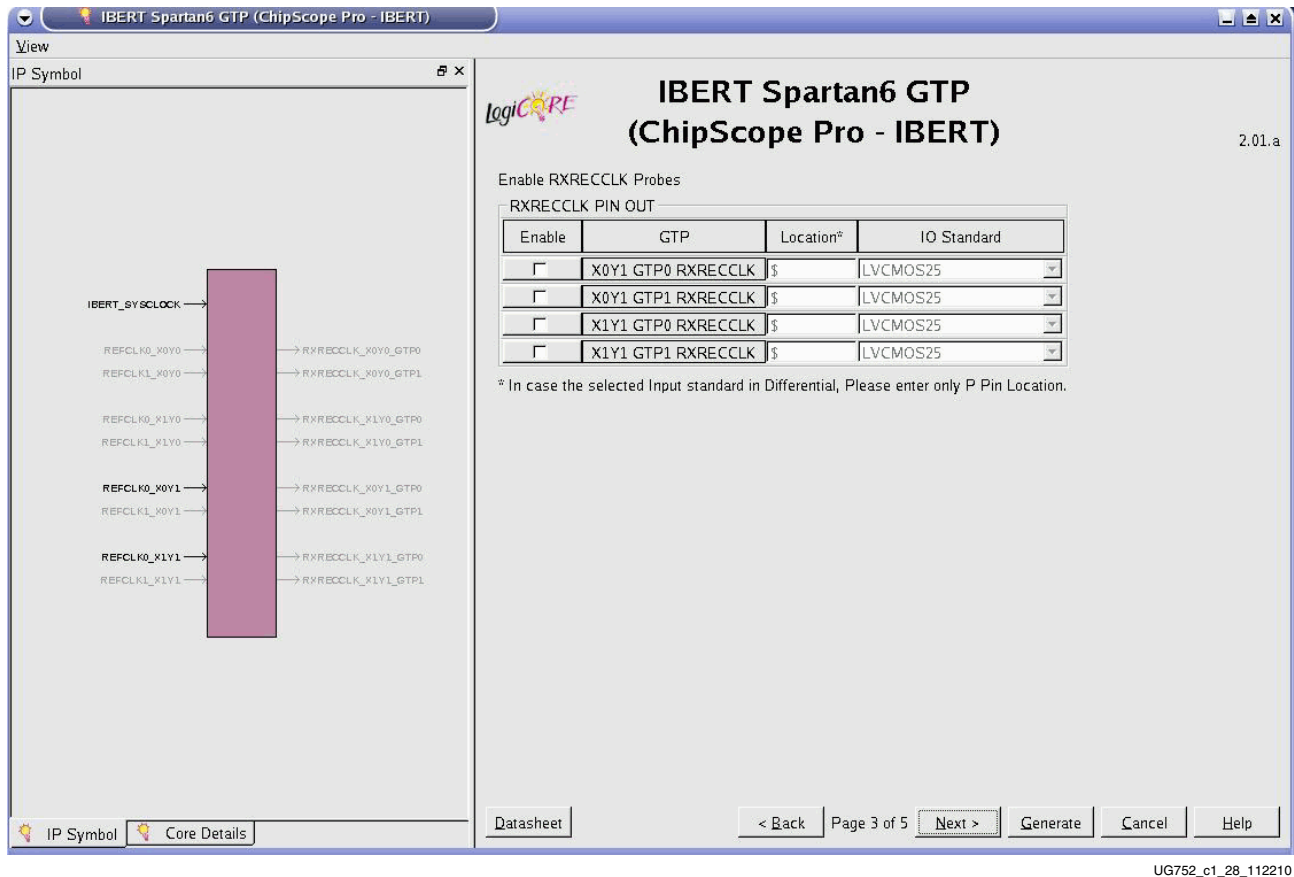
UG752\_c1\_27\_112210

Figure 1-24: IP Customization, Page 2

After entering the changes to page 2, click **Next >** to continue to page 3.

13. Leave page 3 settings as they are. [Figure 1-25](#) shows the correct settings.

Click **Next >** to continue to page 4.



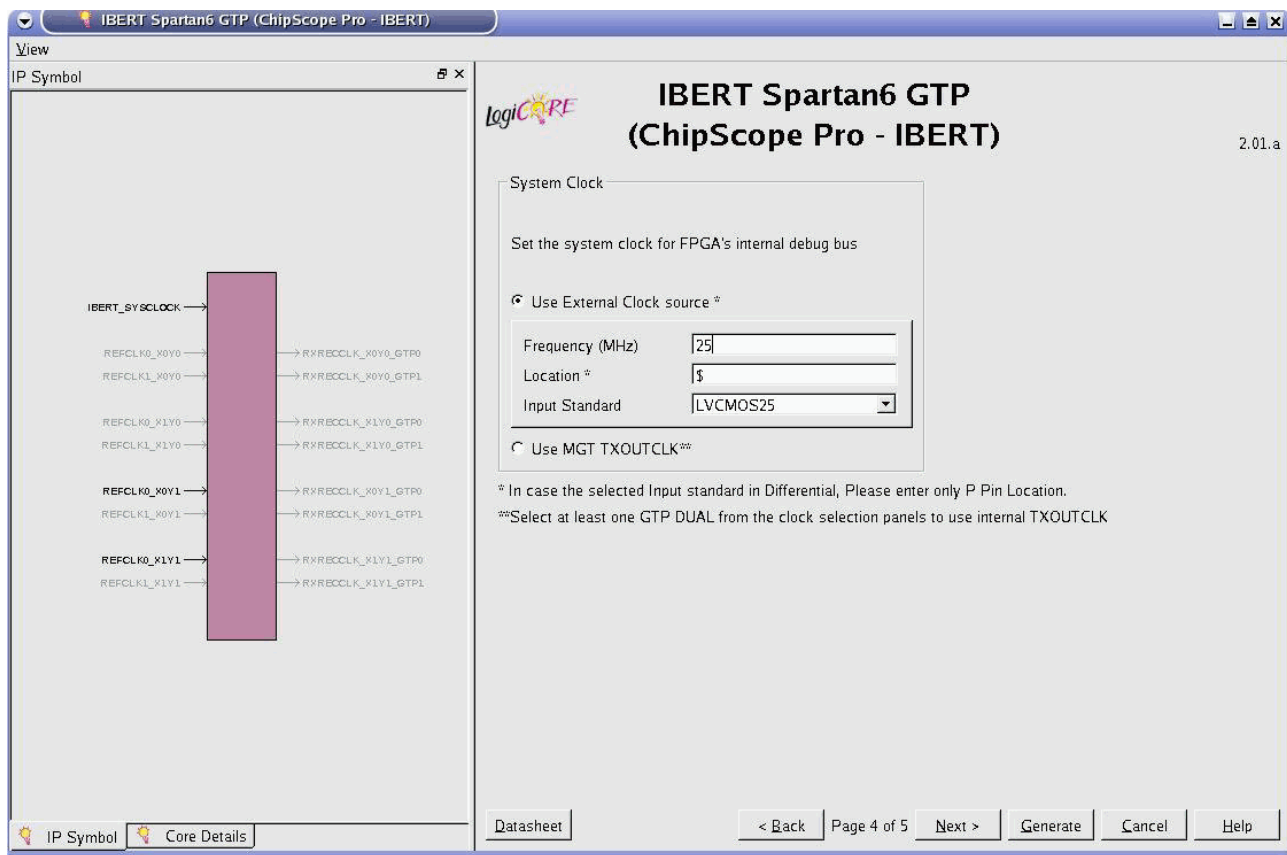
UG752\_c1\_28\_112210

Figure 1-25: IP Customization, Page 3

14. When page 4 of the IP customization window appears, select **Use External Clock Source** with the following parameters:
  - Frequency (MHz): **25**
  - Location: **\$**
  - Input Standard: **LVC MOS25**

Figure 1-26 shows the correct settings.

After entering the changes to page 4, Click **Next >** to continue to page 5.

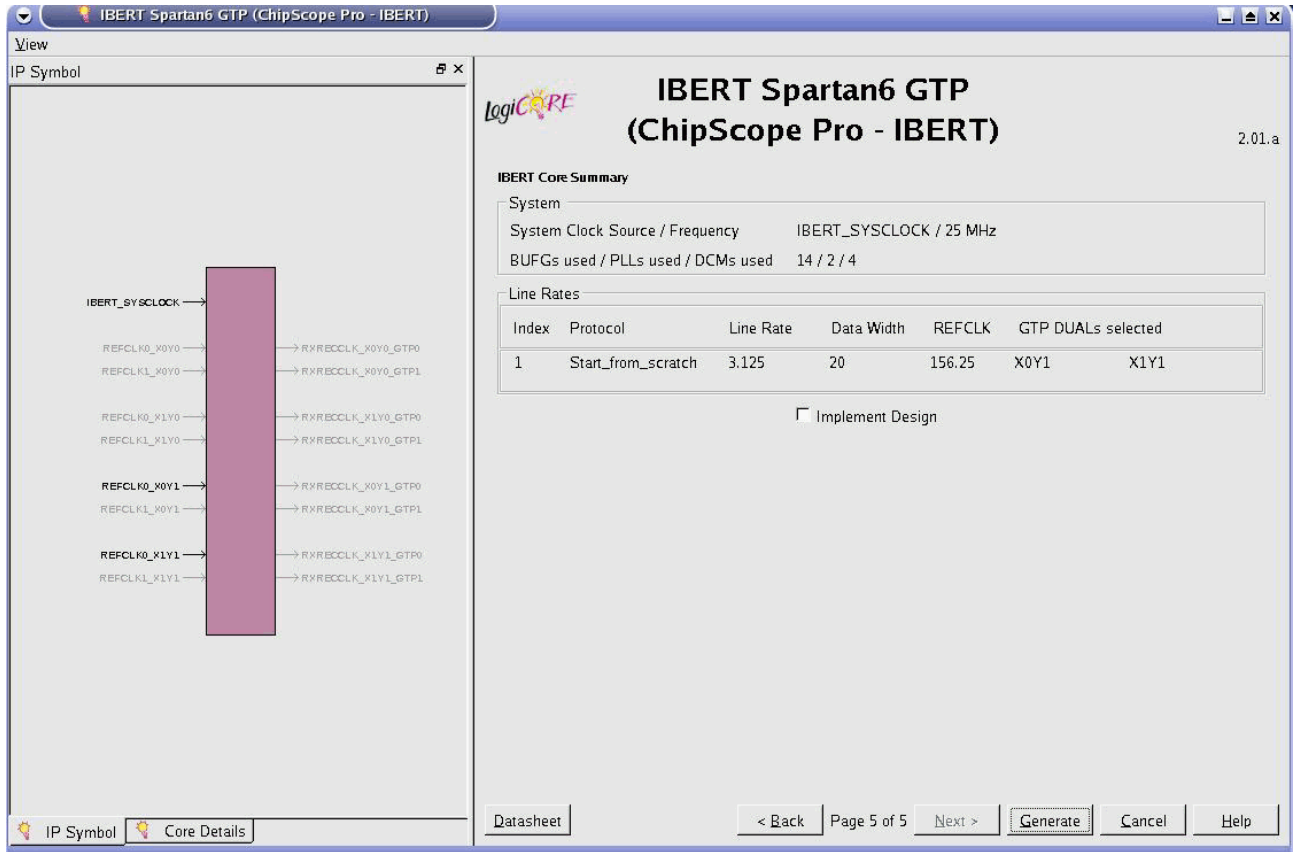


UG752\_c1\_29\_112210

Figure 1-26: IP Customization, Page 4

15. After page 5 of the IP customization window appears, uncheck the **Implement Design** box and click **Generate** (Figure 1-27).





UG752\_c1\_30\_112310

Figure 1-27: IP Customization, Page 5

16. A readme window for the **ibert\_s6\_top** core opens after core generation completes (Figure 1-28). Review the list of files created and click **Close** when finished.

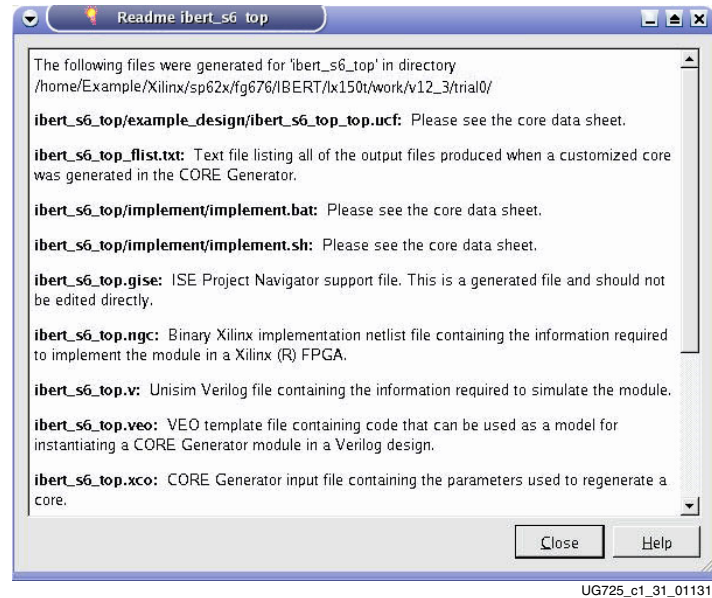


Figure 1-28: IBERT Core Readme

17. After the module has been compiled, copy the files to a working directory. In a Linux command window, execute the following commands from the top-level directory:

```
% cp ibert_s6_top.ngc SP623_top/par
```

```
cp ibert_s6_top/example_design/ibert_s6_top_top.ucf SP623_top/par/ibert_s6_top.ncf
```

18. Using a text editor, open the NCF file copied during the previous step and delete the line:

```
NET "IBERT_SYSCLOCK_P_IPAD" LOC = $ | IOSTANDARD = LVCMOS25;
```

19. The module is now ready to be used in your design (Note: Refer to `ibert_s6_top.veo` for information on the correct port names for instantiation). Move the module to the `SP623_top/src` directory by executing the following command:

```
% cp ibert_s6_top.v SP623_top/src/ibert_s6_top_bb.v
```

## Recompiling the Project

To generate a new bitstream from the IBERT core created in the previous section ([Recreating IBERT Module with CORE Generator, page 22](#)), follow these steps:

1. Using the Linux system with ISE Design Suite v12.3, open a command window and navigate down to the `SP623_top` design directory:

```
% cd SP623_top
```

2. Synthesize the design with the following command:

```
% xst -ifn src/top.xst
```

**Note:** This function uses the `src/top.prj` file and places the result in the `./par` directory.

3. Change to the `par` directory:

```
% cd par
```

4. Run the ISE tool chain through to bitgen:  

```
% ../../scripts/run_simple_top xc6slx150t-fgg676-3
```
5. The resulting bitstream is named `top_par.bit`. Consider renaming the file to distinguish it from the other design (e.g. `ibert_top.bit`).

## References

UG029, *ChipScope Pro Software and Cores User Guide*

[UG751](#), *SP623 Spartan-6 FPGA GTP Transceiver Characterization Board User Guide*

[UG770](#), *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide*

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## Running the IBERT Demonstration on Duals 245 and 267

To run the demonstration on Duals 245 and 267, follow the procedure described in [Running the IBERT Demonstration, page 6](#), with the changes described here:

- Substitute the connections for Duals 245 and 267 listed in [Table A-1](#) and [Table A-2](#)
- Set dip switch SW3 to 001 for Duals 245 and 267 ([Figure A-2](#))
- Run the IBERT demonstration with `sp623_bot.cpj` ([Figure A-3](#))

### GTP Transceiver Clock Connections

**Table A-1: Duals 245 and 267 Reference Clock Connections**

| Source              |               | Destination   |               |
|---------------------|---------------|---------------|---------------|
| SuperClock-2 Module |               | SP623 Board   |               |
| Net Name            | SMA Connector | Net Name      | SMA Connector |
| CKOUT1_P            | J5            | 245_REFCLK0_P | J80           |
| CKOUT1_N            | J6            | 245_REFCLK0_N | J81           |
| CKOUT2_P            | J7            | 267_REFCLK0_P | J92           |
| CKOUT2_N            | J8            | 267_REFCLK0_N | J93           |

### GTP TX/RX Connections

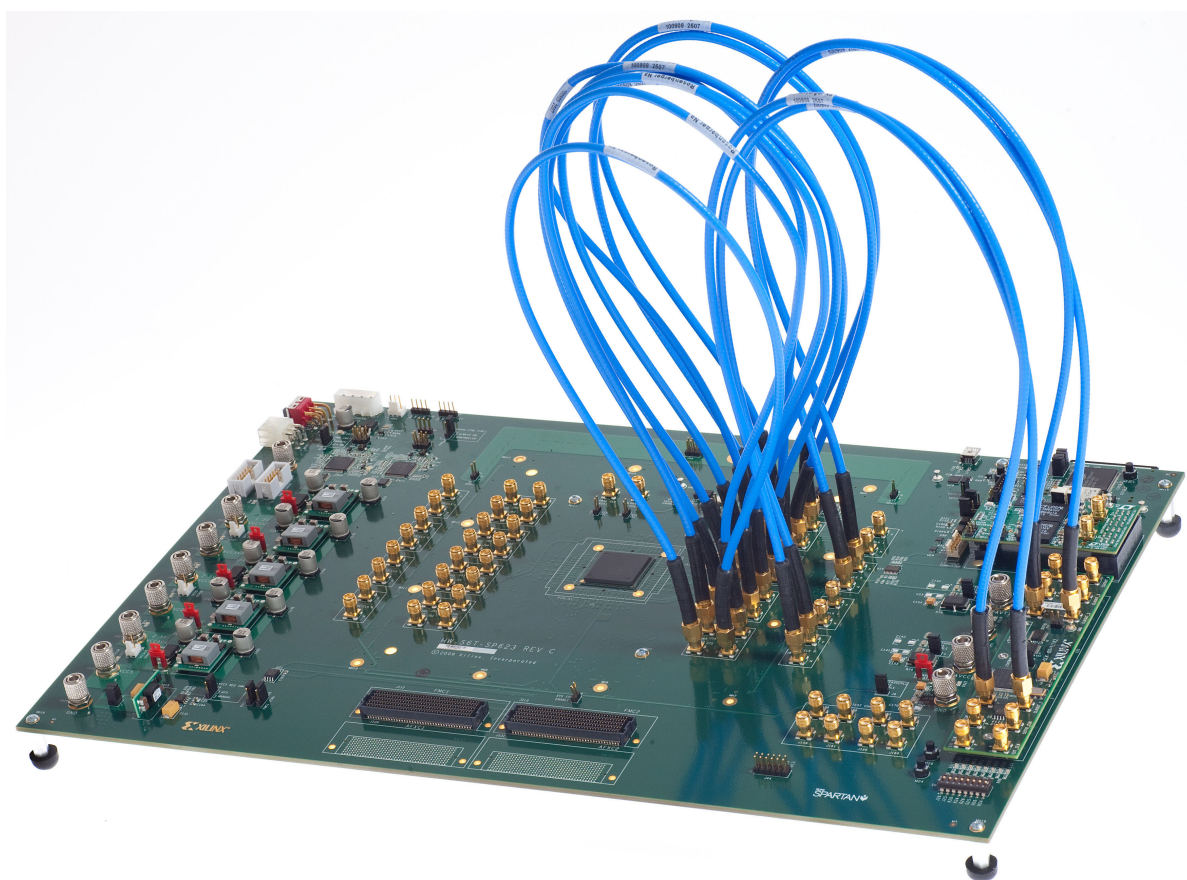
**Table A-2: Duals 245 and 267 TX/RX Connections**

| Transmitter |               | Receiver  |               |
|-------------|---------------|-----------|---------------|
| Net Name    | SMA Connector | Net Name  | SMA Connector |
| 245_TX0_P   | J74           | 245_RX0_P | J48           |
| 245_TX0_N   | J75           | 245_RX0_N | J73           |
| 245_TX1_P   | J78           | 245_RX1_P | J76           |
| 245_TX1_N   | J79           | 245_RX1_N | J77           |
| 267_TX0_P   | J86           | 267_RX0_P | J84           |
| 267_TX0_N   | J87           | 267_RX0_N | J85           |

Table A-2: Duals 245 and 267 TX/RX Connections (Cont'd)

| Transmitter |               | Receiver  |               |
|-------------|---------------|-----------|---------------|
| Net Name    | SMA Connector | Net Name  | SMA Connector |
| 267_TX1_P   | J90           | 267_RX1_P | J88           |
| 267_TX1_N   | J91           | 267_RX1_N | J89           |

The final SMA cable connections for Duals 245 and 267 are shown in [Figure A-1](#).



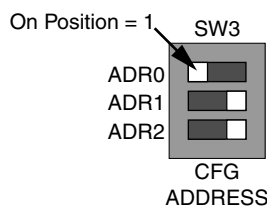
UG752\_aA\_01\_112310

Figure A-1: SMA Cable Connections for Dual 245 and 267 Transceivers and Clocks

## Switch SW3 Setting

To run the IBERT demonstration on Duals 245 and 267, set the System Ace Controller Configuration Address switch SW3 to 001 as shown in [Figure A-2](#).

Configuration Address for Dual 245 and Dual 267 (001)

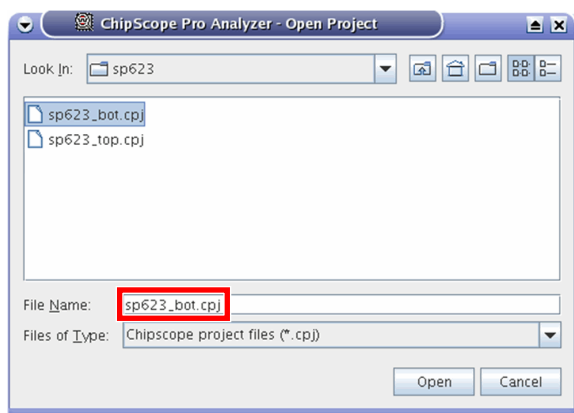


UG752\_aA\_02\_112310

Figure A-2: DIP Switch SW3 Settings For Duals 245 and 267

## Project Selection

Select `sp623_bot.cpj` and click **Open** (Figure A-3).



UG752\_aA\_03\_112310

Figure A-3: Open Project Window

