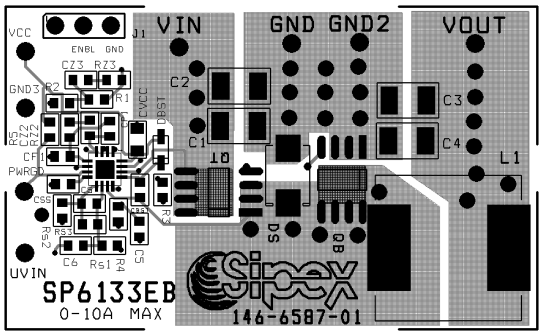
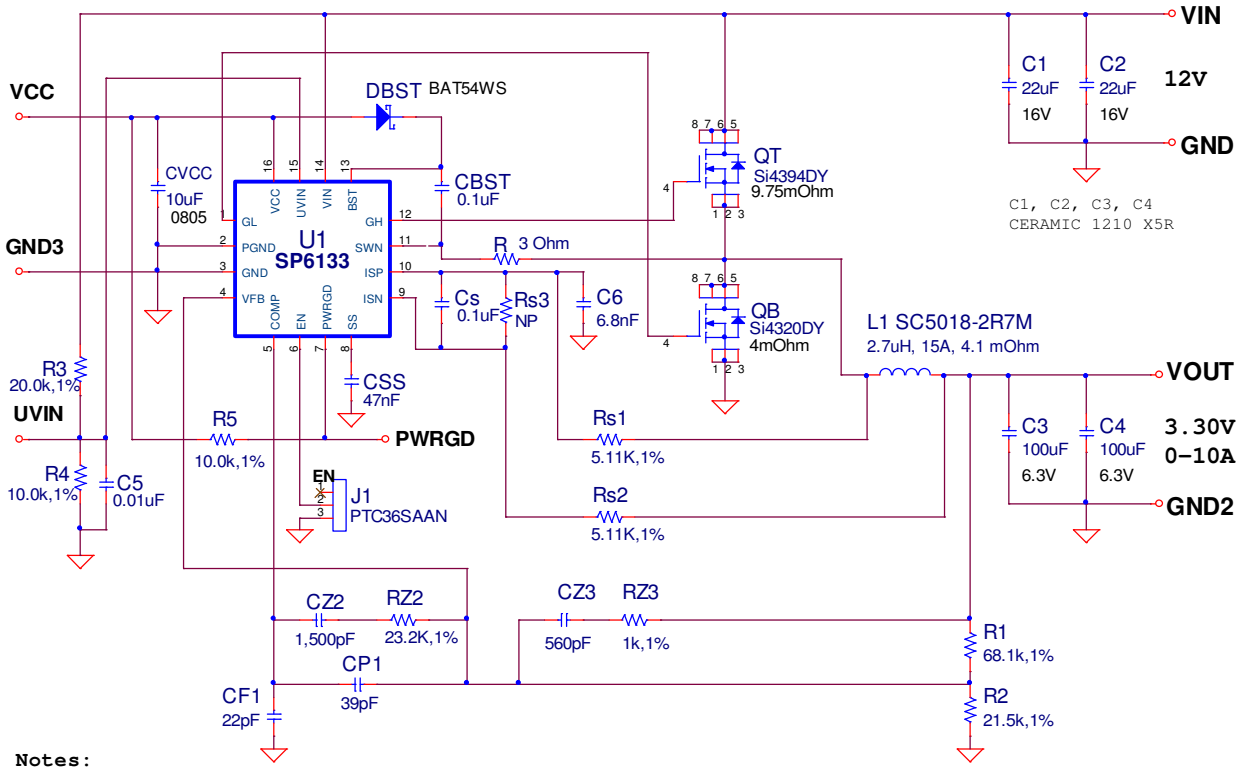
SP6133 (10A MAX.) Evaluation Board Manual

- Easy Evaluation for the SP6133ER1 12V Input, 0 to 10A Output Synchronous Buck Converter
- Precision 0.80V, ±1% High Accuracy Reference
- Small form factor
- Feature Rich:
  Single supply operation, Over-current protection with auto-restart, Power Good Output, Enable input, Fast transient response, Short Circuit Shutdown Protection, Programmable soft start.



SP6133EB SCHEMATIC



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USING THE EVALUATION BOARD

1) Powering Up the SP6133EB Circuit

Connect the SP6133 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the "VIN" and "GND" posts. Connect a Load between the "VOUT" and "GND2" posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

It's best to GND reference scope and digital meters using the Star GND post in the center of the board. VOUT ripple can best be seen touching probe tip to the pad for COUT and scope GND collar touching Star GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP6133 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP6133 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin VFB, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$Vout = 0.80V \left(R1 / R2 + 1 \right) \Rightarrow R2 = R1 / \left[\left(Vout / 0.80V \right) - 1 \right]$$

Where R1 = 68.1KΩ and for Vout = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that $50K\Omega \leq R1 \leq 100K\Omega$ for overall system loop stability.

Note that since the SP6133 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section.

POWER SUPPLY DATA

The SP6133EB is designed with an accurate 1.5% reference over line, load and temperature. Figure 1 data shows a typical SP6133ER Evaluation Board efficiency plot, with efficiencies to 95% and output currents to 10A. SP6133ER Load Regulation in Figure 2 shows only 0.09% change in output voltage from no load to 10A load. Figures 3 and 4 show the fast transient response of the SP6133. Start-up response in Figures 5, 6 and 7 show a controlled start-up with different output load behavior when power is applied where the input current rises smoothly as the soft-start ramp increases. In Figure 8 the hiccup mode gets activated in response to an output dead short circuit condition and will soft-start until the over-load is removed. Figure 9 and 10 show output voltage ripple less than 30mV over complete load range.

While data on individual power supply boards may vary, the capability of the SP6133ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

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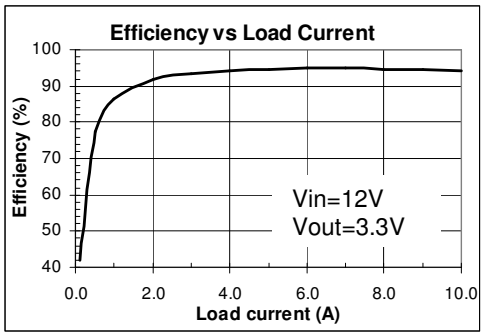


Figure 1. Efficiency vs Load

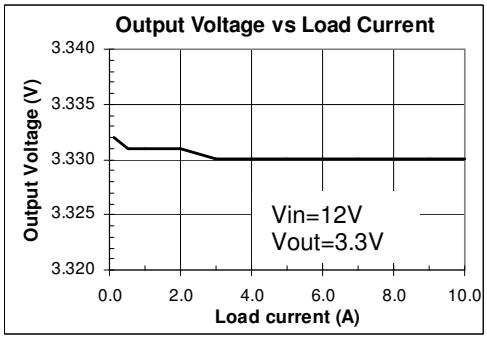


Figure 2. Load Regulation

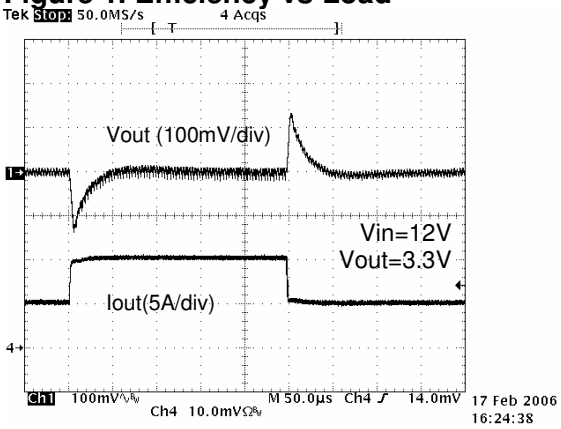


Figure 3. Load Step Response: 5->10A

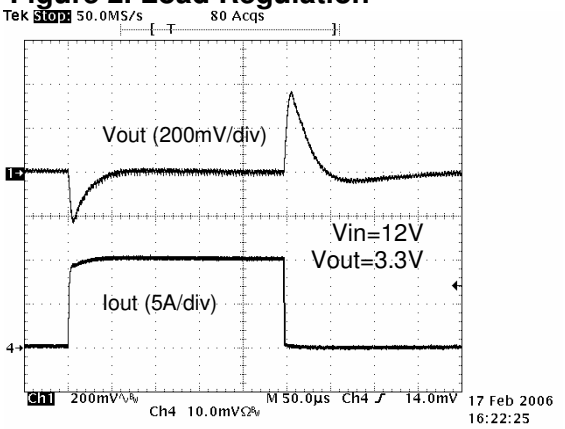


Figure 4. Load Step Response: 0->10A

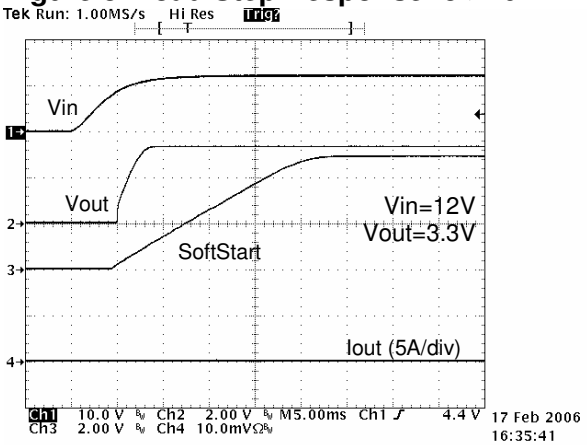


Figure 5. Start-Up Response: No Load

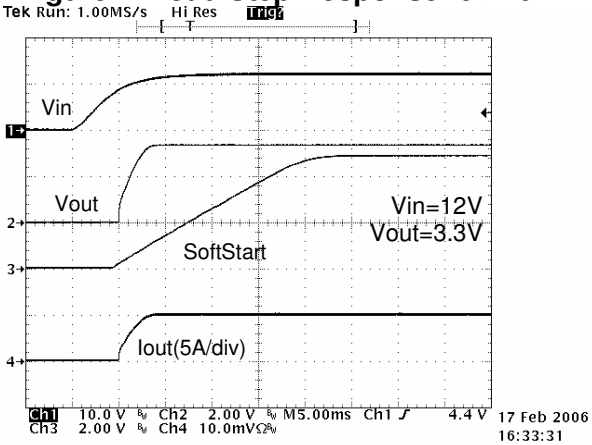


Figure 6. Start-Up Response: 5A Load

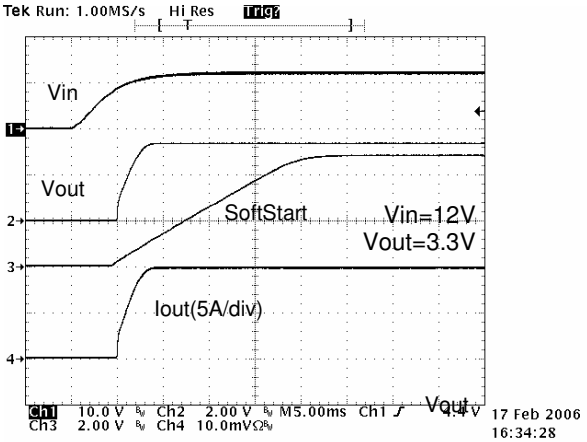


Figure 7. Start-Up Response: 10A Load

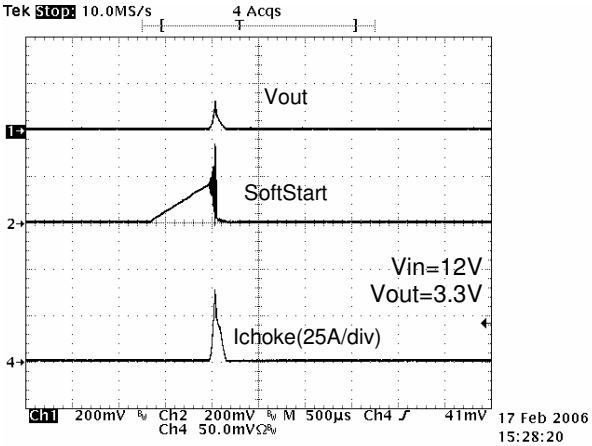


Figure 8. Output Load Short Circuit

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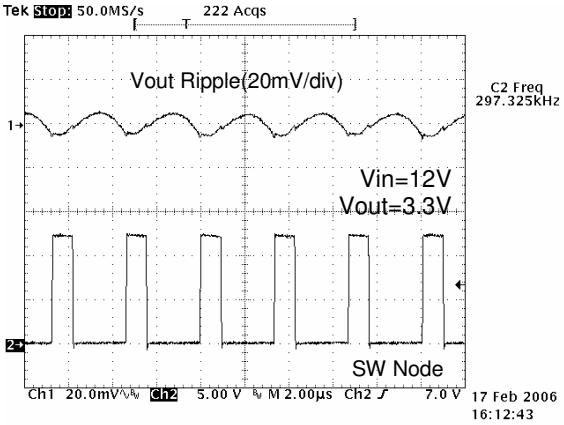


Figure 9. Output Noise at No Load

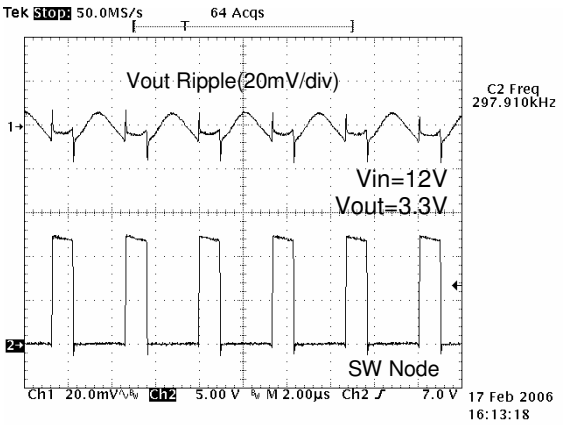


Figure 10. Output Noise at 10A Load

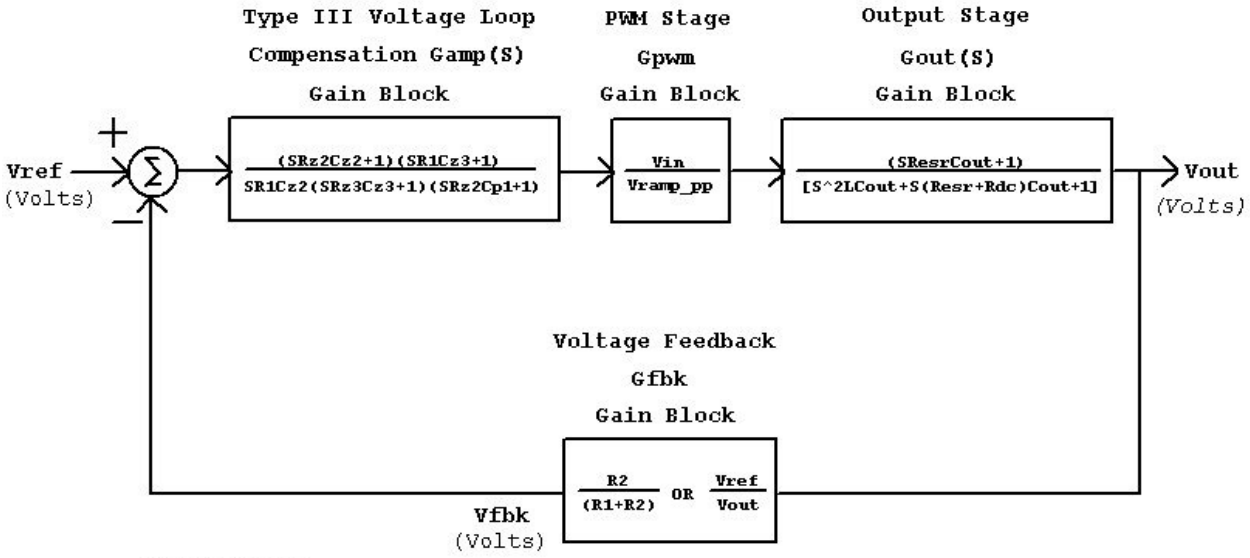
INDUCTORS - SURFACE MOUNT								
Inductance (uH)	Manufacturer/Part No.	Inductor Specification						Manufacturer Website
		Series R mOhms	Isat (A)	Size LxW(mm)	Ht.(mm)	Inductor Type		
2.7	Inter-Technical SC5018-2R7	4.1	15.00	12.6x12.6	4.50	Shielded Ferrite Core		www.inter-technical.com
CAPACITORS - SURFACE MOUNT								
Capacitance(uF)	Manufacturer/Part No.	Capacitor Specification						Manufacturer Website
		ESR ohms (max)	Ripple Current (A) @45C	Size LxW(mm)	Ht.(mm)	Voltage (V)	Capacitor Type	
22	TDK C4532X5R1C336M	0.005	4.00	3X2	2.00	16.0	X5R Ceramic	www.TDK.com
100	TDK C3225X5R0J107M	0.005	4.00	3X2	2.00	6.3	X5R Ceramic	www.TDK.com
MOSFETS - SURFACE MOUNT								
MOSFET	Manufacturer/Part No.	MOSFET Specification						Manufacturer Website
		RDS(on) ohms (max)	ID Current (A)	Qg nC (Typ)	nC (Max)	Voltage (V)	Foot Print	
N-Ch	VISHAY Si4394DY	9.75	14.0	12.5		30.0	SO-8	www.vishay.com
N-Ch	VISHAY Si4320DY	4	22.0	45.0	70.0	30.0	SO-8	www.vishay.com

Table 1: SP6133EB Suggested Components and Vendor Lists

LOOP COMPENSATION DESIGN

The open loop gain of the SP6133EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to cross over at the selected frequency **fc**, the gain of the error amplifier must compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec.

The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 of the switching frequency **fs** to insure proper operation. Since the SP6133EB is designed with ceramic type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** under damped resonance double pole frequency.



Definitions:

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP6134 Internal RAMP Amplitude Peak to Peak Voltage

Conditions:

Cz2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> Resr and Rdc

Figure 11. SP6133EB Voltage Mode Control Loop with Loop Dynamic

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The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows:

$$R1 = 68.1K$$

$$R2 = \frac{0.8 \times R1}{Vout - 0.8}$$ (sets output voltage)

$$CZ3 = \frac{1}{ZSF \times R1 \times \frac{1}{\sqrt{LC}}}$$ (sets first zero)

$$RZ2 = \frac{\left((6.28 \times fc)^2 \times L \times Cout\right) + 1}{6.28 \times fc \times CZ3} \times \frac{Vramp}{Vin}$$ (sets the cross-over frequency, fc)

$$CZ2 = \frac{1}{ZSF \times RZ2 \times \frac{1}{\sqrt{LC}}}$$ (sets second zero)

$$CP1 = \frac{1}{6.28 \times fs \times RZ2}$$ (sets first high-frequency pole)

$$RZ3 = \frac{1}{6.28 \times fs \times CZ3}$$ (sets second high-frequency pole)

Where ZSF=(f compensation double zero)/(f circuit double pole)
Here ZSF is set at 0.7.

As a particular example, consider for the following SP6133EB, 10A MAX with component selections for a type III Voltage Loop Compensation:

Vin = 12V
Vout = 3.30V @ 0 to 10A load
Select L = 2.7 uH => 30% current ripple.
Select Cout = 200uF 2x100uF Ceramic capacitors (Resr ≈ 2.5mΩ)
fs = 300KHz SP6133ER1 internal Oscillator Frequency
Vramp_pp = 1.0V SP6133ER1 internal Ramp Peak to Peak Amplitude

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Step by step design procedures:

a. **R2** = 21.8Ω

b. **CZ3** = 487pF

c. **Let fc** =40KHz then:

d. **RZ2** = 32.9kΩ

e. **CZ2** = 1390pF

f. **CP1** = 22pF

g. **RZ3** = 1.09KΩ

h. **CF1** = 22pF to stabilize SP6138ER1 internal Error Amplifier

The above component values were used as a starting point for compensating the converter and after laboratory testing the values shown in circuit schematic of page 1 were used for optimum operation.

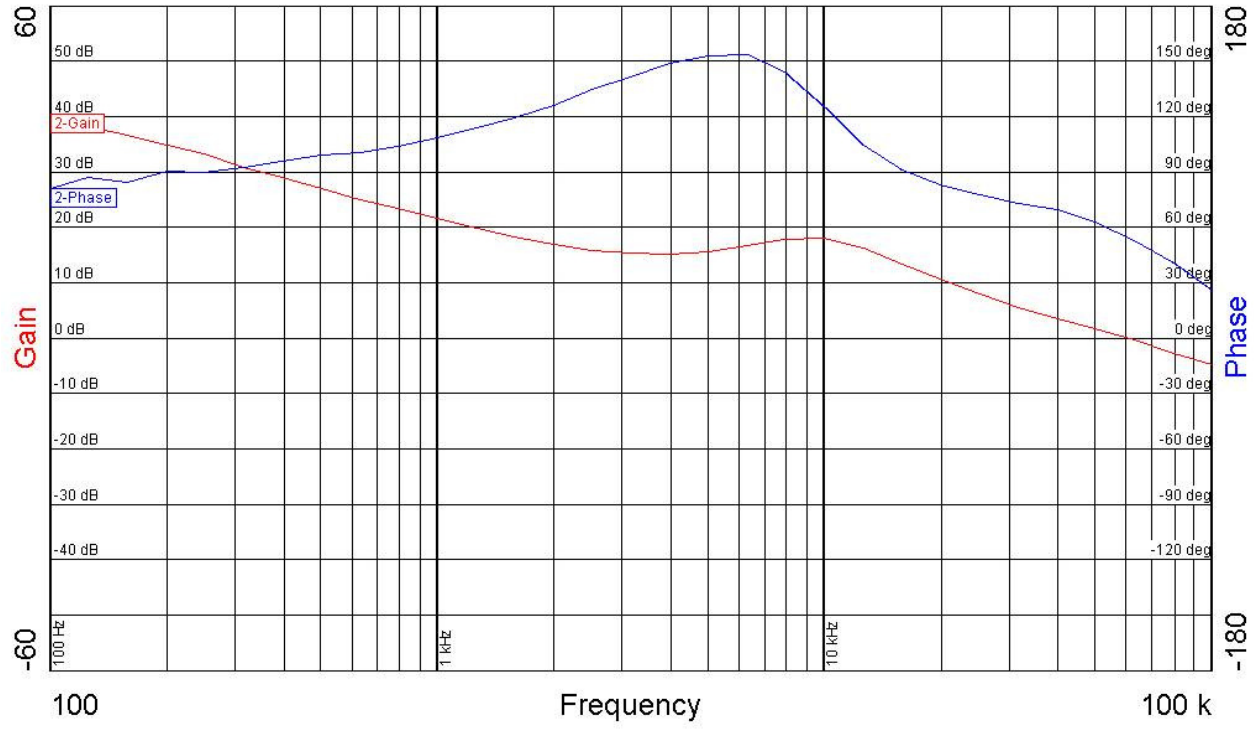


Figure 12- Gain/Phase measurement of SP6133EB shown on page 1, cross-over frequency (fc) is 60KHz with a corresponding phase of 50 degrees

PCB LAYOUT DRAWINGS

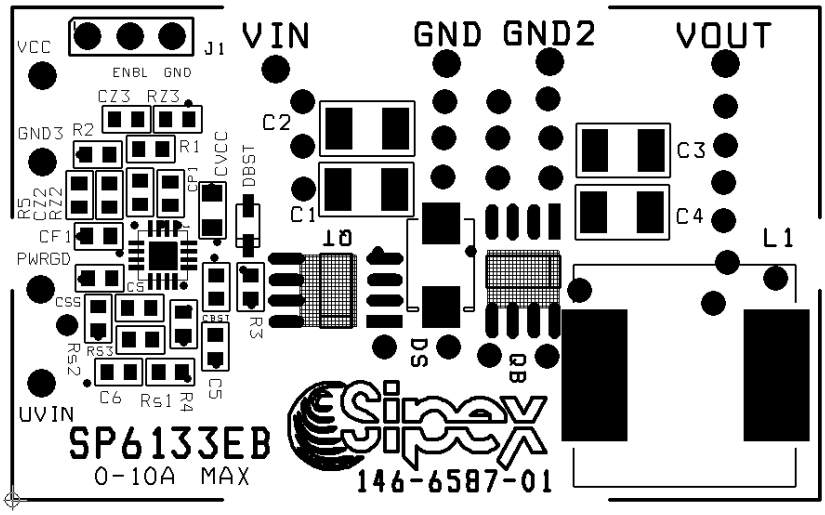


Figure 13. SP6133EB Component Placement

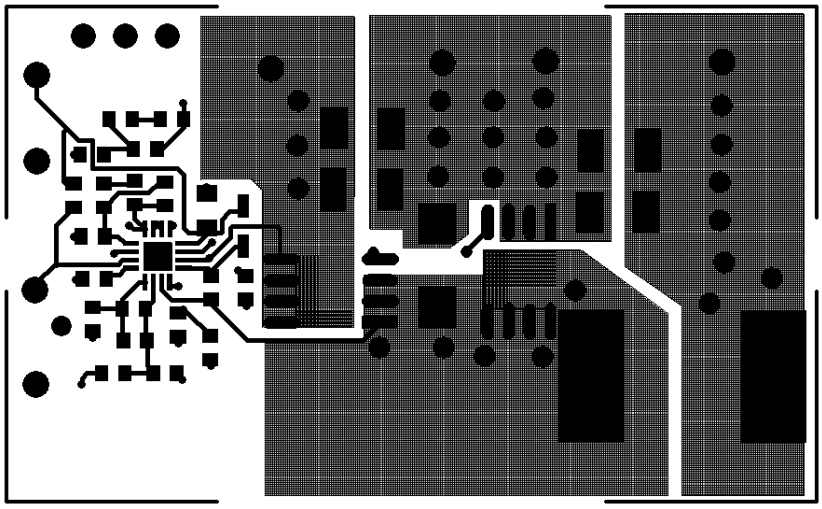


Figure 14. SP6133EB PCB Layout Top Side

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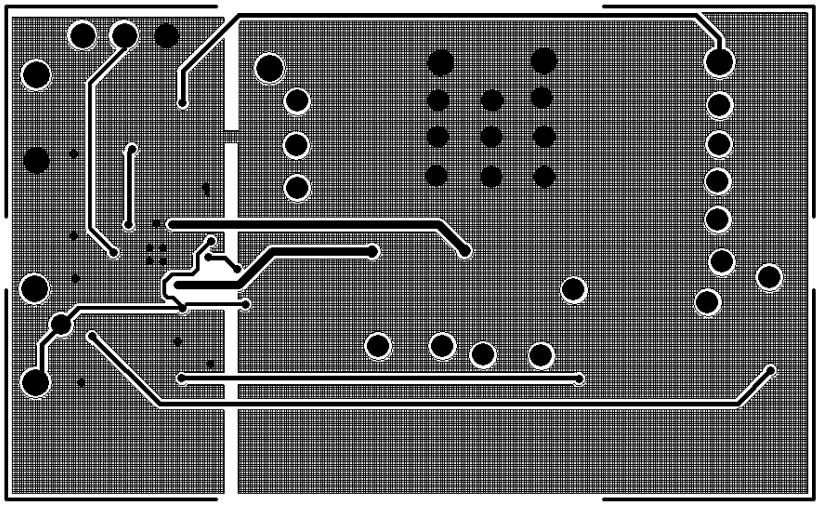


Figure 15. SP6133EB PCB Layout Bottom Side

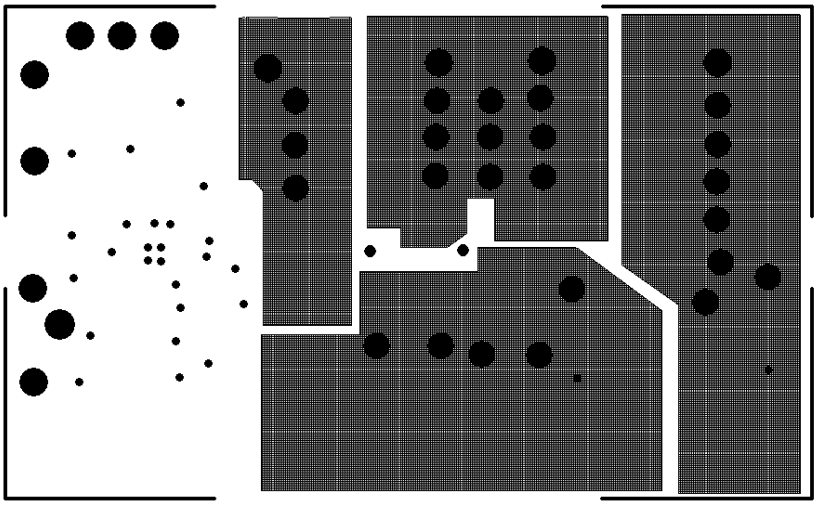


Figure 16. SP6133EB PCB Layout Inner Layer 1 & Inner Layer 2

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Table 2: SP6133EB List of Materials

Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone #
1	PCB	1	Sipex	146-6587-00	1.125"X1.875"	SP6133EB	978-667-7800
2	U1	1	Sipex	SP6133	QFN-16	Synchronous Buck Controller	978-667-7800
3	QT	1	Vishay Semi	Si4394DY	SO-8	NFET 30V, 9.75mOhm	402-563-6866
4	QB	1	Vishay Semi	Si4320DY	SO-8	NFET 30V, 4mOhm	402-563-6866
5	DS	0		Not populated			
6	DBST	1	Vishay Semi	BAT54WS	SOD-323	200mA-30V Schottky Diode	800-344-4539
7	L1	1	Inter-Technical	SC5018-2R7M	12.6X12.6mm	2.7uH Coil, 15A, 4.10 mOhm	914-347-2474
8	C1, C2	2	TDK	C4532X5R1C336M	1812	22uF Ceramic X5R 16V	978-779-3111
9	C3, C4	2	TDK	C3225X5R0J107M	1210	100uF Ceramic X5R 6.3V	978-779-3111
10	C5	1	TDK	C1608X7R1H103K	0603	0.01uF Ceramic X7R 50V	978-779-3111
11	C6	1	TDK	C1608JB1H682K	0603	6.8nF Ceramic X5R 50V	978-779-3111
12	CBST, CS	2	TDK	C1608X7R1H104K	0603	0.1uF Ceramic X7R 16V	978-779-3111
13	CF1	1	TDK	C1608COG1H220J	0603	22pF Ceramic COG 50V	978-779-3111
14	CP1	1	TDK	C1608COG1H390J	0603	39pF Ceramic COG 50V	978-779-3111
15	CSS	1	TDK	C1608X7R1H473K	0603	47,000pF Ceramic X7R 50V	978-779-3111
16	CVCC	1	TDK	C2012X5R0J106M	0805	10uF Ceramic X5R 6.3V	978-779-3111
17	CZ2	1	TDK	C1608COG1H152J	0603	1,500pF Ceramic COG 50V	978-779-3111
18	CZ3	1	TDK	C1608COG1H561J	0603	560pF Ceramic COG 50V	978-779-3111
19	R1	1	Panasonic	ERJ-3EKF6812V	0603	68.1K Ohm Thick Film Res 1%	800-344-4539
20	R2	1	Panasonic	ERJ-3EKF2152V	0603	21.5K Ohm Thick Film Res 1%	800-344-4539
21	R3	1	Panasonic	ERJ-3EKF2002V	0603	20.0K Ohm Thick Film Res 1%	800-344-4539
22	R4,R5	2	Panasonic	ERJ-3EKF1002V	0603	10.0K Ohm Thick Film Res 1%	800-344-4539
23	RS1, RS2	2	Panasonic	ERJ-3EKF5111V	0603	5.11K Ohm Thick Film Res 1%	800-344-4540
24	RS3	0		Not populated			
25	RZ2	1	Panasonic	ERJ-3EKF2322V	0603	23.2K Ohm Thick Film Res 1%	800-344-4539
26	RZ3	1	Panasonic	ERJ-3EKF1001V	0603	1K Ohm Thick Film Res 1%	800-344-4539
27	J1	1	Sullins	PTC36SAAN	.32x.12	36-Pin (3x12) Header	800-344-4539
28	(J1)	1	Sullins	STC02SYAN	.2x.1	Shunt	800-344-4539
29	VIN, VOUT, VCC, GND, GND2, GND3, UVIN, PWRGD	8	Vector Electronic	K24C/M	.042 Dia	Test Point Post	800-344-4539

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6133EB	– 40°C to +85°C	SP6133 Evaluation Board
SP6133ER1	– 40°C to +85°C	16-pin QFN

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