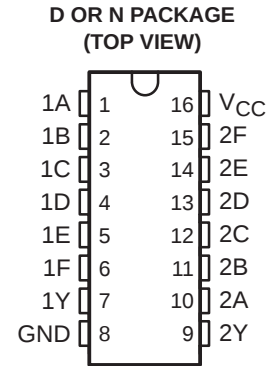


- Meets or Exceeds the Requirements of IBM™ System 360 Input/Output Interface Specification
- Operate From Single 5-V Supply
- TTL Compatible
- 3.11-V Output at $I_{OH} = -59.3 \text{ mA}$
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration
- Designed for Use With Triple Line Receiver SN75124
- Designed to Be Interchangeable With N8T13 and N8T23



THE SN751730 IS RECOMMENDED
FOR NEW IBM 360/370 INTERFACE DESIGNS.

description

The SN75123 is a dual line driver specifically designed to meet the input/output interface specifications for IBM System 360. It also is compatible with standard-TTL logic and supply-voltage levels.

The SN75123 low-impedance emitter-follower outputs drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All the inputs are in conventional TTL configuration, and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN75123 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT Y
A	B	C	D	E	F	
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

H = high level, L = low level, X = irrelevant



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

IBM is a trademark of International Business Machines Corp.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



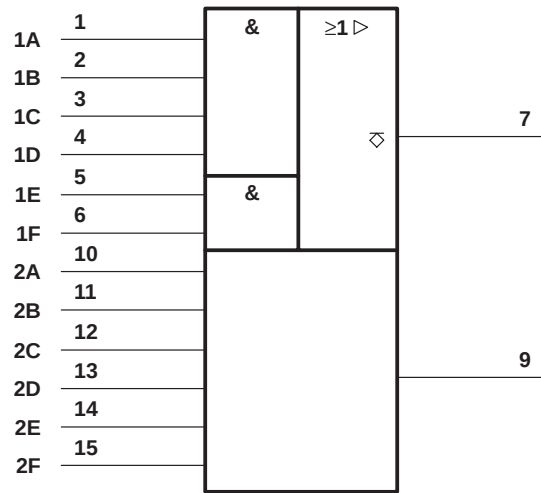
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

SN75123
DUAL LINE DRIVER

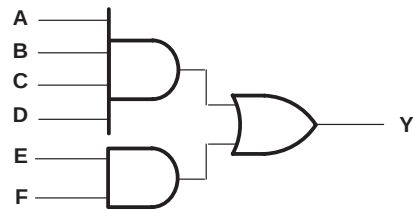
SLLS086C – SEPTEMBER 1973 – REVISED APRIL 1998

logic symbol†

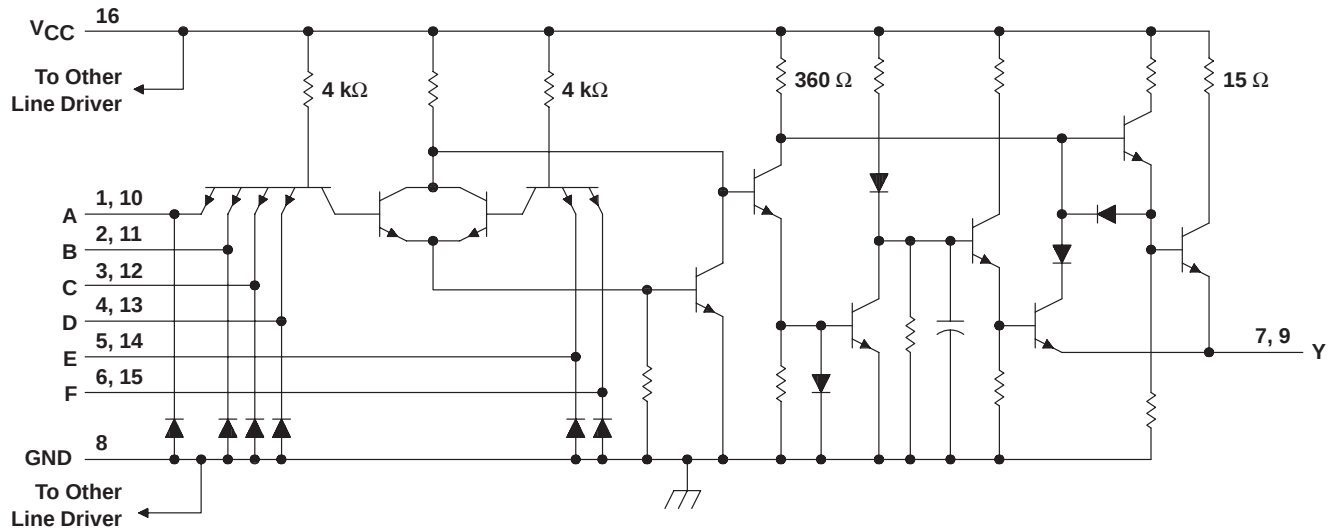


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Output voltage, V_O	7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): D package	950 mW
N package	1150 mW
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–100	mA
Operating free-air temperature, T_A	0		70	°C

SN75123

DUAL LINE DRIVER

SLLS086C – SEPTEMBER 1973 – REVISED APRIL 1998

electrical characteristics, $V_{CC} = 4.75\text{ V to }5.25\text{ V}$, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT	
V _{IK}	Input clamp voltage	V _{CC} = 5 V, I _I = −12 mA		−1.5		V	
V _{I(BR)}	Input breakdown voltage	V _{CC} = 5 V, I _I = 10 mA		5.5		V	
V _{OH}	High-level output voltage	V _{CC} = 5 V, V _{IH} = 2 V, I _{OH} = −59.3 mA, See Note 3	T _A = 25°C	3.11		V	
			T _A = 0°C to 70°C	2.9			
V _{OL}	Low-level output voltage	V _{IL} = 0.8 V, I _{OL} = −240 μA, See Note 3		0.15		V	
I _{OH}	High-level output current	V _{CC} = 5 V, V _{IH} = 4.5 V, V _{OH} = 2 V, T _A = 25°C, See Note 3			−100	−250	mA
I _{O(off)}	Off-state output current	V _{CC} = 0, V _O = 3 V			40		μA
I _{IH}	High-level input current	V _I = 4.5 V			40		μA
I _{IL}	Low-level input current	V _I = 0.4 V			−0.1	−1.6	mA
I _{OS}	Short-circuit output current†	V _{CC} = 5 V, T _A = 25°C		−30		mA	
I _{CCH}	Supply current, outputs high	V _{CC} = 5.25 V,	All inputs at 2 V,	Outputs open		28	mA
I _{CCL}	Supply current, outputs low	V _{CC} = 5.25 V,	All inputs at 0.8 V,	Outputs open		60	mA

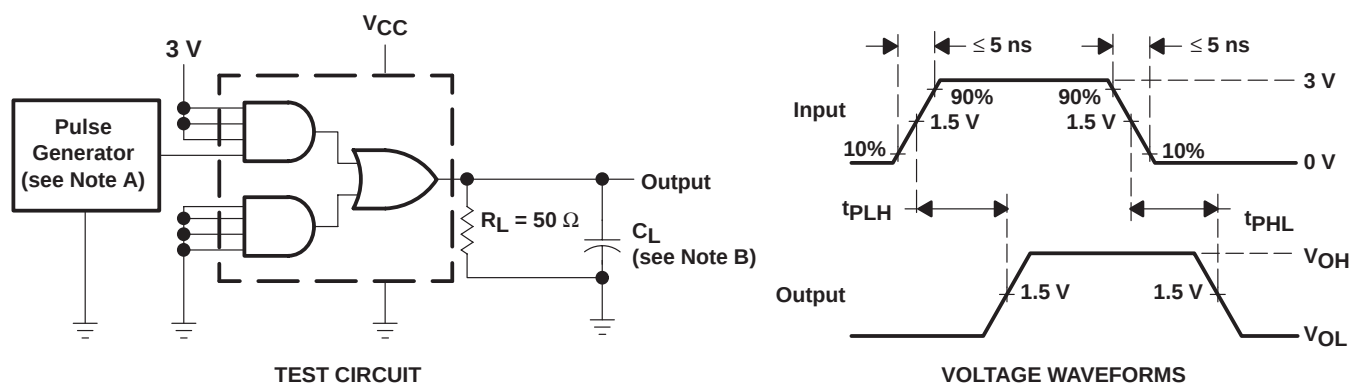
† Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$R_L = 50\text{ }\Omega$, $C_L = 15\text{ pF}$, See Figure 1		12	20	ns
t_{PHL} Propagation delay time, high- to low-level output	$R_L = 50\text{ }\Omega$, $C_L = 15\text{ pF}$, See Figure 1		12	20	ns
t_{PLH} Propagation delay time, low- to high-level output	$R_L = 50\text{ }\Omega$, $C_L = 100\text{ pF}$, See Figure 1		20	35	ns
t_{PHL} Propagation delay time, high- to low-level output	$R_L = 50\text{ }\Omega$, $C_L = 100\text{ pF}$, See Figure 1		15	25	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_O = 50\text{ }\Omega$, $t_w = 200\text{ ns}$, duty cycle = 50%.

B. C_L Includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

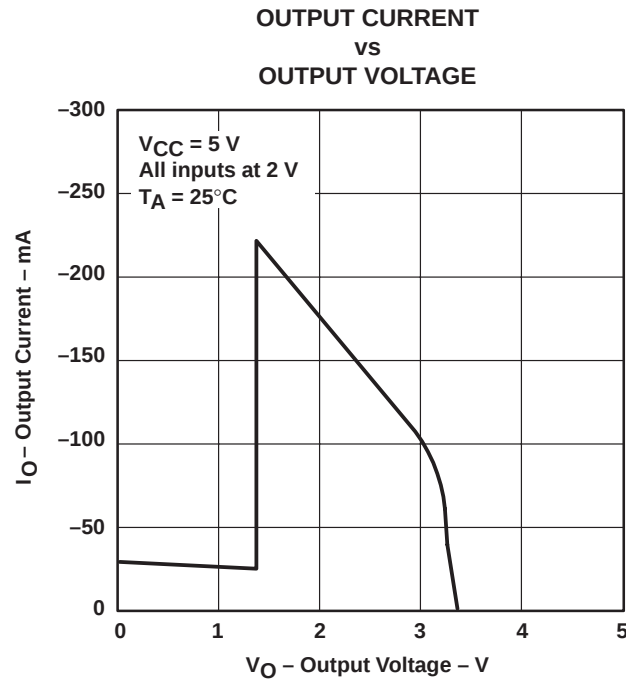


Figure 2

APPLICATION INFORMATION

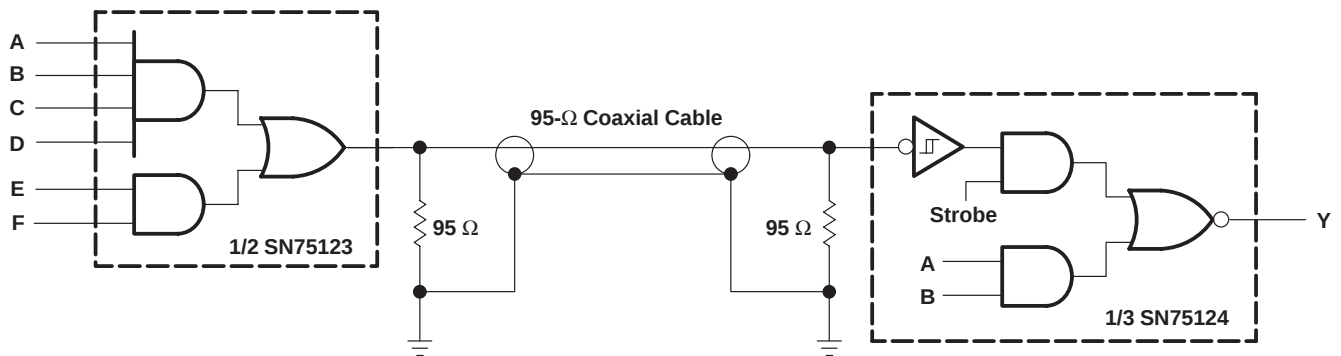


Figure 3. Unbalanced Line Communication Using SN75123 and SN75124

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75123N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN75123N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

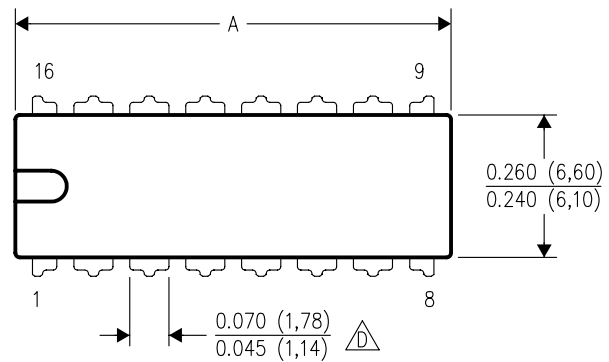
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

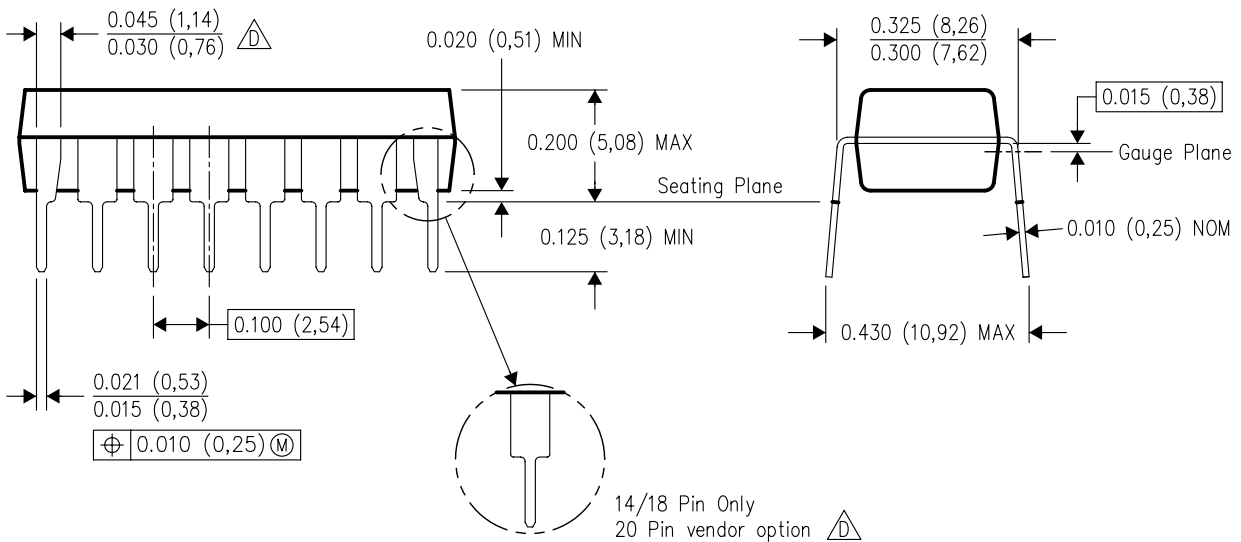
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated