



## SNx4LVC541A Octal Buffers/Drivers With 3-State Outputs

### 1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.1 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Wellness Devices
- Telecom Infrastructures
- Electronic Points of Sale

### 3 Description

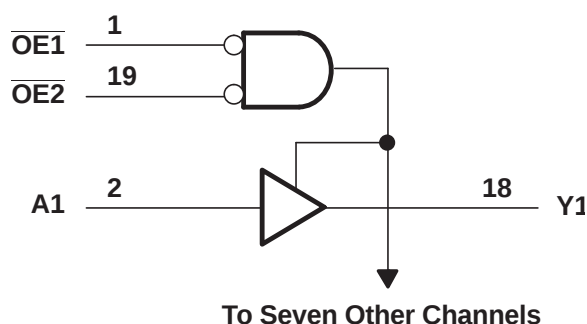
The SN54LVC541A octal buffer/driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC541A octal buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

**Device Information<sup>(1)</sup>**

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)    |
|-------------|------------|--------------------|
| SN74LVC541A | SSOP (20)  | 7.20 mm × 5.30 mm  |
|             | TVSOP (20) | 5.00 mm × 4.40 mm  |
|             | VQFN (20)  | 4.50 mm × 3.50 mm  |
|             | SOIC (20)  | 12.80 mm × 7.50 mm |
|             | TSSOP (20) | 6.50 mm × 4.40 mm  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



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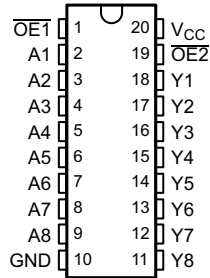
## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

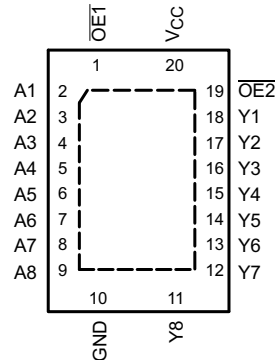
| Changes from Revision M (May 2005) to Revision N                                             | Page |
|----------------------------------------------------------------------------------------------|------|
| • Updated document to new TI data sheet format                                               | 1    |
| • Removed Ordering Information table                                                         | 1    |
| • Updated $I_{off}$ Feature bullet                                                           | 1    |
| • Updated Features to include Military Disclaimer                                            | 1    |
| • Added Applications                                                                         | 1    |
| • Added Device Information table                                                             | 1    |
| • Added Handling Ratings table                                                               | 4    |
| • Changed MAX operating free-air temperature from 85°C to 125°C for SN74LVC541A              | 5    |
| • Updated Thermal Information table                                                          | 5    |
| • Added –40°C TO 125°C temperature range to Electrical Characteristics table for SN74LVC541A | 6    |
| • Added Switching Characteristics table –40°C TO 125°C temperature range for SN74LVC541A     | 7    |
| • Added Typical Characteristics                                                              | 8    |

## 6 Pin Configuration and Functions

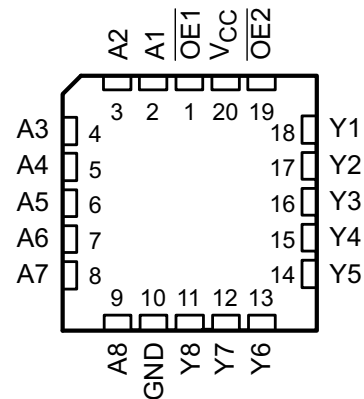
**SN54LVC541A . . . J OR W PACKAGE  
SN74LVC541A . . . DB, DGV, DW, NS,  
OR PW PACKAGE  
(TOP VIEW)**



**SN74LVC541A . . . RGY PACKAGE  
(TOP VIEW)**



**SN54LVC541A . . . FK PACKAGE  
(TOP VIEW)**



### Pin Functions

| PIN |                  | I/O | DESCRIPTION   |
|-----|------------------|-----|---------------|
| NO. | NAME             |     |               |
| 1   | $\overline{OE1}$ | I   | Output enable |
| 2   | A1               | I   | A1 input      |
| 3   | A2               | I   | A2 input      |
| 4   | A3               | I   | A3 input      |
| 5   | A4               | I   | A4 input      |
| 6   | A5               | I   | A5 input      |
| 7   | A6               | I   | A6 input      |
| 8   | A7               | I   | A7 input      |
| 9   | A8               | I   | A8 input      |
| 10  | GND              | —   | Ground pin    |
| 11  | Y8               | O   | Y8 output     |
| 12  | Y7               | O   | Y7 output     |
| 13  | Y6               | O   | Y6 output     |
| 14  | Y5               | O   | Y5 output     |
| 15  | Y4               | O   | Y4 output     |
| 16  | Y3               | O   | Y3 output     |
| 17  | Y2               | O   | Y2 output     |
| 18  | Y1               | O   | Y1 output     |
| 19  | $\overline{OE2}$ | I   | Output enable |
| 20  | VCC              | —   | Power pin     |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                                                                             | MIN                | MAX                   | UNIT   |
|-----------------|---------------------------------------------------------------------------------------------|--------------------|-----------------------|--------|
| V <sub>CC</sub> | Supply voltage range                                                                        | –0.5               | 6.5                   | V      |
| V <sub>I</sub>  | Input voltage range <sup>(2)</sup>                                                          | –0.5               | 6.5                   | V      |
| V <sub>O</sub>  | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | –0.5               | 6.5                   | V      |
| V <sub>O</sub>  | Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>              | –0.5               | V <sub>CC</sub> + 0.5 | V      |
| I <sub>IK</sub> | Input clamp current                                                                         | V <sub>I</sub> < 0 |                       | –50 mA |
| I <sub>OK</sub> | Output clamp current                                                                        | V <sub>O</sub> < 0 |                       | –50 mA |
| I <sub>O</sub>  | Continuous output current                                                                   |                    | ±50                   | mA     |
|                 | Continuous current through V <sub>CC</sub> or GND                                           |                    | ±100                  | mA     |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 7.2 Handling Ratings

|                    |                           |                                                                                          | MIN | MAX  | UNIT |
|--------------------|---------------------------|------------------------------------------------------------------------------------------|-----|------|------|
| T <sub>stg</sub>   | Storage temperature range |                                                                                          | −65 | 150  | °C   |
| V <sub>(ESD)</sub> | Electrostatic discharge   | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | 0   | 2000 | V    |
|                    |                           | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | 0   | 1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                |                                    | SN54LVC541A |                 | SN74LVC541A            |                 | UNIT |
|-----------------|--------------------------------|------------------------------------|-------------|-----------------|------------------------|-----------------|------|
|                 |                                |                                    | MIN         | MAX             | MIN                    | MAX             |      |
| V <sub>CC</sub> | Supply voltage                 | Operating                          | 2           | 3.6             | 1.65                   | 3.6             | V    |
|                 |                                | Data retention only                | 1.5         |                 | 1.5                    |                 |      |
| V <sub>IH</sub> | High-level input voltage       | V <sub>CC</sub> = 1.65 V to 1.95 V |             |                 | 0.65 × V <sub>CC</sub> |                 | V    |
|                 |                                | V <sub>CC</sub> = 2.3 V to 2.7 V   |             |                 | 1.7                    |                 |      |
|                 |                                | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2           |                 | 2                      |                 |      |
| V <sub>IL</sub> | Low-level input voltage        | V <sub>CC</sub> = 1.65 V to 1.95 V |             |                 | 0.35 × V <sub>CC</sub> |                 | V    |
|                 |                                | V <sub>CC</sub> = 2.3 V to 2.7 V   |             |                 | 0.7                    |                 |      |
|                 |                                | V <sub>CC</sub> = 2.7 V to 3.6 V   |             | 0.8             | 0.8                    |                 |      |
| V <sub>I</sub>  | Input voltage                  |                                    | 0           | 5.5             | 0                      | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                 | High or low state                  | 0           | V <sub>CC</sub> | 0                      | V <sub>CC</sub> | V    |
|                 |                                | 3-state                            | 0           | 5.5             | 0                      | 5.5             |      |
| I <sub>OH</sub> | High-level output current      | V <sub>CC</sub> = 1.65 V           |             |                 |                        | –4              | mA   |
|                 |                                | V <sub>CC</sub> = 2.3 V            |             |                 |                        | –8              |      |
|                 |                                | V <sub>CC</sub> = 2.7 V            |             | –12             |                        | –12             |      |
|                 |                                | V <sub>CC</sub> = 3 V              |             | –24             |                        | –24             |      |
| I <sub>OL</sub> | Low-level output current       | V <sub>CC</sub> = 1.65 V           |             |                 |                        | 4               | mA   |
|                 |                                | V <sub>CC</sub> = 2.3 V            |             |                 |                        | 8               |      |
|                 |                                | V <sub>CC</sub> = 2.7 V            |             | 12              |                        | 12              |      |
|                 |                                | V <sub>CC</sub> = 3 V              |             | 24              |                        | 24              |      |
| T <sub>A</sub>  | Operating free-air temperature |                                    | –55         | 125             | –40                    | 125             | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LVC541A |       |      |      |       | UNIT |
|-------------------------------|----------------------------------------------|-------------|-------|------|------|-------|------|
|                               |                                              | DB          | DGV   | DW   | NS   | PW    |      |
|                               |                                              |             |       |      |      |       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 112.1       | 128.9 | 99.4 | 90.3 | 100.8 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 73.6        | 43.8  | 66.9 | 56.6 | 35.2  |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 67.3        | 70.4  | 66.9 | 57.8 | 51.8  |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 33.3        | 3.2   | 33.8 | 28.7 | 2.2   |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 66.9        | 69.7  | 66.5 | 57.4 | 51.2  |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | n/a         | n/a   | n/a  | n/a  | n/a   |      |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, literature number [SPRA953](#).

**SN54LVC541A, SN74LVC541A**

SCAS298N – JANUARY 1993 – REVISED JUNE 2014

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## 7.5 Electrical Characteristics—DC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS                                                              | V <sub>CC</sub>    | –55°C TO 125°C        |                    |     | –40°C TO 85°C         |                    |     | –40°C TO 125°C        |                    |     | UNIT |    |
|------------------|------------------------------------------------------------------------------|--------------------|-----------------------|--------------------|-----|-----------------------|--------------------|-----|-----------------------|--------------------|-----|------|----|
|                  |                                                                              |                    | SN54LVC541A           |                    |     | SN74LVC541A           |                    |     | SN74LVC541A           |                    |     |      |    |
|                  |                                                                              |                    | MIN                   | TYP <sup>(1)</sup> | MAX | MIN                   | TYP <sup>(1)</sup> | MAX | MIN                   | TYP <sup>(1)</sup> | MAX |      |    |
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 μA                                                    | 1.65 V to 3.6 V    |                       |                    |     | V <sub>CC</sub> – 0.2 |                    |     | V <sub>CC</sub> – 0.3 |                    |     | V    |    |
|                  |                                                                              | 2.7 V to 3.6 V     | V <sub>CC</sub> – 0.2 |                    |     |                       |                    |     |                       |                    |     |      |    |
|                  | I <sub>OH</sub> = –4 mA                                                      | 1.65 V             |                       |                    |     | 1.20                  |                    |     | 1.20                  |                    |     |      |    |
|                  | I <sub>OH</sub> = –8 mA                                                      | 2.3 V              |                       |                    |     | 1.7                   |                    |     | 1.7                   |                    |     |      |    |
|                  | I <sub>OH</sub> = –12 mA                                                     | 2.7 V              | 2.2                   |                    |     | 2.2                   |                    |     | 2.2                   |                    |     |      |    |
|                  |                                                                              | 3 V                | 2.4                   |                    |     | 2.4                   |                    |     | 2.4                   |                    |     |      |    |
|                  | I <sub>OH</sub> = –24 mA                                                     | 3 V                | 2.2                   |                    |     | 2.2                   |                    |     | 2.2                   |                    |     |      |    |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA                                                     | 1.65 V to 3.6 V    |                       |                    |     | 0.2                   |                    |     | 0.3                   |                    |     | V    |    |
|                  |                                                                              | 2.7 V to 3.6 V     | 0.2                   |                    |     |                       |                    |     |                       |                    |     |      |    |
|                  | I <sub>OL</sub> = 4 mA                                                       | 1.65 V             |                       |                    |     | 0.45                  |                    |     | 0.45                  |                    |     |      |    |
|                  | I <sub>OL</sub> = 8 mA                                                       | 2.3 V              |                       |                    |     | 0.7                   |                    |     | 0.7                   |                    |     |      |    |
|                  | I <sub>OL</sub> = 12 mA                                                      | 2.7 V              | 0.4                   |                    |     | 0.4                   |                    |     | 0.4                   |                    |     |      |    |
|                  | I <sub>OL</sub> = 24 mA                                                      | 3 V                | 0.55                  |                    |     | 0.55                  |                    |     | 0.55                  |                    |     |      |    |
| I <sub>I</sub>   | V <sub>I</sub> = 0 to 5.5 V                                                  | 3.6 V              | ±5                    |                    |     | ±5                    |                    |     | ±5                    |                    |     | μA   |    |
| I <sub>off</sub> | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                                     | 0                  |                       |                    |     | ±10                   |                    |     | ±10                   |                    |     | μA   |    |
| I <sub>OZ</sub>  | V <sub>O</sub> = 0 to 5.5 V                                                  | 3.6 V              | ±15                   |                    |     | ±10                   |                    |     | ±10                   |                    |     | μA   |    |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | I <sub>O</sub> = 0 | 3.6 V                 | 10                 |     |                       | 10                 |     |                       | 10                 |     |      | μA |
|                  | 3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>                                |                    | 10                    |                    |     | 10                    |                    |     | 10                    |                    |     |      |    |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V     | 500                   |                    |     | 500                   |                    |     | 500                   |                    |     | μA   |    |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V              | 4                     |                    |     | 4                     |                    |     | 4                     |                    |     | pF   |    |
| C <sub>o</sub>   | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.3 V              | 5.5                   |                    |     | 5.5                   |                    |     | 5.5                   |                    |     | pF   |    |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This applies in the disabled state only.

## 7.6 Switching Characteristics—AC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER        | FROM<br>(INPUT)        | TO<br>(OUTPUT) | SN54LVC541A             |     |                                 |     | UNIT |
|------------------|------------------------|----------------|-------------------------|-----|---------------------------------|-----|------|
|                  |                        |                | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |     |      |
|                  |                        |                | MIN                     | MAX | MIN                             | MAX |      |
| t <sub>pd</sub>  | A                      | Y              | 5.6                     |     | 1                               | 5.1 | ns   |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | Y              | 7.5                     |     | 1                               | 7   | ns   |
| t <sub>dis</sub> | $\overline{\text{OE}}$ | Y              | 7.7                     |     | 1                               | 7   | ns   |

## 7.7 Switching Characteristics, SN74LVC541A –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| PARAMETER          | FROM<br>(INPUT)        | TO<br>(OUTPUT) | SN74LVC541A                         |      |                                    |      |                         |     |                                    |     | UNIT |
|--------------------|------------------------|----------------|-------------------------------------|------|------------------------------------|------|-------------------------|-----|------------------------------------|-----|------|
|                    |                        |                | –40°C TO 85°C                       |      |                                    |      |                         |     |                                    |     |      |
|                    |                        |                | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |      | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |      | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     |      |
|                    |                        |                | MIN                                 | MAX  | MIN                                | MAX  | MIN                     | MAX | MIN                                | MAX |      |
| t <sub>pd</sub>    | A                      | Y              | 1                                   | 15.7 | 1                                  | 7.8  | 1                       | 5.6 | 1.5                                | 5.1 | ns   |
| t <sub>en</sub>    | $\overline{\text{OE}}$ | Y              | 1                                   | 17.5 | 1                                  | 10.5 | 1                       | 7.5 | 1.5                                | 7   | ns   |
| t <sub>dis</sub>   | $\overline{\text{OE}}$ | Y              | 1                                   | 16.5 | 1                                  | 9    | 1                       | 7.7 | 1.5                                | 7   | ns   |
| t <sub>sk(o)</sub> |                        |                |                                     |      |                                    |      |                         |     |                                    | 1   | ns   |

## 7.8 Switching Characteristics, SN74LVC541A –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

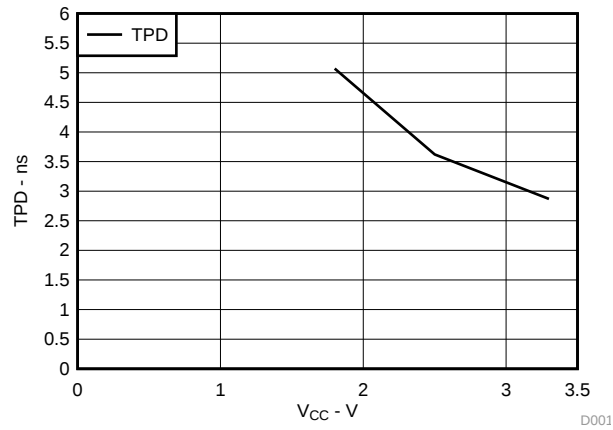
| PARAMETER          | FROM<br>(INPUT)        | TO<br>(OUTPUT) | SN74LVC541A                         |      |                                    |      |                         |     |                                    |     | UNIT |
|--------------------|------------------------|----------------|-------------------------------------|------|------------------------------------|------|-------------------------|-----|------------------------------------|-----|------|
|                    |                        |                | –40°C TO 125°C                      |      |                                    |      |                         |     |                                    |     |      |
|                    |                        |                | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |      | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |      | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     |      |
|                    |                        |                | MIN                                 | MAX  | MIN                                | MAX  | MIN                     | MAX | MIN                                | MAX |      |
| t <sub>pd</sub>    | A                      | Y              | 1                                   | 16.3 | 1                                  | 8.3  | 1                       | 6.1 | 1                                  | 5.6 | ns   |
| t <sub>en</sub>    | $\overline{\text{OE}}$ | Y              | 1                                   | 18.5 | 1                                  | 11.1 | 1                       | 8   | 1                                  | 7.5 | ns   |
| t <sub>dis</sub>   | $\overline{\text{OE}}$ | Y              | 1                                   | 17.3 | 1                                  | 9.7  | 1                       | 8.2 | 1                                  | 7.5 | ns   |
| t <sub>sk(o)</sub> |                        |                |                                     |      |                                    |      |                         |     |                                    | 1.5 | ns   |

## 7.9 Operating Characteristics

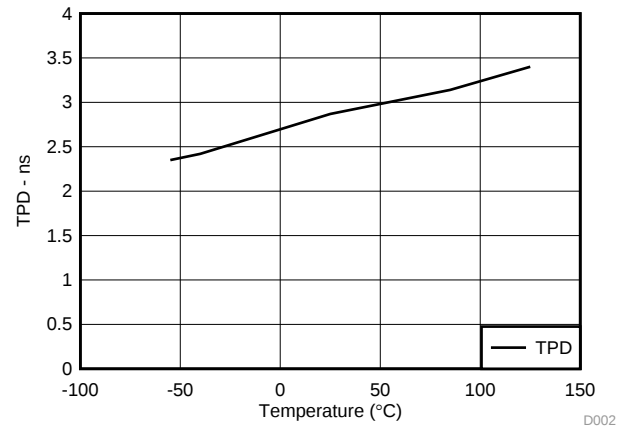
T<sub>A</sub> = 25°C

| PARAMETER       |                                                    |                  | TEST<br>CONDITIONS | V <sub>CC</sub> = 1.8 V | V <sub>CC</sub> = 2.5 V | V <sub>CC</sub> = 3.3 V | UNIT |
|-----------------|----------------------------------------------------|------------------|--------------------|-------------------------|-------------------------|-------------------------|------|
|                 |                                                    |                  |                    | TYP                     | TYP                     | TYP                     |      |
| C <sub>pd</sub> | Power dissipation capacitance<br>per buffer/driver | Outputs enabled  | f = 10 MHz         | 65                      | 58                      | 33                      | pF   |
|                 |                                                    | Outputs disabled |                    | 2                       | 2                       | 2                       |      |

## 7.10 Typical Characteristics

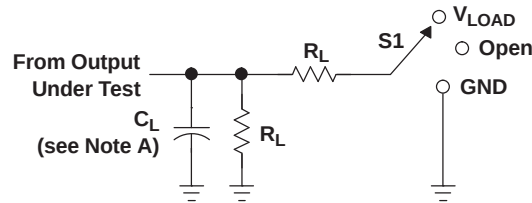


**Figure 1. SN74LVC541A TPD Across V<sub>CC</sub> at 25°C**



**Figure 2. SN74LVC541A TPD Across Temperature at 3.3 V**

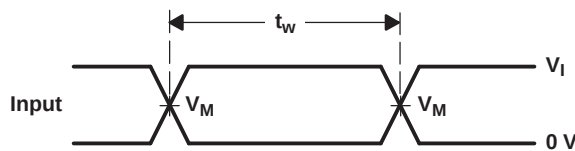
## 8 Parameter Measurement Information



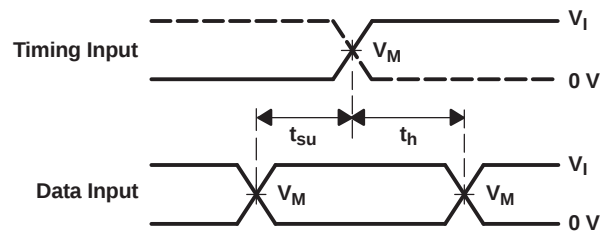
LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

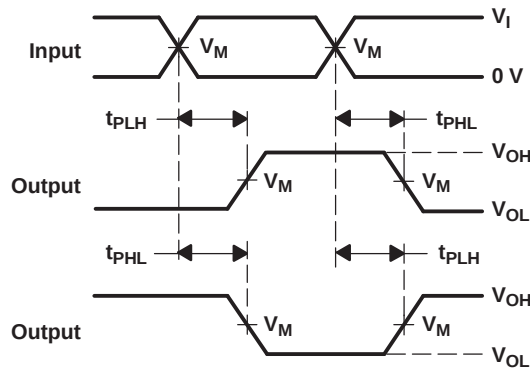
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



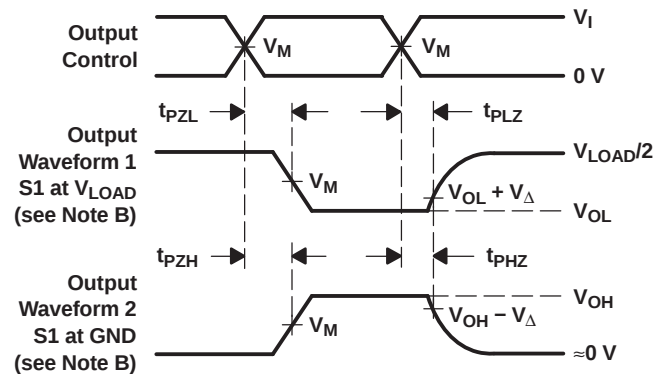
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

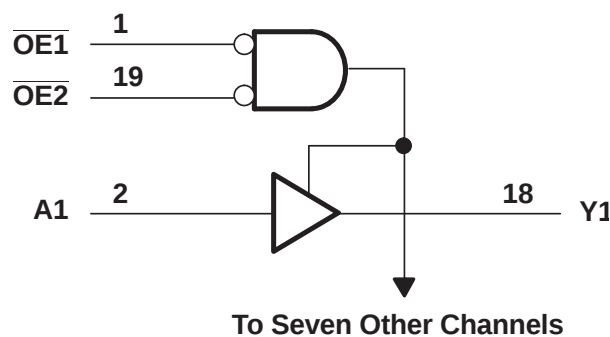
## 9 Detailed Description

### 9.1 Overview

The 'LVC541A devices are ideal for driving bus lines or buffering memory address registers.

These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout. The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment. These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$  feature
  - Allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V

### 9.4 Device Functional Modes

**Table 1. Function Table**

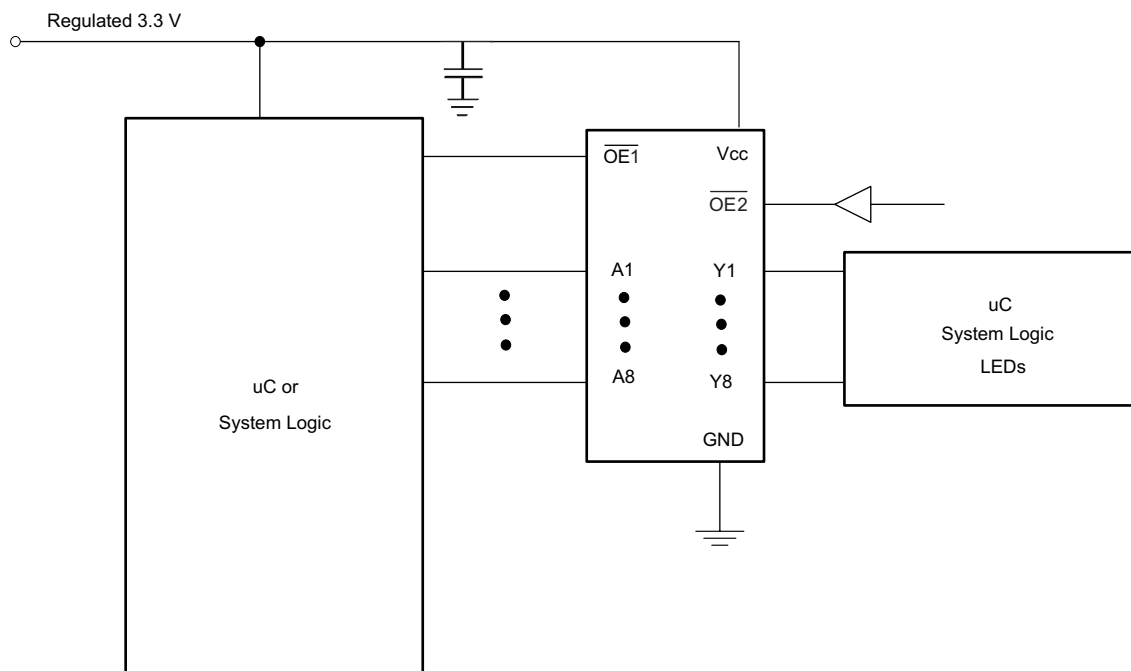
| INPUTS           |                  |   | OUTPUT<br>Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A |             |
| L                | L                | L | L           |
| L                | L                | H | H           |
| H                | X                | X | Z           |
| X                | H                | X | Z           |

## 10 Application and Implementation

### 10.1 Application Information

The SN74LVC541A is a high-drive CMOS device that can be used for a multitude of bus-interface type applications where the data needs to be retained or latched. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple outputs and for high-speed applications up to 100 Mhz. The inputs are 5.5 V tolerant allowing the device to translate down to  $V_{CC}$ .

### 10.2 Typical Application



**Figure 4. Typical Application Diagram**

#### 10.2.1 Design Requirements

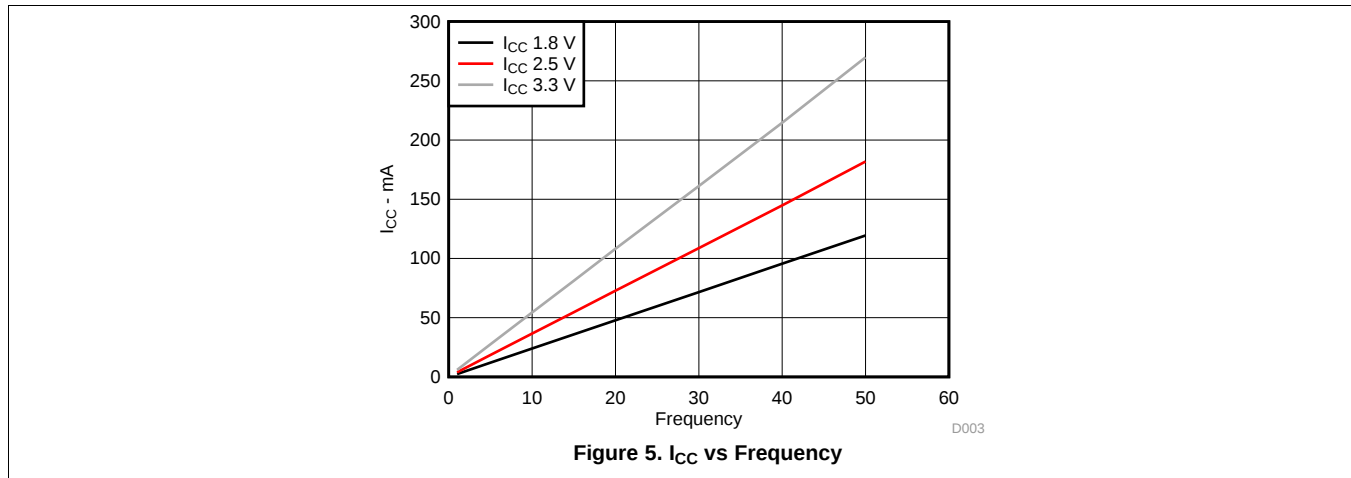
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

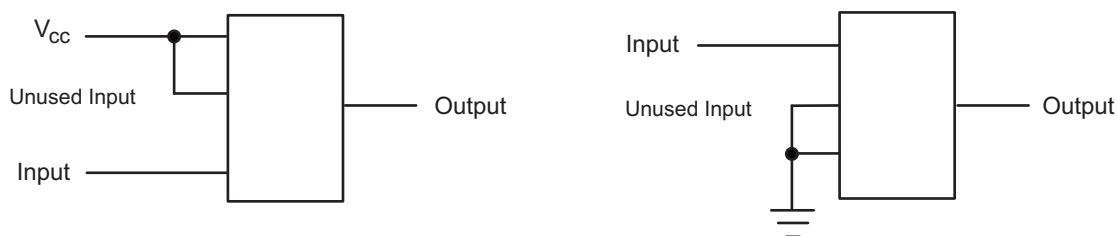
## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 6](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 12.2 Layout Example



**Figure 6. Layout Diagram**

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS       | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LVC541A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74LVC541A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                   | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------------------------|-------------------------|
| 5962-9759501Q2A   | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>9759501Q2A<br>SNJ54LVC<br>541AFK | <a href="#">Samples</a> |
| 5962-9759501QRA   | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9759501QR<br>A<br>SNJ54LVC541AJ      | <a href="#">Samples</a> |
| 5962-9759501QSA   | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9759501QS<br>A<br>SNJ54LVC541AW      | <a href="#">Samples</a> |
| SN74LVC541ADBLE   | OBSOLETE      | SSOP         | DB                 | 20   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |                                           |                         |
| SN74LVC541ADBR    | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541ADBRG4  | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541ADGVR   | ACTIVE        | TVSOP        | DGV                | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541ADGVRE4 | ACTIVE        | TVSOP        | DGV                | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541ADGVRG4 | ACTIVE        | TVSOP        | DGV                | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541ADW     | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC541A                                   | <a href="#">Samples</a> |
| SN74LVC541ADWG4   | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC541A                                   | <a href="#">Samples</a> |
| SN74LVC541ADWR    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC541A                                   | <a href="#">Samples</a> |
| SN74LVC541ADWRE4  | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC541A                                   | <a href="#">Samples</a> |
| SN74LVC541ANSR    | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LVC541A                                   | <a href="#">Samples</a> |
| SN74LVC541APW     | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541APWE4   | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                   | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------------------------|-------------------------|
| SN74LVC541APWG4   | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541APWLE   | OBSOLETE      | TSSOP        | PW                 | 20   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |                                           |                         |
| SN74LVC541APWR    | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541APWRE4  | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541APWRG4  | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541APWT    | ACTIVE        | TSSOP        | PW                 | 20   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541ARGYR   | ACTIVE        | VQFN         | RGY                | 20   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SN74LVC541ARGYRG4 | ACTIVE        | VQFN         | RGY                | 20   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | LC541A                                    | <a href="#">Samples</a> |
| SNJ54LVC541AFK    | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>9759501Q2A<br>SNJ54LVC<br>541AFK | <a href="#">Samples</a> |
| SNJ54LVC541AJ     | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9759501QR<br>A<br>SNJ54LVC541AJ      | <a href="#">Samples</a> |
| SNJ54LVC541AW     | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9759501QS<br>A<br>SNJ54LVC541AW      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC541A, SN74LVC541A :**

- Catalog: [SN74LVC541A](#)
- Automotive: [SN74LVC541A-Q1](#), [SN74LVC541A-Q1](#)
- Enhanced Product: [SN74LVC541A-EP](#), [SN74LVC541A-EP](#)
- Military: [SN54LVC541A](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- 
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
  - Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC541ADBR  | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVC541ADGVR | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC541ADWR  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LVC541ANSR  | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.2     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LVC541APWR  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVC541APWT  | TSSOP        | PW              | 20   | 250  | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LVC541ARGYR | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.8     | 4.8     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC541ADBR  | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LVC541ADGVR | TVSOP        | DGV             | 20   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LVC541ADWR  | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVC541ANSR  | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVC541APWR  | TSSOP        | PW              | 20   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LVC541APWT  | TSSOP        | PW              | 20   | 250  | 367.0       | 367.0      | 38.0        |
| SN74LVC541ARGYR | VQFN         | RGY             | 20   | 3000 | 367.0       | 367.0      | 35.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

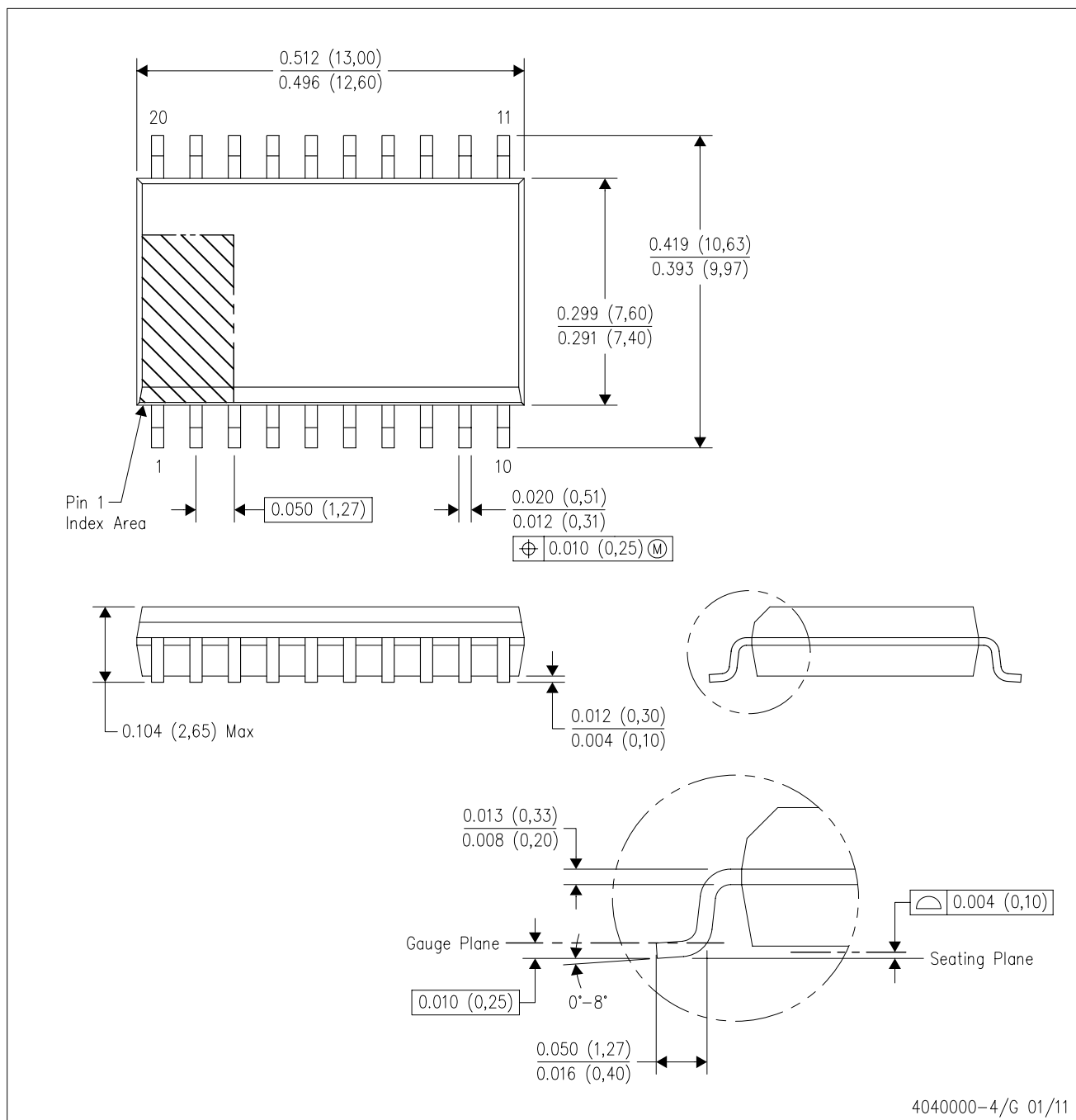
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

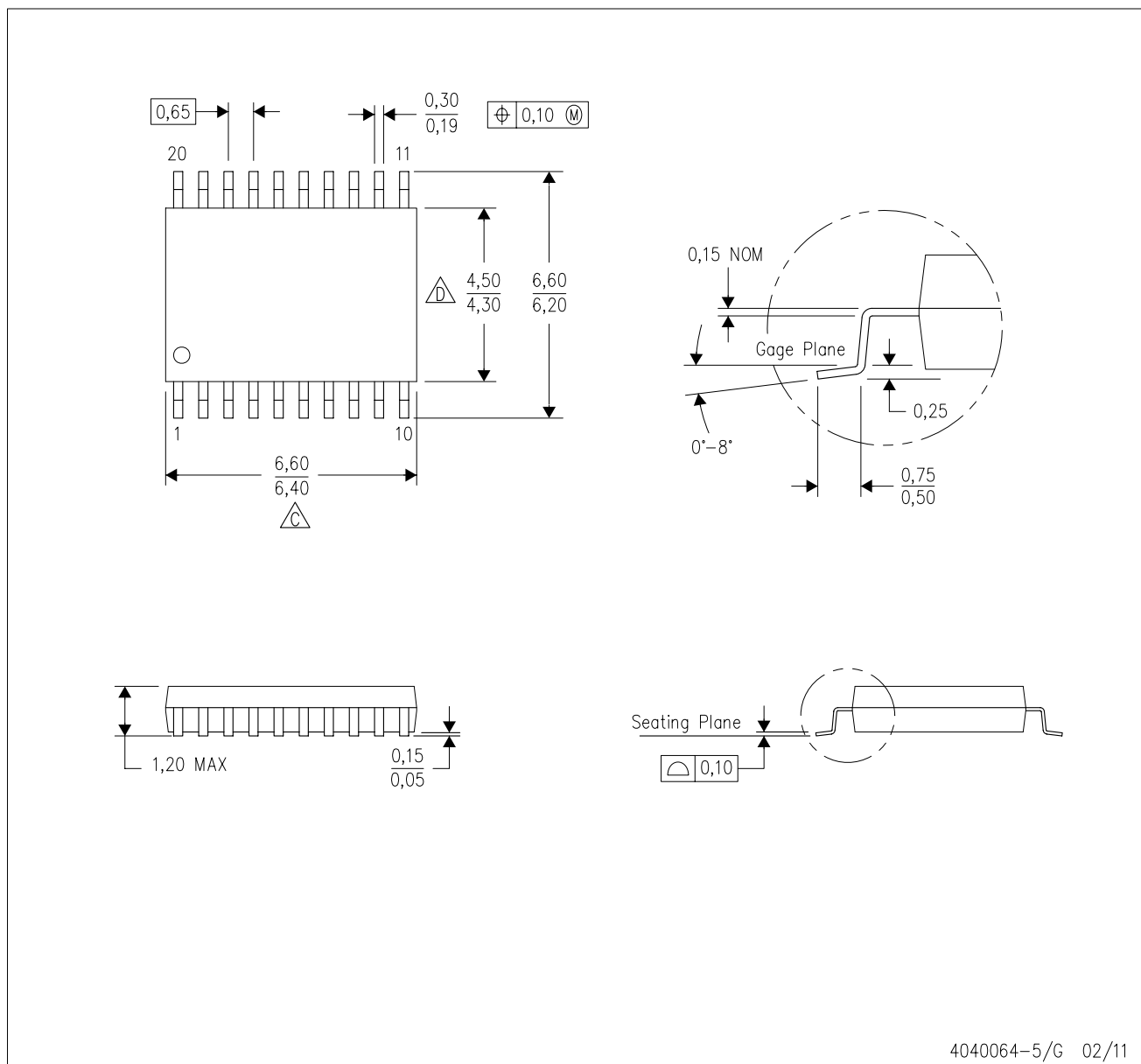
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



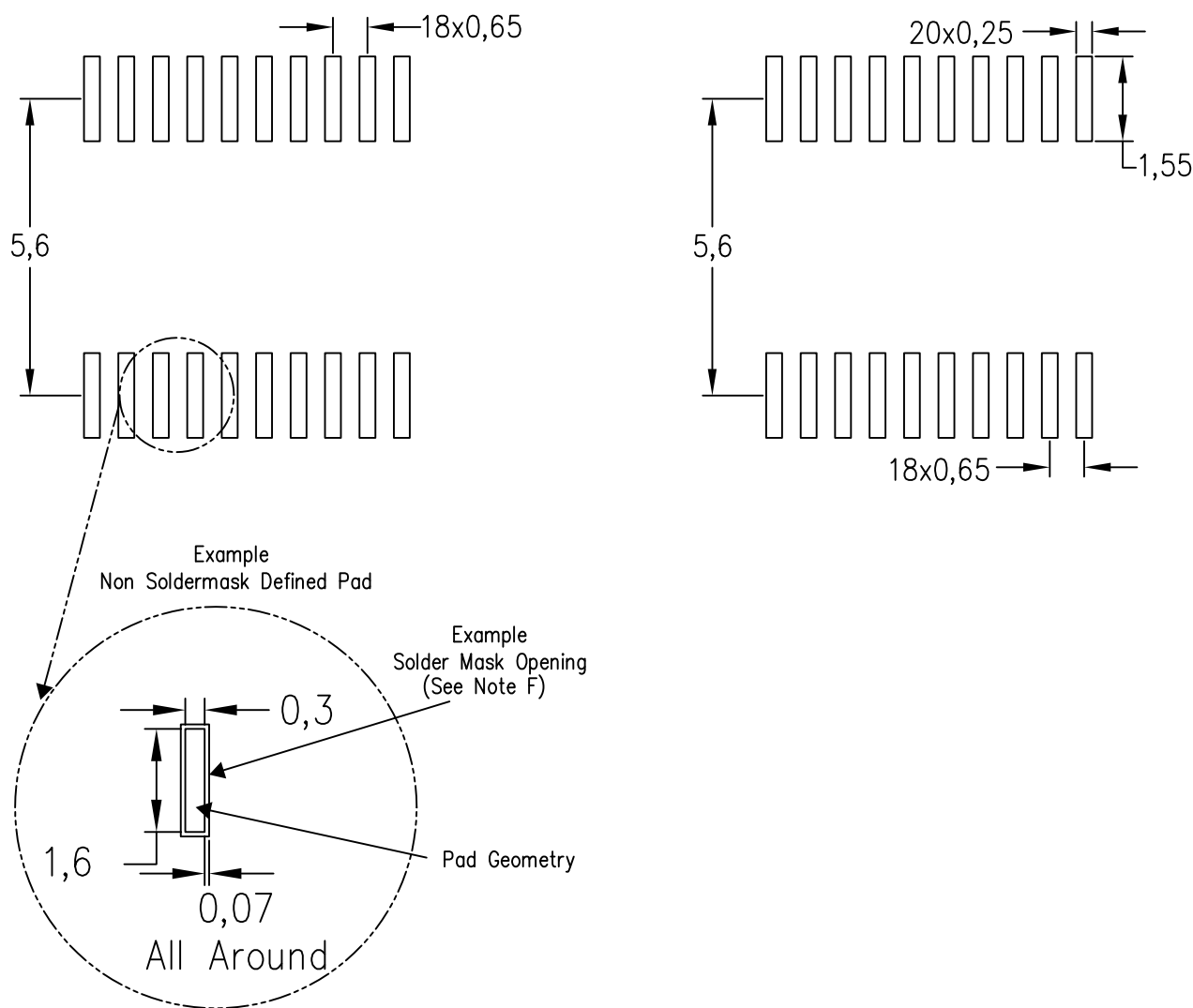
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).



4211284-5/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

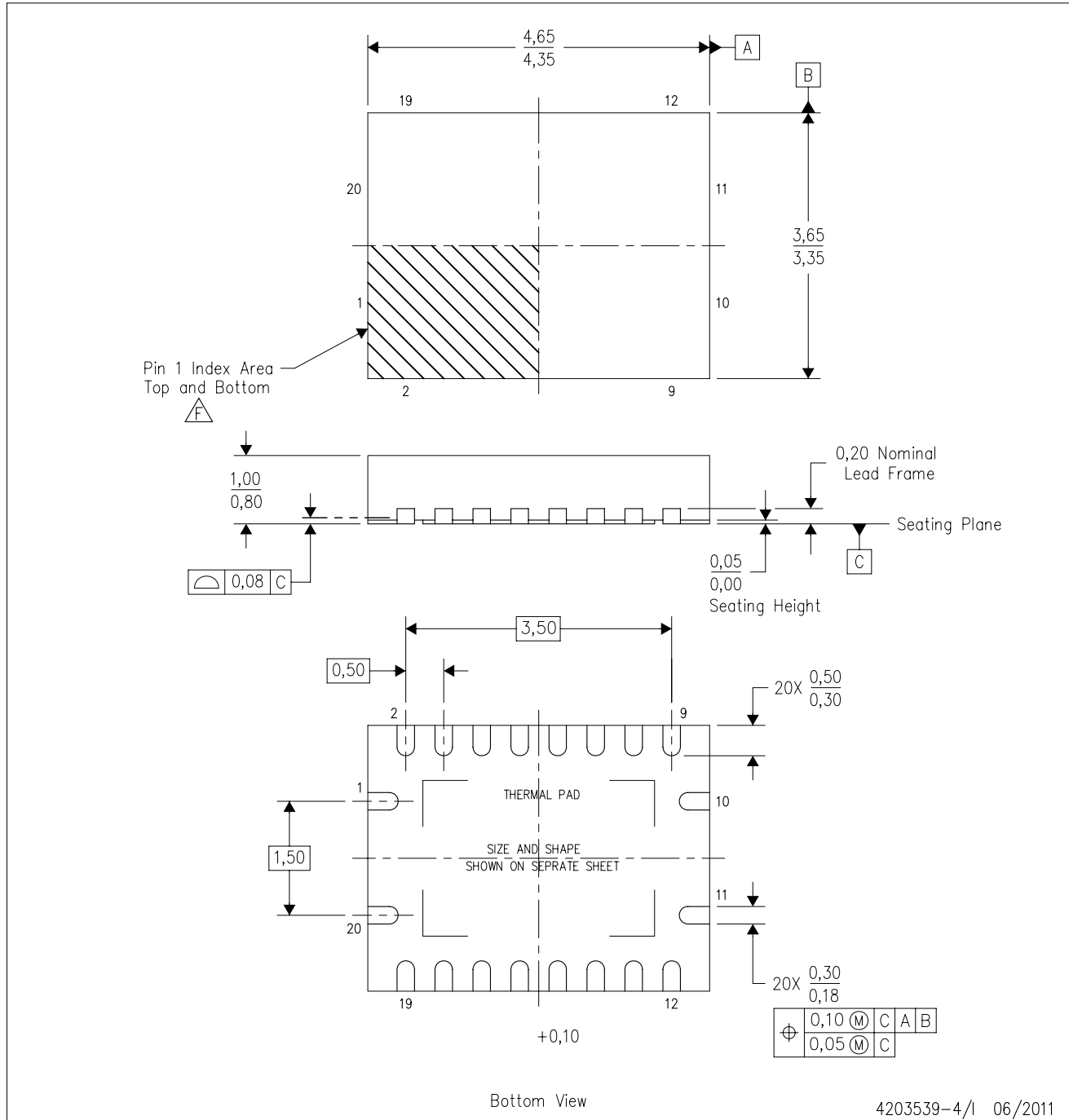
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N20)

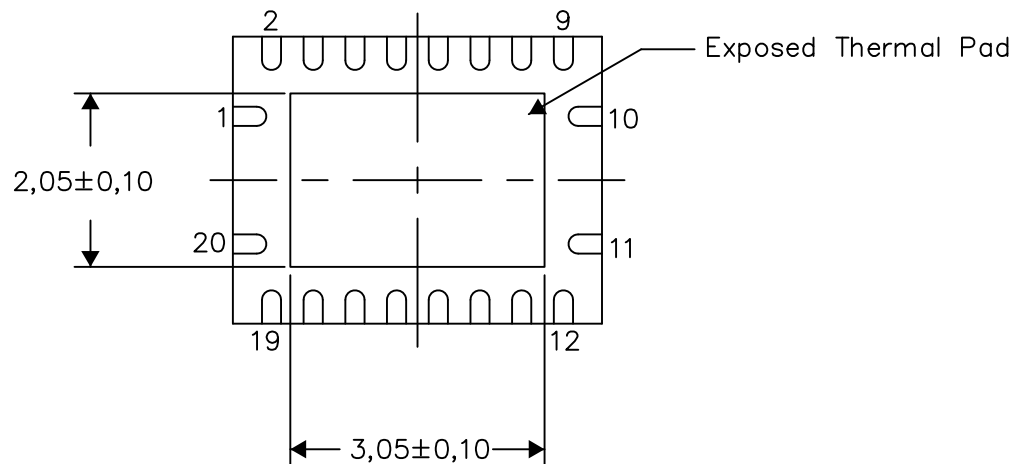
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

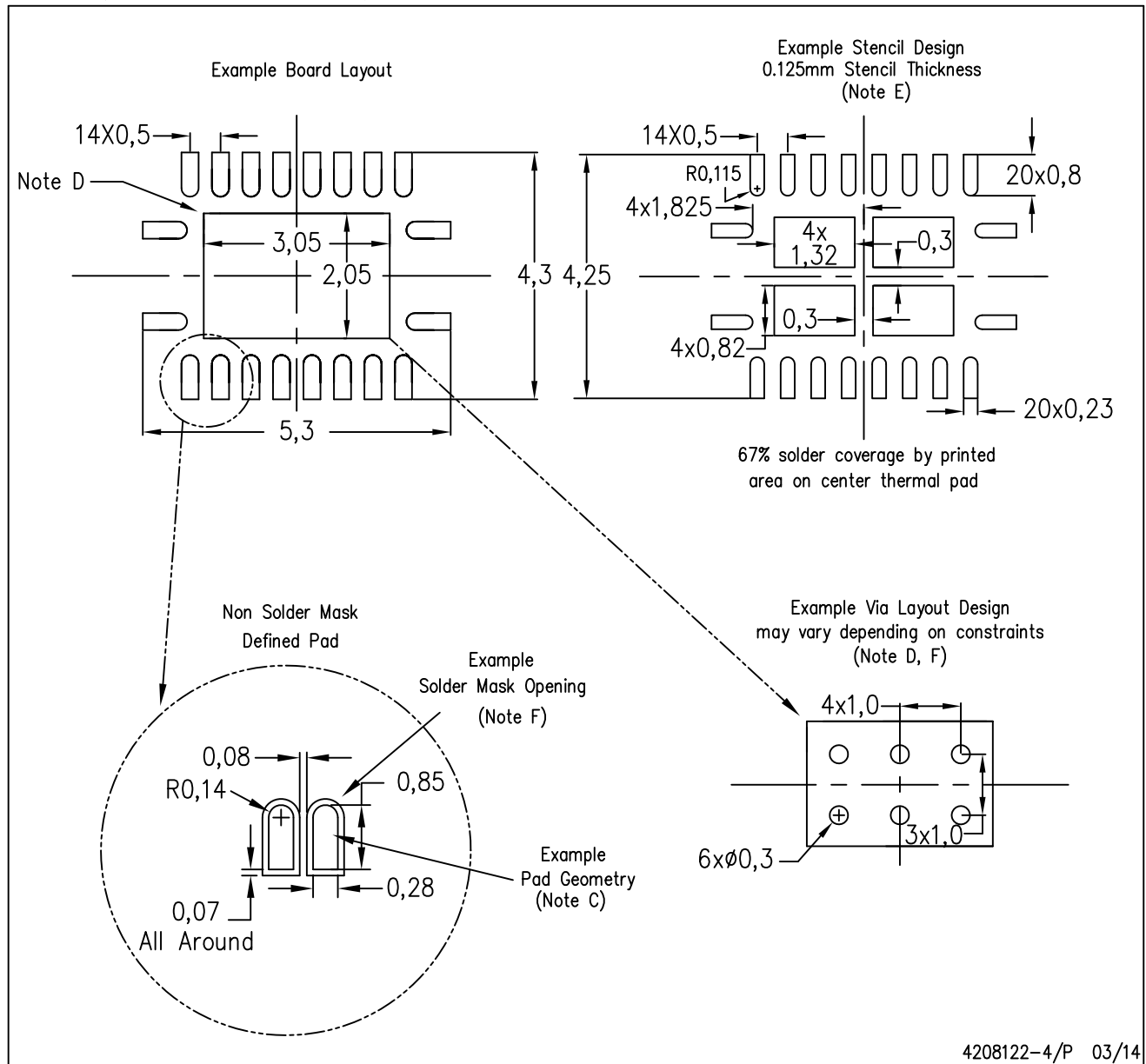
Exposed Thermal Pad Dimensions

4206353-4/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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