# SN74HCS10 Triple 3-Input NAND Gates with Schmitt-Trigger Inputs

## 1 Features

- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical $I_{CC}$ of 100 nA
  - Typical input leakage current of ±100 nA
- ±7.8-mA output drive at 5 V
- Extended ambient temperature range: –40°C to +125°C, $T_A$

## 2 Applications

- Alarm / tamper detect circuit
- S-R latch

## 3 Description

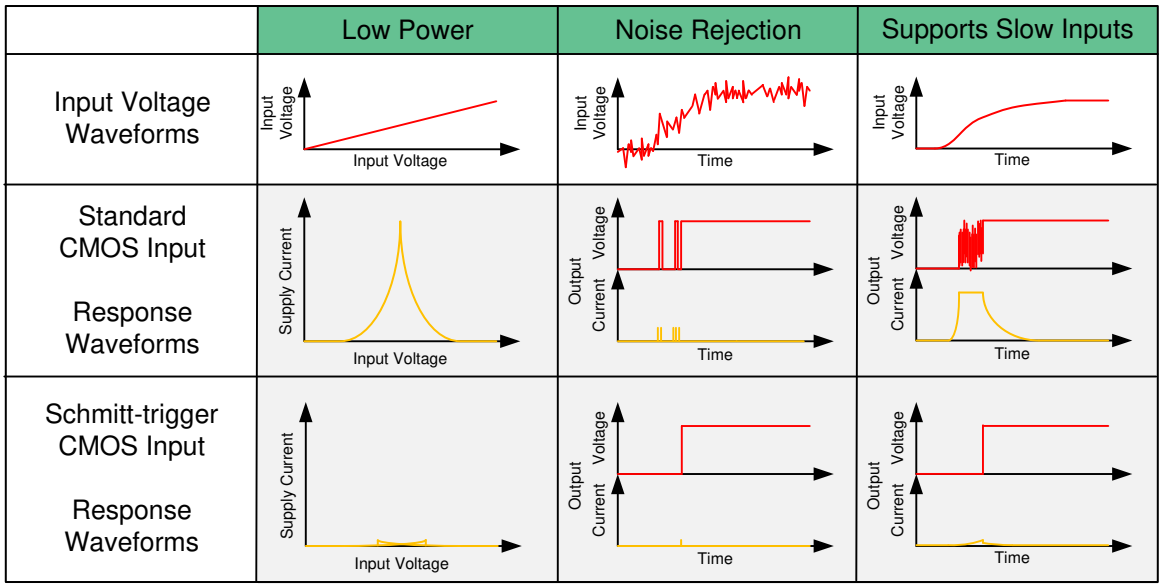
This device contains three independent 3-input NAND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = $\overline{A \bullet B \bullet C}$ in positive logic.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74HCS10DR | SOIC (14) | 8.70 mm × 3.90 mm |
| SN74HCS10PWR | TSSOP (14) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Benefits of Schmitt-trigger Inputs**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features** ... 1
**2 Applications** ... 1
**3 Description** ... 1
**4 Revision History** ... 2
**5 Pin Configuration and Functions** ... 3
**6 Specifications** ... 3
6.1 Absolute Maximum Ratings ... 3
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 4
6.6 Switching Characteristics ... 5
6.7 Typical Characteristics ... 5
**7 Parameter Measurement Information** ... 6
**8 Detailed Description** ... 7
8.1 Overview ... 7
8.2 Functional Block Diagram ... 7
8.3 Feature Description ... 7
8.4 Device Functional Modes ... 8
**9 Application and Implementation** ... 9
9.1 Application Information ... 9
9.2 Typical Application ... 9
**10 Power Supply Recommendations** ... 12
**11 Layout** ... 12
11.1 Layout Guidelines ... 12
11.2 Layout Example ... 12
**12 Device and Documentation Support** ... 13
12.1 Documentation Support ... 13
12.2 Related Links ... 13
12.3 Community Resources ... 13
12.4 Trademarks ... 13
12.5 Electrostatic Discharge Caution ... 13
12.6 Glossary ... 13
**13 Mechanical, Packaging, and Orderable Information** ... 13

## 4 Revision History

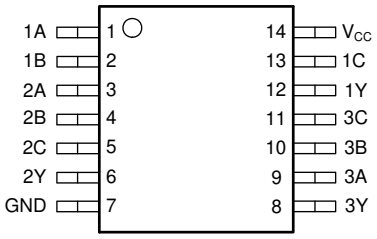
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (January 2020) to Revision A | Page |
|---|---|
| • Added D package to Device Information table | 1 |
| • Added D package information to *Pin Configuration and Functions* | 3 |
| • Added D package column to *Thermal Information* table | 4 |


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# 5 Pin Configuration and Functions

**D or PW Package**
**14-Pin SOIC or TSSOP**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | Input | Channel 1, Input A |
| 1B | 2 | Input | Channel 1, Input B |
| 2A | 3 | Input | Channel 2, Input A |
| 2B | 4 | Input | Channel 2, Input B |
| 2C | 5 | Input | Channel 2, Input C |
| 2Y | 6 | Output | Channel 2, Output Y |
| GND | 7 | — | Ground |
| 3Y | 8 | Output | Channel 3, Output Y |
| 3A | 9 | Input | Channel 3, Input A |
| 3B | 10 | Input | Channel 3, Input B |
| 3C | 11 | Input | Channel 3, Input C |
| 1Y | 12 | Output | Channel 1, Output Y |
| 1C | 13 | Input | Channel 1, Input C |
| $V_{CC}$ | 14 | — | Positive Supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_J$ | Junction temperature(3) | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

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## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2 | 5 | 6 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | V |
| $T_A$ | Ambient temperature | –55 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC | | SN74HCS10 | | UNIT |
|---|---|---|---|---|
| | | PW (TSSOP) | D (SOIC) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 151.7 | 133.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 79.4 | 89.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 94.7 | 89.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 25.2 | 45.5 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 94.1 | 89.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive switching threshold | | | 2 V | 0.7 | | 1.5 | V |
| | | | | 4.5 V | 1.7 | | 3.15 | |
| | | | | 6 V | 2.1 | | 4.2 | |
| $V_{T-}$ | Negative switching threshold | | | 2 V | 0.3 | | 1.0 | V |
| | | | | 4.5 V | 0.9 | | 2.2 | |
| | | | | 6 V | 1.2 | | 3.0 | |
| $\Delta V_T$ | Hysteresis ($V_{T+}$ - $V_{T-}$) | | | 2 V | 0.2 | | 1.0 | V |
| | | | | 4.5 V | 0.4 | | 1.4 | |
| | | | | 6 V | 0.6 | | 1.6 | |
| $V_{OH}$ | High-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 µA | 2 V to 6 V | $V_{CC}$ – 0.1 | $V_{CC}$ – 0.002 | | V |
| | | | $I_{OH}$ = -6 mA | 4.5 V | 4.0 | 4.3 | | |
| | | | $I_{OH}$ = -7.8 mA | 6 V | 5.4 | 5.75 | | |
| $V_{OL}$ | Low-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V to 6 V | | 0.002 | 0.1 | V |
| | | | $I_{OL}$ = 6 mA | 4.5 V | | 0.18 | 0.30 | |
| | | | $I_{OL}$ = 7.8 mA | 6 V | | 0.22 | 0.33 | |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or 0 | | 6 V | | ±100 | ±1000 | nA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or 0, $I_O$ = 0 | | 6 V | | 0.1 | 2 | µA |
| $C_i$ | Input capacitance | | | 2 V to 6 V | | | 5 | pF |


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## Electrical Characteristics (continued)

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | No load | 2 V to 6 V | | 10 | | pF |

## 6.6 Switching Characteristics

$C_L$ = 50 pF; over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See Parameter Measurement Information.

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay | A or B or C | Y | 2 V | | 14 | 40 | ns |
| | | | | 4.5 V | | 6 | 17 | |
| | | | | 6 V | | 5 | 16 | |
| $t_t$ | Transition-time | | Y | 2 V | | 9 | 16 | ns |
| | | | | 4.5 V | | 5 | 9 | |
| | | | | 6 V | | 4 | 8 | |

## 6.7 Typical Characteristics

$T_A$ = 25°C

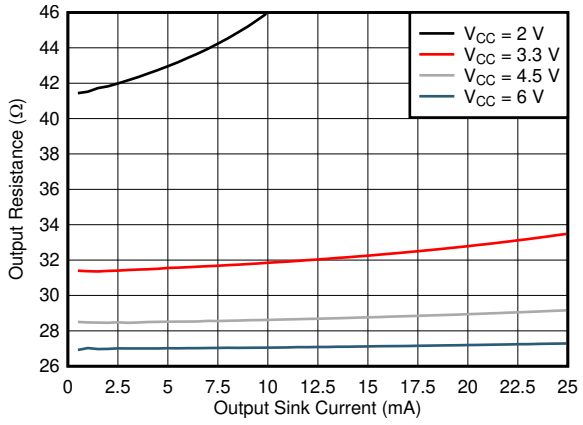



**Figure 1. Output driver resistance in Low state**

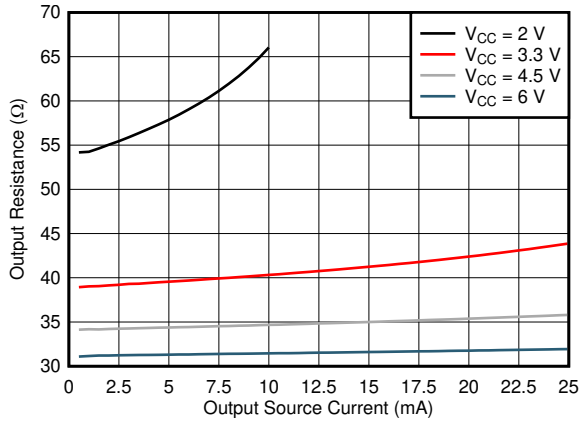



**Figure 2. Output driver resistance in High state**

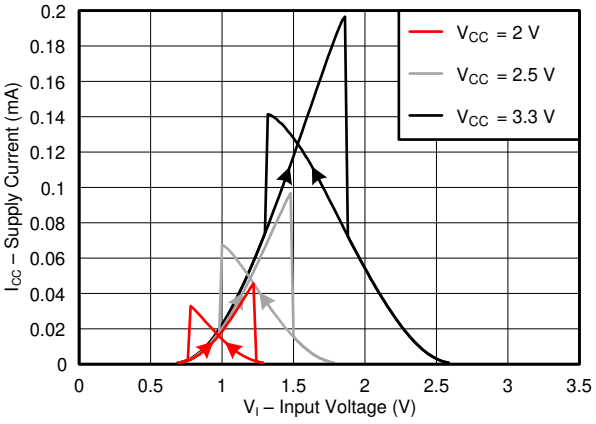



**Figure 3. Typical supply current versus input voltage across common supply values (2 V to 3.3 V)**

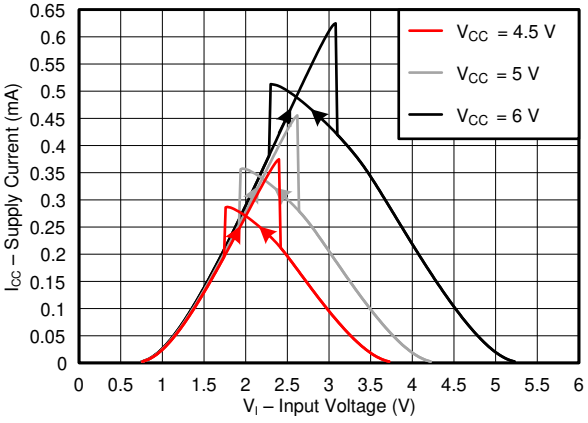
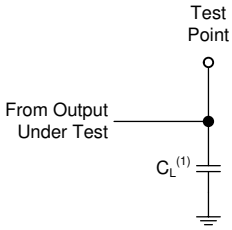



**Figure 4. Typical supply current versus input voltage across common supply values (4.5 V to 6 V)**

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## 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 2.5 ns.
- The outputs are measured one at a time, with one input transition per measurement.




$C_L$ = 50 pF and includes probe and jig capacitance.

**Figure 5. Load Circuit**

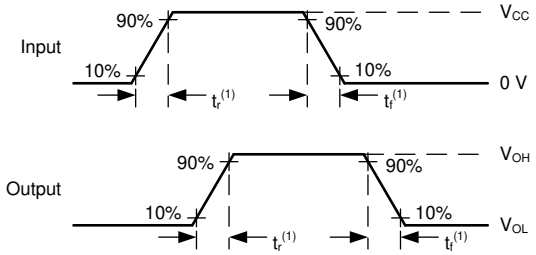
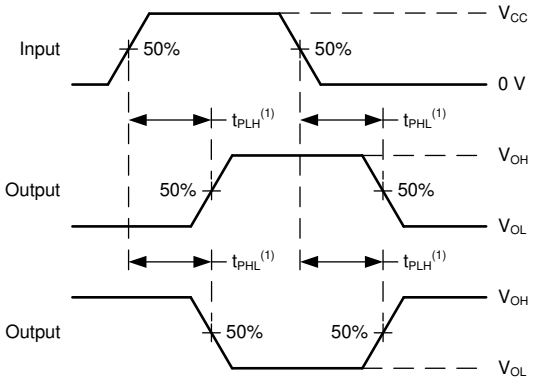



**Figure 6. Voltage Waveforms Transition Times**




The maximum between $t_{PLH}$ and $T_{PHL}$ is used for $t_{pd}$.

**Figure 7. Voltage Waveforms Propagation Delays**

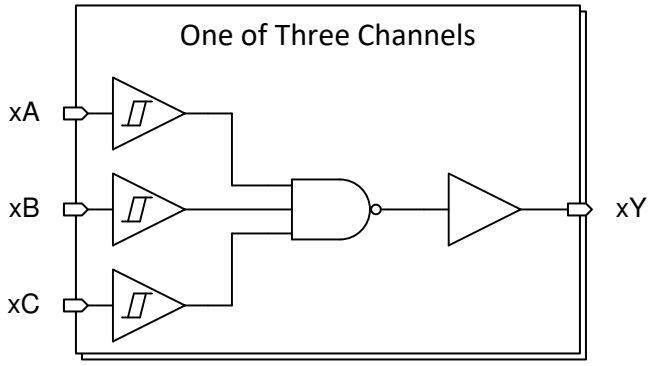

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# 8 Detailed Description

## 8.1 Overview

This device contains three independent 3-input NAND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A ● B ● C in positive logic.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

### 8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 8.

**CAUTION**

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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## Feature Description (continued)

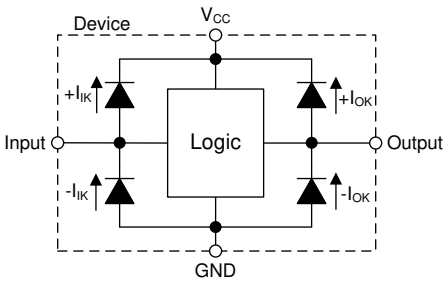



**Figure 8. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**Table 1. Function Table**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | L |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |


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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

In this application, two 3-input NAND gates are used to create an active-low SR latch as shown in Figure 9. The additional gate can be used elsewhere in the system, or the inputs can be grounded and left unused.

The SN74HCS10 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

The inputs of this active-low SR latch can often be driven by open-drain outputs which can produce slow input transition rates when they transition from LOW to Hi-Z. This makes the SN74HCS10 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

## 9.2 Typical Application

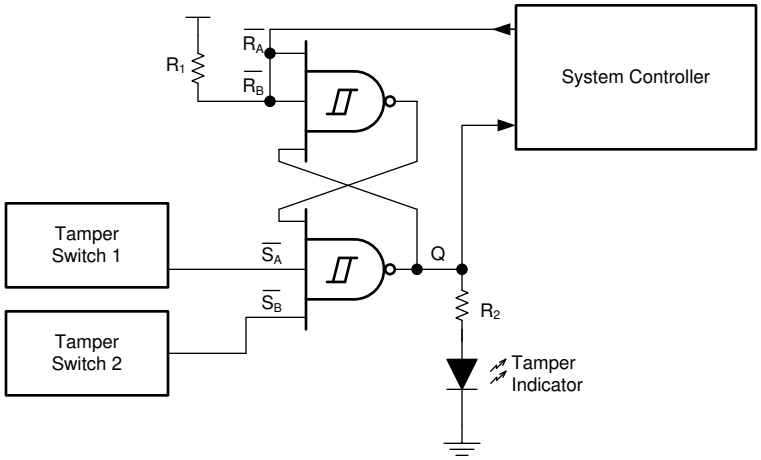



**Figure 9. Typical application block diagram**

### 9.2.1 Design Requirements

- All signals in the system operate at 5 V
- Avoid unstable state by not having LOW signals on both $\overline{R}$ and $\overline{S}$ inputs
- Q output is HIGH when any $\overline{S}$ input is LOW
  - Q output remains HIGH until any $\overline{R}$ input is LOW

#### *9.2.1.1 Power Considerations*

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS10 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The SN74HCS10 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF.

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## Typical Application (continued)

Total power consumption can be calculated using the information provided in CMOS Power Consumption and $C_{pd}$ Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

**CAUTION**

The maximum junction temperature, $T_J$(max) listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 9.2.1.2 Input Considerations

Input signals must cross $V_{t-}$(min) to be considered a logic LOW, and $V_{t+}$(max) to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS10, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS10 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_T$(min) in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

#### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*. The plots in and provide a typical relationship between output voltage and current for this device.

Unused outputs can be left floating.

Refer to *Feature Description* for additional information regarding the outputs for this device.


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## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout*.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS10 to the receiving device.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / 25 mA) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

### 9.2.3 Application Curves

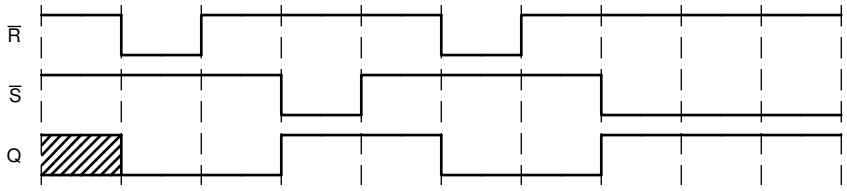



**Figure 10. Application timing diagram**

# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Figure 11*.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or VCC, whichever makes more sense for the logic function or is more convenient.

## 11.2 Layout Example

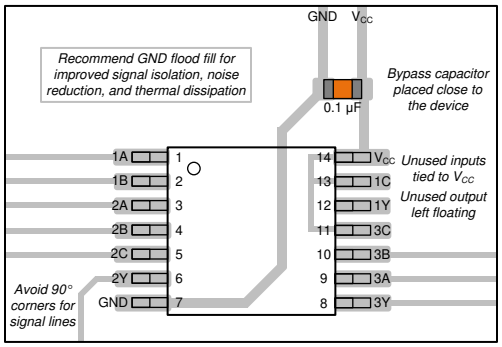



**Figure 11. Example layout for the SN74HCS10**


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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing with Logic

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

## 12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCS10DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | HCS10 | Samples |
| SN74HCS10PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | HCS10 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74HCS10 :**

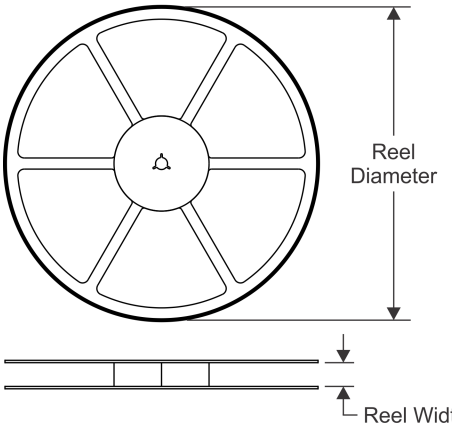
- Automotive: SN74HCS10-Q1

NOTE: Qualified Version Definitions:

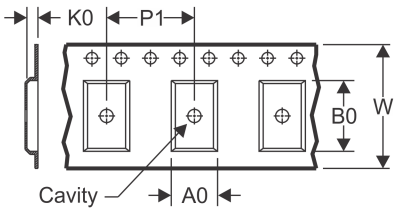
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

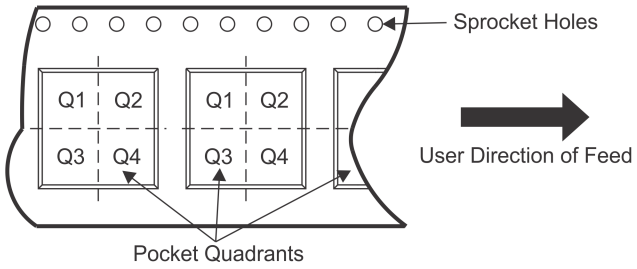



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

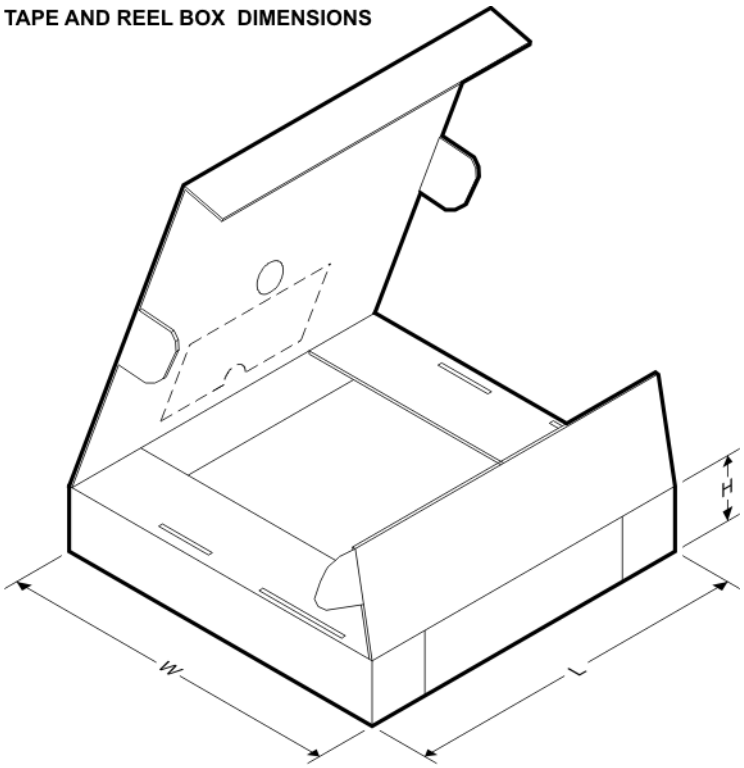
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCS10DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCS10DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.6 | 9.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCS10PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCS10PWR | TSSOP | PW | 14 | 2000 | 330.0 | 16.4 | 6.8 | 5.4 | 1.6 | 8.0 | 16.0 | Q1 |

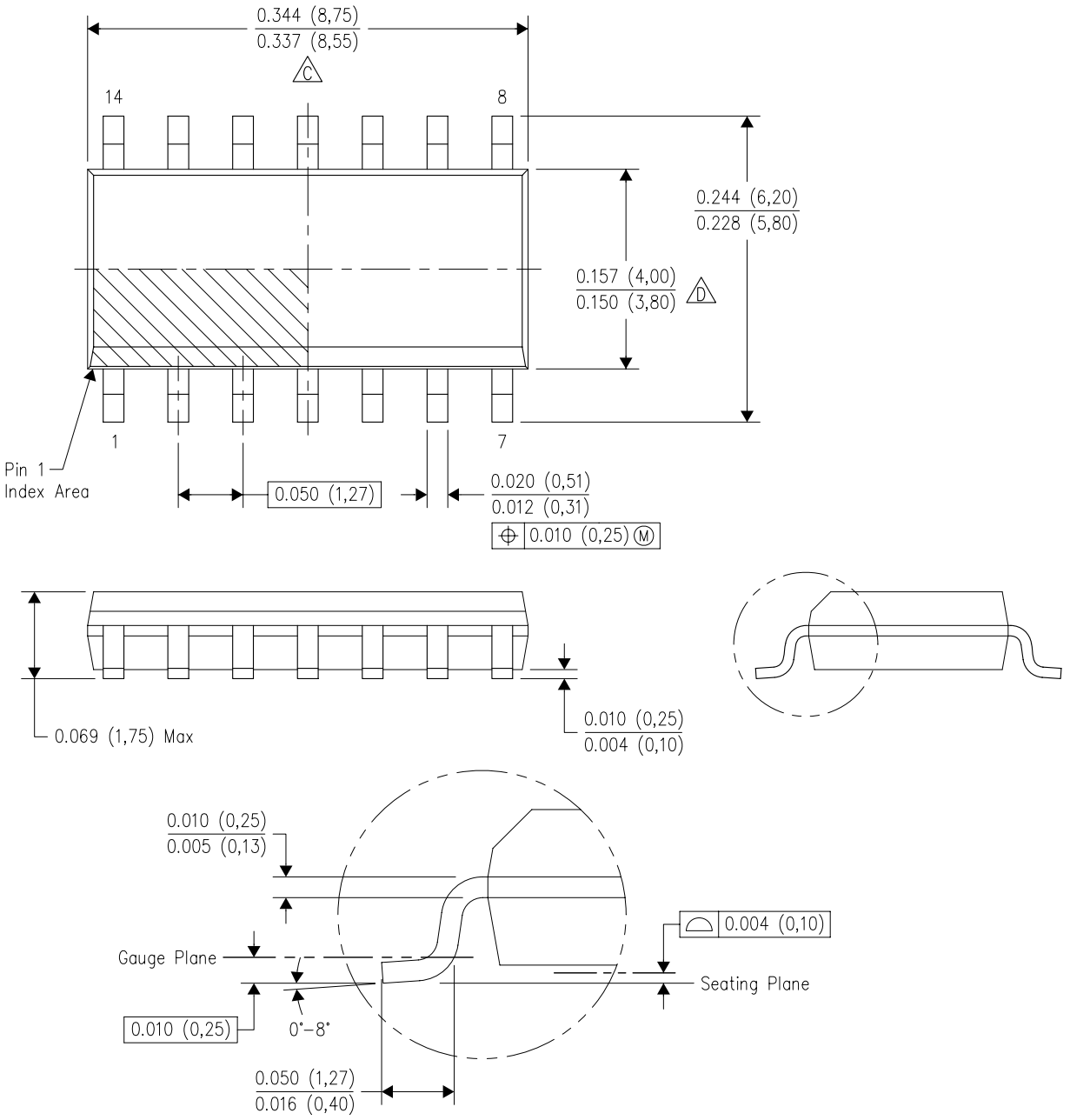
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HCS10DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74HCS10DR | SOIC | D | 14 | 2500 | 366.0 | 364.0 | 50.0 |
| SN74HCS10PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74HCS10PWR | TSSOP | PW | 14 | 2000 | 366.0 | 364.0 | 50.0 |

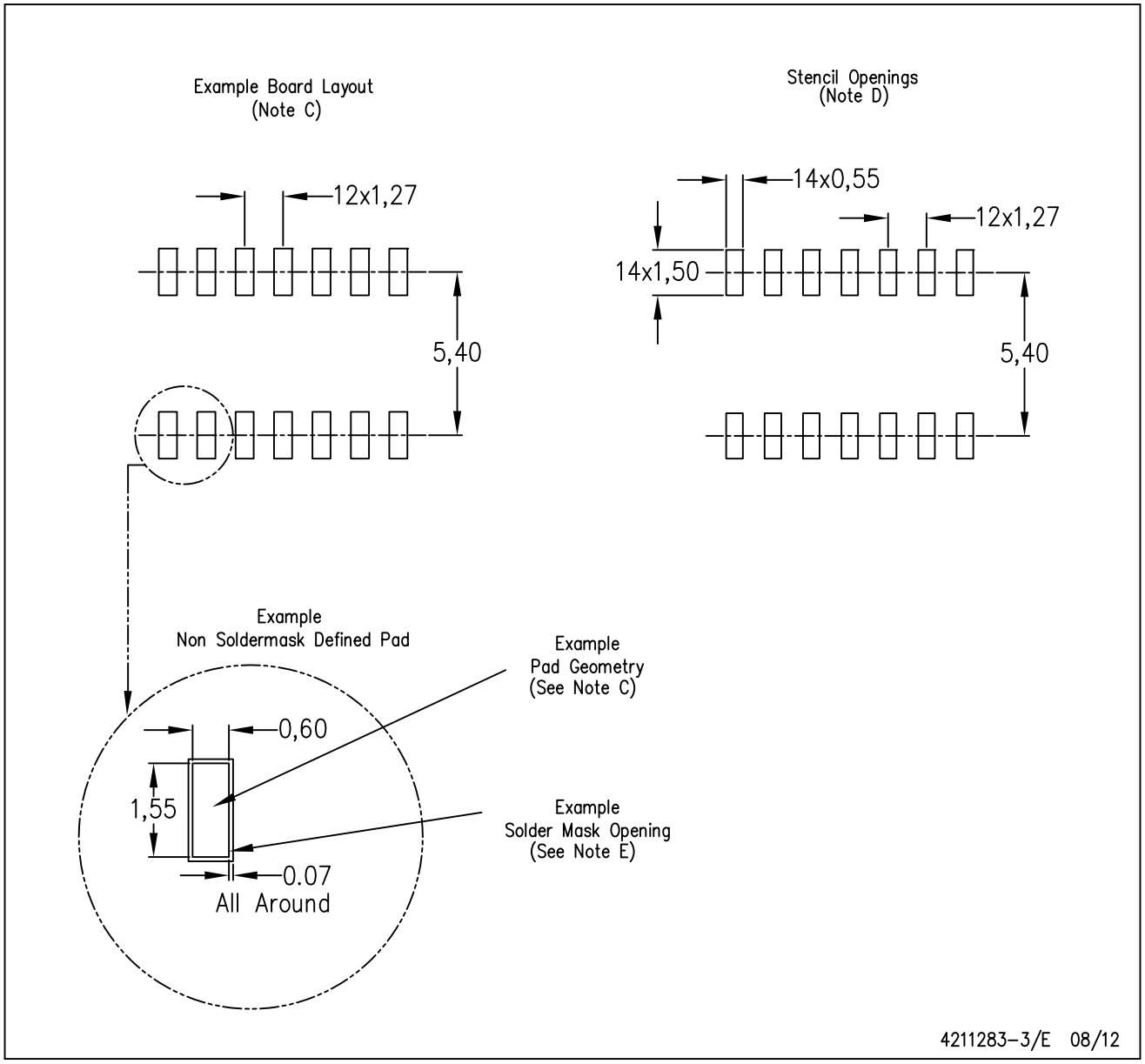
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

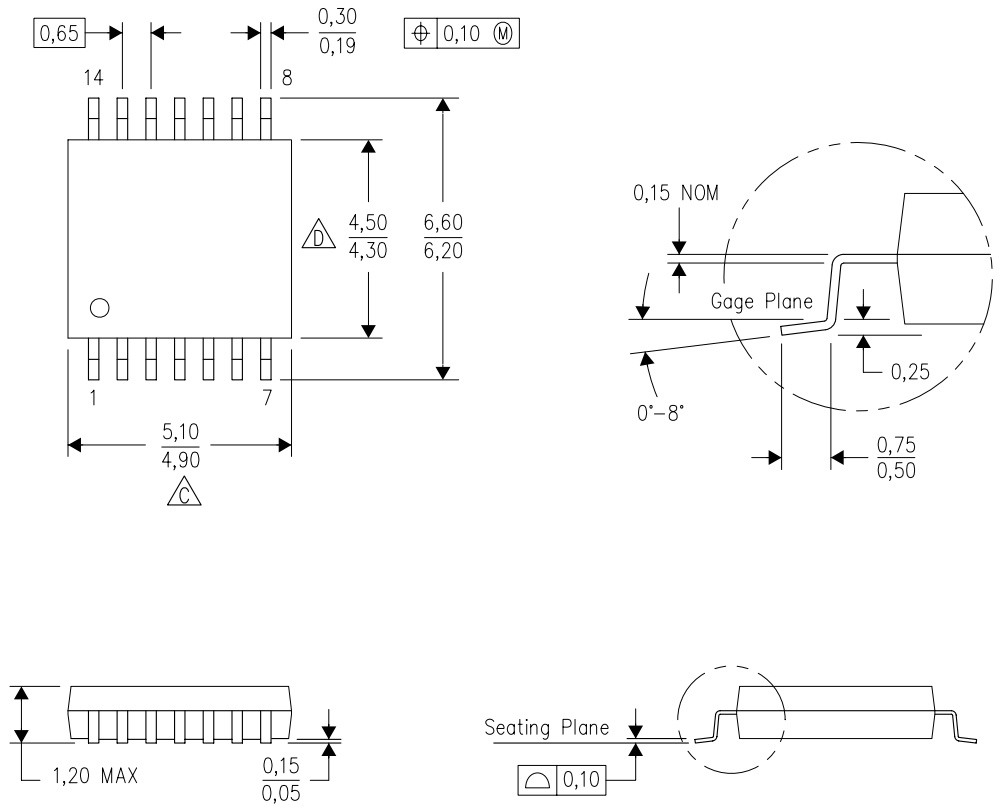
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

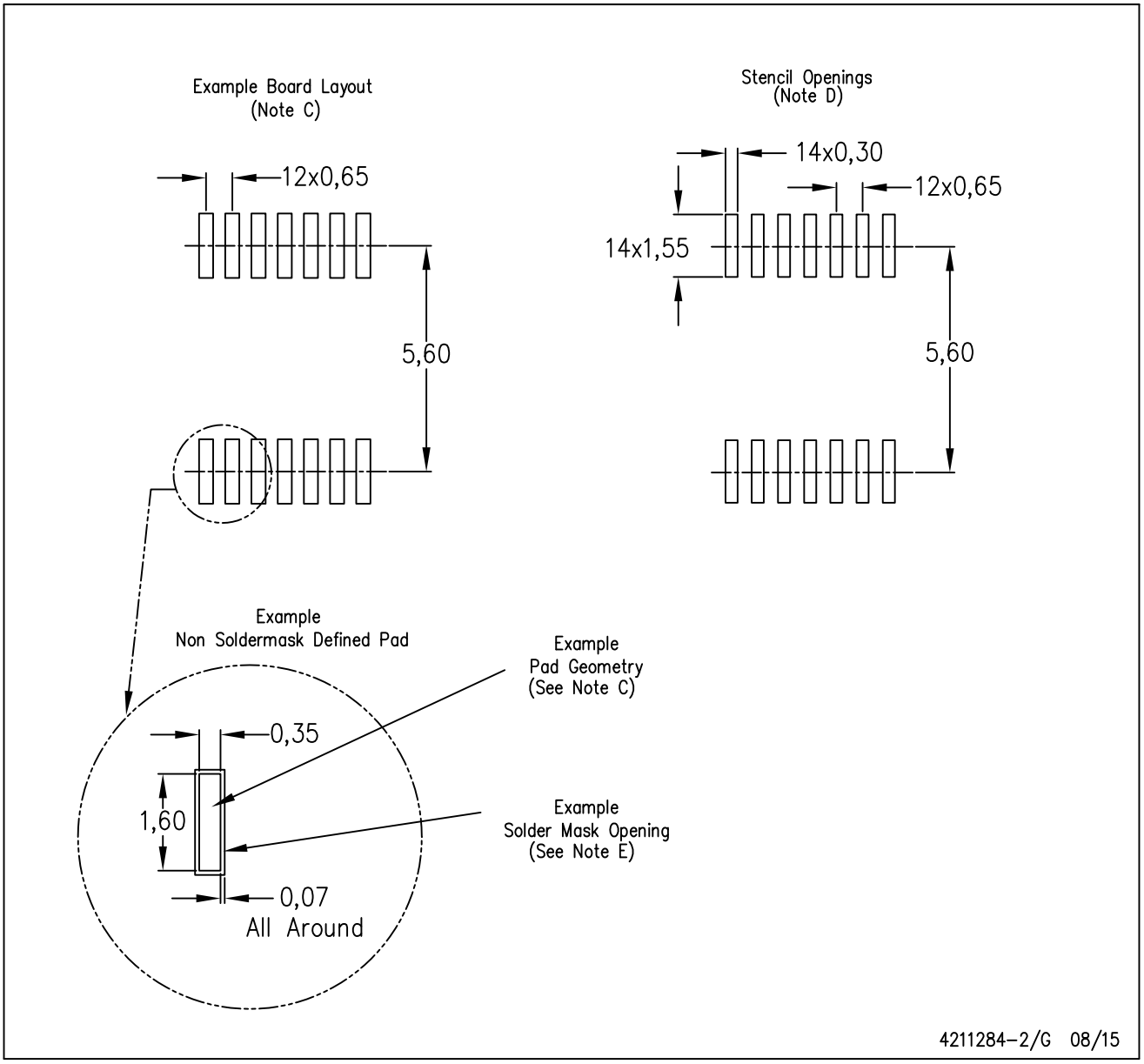
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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