SN74AXC2T45-Q1 2-Bit Translating Transceiver with Configurable Level-Shifting

1 Features

- AEC-Q100 automotive qualified
- Fully Configurable Dual-Rail Design Allows Each Port to Operate With a Power Supply Range From 0.65 V to 3.6 V
- Operating Temperature From –40°C to +125°C
- Glitch-free Power Supply Sequencing
- Up to 380 Mbps Support When Translating from 1.8 V to 3.3 V
- V_{CC} Isolation Feature
  - If Either V_{CC} Input is Below 100 mV, All I/Os Outputs are Disabled and Become High-Impedance
- I_{off} Supports Partial-Power-Down Mode Operation
- Compatible With AVC Family Level Shifters
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model
  - 1000-V Charged-Device Model

2 Applications

- Enterprise and Communications
- Industrial
- Personal Electronics
- Wireless Infrastructure
- Building Automation
- Point of Sale

3 Description

The SN74AXC2T45-Q1 is a two-bit noninverting bus transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCA} and V_{CCB} supplies as low as 0.65 V. The A port is designed to track V_{CCA}, which accepts any supply voltage from 0.65 V to 3.6 V. The B port is designed to track V_{CCB}, which also accepts any supply voltage from 0.65 V to 3.6 V. Additionally the SN74AXC2T45-Q1 is compatible with a single-supply system.

The SN74AXC2T45-Q1 device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level of the direction-control input (DIR). The SN74AXC2T45-Q1 device is designed so the control pin (DIR) is referenced to V_{CCA}.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specific voltage while the device is powered down.

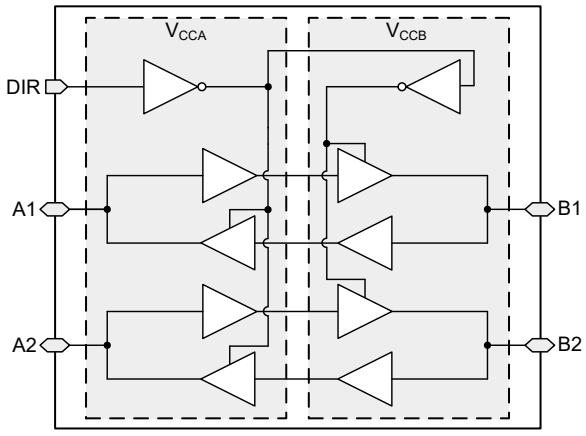
The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} is less than 100 mV, both I/O ports enter a high-impedance state by disabling their outputs.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AXC2T45DCU-Q1	VSSOP (8)	2.30 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Pin Configuration and Functions....3
6 Specifications....4
6.1 Absolute Maximum Ratings....4
6.2 ESD Ratings....4
6.3 Recommended Operating Conditions....5
6.4 Thermal Information....5
6.5 Electrical Characteristics....6
6.6 Switching Characteristics, V_{CCA} = 0.7 ± 0.05 V....7
6.7 Switching Characteristics, V_{CCA} = 0.8 ± 0.04 V....8
6.8 Switching Characteristics, V_{CCA} = 0.9 ± 0.045 V....9
6.9 Switching Characteristics, V_{CCA} = 1.2 ± 0.1 V....10
6.10 Switching Characteristics, V_{CCA} = 1.5 ± 0.1 V....11
6.11 Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V....12
6.12 Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V....13
6.13 Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V....14
6.14 Operating Characteristics: T_A = 25°C....15
6.15 Typical Characteristics....16
7 Parameter Measurement Information....17
7.1 Load Circuit and Voltage Waveforms....17
8 Detailed Description....19
8.1 Overview....19
8.2 Functional Block Diagram....19
8.3 Feature Description....19
8.4 Device Functional Modes....20
9 Application and Implementation....21
9.1 Application Information....21
9.2 Typical Application....21
10 Power Supply Recommendations....23
11 Layout....23
11.1 Layout Guidelines....23
11.2 Layout Example....23
12 Device and Documentation Support....24
12.1 Documentation Support....24
12.2 Receiving Notification of Documentation Updates....24
12.3 Support Resources....24
12.4 Trademarks....24
12.5 Electrostatic Discharge Caution....24
12.6 Glossary....24
13 Mechanical, Packaging, and Orderable Information....25
13.1 Tape and Reel Information....29

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2021	*	Initial Release

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5 Pin Configuration and Functions

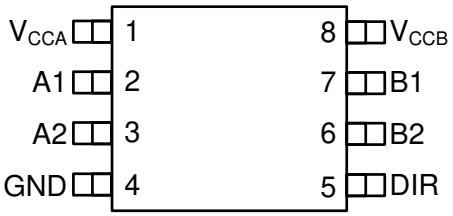


Figure 5-1. DCU Package 8-Pin VSSOP Top View

Table 5-1. Pin Functions

PIN	NO.	DESCRIPTION
NAME	DCU	
V_{CCA}	1	A-port power supply voltage. 0.65 V ≤ V_{CCA} ≤ 3.6 V
A1	2	Input/output A1. Referenced to V_{CCA}.
A2	3	Input/output A2. Referenced to V_{CCA}.
GND	4	Ground
DIR	5	Direction-control in for both ports. Referenced to V_{CCA}
B2	6	Input/output B2. Referenced to V_{CCB}.
B1	7	Input/output B1. Referenced to V_{CCB}.
V_{CCB}	8	B-port power supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNITS
V_{CCA}	Supply voltage A		–0.5	4.2	V
V_{CCB}	Supply voltage B		–0.5	4.2	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.2	V
		I/O Ports (B Port)	–0.5	4.2	
		Control Inputs	–0.5	4.2	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.2	V
		B Port	–0.5	4.2	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.2	V
		B Port	–0.5	V_{CCB} + 0.2	
I_{IK}	Input clamp current	V_I < 0	–50		mA
I_{OK}	Output clamp current	V_O < 0	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±8000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			0.65	3.6	V
V_{CCB}	Supply voltage B			0.65	3.6	V
V_{IH}	High-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V	V_{CCI} x 0.70		
			V_{CCI} = 0.76 V - 1 V	V_{CCI} x 0.70		
			V_{CCI} = 1.1 V - 1.95 V	V_{CCI} x 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	2		
		Control Input (DIR), Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	V_{CCA} x 0.70		
			V_{CCA} = 0.76 V - 1 V	V_{CCA} x 0.70		
			V_{CCA} = 1.1 V - 1.95 V	V_{CCA} x 0.65		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	2		
V_{IL}	Low-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V		V_{CCI} x 0.30	V
			V_{CCI} = 0.76 V - 1 V		V_{CCI} x 0.30	
			V_{CCI} = 1.1 V - 1.95 V		V_{CCI} x 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control Input (DIR), Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		V_{CCA} x 0.30	
			V_{CCA} = 0.76 V - 1 V		V_{CCA} x 0.30	
			V_{CCA} = 1.1 V - 1.95 V		V_{CCA} x 0.35	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage (3)			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
$\Delta t/\Delta v$(2)	Input transition rise and fall time				10	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.

6.4 Thermal Information

THERMAL METRIC (1)		SN74AXC2T45-Q1 DCU (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	242.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	153.3	°C/W
Y_{JT}	Junction-to-top characterization parameter	38.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	152.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
						-40°C to 85°C			-40°C to 125°C			
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = -100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = -50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = -200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = -500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = -12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_I	Input leakage current	Control input (DIR):V_I = V_{CCA} or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	–0.5		0.5	–1		1	µA
		Data Inputs (Ax, Bx),V_I = V_{CCI} or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	–4		4	–8		8	µA
I_{off}	Partial power down current	A Port: V_I or V_O = 0 V - 3.6 V		0 V	0 V - 3.6 V	–4		4	–8		8	µA
		B Port: V_I or V_O = 0 V - 3.6 V		0 V - 3.6 V	0 V	–4		4	–8		8	
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			8			14	µA
				0 V	3.6 V	–2			–12			
				3.6 V	0 V			4			8	
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			8			14	µA
				0 V	3.6 V			4			8	
				3.6 V	0 V	–2			–12			
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			16			23	µA
C_i	Control Input (DIR) Capacitance	V_I = 3.3 V or GND		3.3 V	3.3 V		3.3			3.3		pF
C_{io}	Data I/O Capacitance	V_O = 1.65V DC +1 MHz -16 dBm sine wave		3.3 V	3.3 V		5.4			5.4		pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All typical data is taken at 25°C.

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6.6 Switching Characteristics, V_{CCA} = 0.7 ± 0.05 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	170	0.5	115	0.5	84	0.5	50	0.5	50	0.5	56	0.5	71	0.5	106	ns
				-40°C to 125°C	0.5	170	0.5	115	0.5	84	0.5	50	0.5	50	0.5	56	0.5	71	0.5	106	
		B	A	-40°C to 85°C	0.5	170	0.5	149	0.5	122	0.5	83	0.5	79	0.5	78	0.5	77	0.5	76	
				-40°C to 125°C	0.5	170	0.5	149	0.5	122	0.5	83	0.5	79	0.5	78	0.5	77	0.5	76	
t_{dis}	Disable time	DIR	A	-40°C to 85°C	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	ns
				-40°C to 125°C	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	0.5	140	
		DIR	B	-40°C to 85°C	0.5	143	0.5	105	0.5	84	0.5	41	0.5	39	0.5	42	0.5	56	0.5	107	
				-40°C to 125°C	0.5	143	0.5	105	0.5	84	0.5	41	0.5	39	0.5	42	0.5	56	0.5	107	
t_{en}	Enable time	DIR	A	-40°C to 85°C	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	ns
				-40°C to 125°C	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	0.5	311	
		DIR	B	-40°C to 85°C	0.5	306	0.5	247	0.5	216	0.5	186	0.5	182	0.5	183	0.5	194	0.5	228	
				-40°C to 125°C	0.5	306	0.5	247	0.5	216	0.5	186	0.5	182	0.5	183	0.5	194	0.5	228	

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6.7 Switching Characteristics, V_{CCA} = 0.8 ± 0.04 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	150	0.5	94	0.5	63	0.5	33	0.5	28	0.5	27	0.5	28	0.5	34	ns
				-40°C to 125°C	0.5	150	0.5	94	0.5	63	0.5	33	0.5	28	0.5	27	0.5	28	0.5	34	
		B	A	-40°C to 85°C	0.5	115	0.5	94	0.5	76	0.5	50	0.5	41	0.5	40	0.5	38	0.5	38	
				-40°C to 125°C	0.5	115	0.5	94	0.5	76	0.5	50	0.5	41	0.5	40	0.5	38	0.5	38	
t_{dis}	Disable time	DIR	A	-40°C to 85°C	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	ns
				-40°C to 125°C	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	0.5	96	
		DIR	B	-40°C to 85°C	0.5	136	0.5	97	0.5	76	0.5	33	0.5	27	0.5	26	0.5	28	0.5	35	
				-40°C to 125°C	0.5	136	0.5	97	0.5	76	0.5	33	0.5	27	0.5	26	0.5	28	0.5	35	
t_{en} (1)	Enable time	DIR	A	-40°C to 85°C	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	ns
				-40°C to 125°C	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	0.5	246	
		DIR	B	-40°C to 85°C	0.5	243	0.5	188	0.5	157	0.5	128	0.5	123	0.5	122	0.5	123	0.5	125	
				-40°C to 125°C	0.5	243	0.5	188	0.5	157	0.5	128	0.5	123	0.5	122	0.5	123	0.5	125	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

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6.8 Switching Characteristics, V_{CCA} = 0.9 ± 0.045 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	122	0.5	76	0.5	51	0.5	23	0.5	18	0.5	16	0.5	15	0.5	17	ns
				-40°C to 125°C	0.5	122	0.5	76	0.5	51	0.5	23	0.5	18	0.5	16	0.5	15	0.5	17	
		B	A	-40°C to 85°C	0.5	84	0.5	63	0.5	51	0.5	39	0.5	28	0.5	24	0.5	21	0.5	21	
				-40°C to 125°C	0.5	84	0.5	63	0.5	51	0.5	39	0.5	28	0.5	24	0.5	21	0.5	21	
t_{dis}	Disable time	DIR	A	-40°C to 85°C	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	ns
				-40°C to 125°C	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	0.5	74	
		DIR	B	-40°C to 85°C	0.5	133	0.5	94	0.5	73	0.5	30	0.5	23	0.5	22	0.5	20	0.5	22	
				-40°C to 125°C	0.5	133	0.5	94	0.5	73	0.5	31	0.5	24	0.5	22	0.5	20	0.5	23	
t_{en} (1)	Enable time	DIR	A	-40°C to 85°C	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	ns
				-40°C to 125°C	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	0.5	211	
		DIR	B	-40°C to 85°C	0.5	192	0.5	146	0.5	120	0.5	93	0.5	88	0.5	86	0.5	85	0.5	87	
				-40°C to 125°C	0.5	192	0.5	146	0.5	120	0.5	93	0.5	88	0.5	86	0.5	85	0.5	87	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

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6.9 Switching Characteristics, V_{CCA} = 1.2 ± 0.1 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	84	0.5	51	0.5	38	0.5	15	0.5	10	0.5	9	0.5	7	0.5	8	ns
				-40°C to 125°C	0.5	84	0.5	51	0.5	38	0.5	15	0.5	11	0.5	9	0.5	8	0.5	8	
		B	A	-40°C to 85°C	0.5	50	0.5	33	0.5	23	0.5	15	0.5	12	0.5	10	0.5	8	0.5	7	
				-40°C to 125°C	0.5	50	0.5	33	0.5	23	0.5	15	0.5	12	0.5	10	0.5	8	0.5	7	
t_{dis}	Disable time	DIR	A	-40°C to 85°C	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	ns
				-40°C to 125°C	0.5	27	0.5	27	0.5	27	0.5	27	0.5	27	0.5	27	0.5	27	0.5	27	
		DIR	B	-40°C to 85°C	0.5	129	0.5	90	0.5	70	0.5	27	0.5	20	0.5	18	0.5	15	0.5	15	
				-40°C to 125°C	0.5	129	0.5	90	0.5	71	0.5	28	0.5	21	0.5	19	0.5	16	0.5	16	
t_{en} (1)	Enable time	DIR	A	-40°C to 85°C	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	ns
				-40°C to 125°C	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	0.5	177	
		DIR	B	-40°C to 85°C	0.5	105	0.5	71	0.5	59	0.5	40	0.5	36	0.5	35	0.5	33	0.5	34	
				-40°C to 125°C	0.5	105	0.5	71	0.5	59	0.5	41	0.5	37	0.5	36	0.5	34	0.5	35	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

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6.10 Switching Characteristics, V_{CCA} = 1.5 ± 0.1 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	79	0.5	41	0.5	28	0.5	12	0.5	9	0.5	7	0.5	6	0.5	6	ns
				-40°C to 125°C	0.5	79	0.5	41	0.5	28	0.5	12	0.5	9	0.5	8	0.5	6	0.5	6	
		B	A	-40°C to 85°C	0.5	50	0.5	28	0.5	18	0.5	10	0.5	9	0.5	8	0.5	6	0.5	5	
				-40°C to 125°C	0.5	50	0.5	28	0.5	18	0.5	11	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis}	Disable time	DIR	A	-40°C to 85°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	ns
				-40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	
		DIR	B	-40°C to 85°C	0.5	128	0.5	89	0.5	69	0.5	26	0.5	19	0.5	17	0.5	13	0.5	13	
				-40°C to 125°C	0.5	128	0.5	89	0.5	70	0.5	27	0.5	20	0.5	18	0.5	14	0.5	14	
t_{en} (1)	Enable time	DIR	A	-40°C to 85°C	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	ns
				-40°C to 125°C	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	0.5	172	
		DIR	B	-40°C to 85°C	0.5	92	0.5	54	0.5	42	0.5	31	0.5	27	0.5	25	0.5	24	0.5	24	
				-40°C to 125°C	0.5	92	0.5	54	0.5	42	0.5	31	0.5	28	0.5	26	0.5	25	0.5	25	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

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6.11 Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	78	0.5	40	0.5	24	0.5	10	0.5	8	0.5	7	0.5	5	0.5	5	ns
				-40°C to 125°C	0.5	78	0.5	40	0.5	24	0.5	10	0.5	8	0.5	7	0.5	6	0.5	5	
		B	A	-40°C to 85°C	0.5	56	0.5	27	0.5	16	0.5	9	0.5	7	0.5	7	0.5	5	0.5	4	
				-40°C to 125°C	0.5	56	0.5	27	0.5	16	0.5	9	0.5	8	0.5	7	0.5	5	0.5	5	
t_{dis}	Disable time	DIR	A	-40°C to 85°C	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	ns
				-40°C to 125°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	
		DIR	B	-40°C to 85°C	0.5	127	0.5	88	0.5	69	0.5	25	0.5	18	0.5	16	0.5	12	0.5	12	
				-40°C to 125°C	0.5	127	0.5	88	0.5	70	0.5	26	0.5	19	0.5	17	0.5	13	0.5	13	
t_{en} (1)	Enable time	DIR	A	-40°C to 85°C	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	ns
				-40°C to 125°C	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	0.5	171	
		DIR	B	-40°C to 85°C	0.5	89	0.5	50	0.5	36	0.5	26	0.5	23	0.5	22	0.5	21	0.5	20	
				-40°C to 125°C	0.5	89	0.5	50	0.5	36	0.5	27	0.5	24	0.5	23	0.5	22	0.5	21	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

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6.12 Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	77	0.5	38	0.5	21	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	ns
				-40°C to 125°C	0.5	77	0.5	38	0.5	21	0.5	8	0.5	6	0.5	5	0.5	5	0.5	5	
		B	A	-40°C to 85°C	0.5	71	0.5	28	0.5	15	0.5	7	0.5	6	0.5	5	0.5	5	0.5	4	
				-40°C to 125°C	0.5	71	0.5	28	0.5	15	0.5	8	0.5	6	0.5	6	0.5	5	0.5	4	
t_{dis}	Disable time	DIR	A	-40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	ns
				-40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	
		DIR	B	-40°C to 85°C	0.5	127	0.5	88	0.5	68	0.5	25	0.5	18	0.5	15	0.5	12	0.5	11	
				-40°C to 125°C	0.5	127	0.5	88	0.5	69	0.5	26	0.5	19	0.5	16	0.5	12	0.5	12	
t_{en} (1)	Enable time	DIR	A	-40°C to 85°C	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	ns
				-40°C to 125°C	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	0.5	182	
		DIR	B	-40°C to 85°C	0.5	84	0.5	46	0.5	29	0.5	18	0.5	17	0.5	16	0.5	15	0.5	15	
				-40°C to 125°C	0.5	84	0.5	46	0.5	29	0.5	19	0.5	18	0.5	17	0.5	16	0.5	16	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

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6.13 Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Condtions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	76	0.5	38	0.5	21	0.5	7	0.5	5	0.5	4	0.5	4	0.5	4	ns
				-40°C to 125°C	0.5	76	0.5	38	0.5	21	0.5	7	0.5	5	0.5	5	0.5	4	0.5	4	
		B	A	-40°C to 85°C	0.5	105	0.5	34	0.5	17	0.5	8	0.5	6	0.5	5	0.5	4	0.5	4	
				-40°C to 125°C	0.5	105	0.5	34	0.5	17	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	
t_{dis}	Disable time	DIR	A	-40°C to 85°C	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	ns
				-40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	
		DIR	B	-40°C to 85°C	0.5	128	0.5	88	0.5	68	0.5	24	0.5	17	0.5	15	0.5	11	0.5	11	
				-40°C to 125°C	0.5	128	0.5	88	0.5	69	0.5	26	0.5	19	0.5	16	0.5	12	0.5	11	
t_{en} (1)	Enable time	DIR	A	-40°C to 85°C	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	ns
				-40°C to 125°C	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	0.5	218	
		DIR	B	-40°C to 85°C	0.5	83	0.5	45	0.5	28	0.5	17	0.5	15	0.5	14	0.5	14	0.5	14	
				-40°C to 125°C	0.5	83	0.5	45	0.5	28	0.5	18	0.5	16	0.5	15	0.5	15	0.5	15	

(1) The enable time is a calculated value, derived using the formula shown in the Enable Times section.

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6.14 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance per transceiver (A to B)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.2		pF
			0.8 V	0.8 V		2.0		
			0.9 V	0.9 V		2.0		
			1.2 V	1.2 V		2.0		
			1.5 V	1.5 V		2.0		
			1.8 V	1.8 V		2.1		
			2.5 V	2.5 V		2.5		
			3.3 V	3.3 V		3.0		
	Power Dissipation Capacitance per transceiver (B to A)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		10.6		pF
			0.8 V	0.8 V		10.7		
			0.9 V	0.9 V		10.6		
			1.2 V	1.2 V		10.8		
			1.5 V	1.5 V		11.1		
			1.8 V	1.8 V		12.2		
			2.5 V	2.5 V		15.9		
			3.3 V	3.3 V		19.6		
C_{pdB}	Power Dissipation Capacitance per transceiver (A to B)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		10.6		pF
			0.8 V	0.8 V		10.7		
			0.9 V	0.9 V		10.6		
			1.2 V	1.2 V		10.8		
			1.5 V	1.5 V		11.1		
			1.8 V	1.8 V		12.2		
			2.5 V	2.5 V		15.8		
			3.3 V	3.3 V		19.3		
	Power Dissipation Capacitance per transceiver (B to A)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.2		pF
			0.8 V	0.8 V		2.0		
			0.9 V	0.9 V		2.0		
			1.2 V	1.2 V		2.0		
			1.5 V	1.5 V		2.0		
			1.8 V	1.8 V		2.1		
			2.5 V	2.5 V		2.5		
			3.3 V	3.3 V		3.0		

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6.15 Typical Characteristics

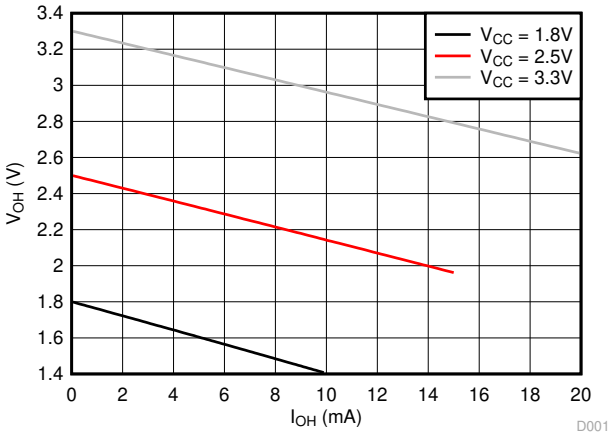


Figure 6-1. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

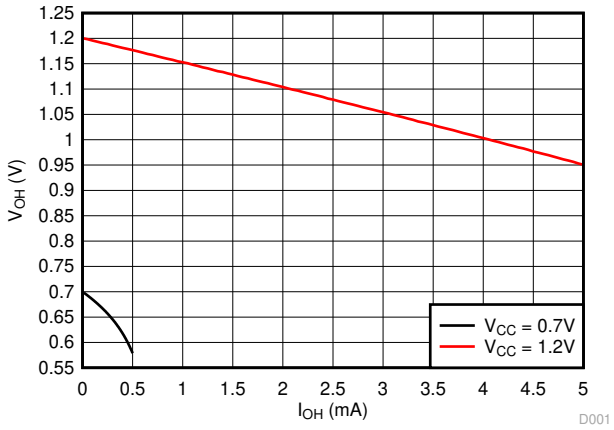


Figure 6-2. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

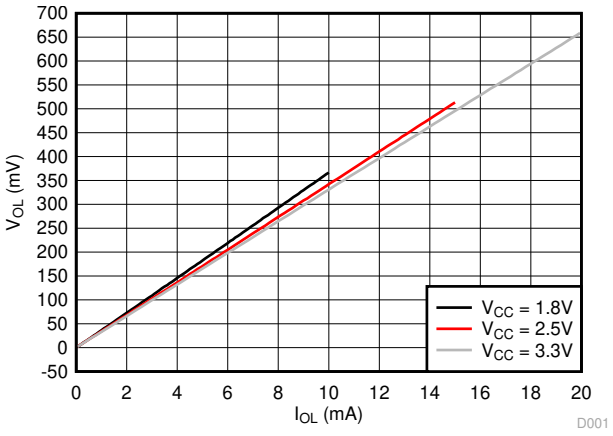


Figure 6-3. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

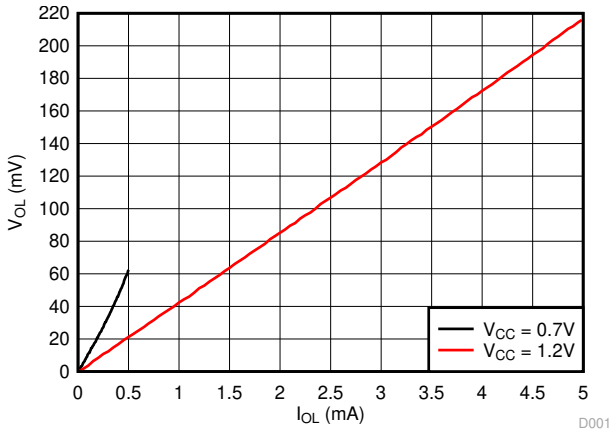


Figure 6-4. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

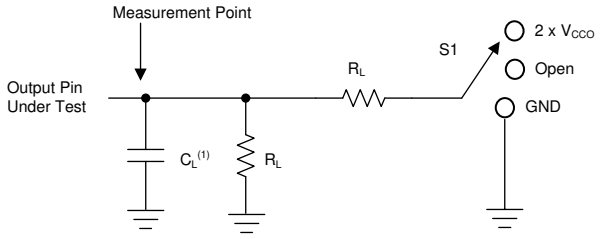
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7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- dv/dt ≤ 1 ns/V

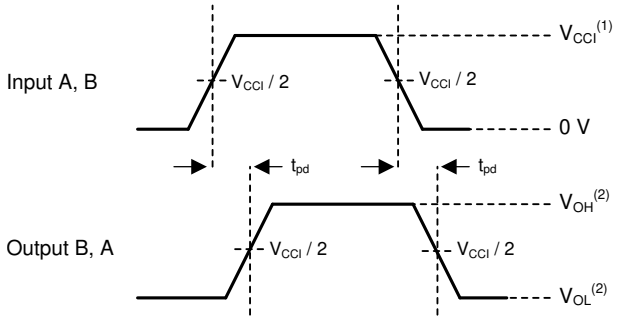


A. C_L includes probe and jig capacitance.

Figure 7-1. Load Circuit

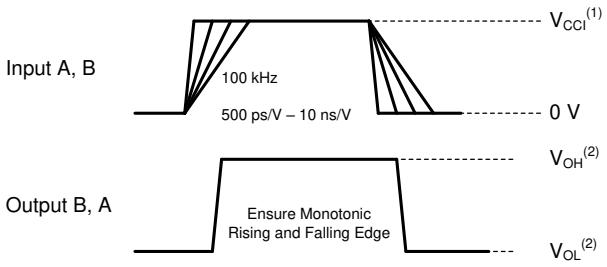
Table 7-1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
Δt/Δv	Input transition rise or fall rate	0.65 V – 3.6 V	1 MΩ	15 pF	Open	N/A
t_{pd}	Propagation (delay) time	1.1 V – 3.6 V	2 kΩ	15 pF	Open	N/A
		0.65 V – 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	2 × V_{CCO}	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	2 × V_{CCO}	0.1 V
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	GND	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	GND	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	GND	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	GND	0.1 V



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

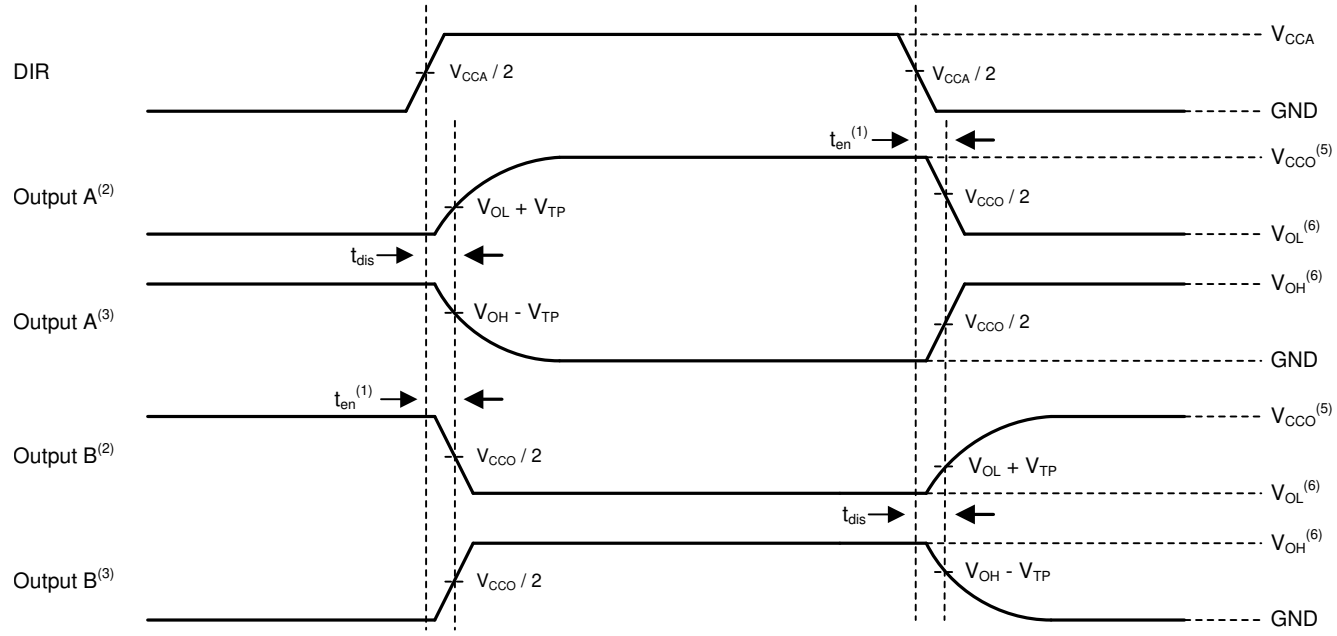
Figure 7-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 7-3. Input Transition Rise or Fall Rate

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A. Illustrative purposes only. Enable Time is a calculation as described in the Application Information section.
B. Output waveform on the condition that input is driven to a valid Logic Low.
C. Output waveform on the condition that input is driven to a valid Logic High.
D. V_{CCI} is the supply pin associated with the input port.
E. V_{CCO} is the supply pin associated with the output port.
F. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

Figure 7-4. Enable Time And Disable Time

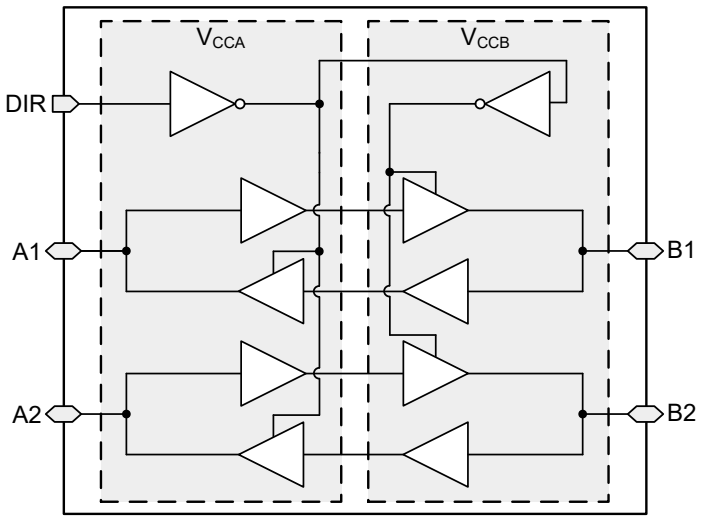
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8 Detailed Description

8.1 Overview

The SN74AXC2T45-Q1 is a 2-bit, dual-supply non-inverting bidirectional voltage level translation device. Ax pins and the DIR pin are referenced to V_{CCA} logic levels, and Bx pins are referenced to V_{CCB} logic levels. The A port is able to accept I/O voltages ranging from 0.65 V to 3.6 V, while the B port can accept I/O voltages from 0.65 V to 3.6 V. A high on DIR enables data transmission from A to B and a low on DIR enables data transmission from B to A. See Device Functional Modes for a summary of the operation of the control logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the Section 6.5. The worst case resistance is calculated with the maximum input voltage, given in the *Section 6.1*, and the maximum input leakage current, given in the Section 6.5, using Ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in *Section 6.3* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Section 6.1* must be followed at all times.

8.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the Section 6.5.

8.3.4 V_{CC} Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is <100 mV.

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Section 6.3*.

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8.3.6 Glitch-free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

8.3.7 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 8-1.

CAUTION

Voltages beyond the values specified in the *Section 6.1* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

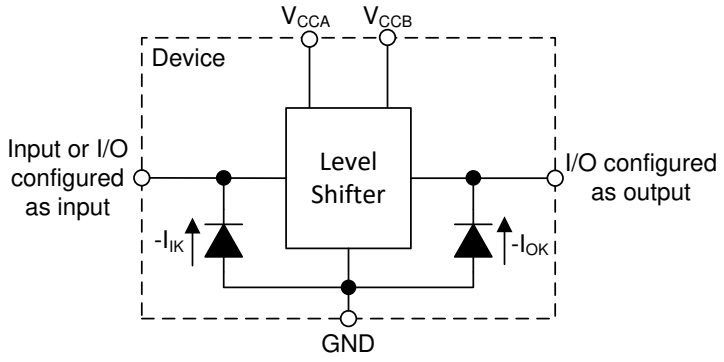


Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.8 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 0.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V and 3.3 V).

8.3.9 Supports High-Speed Translation

The SN74AXC2T45-Q1 device can support high data-rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

8.4 Device Functional Modes

Table 8-1. Function Table

CONTROL INPUT	Port Status		OPERATION
DIR	A PORT	B PORT	
L	Output (Enabled)	Input (Hi-Z)	B data to A bus
H	Input (Hi-Z)	Output (Enabled)	A data to B bus

Caution: Input circuits of the data I/O's are always active.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AXC2T45-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AXC2T45-Q1 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380 Mbps when device translates a signal from 1.8 V to 3.3 V.

One example application is shown in Figure 9-1, where the SN74AXC2T45-Q1 device is used to translate low voltage error signals from a CPU to a higher voltage signal to properly drive the inputs of a system controller, thus alerting the system of any CPU errors such as overheating or other catastrophic processor errors.

9.1.1 Enable Times

Calculate the enable times for the SN74AXC2T45-Q1 using the following formulas:

$$t_{A_en}\ (\text{DIR to A}) = t_{dis}\ (\text{DIR to B}) + t_{pd}\ (\text{B to A}) \quad (1)$$

$$t_{B_en}\ (\text{DIR to A}) = t_{dis}\ (\text{DIR to A}) + t_{pd}\ (\text{A to B}) \quad (2)$$

In a bidirectional application, these enable times provide the maximum delay time from the time the DIR bit is switched until an output is expected. For example, if the SN74AXC2T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled (t_{dis}) before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay (t_{pd}). To avoid bus contention care should be taken to not apply an input signal prior to the output port being disabled (t_{dis} max).

9.2 Typical Application

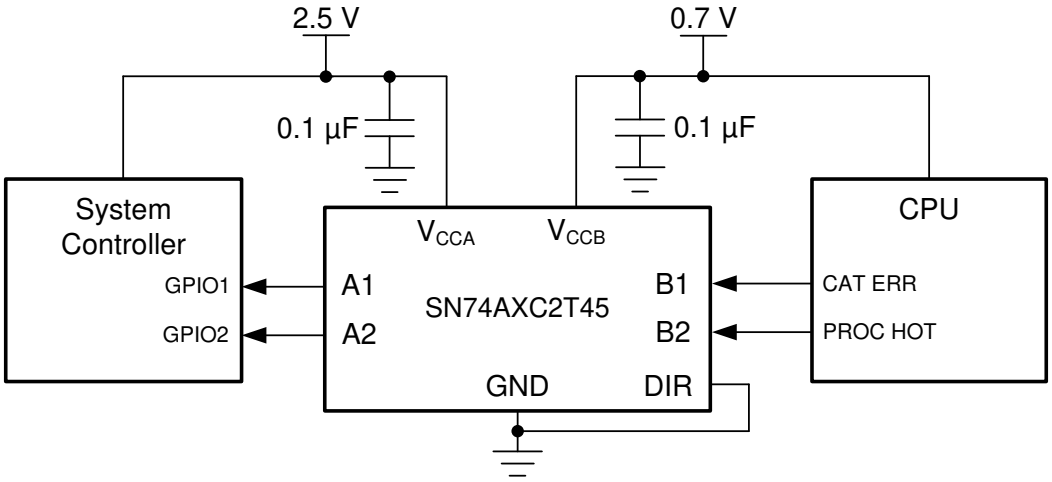


Figure 9-1. Processor Error Application

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9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC2T45-Q1 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXC2T45-Q1 device is driving to determine the output voltage range.

9.2.3 Application Curve

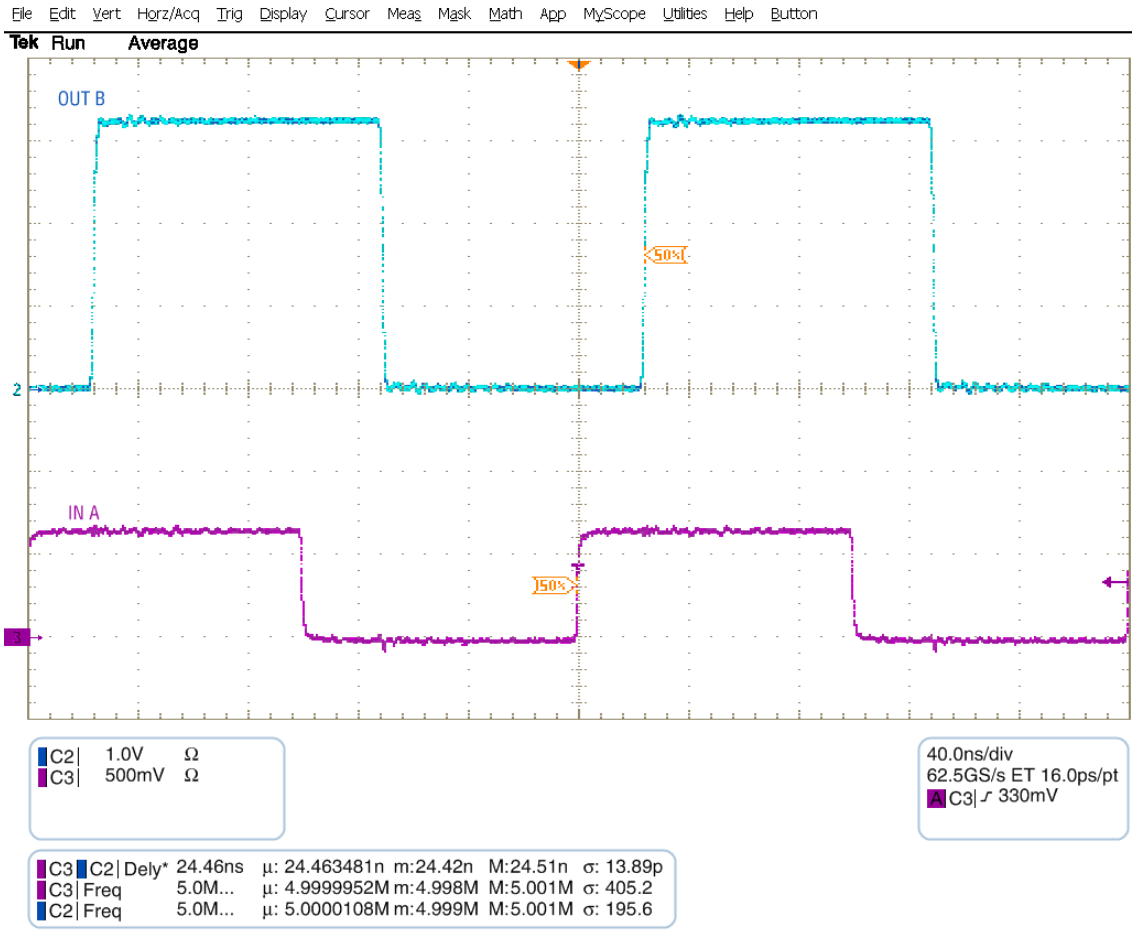


Figure 9-2. Up Translation at 2.5 MHz (0.7 V to 3.3 V)

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10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device is designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

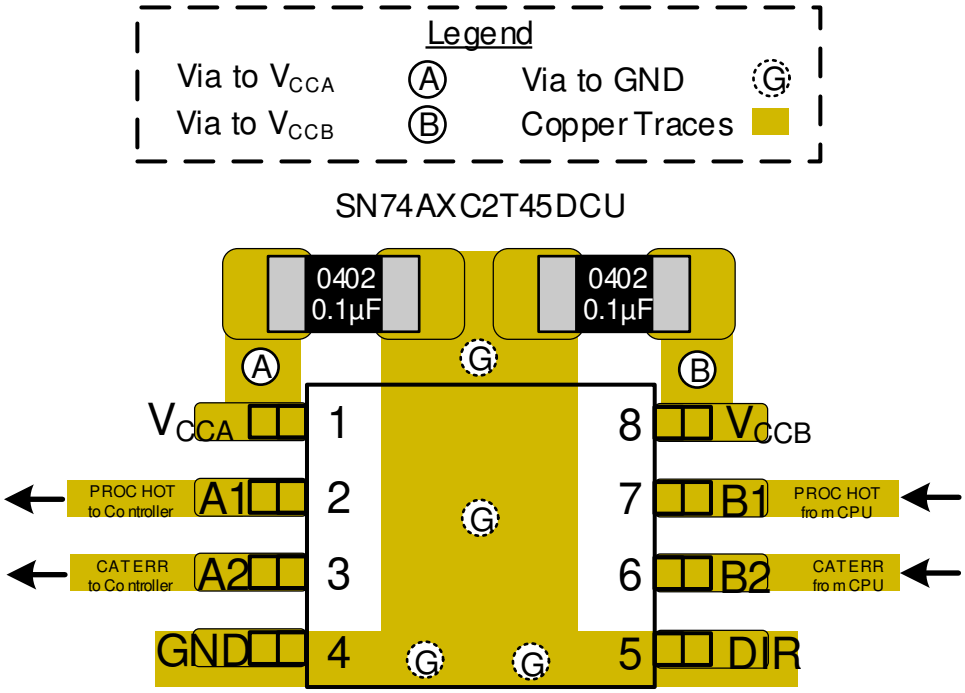
11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 µF capacitor is recommended, but transient performance can be improved by having both 1 µF and 0.1 µF capacitors in parallel as bypass capacitors.
- Use short trace lengths to avoid excessive loading.

11.2 Layout Example



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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report.
- Texas Instruments, *Power Sequencing for AXC Family of Devices* application report.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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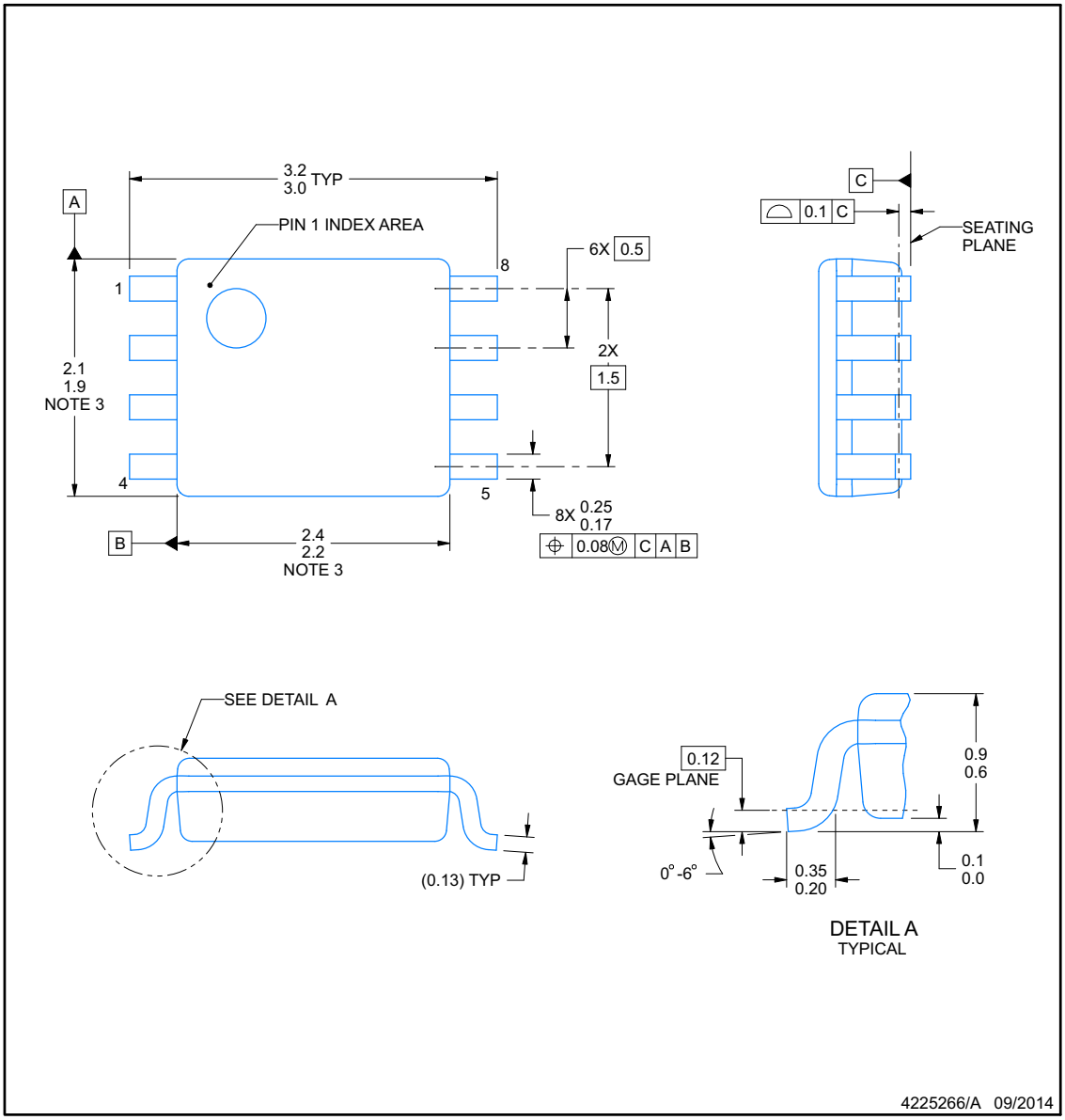
PACKAGE OUTLINE

DCU0008A



VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

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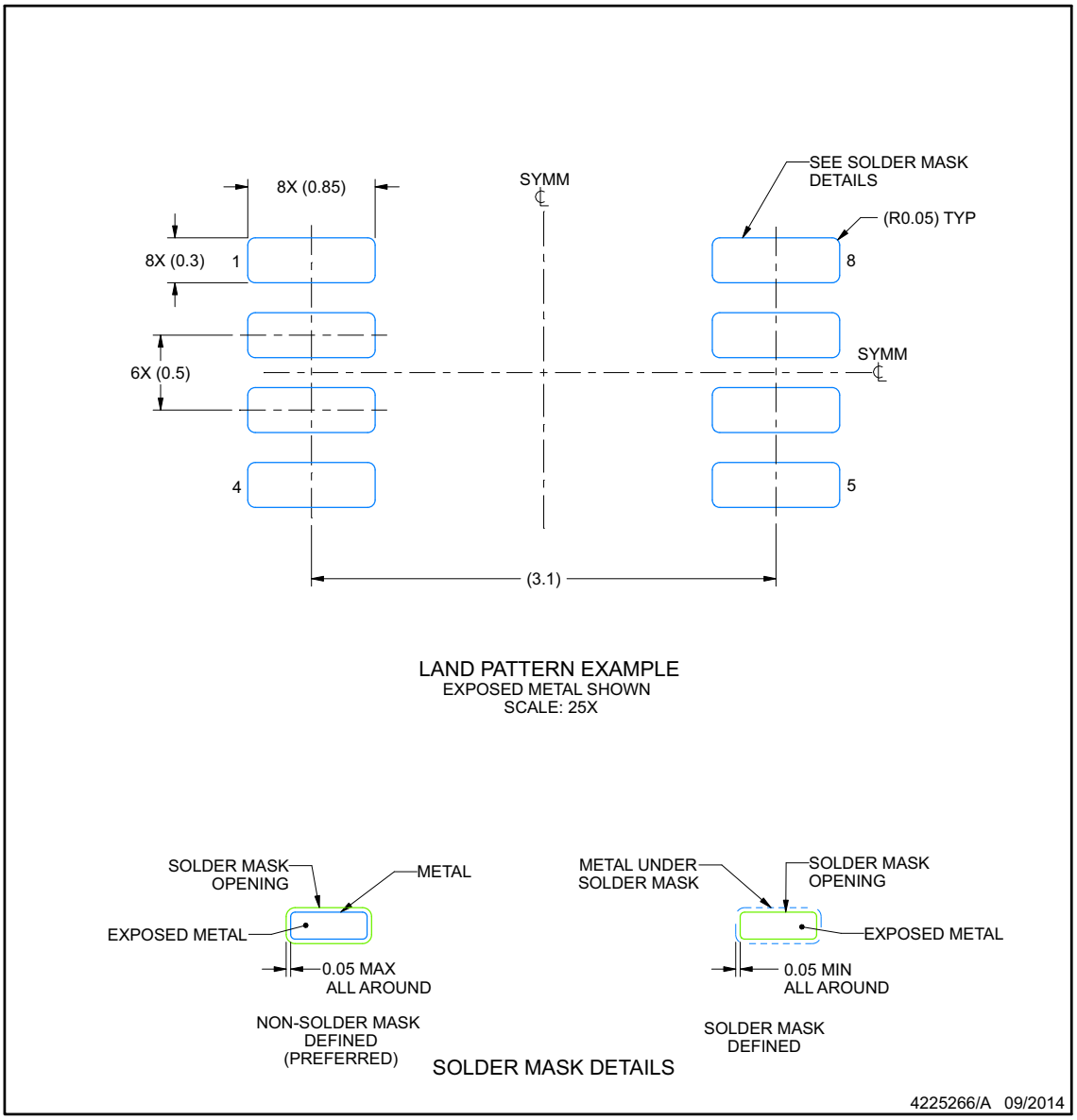
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EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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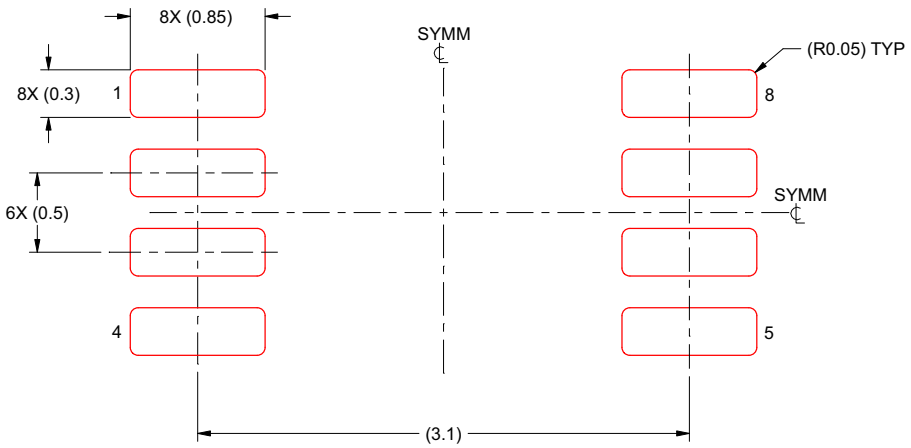
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EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

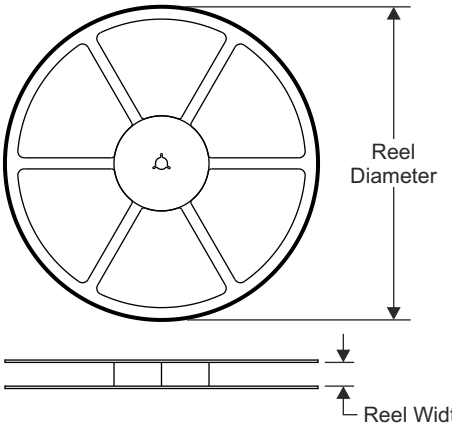
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

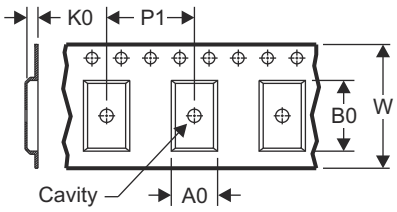
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13.1 Tape and Reel Information

REEL DIMENSIONS

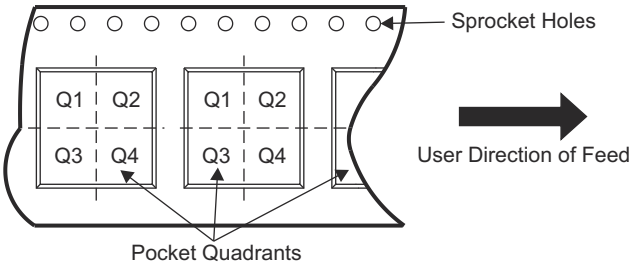


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

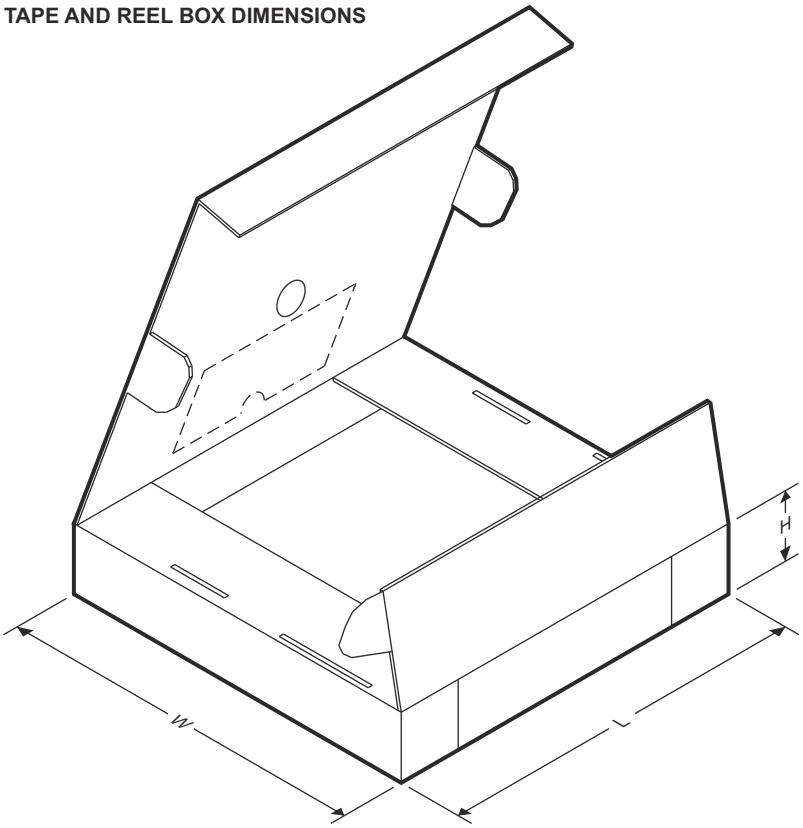


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXC2T45DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8	Q3

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXC2T45DCUR	VSSOP	DCU	8	3000	180	180	18.0

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCAXC2T45QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74AXC2T45-Q1 :

- Catalog : SN74AXC2T45

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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