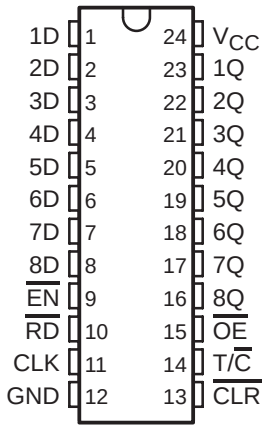
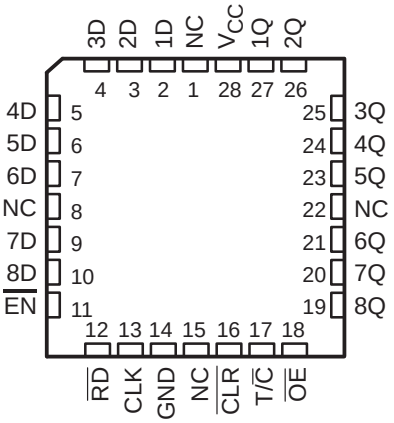
SDAS098B − OCTOBER 1984 − REVISED JANUARY 1995

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **T/$\overline{C}$ Determines True or Complementary Data at Q Outputs**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54ALS996 . . . JT PACKAGE
SN74ALS996 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS996 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description

These 8-bit latches are designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) input when the enable ($\overline{EN}$) input is low. Data can be read back onto the data inputs by taking the read ($\overline{RD}$) input low, in addition to having $\overline{EN}$ low. When $\overline{EN}$ is high, both the read-back and write modes are disabled. Transitions on $\overline{EN}$ should only be made with CLK high to prevent false clocking.

The polarity of the Q outputs can be controlled by the polarity (T/$\overline{C}$) input. When T/$\overline{C}$ is high, Q is the same as is stored in the flip-flops. When T/$\overline{C}$ is low, the output data is inverted. The Q outputs can be placed in the high-impedance state by taking the output-enable ($\overline{OE}$) input high. $\overline{OE}$ does not affect the internal operation of the register. Old data can be retained or new data can be entered while the outputs are off.

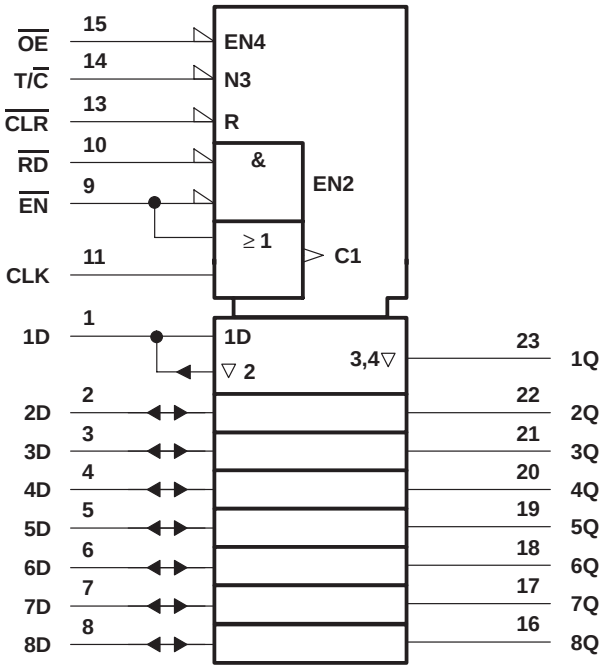
A low level at the clear ($\overline{CLR}$) input resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

The -1 version of the SN74ALS996 is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is increased to 48 mA. There is no -1 version of the SN54ALS996.

The SN54ALS996 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS996 is characterized for operation from 0°C to 70°C.

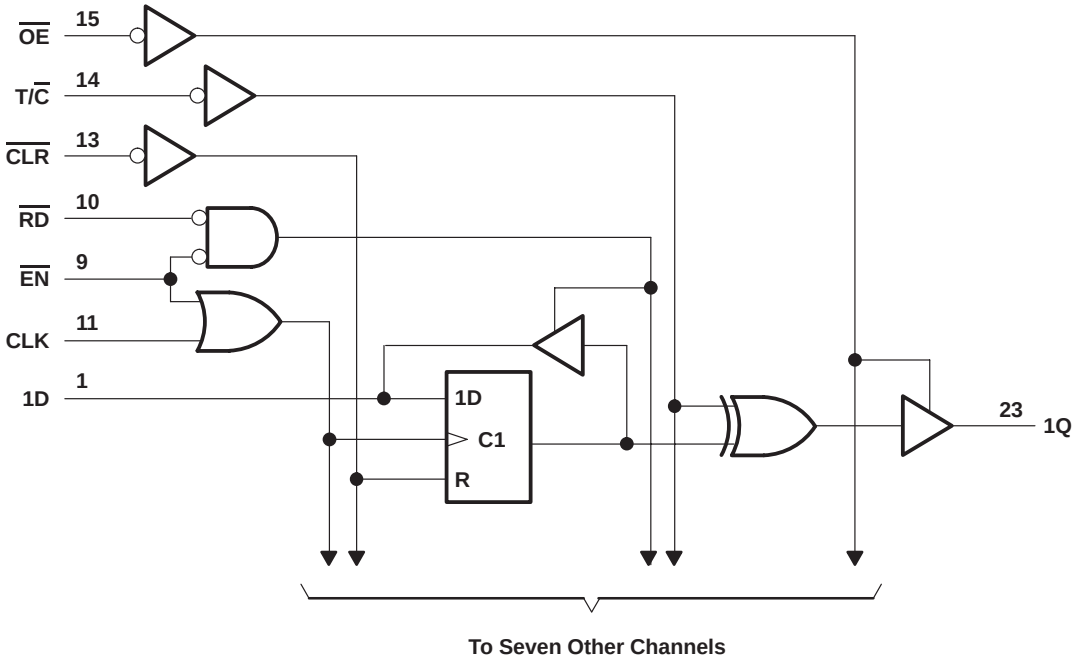
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

logic symbol†



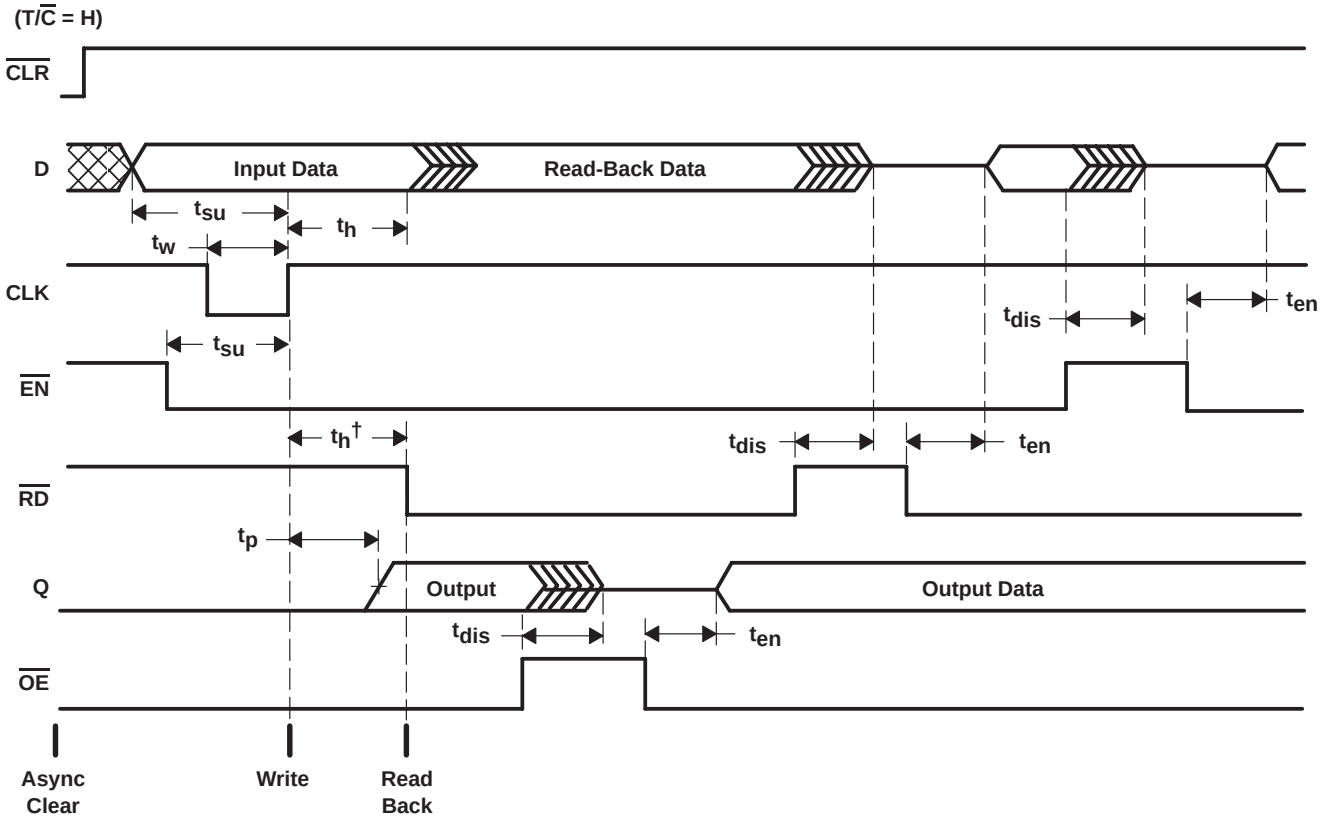
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

timing diagram



† This hold time ensures that the read-back circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I ($\overline{OE}$, $\overline{RD}$, $\overline{EN}$, CLK, $\overline{CLR}$, and T/$\overline{C}$) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS996 . . . . . −55°C to 125°C
SN74ALS996 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS996			SN74ALS996			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	All inputs				2			V
		All inputs except $\overline{OE}$, $\overline{RD}$	2						
		$\overline{OE}$, $\overline{RD}$	2.2						
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q			−1			−2.6	mA
		D			−0.4			−0.4	
I_{OL}	Low-level output current	Q			12			24	mA
								48†	
		D			8			8	
f_{clock}	Clock frequency		0		35	0		35	MHZ
t_w	Pulse duration	$\overline{CLR}$ low	10			10			ns
		CLK low	14.5			14.5			
		CLK high	14.5			14.5			
t_{su}	Setup time	Data before CLK↑	15			15			ns
		$\overline{EN}$ low before CLK↑	10			10			
		CLK high before $\overline{EN}$↑‡	15			15			
		$\overline{CLR}$ high (inactive) before CLK↑	10			10			
t_h	Hold time	Data after CLK↑	1			0			ns
		$\overline{EN}$ low after CLK↑	5			5			
		$\overline{RD}$ high after CLK↑§	5			5			
T_A	Operating free-air temperature		−55		125	0		70	°C

† Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V
‡ This setup time ensures that $\overline{EN}$ will not false clock the data register.
§ This hold time ensures that there will be no conflict on the input data bus.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS996			SN74ALS996			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = − 0.4 mA	V_{CC} −2			V_{CC} −2			V
	Q	V_{CC} = 4.5 V	I_{OH} = − 1 mA	2.4	3.2					
			I_{OH} = − 2.6 mA				2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4				V
			I_{OL} = 8 mA					0.35	0.5	
	Q	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 24 mA					0.35	0.5	
			I_{OL} = 48 mA‡					0.35	0.5	
I_{OZH}	Q	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	Q	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	µA
I_I	D inputs	V_{CC} = 5.5 V	V_I = 5.5 V			0.1			0.1	mA
	All others		V_I = 7 V			0.1			0.1	
I_{IH}	D inputs§	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	All others					20			20	
I_{IL}	D inputs§	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	All others					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V, $\overline{CLR}$ = 2.5 V	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V, $\overline{EN}$, $\overline{RD}$ low	Outputs high		35	55		35	55	mA
			Outputs low		55	85		55	85	
			Outputs disabled		42	65		42	65	

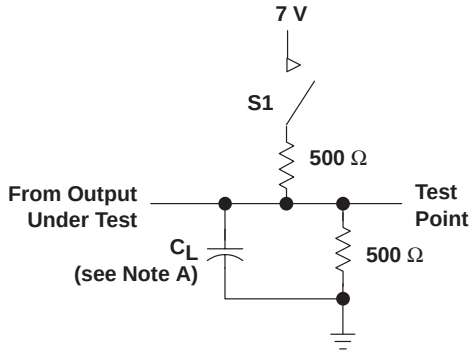
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V
§ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

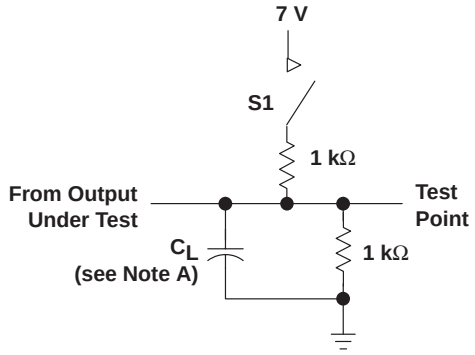
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX†				UNIT
			SN54ALS996		SN74ALS996		
			MIN	MAX	MIN	MAX	
f_{max}			35		35		MHz
t_{PLH}	CLK (T/$\overline{C}$ = H or L)	Q	5	30	5	28	ns
t_{PHL}			5	24	5	28	
t_{PLH}	$\overline{CLR}$ (T/$\overline{C}$ = L)	Q	5	27	7	27	ns
t_{PHL}	$\overline{CLR}$ (T/$\overline{C}$ = H)		5	23	7	23	
t_{PLH}	T/$\overline{C}$	Q	4	23	5	23	ns
t_{PHL}			5	23	5	23	
t_{PHL}	$\overline{CLR}$	D	5	30	8	30	ns
t_{en}‡	$\overline{RD}$	D	2	18	3	16	ns
t_{dis}§			1	19	3	19	
t_{en}‡	$\overline{EN}$	D	2	17	3	16	ns
t_{dis}§			1	19	3	19	
t_{en}‡	$\overline{OE}$	Q	2	15	4	15	ns
t_{dis}§			1	11	1	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ $t_{en} = t_{PZH}$ or t_{PZL}
§ $t_{dis} = t_{PHZ}$ or t_{PLZ}

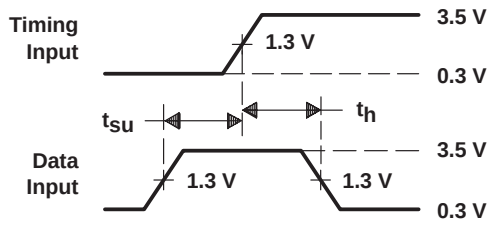
PARAMETER MEASUREMENT INFORMATION



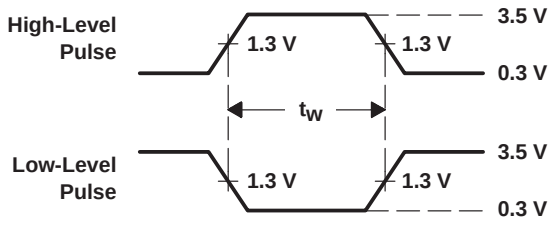
LOAD CIRCUIT FOR Q OUTPUTS



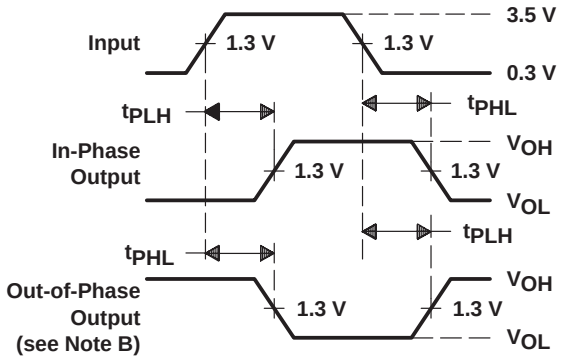
LOAD CIRCUIT FOR D OUTPUTS



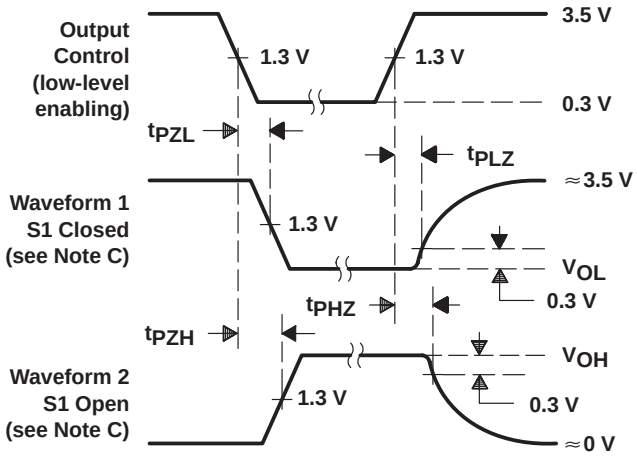
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. When measuring propagation delay times of 3-state outputs, switch S1 is open.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89945013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89945013A SNJ54ALS 996FK	Samples
5962-8994501LA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8994501LA SNJ54ALS996JT	Samples
SN74ALS996DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS996	Samples
SN74ALS996DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS996	Samples
SNJ54ALS996FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89945013A SNJ54ALS 996FK	Samples
SNJ54ALS996JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8994501LA SNJ54ALS996JT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54ALS996, SN74ALS996 :

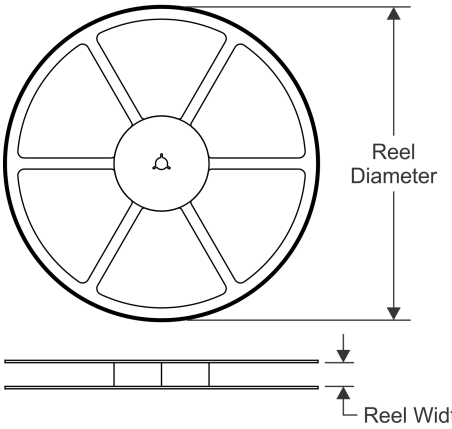
- Catalog: SN74ALS996
- Military: SN54ALS996

NOTE: Qualified Version Definitions:

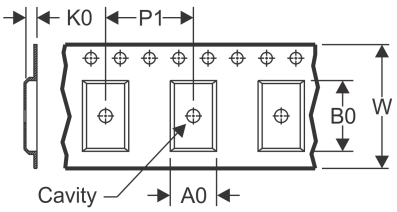
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

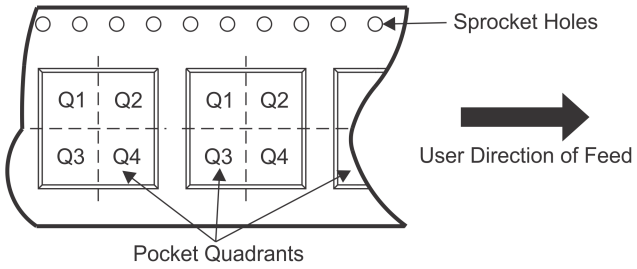


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

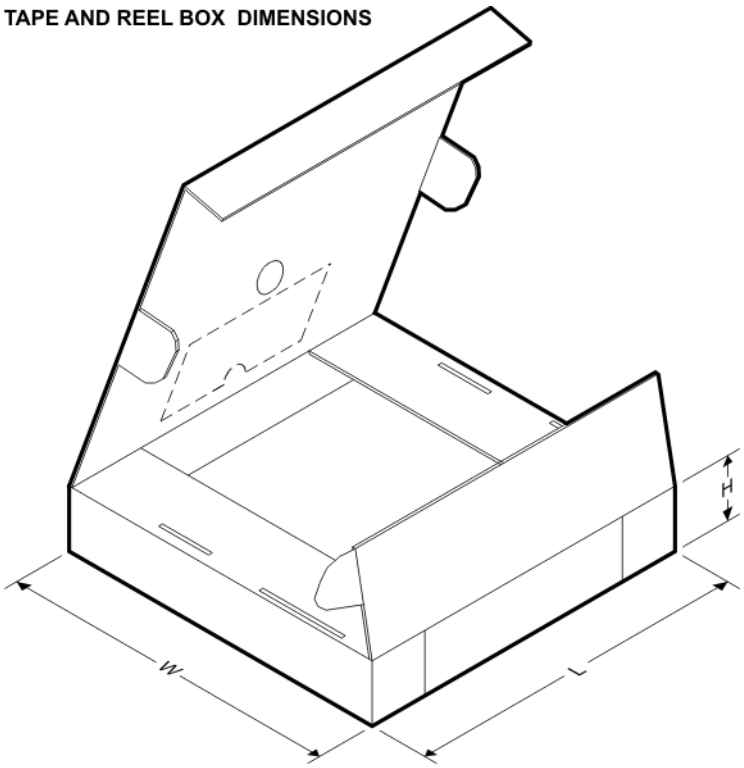
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS996DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



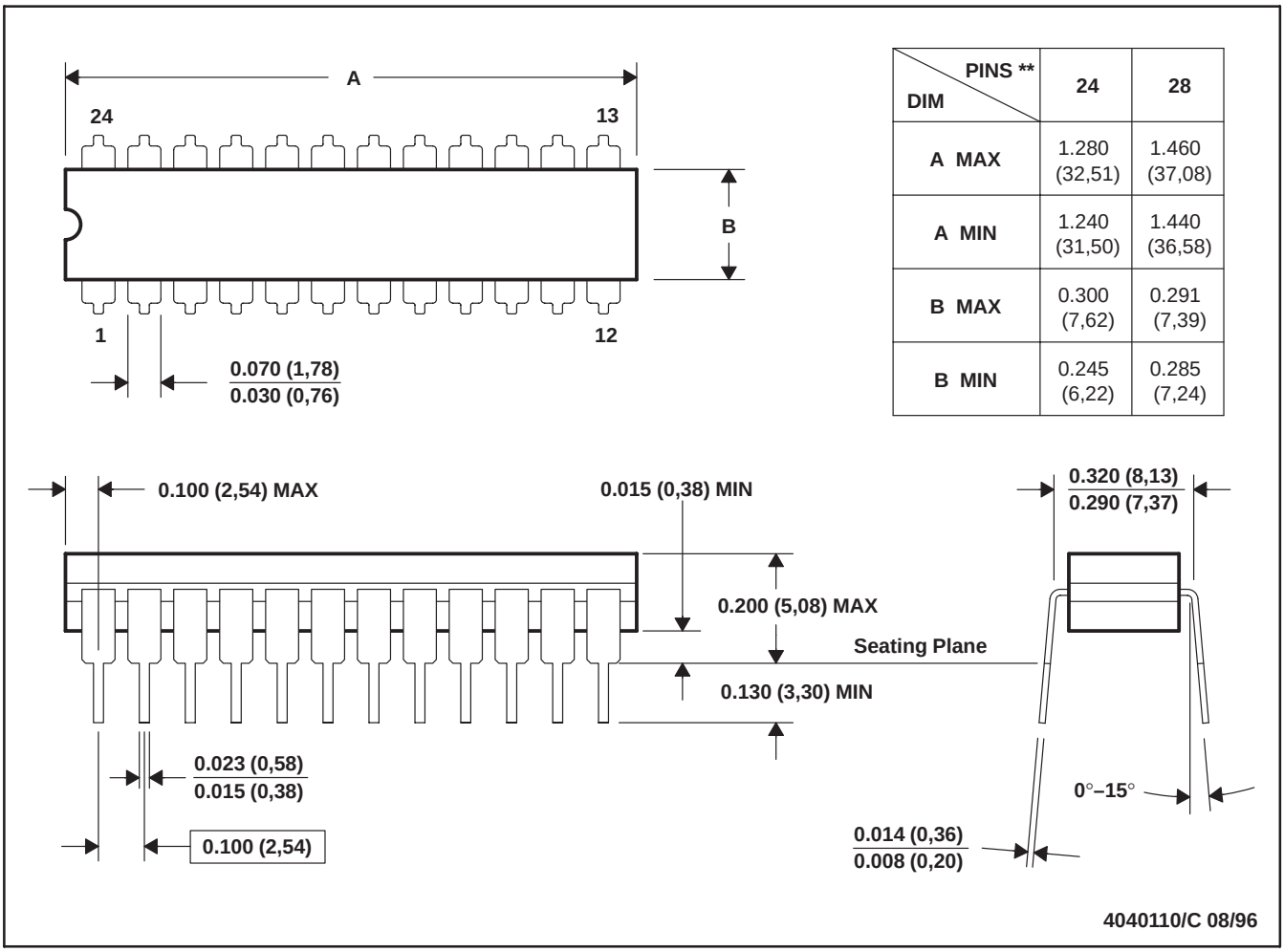
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS996DWR	SOIC	DW	24	2000	350.0	350.0	43.0

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

24 LEADS SHOWN

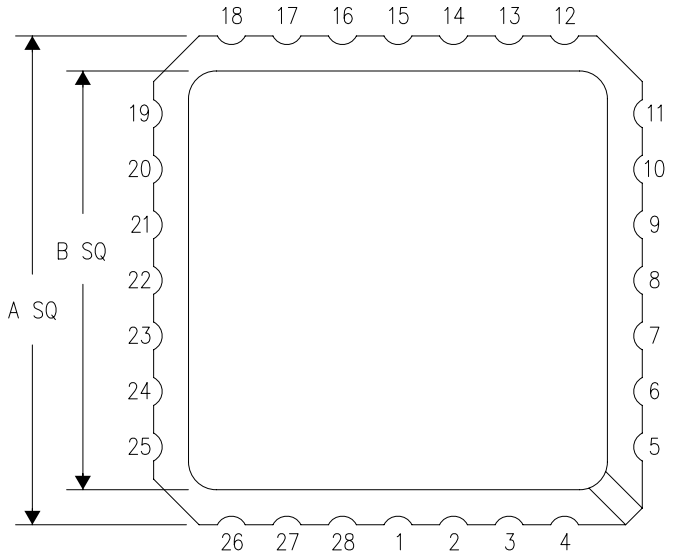


DIM \ PINS **	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

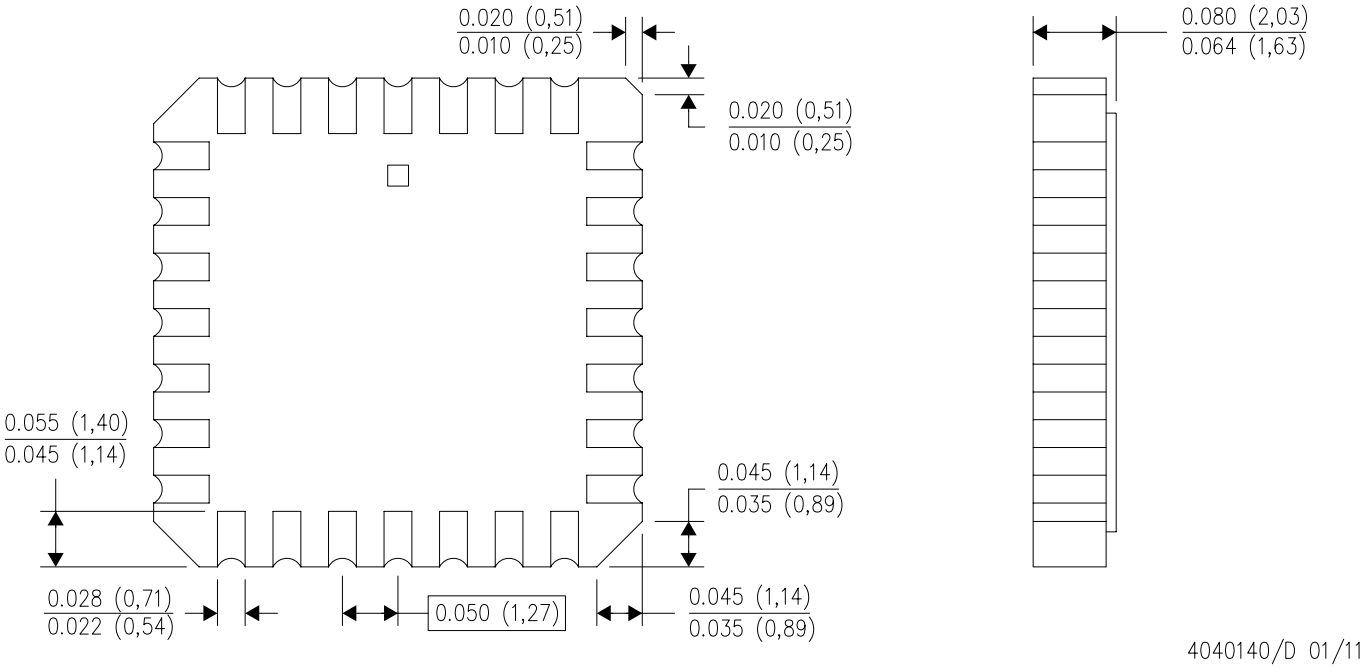
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



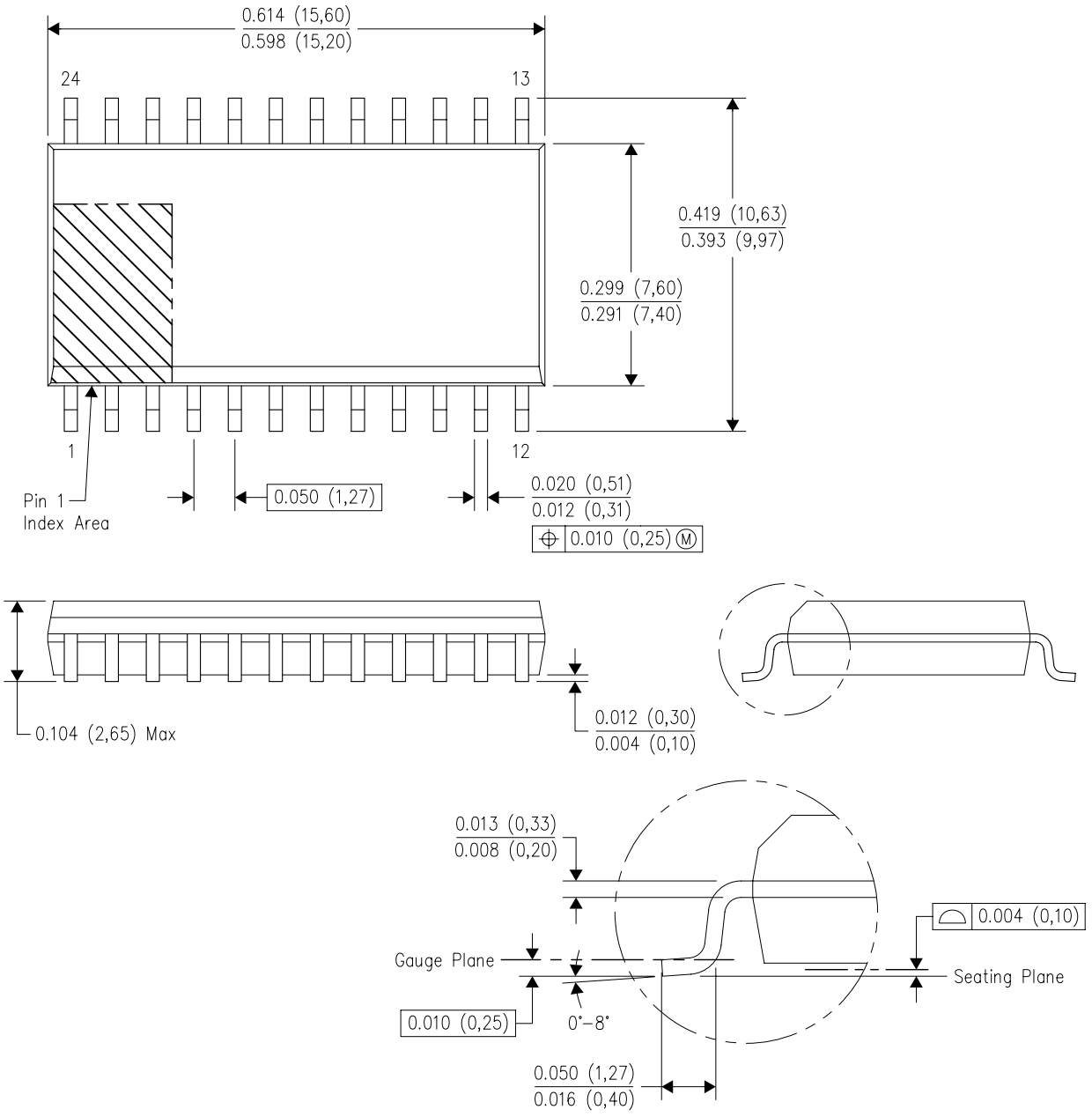
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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