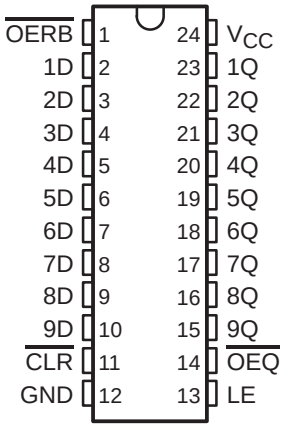
- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **True Logic Outputs**
- **Designed With Nine Bits for Parity Applications**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

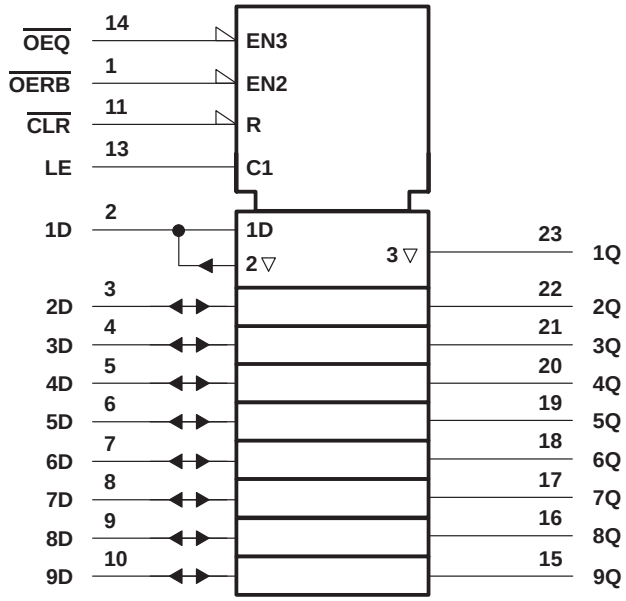
This 9-bit latch is designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. In addition, this device provides a 3-state buffer-type output and is easily implemented in parity applications.

The nine latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. The Q outputs are in the 3-state condition when the output-enable ($\overline{OEQ}$) input is high.

Read back is provided through the output-enable ($\overline{OERB}$) input. When $\overline{OERB}$ is taken low, the data present at the output of the data latches is allowed to pass back onto the input data bus. When $\overline{OERB}$ is taken high, the output of the data latches is isolated from the D inputs. $\overline{OERB}$ does not affect the internal operation of the latches; however, precautions should be taken not to create a bus conflict.

The SN74ALS992 is characterized for operation from 0°C to 70°C.

logic symbol†

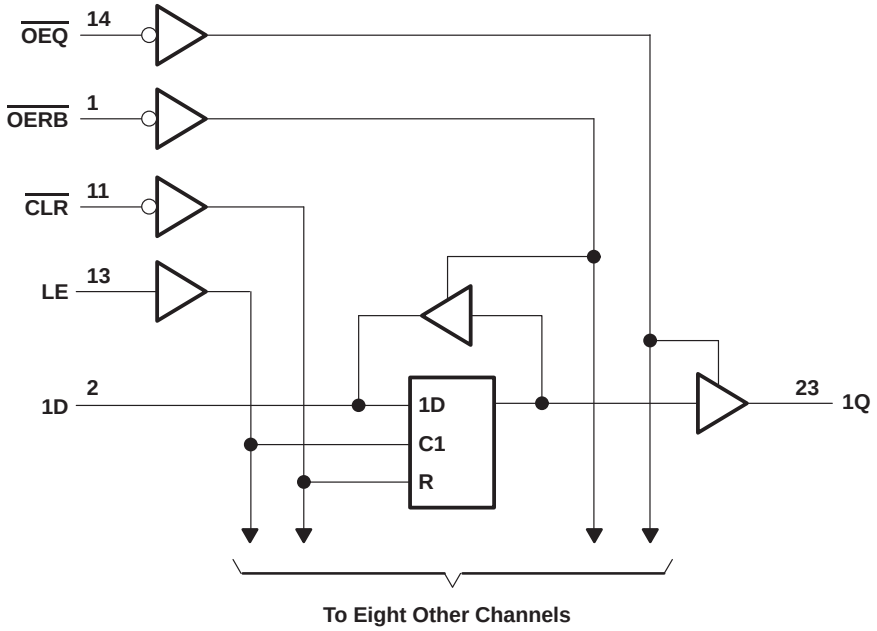


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

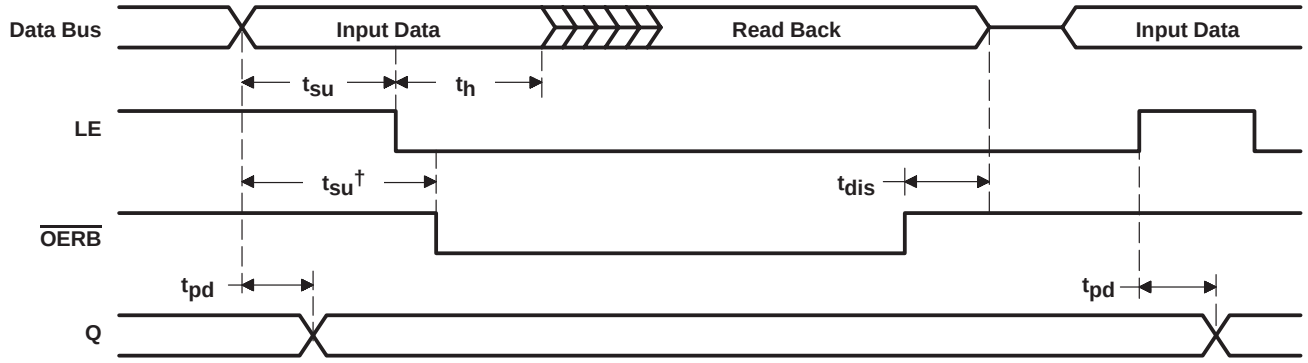
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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logic diagram (positive logic)



timing diagram



$\overline{CLR}$ = H, $\overline{OEQ}$ = L

† This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I ($\overline{OERB}$, $\overline{OEQ}$, $\overline{CLR}$, and LE) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q			–2.6	mA
		D			–0.4	
I_{OL}	Low-level output current	Q			24	mA
		D			8	
t_w	Pulse duration	LE high	10			ns
		$\overline{CLR}$ low	10			
t_{su}	Setup time	Data before LE↓	10			ns
		Data before $\overline{OERB}$↓	10			
t_h	Hold time, data after LE↓		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = – 0.4 mA	V_{CC} –2			V
	Q	V_{CC} = 4.5 V,	I_{OH} = – 2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	V
			I_{OL} = 8 mA		0.35	0.5	
	Q	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	
			I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	Q	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}	Q	V_{CC} = 5.5 V,	V_O = 0.4 V			–20	µA
I_I	D inputs	V_{CC} = 5.5 V	V_I = 5.5 V			0.1	mA
	All others		V_I = 7 V			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	All others					20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1	mA
	All others					–0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V, $\overline{OERB}$ high	Outputs high		30	50	mA
			Outputs low		50	80	
			Outputs disabled		35	55	

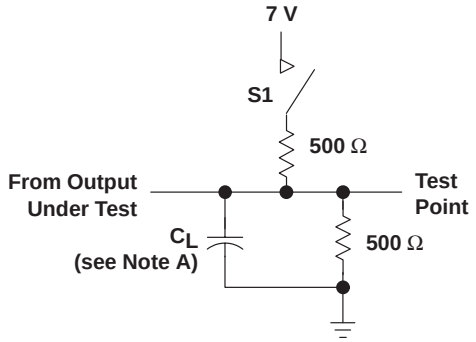
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

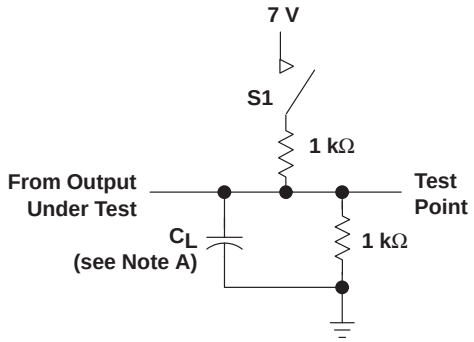
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX†		UNIT
			MIN	MAX	
t_{PLH}	D	Q	3	14	ns
t_{PHL}			4	16	
t_{PLH}	LE	Q	6	20	ns
t_{PHL}			8	25	
t_{PHL}	$\overline{CLR}$	Q	6	20	ns
		D	8	26	
t_{en}‡	$\overline{OERB}$	D	4	21	ns
t_{dis}§			2	14	
t_{en}‡	$\overline{OEQ}$	Q	4	18	ns
t_{dis}§			1	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ $t_{en} = t_{PZH}$ or t_{PZL}
§ $t_{dis} = t_{PHZ}$ or t_{PLZ}

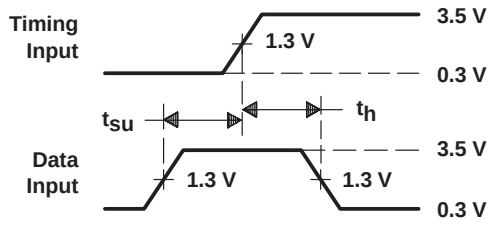
PARAMETER MEASUREMENT INFORMATION



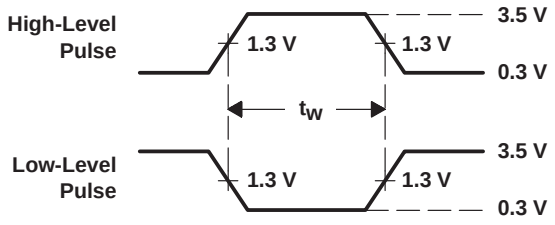
LOAD CIRCUIT FOR Q OUTPUTS



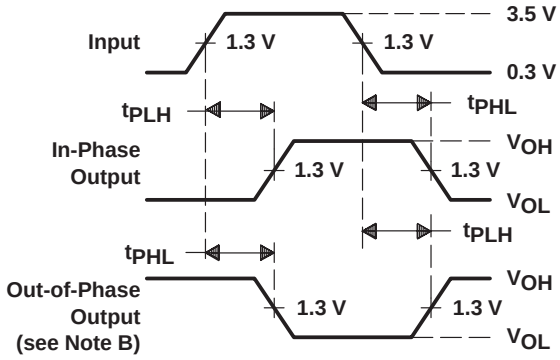
LOAD CIRCUIT FOR D OUTPUTS



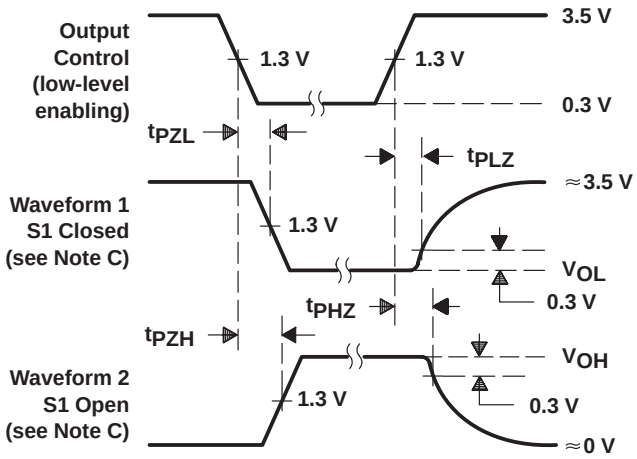
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. When measuring propagation delay times of 3-state outputs, switch S1 is open.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms

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