

SN54AHC138, SN74AHC138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SCLS258J – DECEMBER 1995 – REVISED FEBRUARY 2002

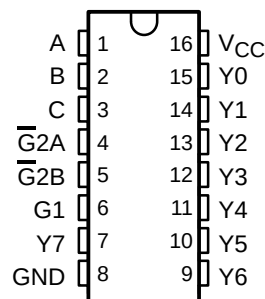
- Operating Range 2-V to 5.5-V V_{CC}
- Designed Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description

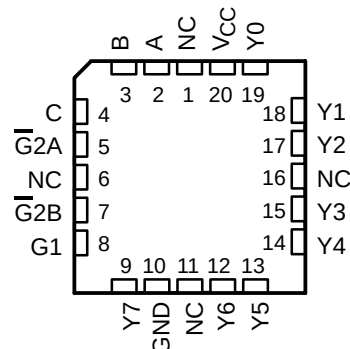
The 'AHC138 decoders/demultiplexers are designed for high-performance memory-decoding and data-routing applications that require very short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

SN54AHC138 . . . J OR W PACKAGE
SN74AHC138 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC138N	SN74AHC138N
	SOIC – D	Tube	SN74AHC138D	AHC138
		Tape and reel	SN74AHC138DR	
	SOP – NS	Tape and reel	SN74AHC138NSR	AHC138
	SSOP – DB	Tape and reel	SN74AHC138DBR	HA138
	TSSOP – PW	Tape and reel	SN74AHC138PWR	HA138
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHC138DGV	HA138
	CDIP – J	Tube	SNJ54AHC138J	SNJ54AHC138J
	CFP – W	Tube	SNJ54AHC138W	SNJ54AHC138W
	LCCC – FK	Tube	SNJ54AHC138FK	SNJ54AHC138FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L



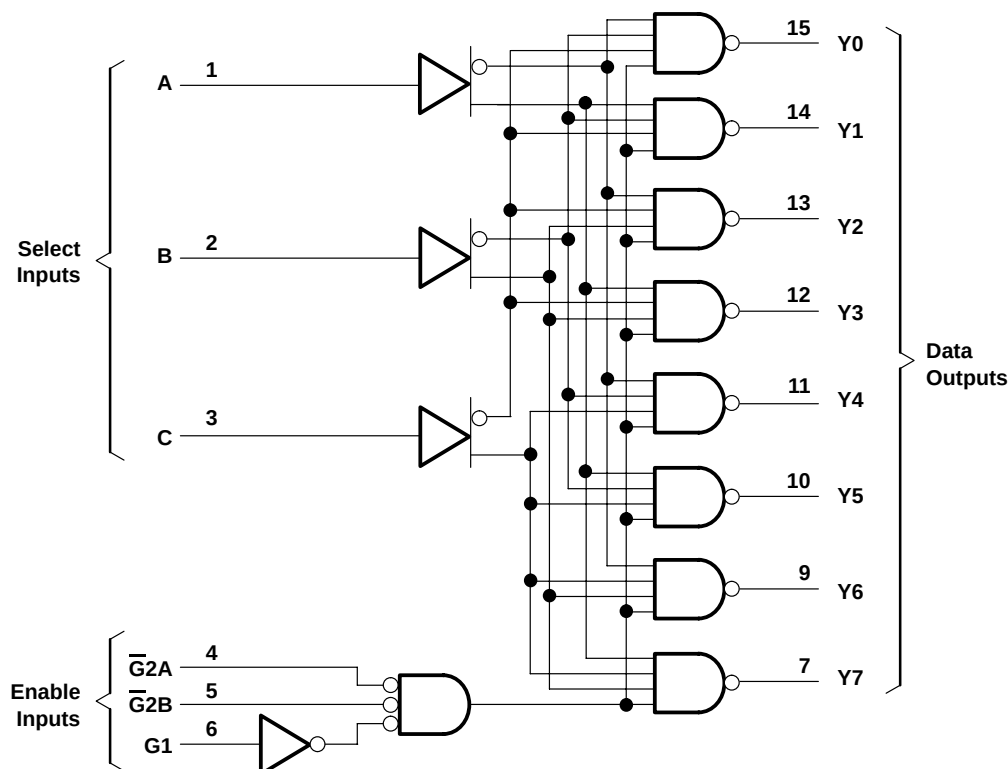
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logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

			SN54AHC138		SN74AHC138		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 3 V	2.1		2.1		
		V _{CC} = 5.5 V	3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 3 V	0.9		0.9		
		V _{CC} = 5.5 V	1.65		1.65		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 3.3 V ± 0.3 V	−4		−4		mA
		V _{CC} = 5 V ± 0.5 V	−8		−8		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 3.3 V ± 0.3 V	4		4		mA
		V _{CC} = 5 V ± 0.5 V	8		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100		100		ns/V
		V _{CC} = 5 V ± 0.5 V	20		20		
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^{\circ}\text{C}$			SN54AHC138		SN74AHC138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\text{ }\mu\text{A}$	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		2.48		
	$I_{OH} = -8\text{ mA}$	4.5 V	3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50\text{ }\mu\text{A}$	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	$I_{OL} = 4\text{ mA}$	3 V			0.36		0.5		0.44	
	$I_{OL} = 8\text{ mA}$	4.5 V			0.36		0.5		0.44	
I_I	$V_I = 5.5\text{ V or GND}$	0 V to 5.5 V			± 0.1		$\pm 1^*$		± 1	μA
I_{CC}	$V_I = V_{CC}\text{ or GND, } I_O = 0$	5.5 V			4		40		40	μA
C_i	$V_I = V_{CC}\text{ or GND}$	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0\text{ V}$.



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC138		SN74AHC138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A, B, C	Any Y	C _L = 15 pF	8.2*	11.4*	1*	13*	1	13	ns	
t _{PHL}				8.2*	11.4*	1*	13*	1	13		
t _{PLH}	G1	Any Y	C _L = 15 pF	8.1*	12.8*	1*	15*	1	15	ns	
t _{PHL}				8.1*	12.8*	1*	15*	1	15		
t _{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	C _L = 15 pF	8.2*	11.4*	1*	13.5*	1	13.5	ns	
t _{PHL}				8.2*	11.4*	1*	13.5*	1	13.5		
t _{PLH}	A, B, C	Any Y	C _L = 50 pF	10	15.8	1	18	1	18	ns	
t _{PHL}				10	15.8	1	18	1	18		
t _{PLH}	G1	Any Y	C _L = 50 pF	10.6	16.3	1	18.5	1	18.5	ns	
t _{PHL}				10.6	16.3	1	18.5	1	18.5		
t _{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	C _L = 50 pF	10.7	14.9	1	17	1	17	ns	
t _{PHL}				10.7	14.9	1	17	1	17		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC138		SN74AHC138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A, B, C	Any Y	C _L = 15 pF	5.7*	8.1*	1*	9.5*	1	9.5	ns	
t _{PHL}				5.7*	8.1*	1*	9.5*	1	9.5		
t _{PLH}	G1	Any Y	C _L = 15 pF	5.6*	8.1*	1*	9.5*	1	9.5	ns	
t _{PHL}				5.6*	8.1*	1*	9.5*	1	9.5		
t _{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	C _L = 15 pF	5.8*	8.1*	1*	9.5*	1	9.5	ns	
t _{PHL}				5.8*	8.1*	1*	9.5*	1	9.5		
t _{PLH}	A, B, C	Any Y	C _L = 50 pF	7.2	10.1	1	11.5	1	11.5	ns	
t _{PHL}				7.2	10.1	1	11.5	1	11.5		
t _{PLH}	G1	Any Y	C _L = 50 pF	7.1	10.1	1	11.5	1	11.5	ns	
t _{PHL}				7.1	10.1	1	11.5	1	11.5		
t _{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	C _L = 50 pF	7.3	10.1	1	11.5	1	11.5	ns	
t _{PHL}				7.3	10.1	1	11.5	1	11.5		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

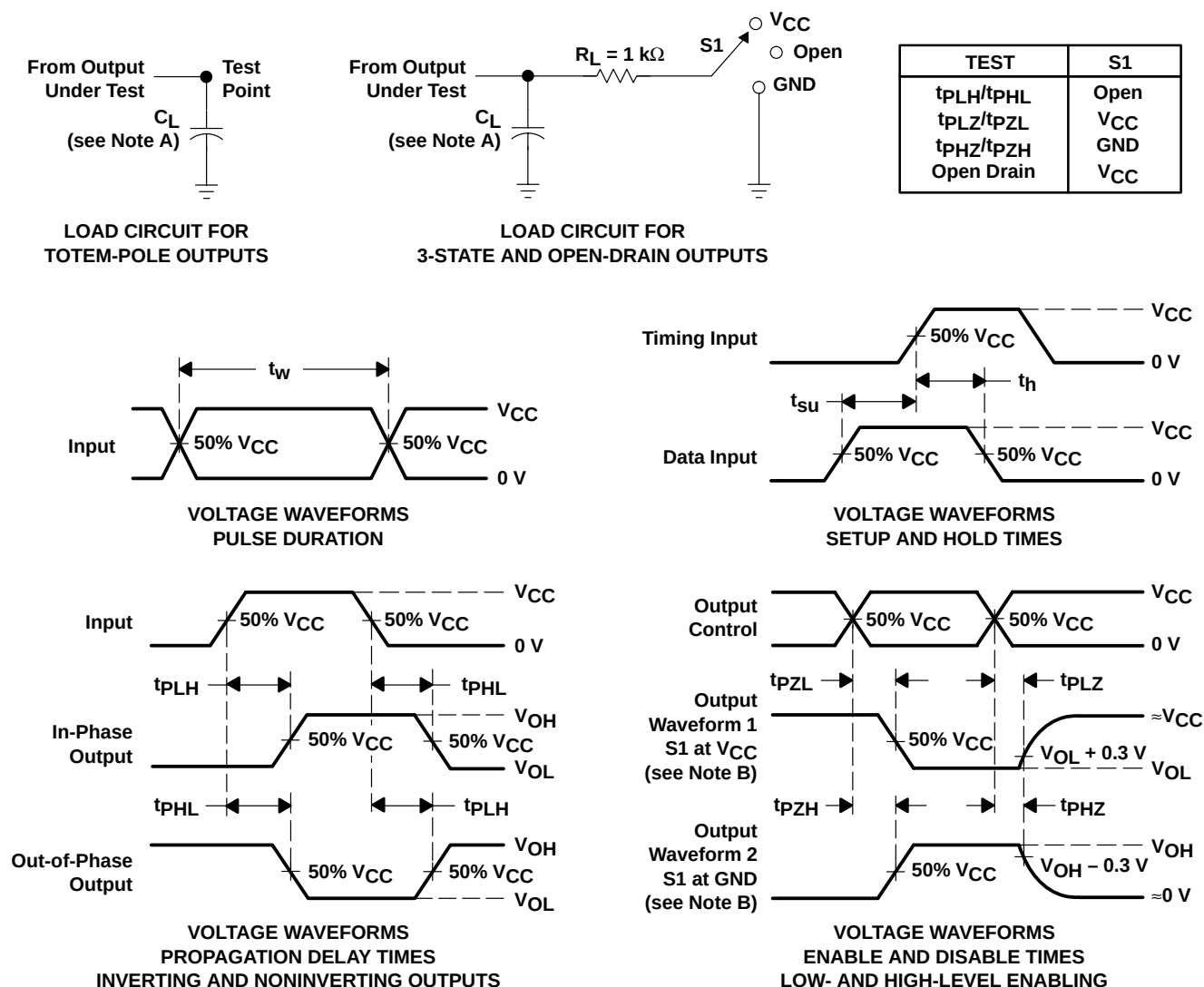
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	13	pF



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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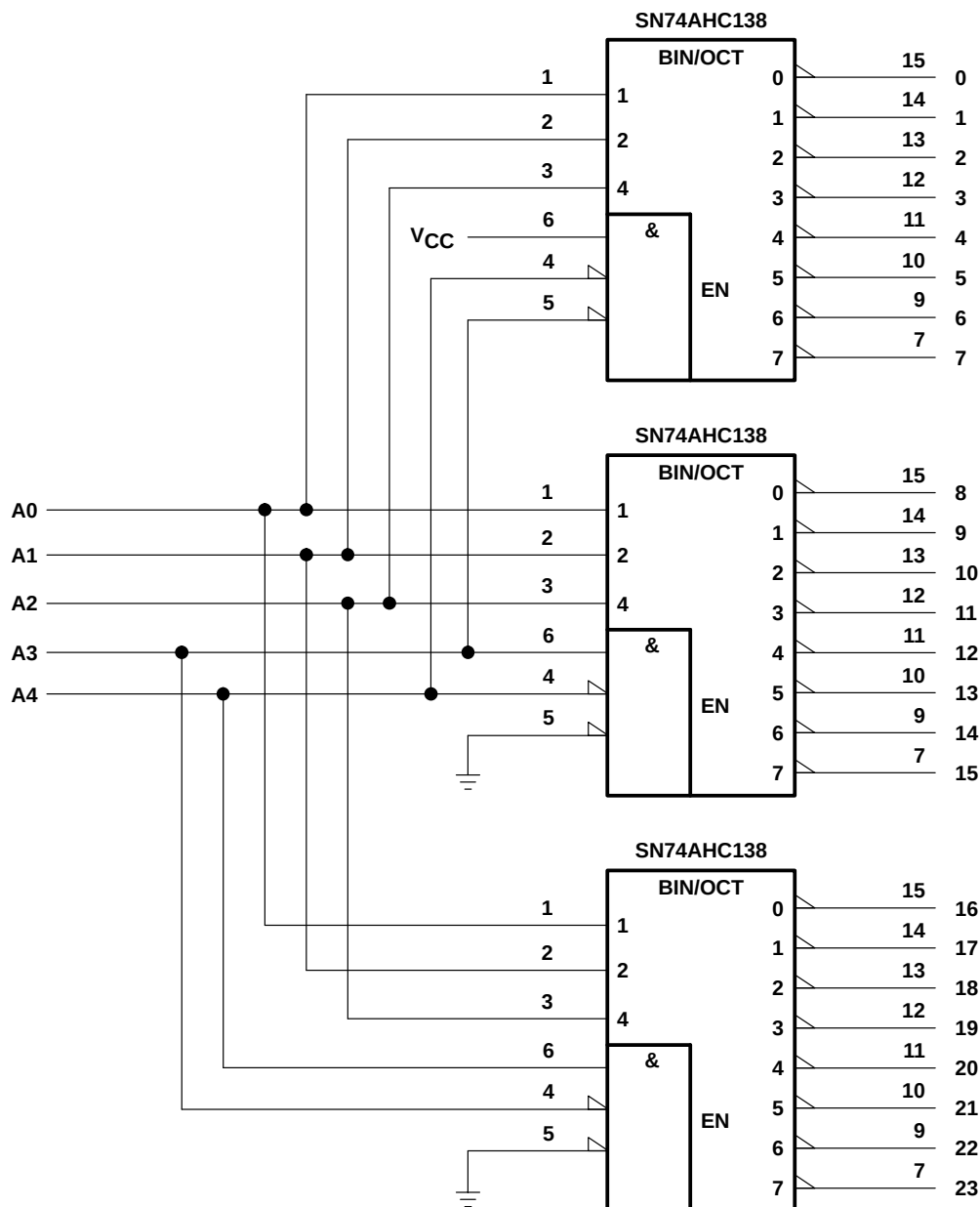


Figure 2. 24-Bit Decoding Scheme

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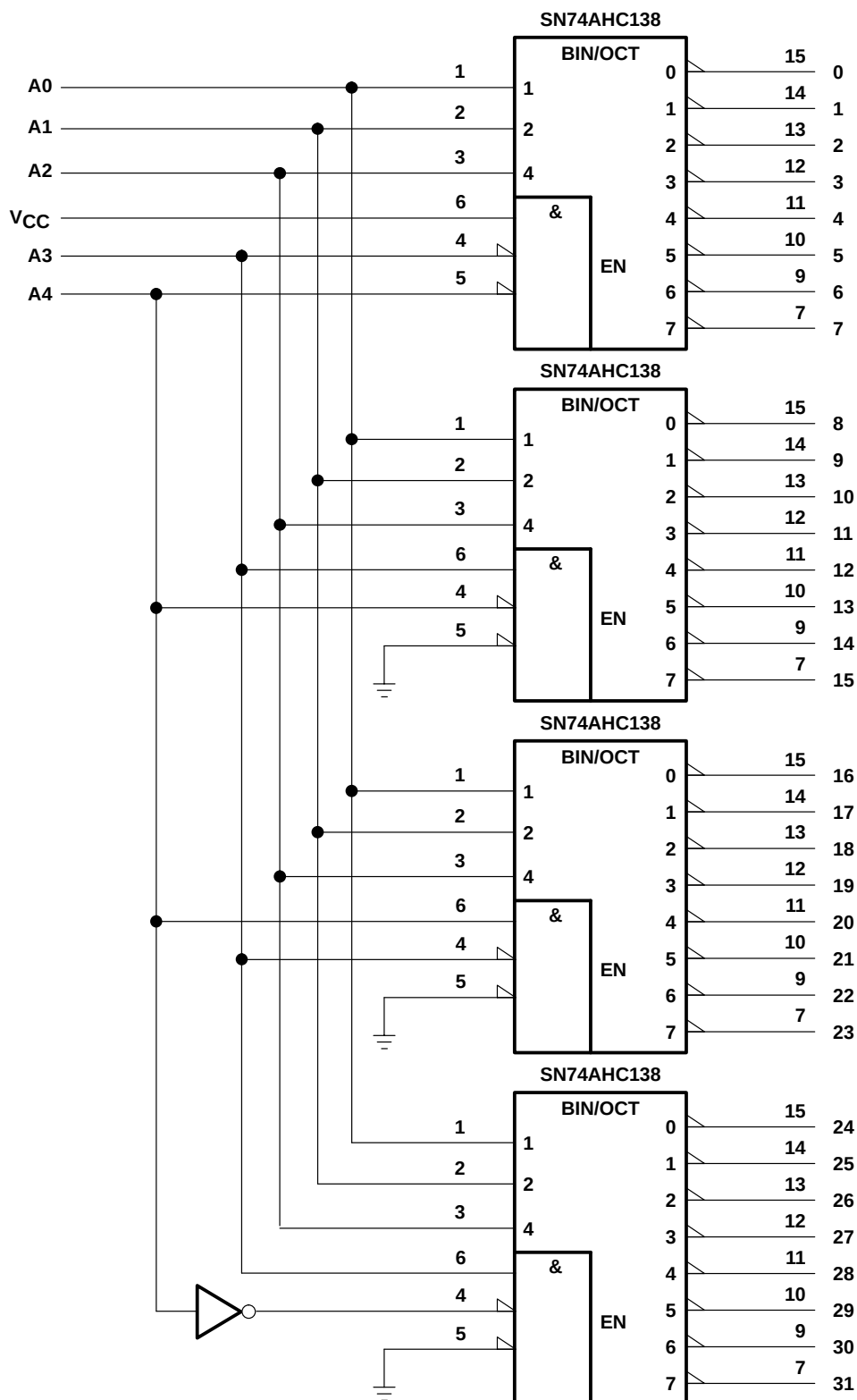


Figure 3. 32-Bit Decoding Scheme

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