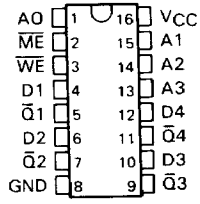
D1416, DECEMBER 1972—REVISED FEBRUARY 1984

- For Application as a "Scratch Pad" Memory with Nondestructive Read-Out
- Fully Decoded Memory Organized as 16 Words of Four Bits Each
- Fast Access Time . . . 33 ns Typical
- Diode-Clamped, Buffered Inputs
- Open-Collector Outputs Provide Wire-AND Capability
- Typical Power Dissipation . . . 375 mW
- Compatible with Most TTL Circuits

SN7489 . . . J OR N PACKAGE
(TOP VIEW)

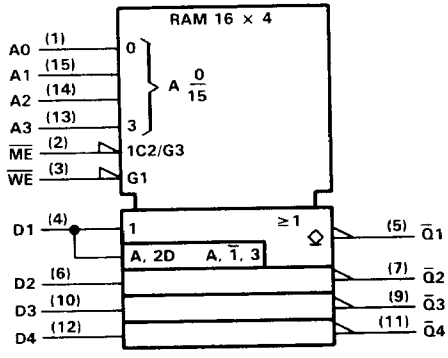


description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wired-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

logic symbol



FUNCTION TABLE

$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

write operation

Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

read operation

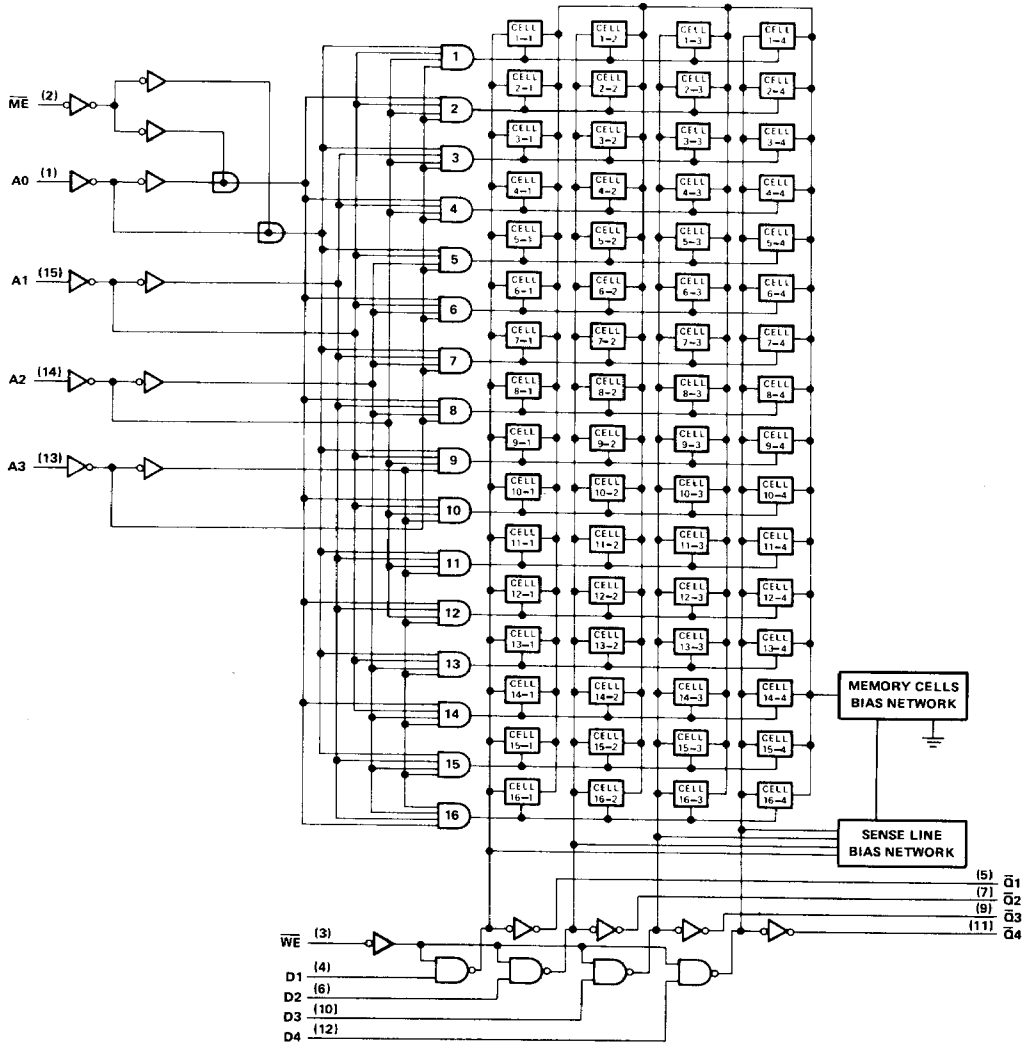
The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

5 RAMs

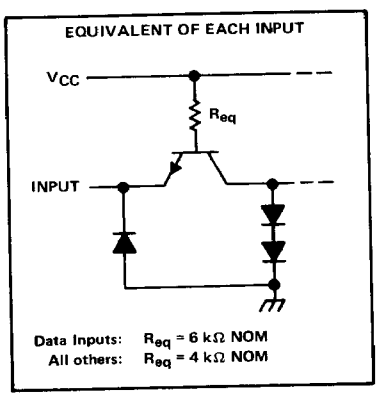
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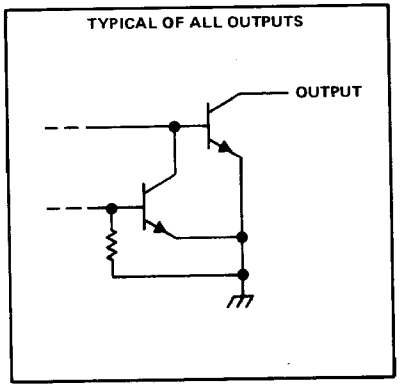
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logic diagram



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
High-level output voltage, V_{OH} (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage that should be applied to any output when it is in the off state.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Width of write-enable pulse, t_w	40			ns
Setup time, data input with respect to write enable, t_{su} (see Figure 1)	40			ns
Hold time, data input with respect to write enable, t_h (see Figure 1)	5			ns
Select input setup time with respect to write enable, t_{su}	0			ns
Select input hold time after writing, t_h (see Figure 1)	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,		I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,		V_{IH} = 2 V, V_{OH} = 5.5 V			20	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OL} = 12 mA			0.4	V
				I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,		V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,		V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,		V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX,		See Note 3		75	105	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz		V_O = 2.4 V,		6.5		pF

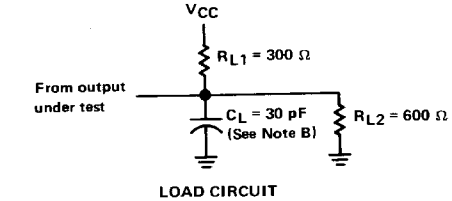
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: I_{CC} is measured with the memory enable grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

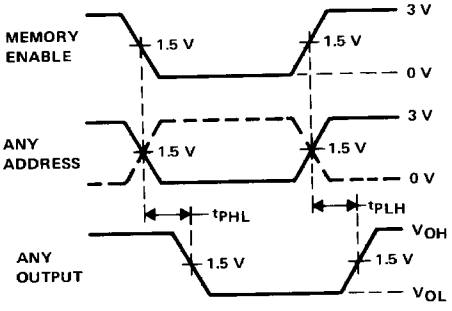
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from memory enable		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		26	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from memory enable				33	50	
t_{PLH}	Propagation delay time, low-to-high-level output from any address input				30	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from any address input				35	60	
t_{SR}	Sense recovery time after writing	Output initially high			39	70	ns
		Output initially low			48	70	

5 RAMs

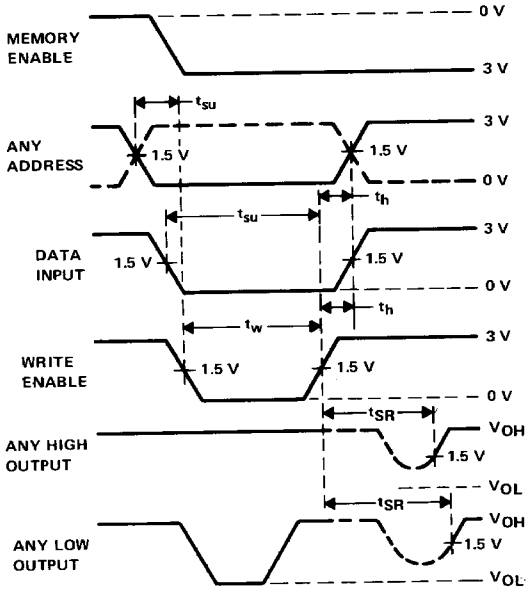
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



READ CYCLE



WRITE CYCLE FROM WRITE ENABLE

NOTES: A. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

5 RAMs

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

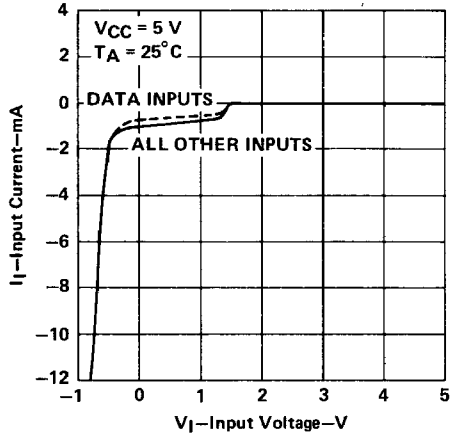


FIGURE 2

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

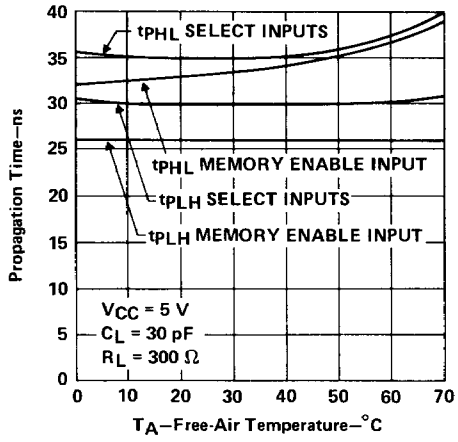


FIGURE 3

5 RAMs