

# SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688, SN74LS682, SN74LS684 THRU SN74LS688 8-BIT MAGNITUDE/IDENTITY COMPARATORS

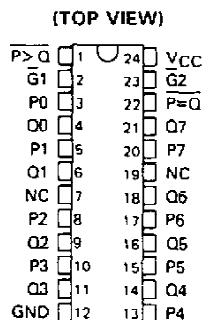
D2617, JANUARY 1981—REVISED MARCH 1988

SDLS008

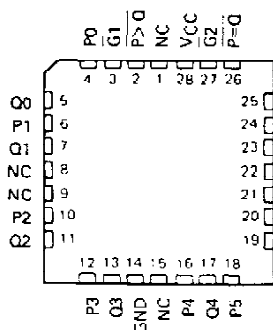
- Compares Two-8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-k $\Omega$  Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 . . . JT and NT 24-Pin, 300-Mil Packages

| TYPE      | P = Q | P > Q | OUTPUT<br>ENABLE | OUTPUT<br>CONFIGURATION | 20-k $\Omega$<br>PULLUP |
|-----------|-------|-------|------------------|-------------------------|-------------------------|
| 'LS682    | yes   | yes   | no               | totem-pole              | yes                     |
| 'LS684    | yes   | yes   | no               | totem-pole              | no                      |
| 'LS685    | yes   | yes   | no               | open-collector          | no                      |
| SN74LS686 | yes   | yes   | yes              | totem-pole              | no                      |
| 'LS687    | yes   | yes   | yes              | open-collector          | no                      |
| 'LS688    | yes   | no    | yes              | totem-pole              | no                      |

SN54LS687 . . . JT PACKAGE  
SN74LS686, SN74LS687 . . . DW OR NT PACKAGE

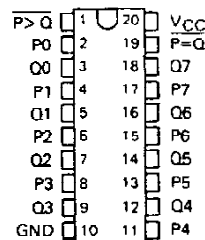


SN54LS687 . . . FK PACKAGE  
(TOP VIEW)

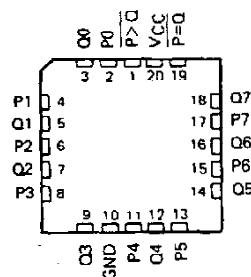


NC—No internal connection

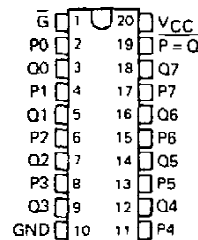
SN54LS682, SN54LS684, SN54LS685 . . . J PACKAGE  
SN74LS682, SN74LS684, SN74LS685 . . . DW OR N PACKAGE  
(TOP VIEW)



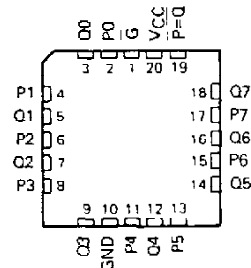
SN54LS682, SN54LS684, SN54LS685 . . . FK PACKAGE  
(TOP VIEW)



SN54LS688 . . . J PACKAGE  
SN74LS688 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54LS688 . . . FK PACKAGE  
(TOP VIEW)



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**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688**  
**SN74LS682, SN74LS684 THRU SN74LS688**  
**8-BIT MAGNITUDE/IDENTITY COMPARATORS**

**description**

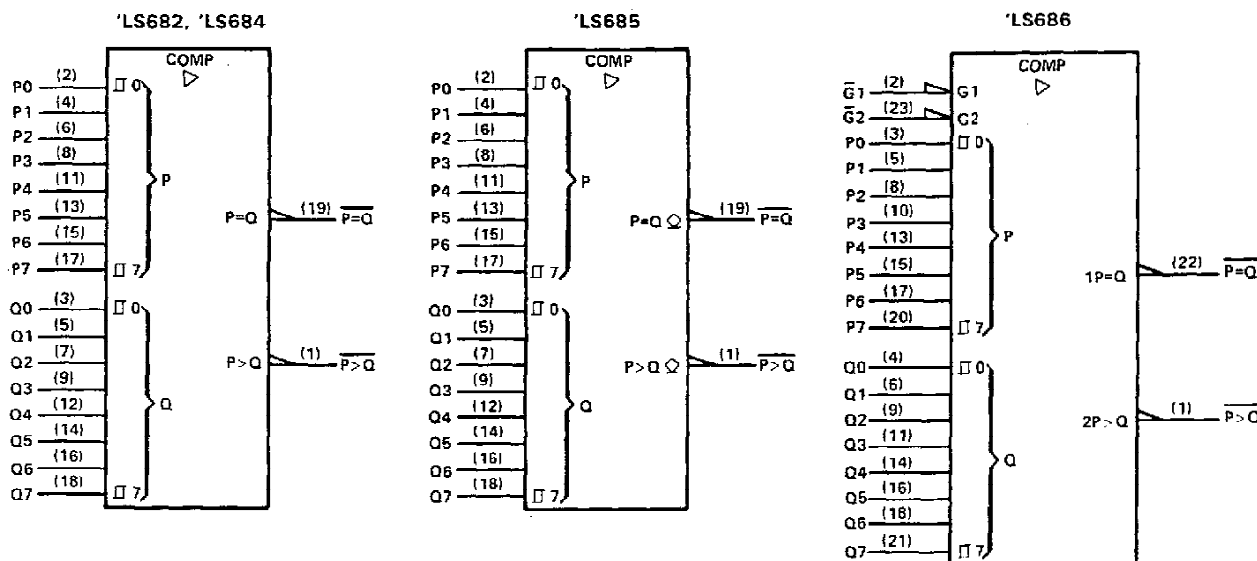
These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide  $\overline{P=Q}$  outputs and all except 'LS688 provide  $\overline{P>Q}$  outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-k $\Omega$  pullup termination resistors on the Q inputs for analog or switch data.

**FUNCTION TABLE**

| INPUTS |                               |                 | OUTPUTS          |                  |
|--------|-------------------------------|-----------------|------------------|------------------|
| DATA   | ENABLES                       |                 | $\overline{P=Q}$ | $\overline{P>Q}$ |
| P, Q   | $\overline{G}, \overline{G1}$ | $\overline{G2}$ |                  |                  |
| P=Q    | L                             | X               | L                | H                |
| P>Q    | X                             | L               | H                | L                |
| P<Q    | X                             | X               | H                | H                |
| P=Q    | H                             | X               | H                | H                |
| P>Q    | X                             | H               | H                | H                |
| X      | H                             | H               | H                | H                |

- NOTES: 1. The last three lines of the function table applies only to the devices having enable inputs, i.e., 'LS686 thru 'LS688.
2. The  $\overline{P<Q}$  function can be generated by applying the  $\overline{P=Q}$  and  $\overline{P>Q}$  outputs to a 2-input NAND gate.
3. For 'LS686 and 'LS687,  $\overline{G1}$  enables  $\overline{P=Q}$  and  $\overline{G2}$  enables  $\overline{P>Q}$ .

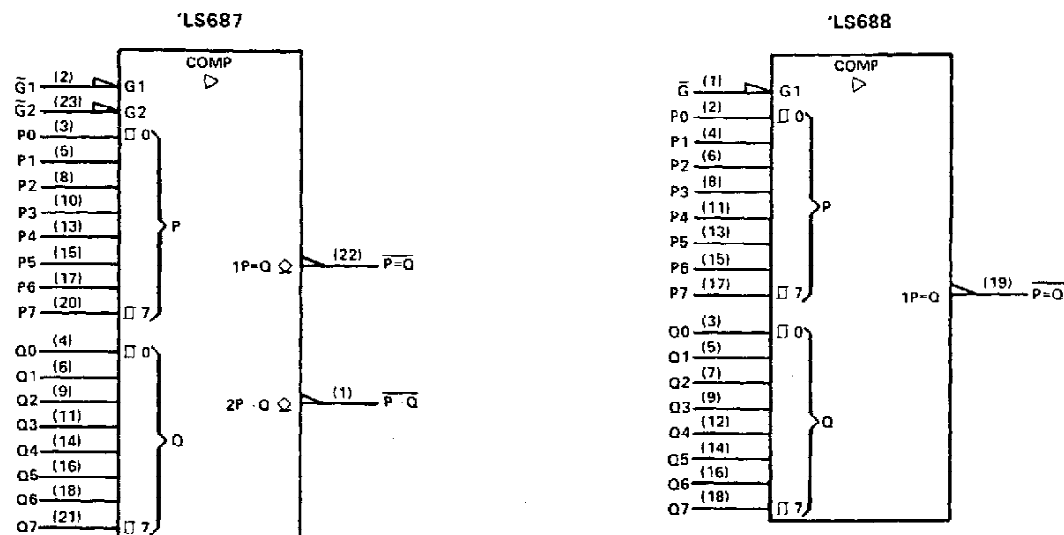
**logic symbols†**



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

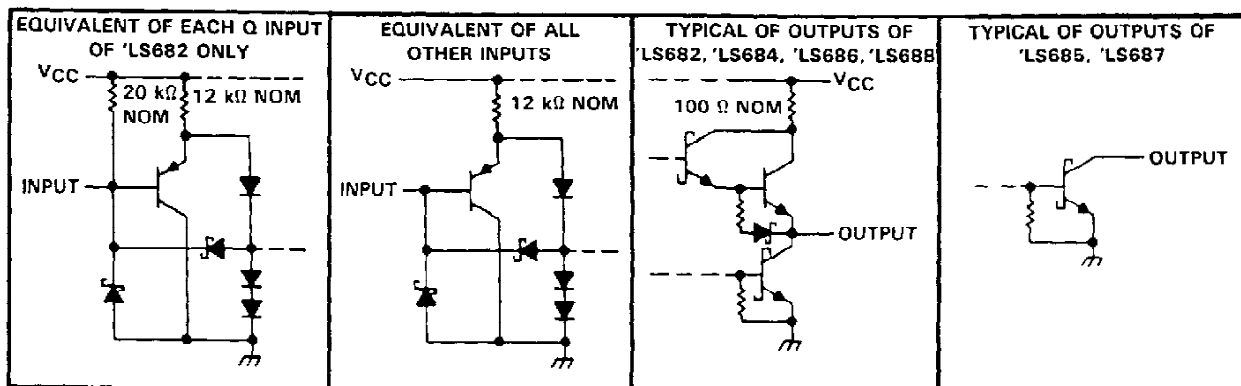
**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688,  
SN74LS682, SN74LS684 THRU SN74LS688  
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

logic symbols† (continued)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

**schematics of inputs and outputs**

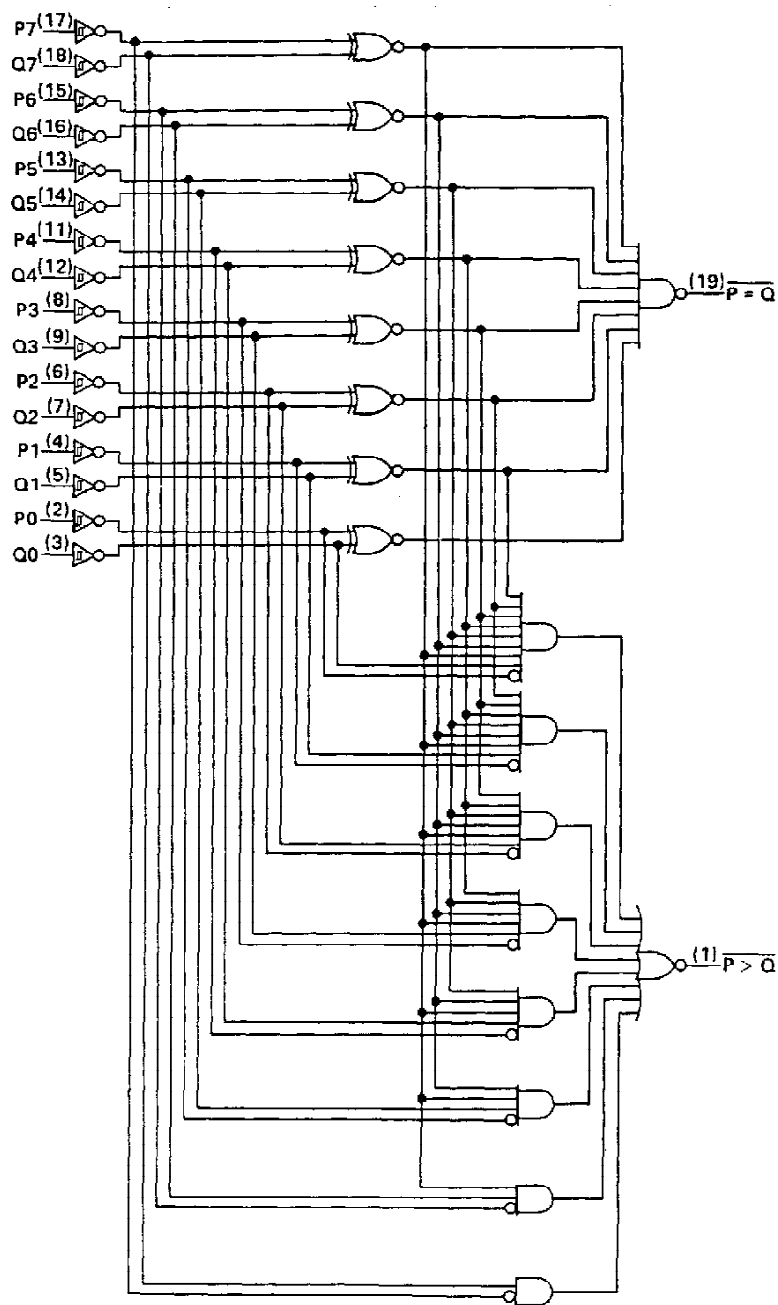


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**SN54LS682, SN54LS684, SN54LS685  
SN74LS682, SN74LS684, SN74LS685  
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

'LS682, 'LS684, 'LS685 logic diagram (positive logic)



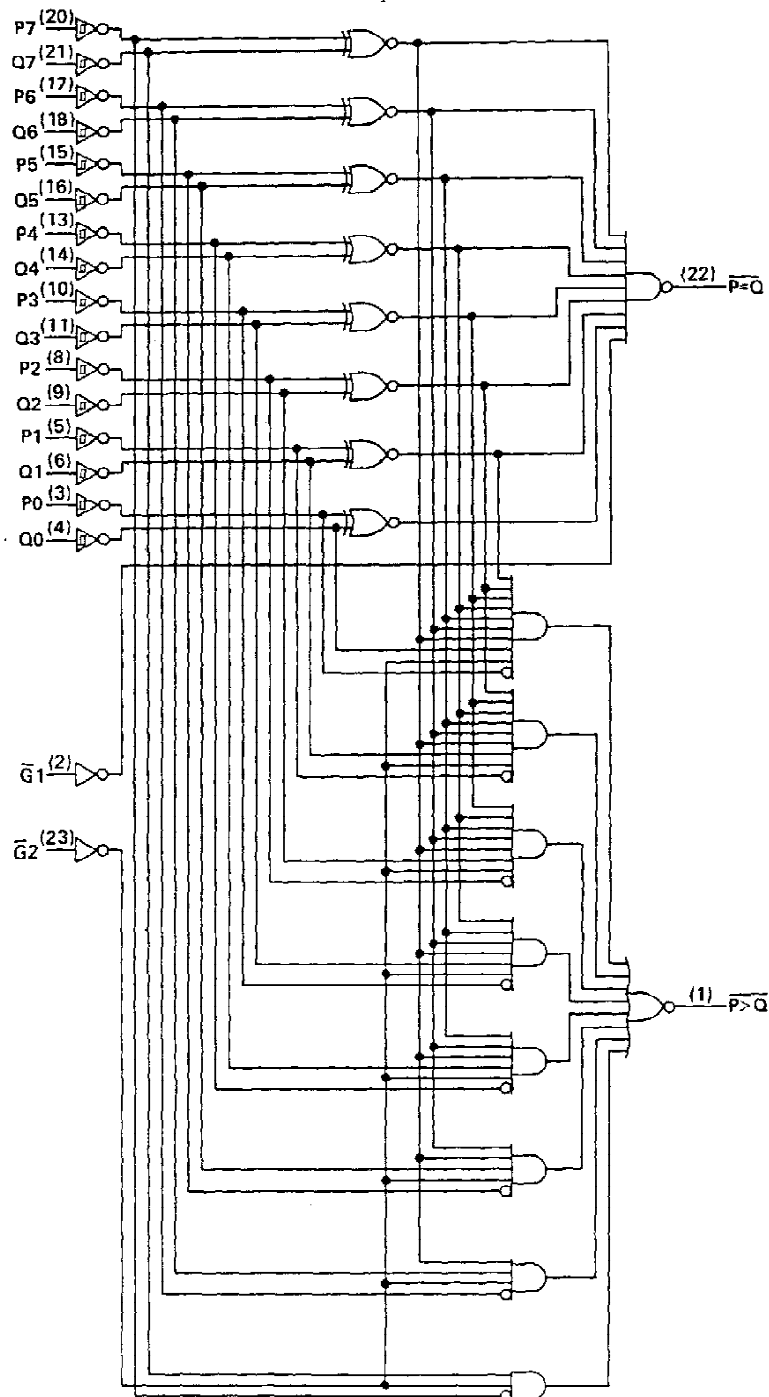
Pin numbers shown are for DW, J, and N packages.

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SN54LS687  
SN74LS686, SN74LS687  
8-BIT MAGNITUDE/IDENTITY COMPARATORS

'LS686, 'LS687 logic diagram (positive logic)



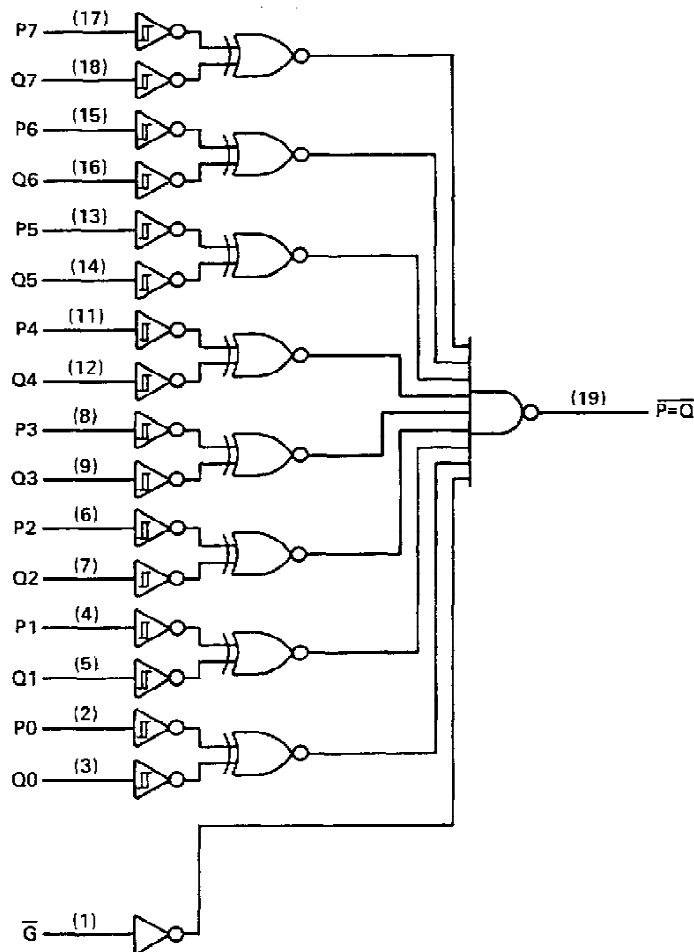
Pin numbers shown are for DW, JT, and NT packages.

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**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688  
SN74LS682, SN74LS684 THRU SN74LS688  
8-BIT IDENTITY COMPARATORS**

'LS688 logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

|                                                       |                |
|-------------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)                 | 7 V            |
| Input voltage: Q inputs of 'LS682                     | 5.5 V          |
| All other inputs                                      | 7 V            |
| Off-state output voltage: 'LS685, 'LS687              | 7 V            |
| Operating free-air temperature range:                 |                |
| SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688 | -55°C to 125°C |
| SN74LS682, SN74LS684 thru SN74LS688                   | 0°C to 70°C    |
| Storage temperature range                             | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

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**SN54LS682, SN54LS684, SN54LS688**  
**SN74LS682, SN74LS684, SN74LS686, SN74LS688**  
**8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

**recommended operating conditions**

|                                       | SN54LS <sup>†</sup> |     |      | SN74LS <sup>†</sup> |     |      | UNIT    |
|---------------------------------------|---------------------|-----|------|---------------------|-----|------|---------|
|                                       | MIN                 | NOM | MAX  | MIN                 | NOM | MAX  |         |
| Supply voltage, $V_{CC}$              | 4.5                 | 5   | 5.5  | 4.85                | 5   | 5.25 | V       |
| High-level output current, $I_{OH}$   |                     |     | -400 |                     |     | -400 | $\mu$ A |
| Low-level output current, $I_{OL}$    |                     |     | 12   |                     |     | 24   | mA      |
| Operating free-air temperature, $T_A$ | -55                 |     | 125  | 0                   |     | 70   | °C      |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER         |                                        |                                          | TEST CONDITIONS†                                                                                  | SN54LS' |      | SN74LS' |      | UNIT          |
|-------------------|----------------------------------------|------------------------------------------|---------------------------------------------------------------------------------------------------|---------|------|---------|------|---------------|
|                   |                                        |                                          |                                                                                                   | MIN     | TYP‡ | MAX     | MIN  |               |
| $V_{IH}$          | High-level input voltage               |                                          |                                                                                                   | 2       |      | 2       |      | V             |
| $V_{IL}$          | Low-level input voltage                |                                          |                                                                                                   | 0.7     |      | 0.8     |      | V             |
| $V_{T+} - V_{T-}$ | Hysteresis                             | P or Q inputs                            | $V_{CC} = \text{MIN}$                                                                             | 0.4     |      | 0.4     |      | V             |
| $V_{IK}$          | Input clamp voltage                    |                                          | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$                                                       | -1.5    |      | -1.5    |      | V             |
| $V_{OH}$          | High-level output voltage              |                                          | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}, I_{OH} = -400 \mu\text{A}$ | 2.5     |      | 2.7     |      | V             |
| $V_{OL}$          | Low-level output voltage               |                                          | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}, I_{OL} = 12 \text{ mA}$    | 0.25    | 0.4  | 0.25    | 0.4  | V             |
|                   |                                        |                                          | $I_{OL} = 24 \text{ mA}$                                                                          |         |      | 0.35    | 0.5  |               |
| $I_I$             | Input current at maximum input voltage | Q inputs, 'LS682                         | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$                                                        | 0.1     |      | 0.1     |      | mA            |
|                   | All other inputs                       | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$ |                                                                                                   |         |      |         |      |               |
| $I_{IH}$          | High-level input current               |                                          | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$                                                        | 20      |      | 20      |      | $\mu\text{A}$ |
| $I_{IL}$          | Low-level input current                | Q inputs, 'LS682                         | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$                                                        | -0.4    |      | -0.4    |      | mA            |
|                   |                                        | All other inputs                         |                                                                                                   | -0.2    |      | -0.2    |      |               |
| $I_{OS}^{\S}$     | Short-circuit output current           |                                          | $V_{CC} = \text{MAX}, V_O = 0$                                                                    | -20     | -100 | -20     | -100 | mA            |
| $I_{CC}$          | Supply current                         | 'LS682                                   | $V_{CC} = \text{MAX},$ See Note 1                                                                 | 42      | 70   | 42      | 70   | mA            |
|                   |                                        | 'LS684                                   |                                                                                                   | 40      | 65   | 40      | 65   |               |
|                   |                                        | 'LS686                                   |                                                                                                   | 44      | 75   | 44      | 75   |               |
|                   |                                        | 'LS688                                   |                                                                                                   | 40      | 65   | 40      | 65   |               |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

<sup>\S</sup> Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1:  $I_{CC}$  is measured with any  $\bar{Q}$  inputs grounded, all other inputs at 4.5 V, and all outputs open.

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**SN54LS682, SN54LS684, SN54LS688**  
**SN74LS682, SN74LS684, SN74LS686, SN74LS688**  
**8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER† | FROM<br>(INPUTS)              | TO<br>(OUTPUT)                | TEST<br>CONDITIONS                                                   | 'LS682 |         | 'LS684 |         | 'LS686 |         | 'LS688 |         | UNIT |
|------------|-------------------------------|-------------------------------|----------------------------------------------------------------------|--------|---------|--------|---------|--------|---------|--------|---------|------|
|            |                               |                               |                                                                      | MIN    | TYP MAX | MIN    | TYP MAX | MIN    | TYP MAX | MIN    | TYP MAX |      |
| tPLH       | P                             | $\overline{P} = \overline{Q}$ | RL = 667 Ω,<br>CL = 45 pF,<br>All other<br>inputs low,<br>See Note 2 | 13     | 25      | 15     | 25      | 13     | 25      | 12     | 18      | ns   |
| tPHL       |                               |                               |                                                                      | 15     | 25      | 17     | 25      | 20     | 30      | 17     | 23      |      |
| tPLH       | Q                             | $\overline{P} = \overline{Q}$ |                                                                      | 14     | 25      | 16     | 25      | 13     | 25      | 12     | 18      | ns   |
| tPHL       |                               |                               |                                                                      | 15     | 25      | 15     | 25      | 21     | 30      | 17     | 23      |      |
| tPLH       | $\overline{Q}, \overline{Q}1$ | $\overline{P} = \overline{Q}$ |                                                                      |        |         |        |         | 11     | 20      | 12     | 18      | ns   |
| tPHL       |                               |                               |                                                                      |        |         |        |         | 19     | 30      | 13     | 20      |      |
| tPLH       | P                             | $\overline{P} > \overline{Q}$ |                                                                      | 20     | 30      | 22     | 30      | 19     | 30      |        |         | ns   |
| tPHL       |                               |                               |                                                                      | 15     | 30      | 17     | 30      | 15     | 30      |        |         |      |
| tPLH       | Q                             | $\overline{P} > \overline{Q}$ |                                                                      | 21     | 30      | 24     | 30      | 18     | 30      |        |         | ns   |
| tPHL       |                               |                               |                                                                      | 19     | 30      | 20     | 30      | 19     | 30      |        |         |      |
| tPLH       | $\overline{Q}2$               | $\overline{P} > \overline{Q}$ |                                                                      |        |         |        |         | 21     | 30      |        |         | ns   |
| tPHL       |                               |                               |                                                                      |        |         |        |         | 16     | 25      |        |         |      |

† $t_{PLH}$  = propagation delay time, low-to-high-level outputs;  $t_{PHL}$  = propagation delay time, high-to-low-level output.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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**SN54LS685, SN54LS687**  
**SN74LS685, SN74LS687, SN74LS688**  
**8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

**recommended operating conditions**

|                                       | SN54LS <sup>*</sup> |     |     | SN74LS <sup>*</sup> |     |      | UNIT |
|---------------------------------------|---------------------|-----|-----|---------------------|-----|------|------|
|                                       | MIN                 | NOM | MAX | MIN                 | NOM | MAX  |      |
| Supply voltage, $V_{CC}$              | 4.5                 | 5   | 5.5 | 4.85                | 5   | 5.25 | V    |
| High-level output current, $V_{OH}$   |                     |     | 5.5 |                     |     | 5.5  | V    |
| Low-level output current, $I_{OL}$    |                     |     | 12  |                     |     | 24   | mA   |
| Operating free-air temperature, $T_A$ | -55                 |     | 125 | 0                   |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER         |                           | TEST CONDITIONS <sup>†</sup>                                                            | SN54LS <sup>*</sup> |      |      | SN74LS <sup>*</sup> |      |      | UNIT          |
|-------------------|---------------------------|-----------------------------------------------------------------------------------------|---------------------|------|------|---------------------|------|------|---------------|
|                   |                           |                                                                                         | MIN                 | TYP  | MAX  | MIN                 | TYP  | MAX  |               |
| $V_{IH}$          | High-level input voltage  |                                                                                         | 2                   |      |      | 2                   |      |      | V             |
| $V_{IL}$          | Low-level input voltage   |                                                                                         |                     |      | 0.7  |                     |      | 0.8  | V             |
| $V_{T+} - V_{T-}$ | Hysteresis                | P or Q inputs                                                                           |                     | 0.4  |      |                     | 0.4  |      | V             |
| $V_{IK}$          | Input clamp voltage       | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$                                             |                     |      | -1.5 |                     |      | -1.5 | V             |
| $I_{OH}$          | High-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, V_{OH} = 5.5 \text{ V}$ |                     |      | 250  |                     |      | 100  | $\mu\text{A}$ |
| $V_{OL}$          | Low-level output voltage  | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OL} = 12 \text{ mA}$ | 0.25                | 0.4  |      | 0.25                | 0.4  |      | V             |
|                   |                           | $I_{OL} = 24 \text{ mA}$                                                                |                     |      |      | 0.35                | 0.5  |      |               |
| $I_I$             |                           | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$                                                |                     | 0.1  |      |                     | 0.1  |      | mA            |
| $I_{IH}$          | High-level input current  | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$                                              |                     | 20   |      |                     | 20   |      | $\mu\text{A}$ |
| $I_{IL}$          | Low-level input current   | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$                                              |                     | -0.2 |      |                     | -0.2 |      | mA            |
| $I_{CC}$          | Supply current            | 'LS685                                                                                  | 40                  | 65   |      | 40                  | 65   |      | mA            |
|                   |                           | 'LS687                                                                                  | 44                  | 75   |      | 44                  | 75   |      |               |

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

<sup>\*</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

NOTE 1:  $I_{CC}$  is measure with any  $\bar{Q}$  inputs grounded, all other inputs at 4.5 V, and all outputs open.

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SN54LS685, SN54LS687

SN74LS685, SN74LS687

8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER        | FROM<br>(INPUT)               | TO<br>(OUTPUT)   | TEST CONDITIONS                                                                              | 'LS685 |     |     | 'LS687 |     |     | UNIT |
|------------------|-------------------------------|------------------|----------------------------------------------------------------------------------------------|--------|-----|-----|--------|-----|-----|------|
|                  |                               |                  |                                                                                              | MIN    | TYP | MAX | MIN    | TYP | MAX |      |
| t <sub>PLH</sub> | P                             | $\overline{P=Q}$ | R <sub>L</sub> = 667 Ω,<br>C <sub>L</sub> = 45 pF,<br>All other<br>inputs low,<br>See Note 2 |        | 30  | 45  |        | 24  | 35  | ns   |
| t <sub>PHL</sub> |                               |                  |                                                                                              |        | 19  | 35  |        | 20  | 30  |      |
| t <sub>PLH</sub> | Q                             | $\overline{P=Q}$ |                                                                                              |        | 24  | 45  |        | 24  | 35  | ns   |
| t <sub>PHL</sub> |                               |                  |                                                                                              |        | 23  | 35  |        | 20  | 30  |      |
| t <sub>PLH</sub> | $\overline{Q}, \overline{Q1}$ | $\overline{P=Q}$ |                                                                                              |        |     |     |        | 21  | 35  | ns   |
| t <sub>PHL</sub> |                               |                  |                                                                                              |        |     |     |        | 18  | 30  |      |
| t <sub>PLH</sub> | P                             | $\overline{P>Q}$ |                                                                                              |        | 32  | 45  |        | 24  | 35  | ns   |
| t <sub>PHL</sub> |                               |                  |                                                                                              |        | 16  | 35  |        | 16  | 30  |      |
| t <sub>PLH</sub> | Q                             | $\overline{P>Q}$ |                                                                                              |        | 30  | 45  |        | 24  | 35  | ns   |
| t <sub>PHL</sub> |                               |                  |                                                                                              |        | 20  | 35  |        | 16  | 30  |      |
| t <sub>PLH</sub> | $\overline{Q2}$               | $\overline{P>Q}$ |                                                                                              |        |     |     |        | 24  | 35  | ns   |
| t <sub>PHL</sub> |                               |                  |                                                                                              |        |     |     |        | 15  | 30  |      |

<sup>†</sup> $t_{PLH}$  = propagation delay time, low-to-high-level outputs;  $t_{PHL}$  = propagation delay time, high-to-low-level output.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)       | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------------|-------------------------|
| 8415101RA        | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415101RA<br>SNJ54LS682J      | <a href="#">Samples</a> |
| 8415101SA        | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415101SA<br>SNJ54LS682W      | <a href="#">Samples</a> |
| 8415101SA        | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415101SA<br>SNJ54LS682W      | <a href="#">Samples</a> |
| 84152012A        | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 84152012A<br>SNJ54LS<br>684FK | <a href="#">Samples</a> |
| 8415201RA        | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415201RA<br>SNJ54LS684J      | <a href="#">Samples</a> |
| 84153012A        | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 84153012A<br>SNJ54LS<br>688FK | <a href="#">Samples</a> |
| 8415301RA        | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415301RA<br>SNJ54LS688J      | <a href="#">Samples</a> |
| 8415301SA        | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415301SA<br>SNJ54LS688W      | <a href="#">Samples</a> |
| SN54LS682J       | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | SN54LS682J                    | <a href="#">Samples</a> |
| SN54LS682J       | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | SN54LS682J                    | <a href="#">Samples</a> |
| SN54LS684J       | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | SN54LS684J                    | <a href="#">Samples</a> |
| SN54LS688J       | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | SN54LS688J                    | <a href="#">Samples</a> |
| SN74LS682DW      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS682                         | <a href="#">Samples</a> |
| SN74LS682DW      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS682                         | <a href="#">Samples</a> |
| SN74LS682DWR     | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS682                         | <a href="#">Samples</a> |
| SN74LS682DWR     | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS682                         | <a href="#">Samples</a> |
| SN74LS682DWRG4   | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS682                         | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)  | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LS682DWRG4   | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS682                    | <a href="#">Samples</a> |
| SN74LS682N       | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74LS682N               | <a href="#">Samples</a> |
| SN74LS682N       | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74LS682N               | <a href="#">Samples</a> |
| SN74LS682NSR     | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 74LS682                  | <a href="#">Samples</a> |
| SN74LS682NSR     | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 74LS682                  | <a href="#">Samples</a> |
| SN74LS684DW      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS684                    | <a href="#">Samples</a> |
| SN74LS684DWR     | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS684                    | <a href="#">Samples</a> |
| SN74LS684N       | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74LS684N               | <a href="#">Samples</a> |
| SN74LS684NSR     | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 74LS684                  | <a href="#">Samples</a> |
| SN74LS688DW      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS688                    | <a href="#">Samples</a> |
| SN74LS688DWR     | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS688                    | <a href="#">Samples</a> |
| SN74LS688N       | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74LS688N               | <a href="#">Samples</a> |
| SN74LS688NE4     | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74LS688N               | <a href="#">Samples</a> |
| SN74LS688NSR     | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 74LS688                  | <a href="#">Samples</a> |
| SNJ54LS682J      | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415101RA<br>SNJ54LS682J | <a href="#">Samples</a> |
| SNJ54LS682J      | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415101RA<br>SNJ54LS682J | <a href="#">Samples</a> |
| SNJ54LS682W      | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415101SA<br>SNJ54LS682W | <a href="#">Samples</a> |
| SNJ54LS682W      | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415101SA<br>SNJ54LS682W | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)       | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|-------------------------|----------------------|--------------|-------------------------------|-------------------------|
| SNJ54LS684FK     | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD             | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 84152012A<br>SNJ54LS<br>684FK | <a href="#">Samples</a> |
| SNJ54LS684J      | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD             | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415201RA<br>SNJ54LS684J      | <a href="#">Samples</a> |
| SNJ54LS688FK     | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD             | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 84153012A<br>SNJ54LS<br>688FK | <a href="#">Samples</a> |
| SNJ54LS688J      | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD             | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415301RA<br>SNJ54LS688J      | <a href="#">Samples</a> |
| SNJ54LS688W      | ACTIVE        | CFP          | W                  | 20   | 1              | TBD             | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8415301SA<br>SNJ54LS688W      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LS682, SN54LS684, SN54LS688, SN74LS682, SN74LS684, SN74LS688 :**

- Catalog: [SN74LS682](#), [SN74LS684](#), [SN74LS688](#)
- Military: [SN54LS682](#), [SN54LS684](#), [SN54LS688](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS682DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LS682NSR | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LS684DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LS684NSR | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LS688DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LS688NSR | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

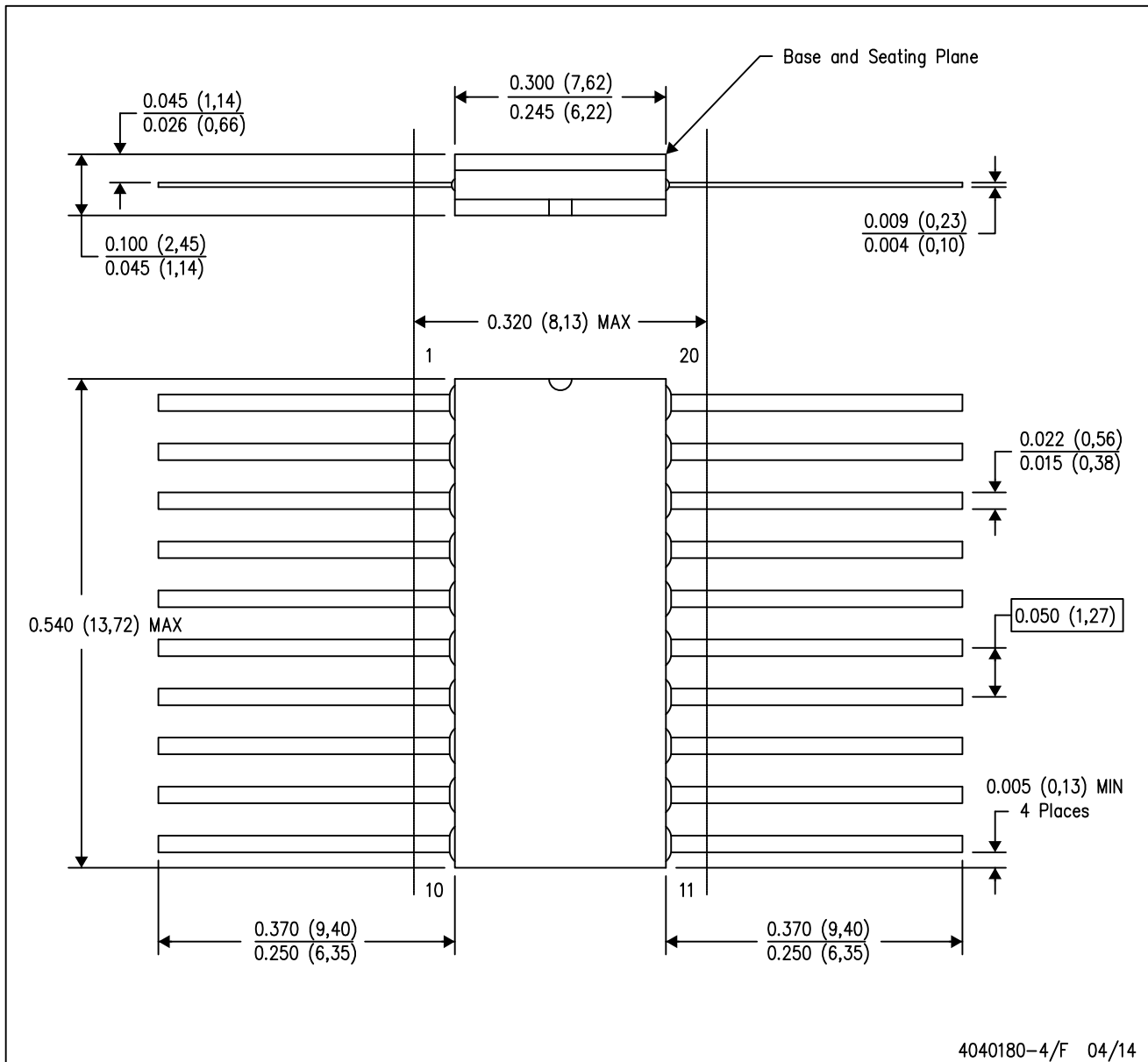


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS682DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LS682NSR | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LS684DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LS684NSR | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LS688DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LS688NSR | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



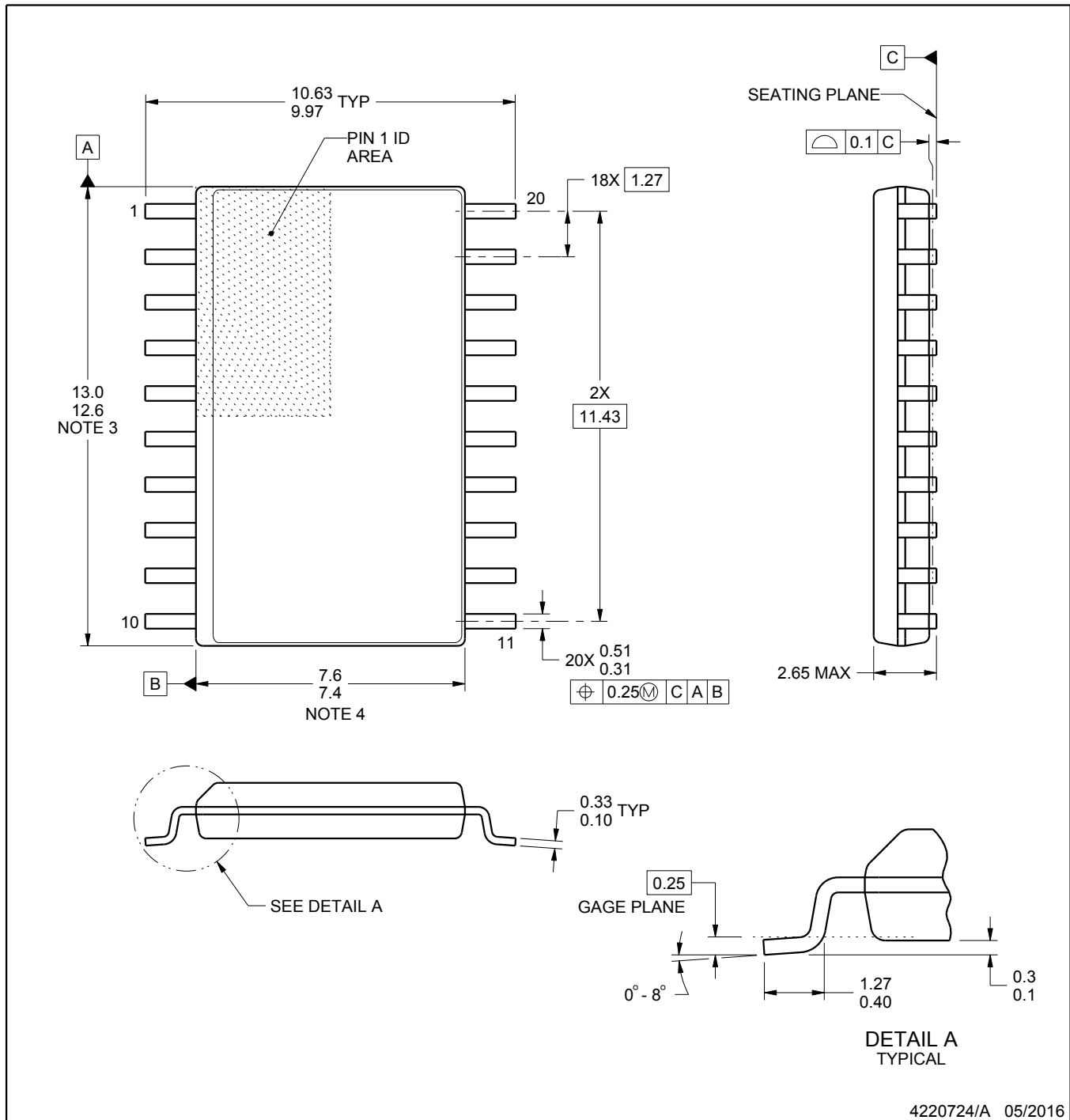
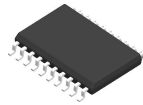
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



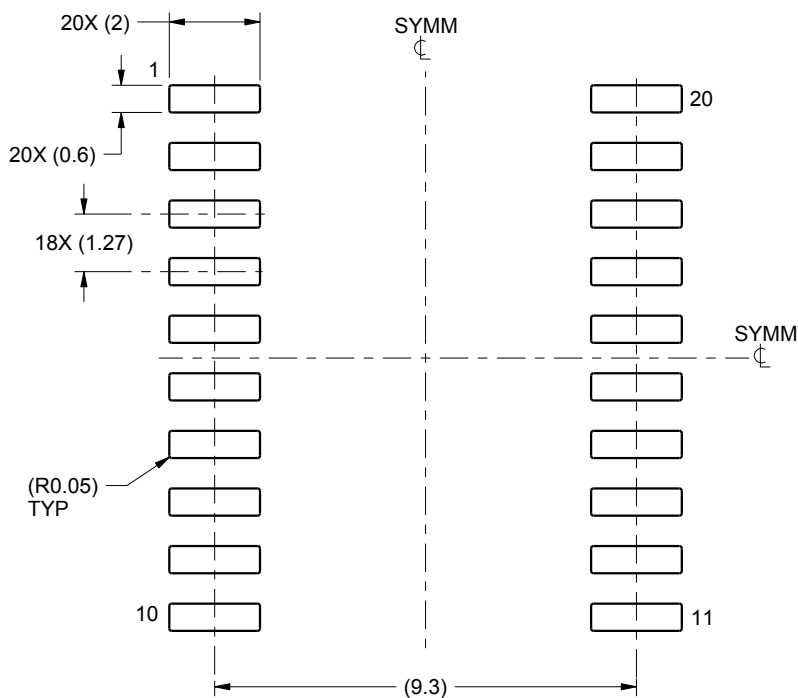
## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

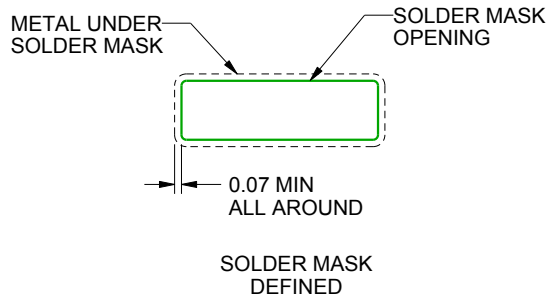
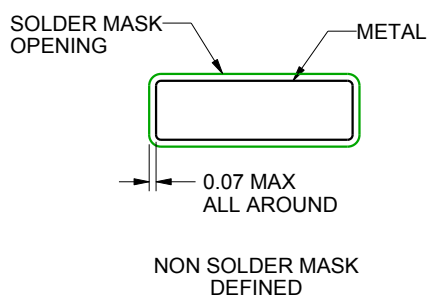
**DW0020A**

### SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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