

SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

SDLS007

D2635, JANUARY 1981 — REVISED MARCH 1988

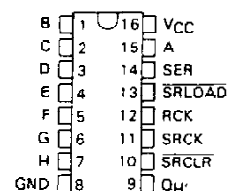
- 8-Bit Parallel Storage Register Inputs ('LS597)
- Parallel 3-State I/O, Storage Register Inputs, Shift Register Outputs ('LS598)
- Shift Register has Direct Overriding Load and Clear
- Accurate Shift-Frequency . . . DC to 20 MHz

description

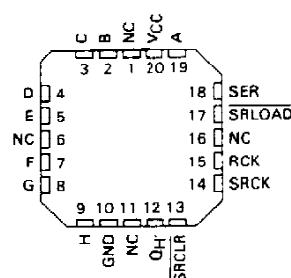
The 'LS597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

The 'LS598 comes in a 20-pin package and has all the features of the 'LS597 plus 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

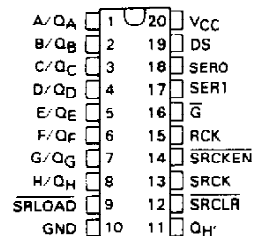
SN54LS597 . . . J OR W PACKAGE
SN74LS597 . . . N PACKAGE
(TOP VIEW)



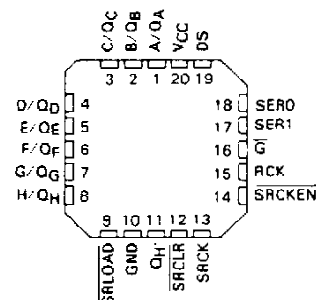
SN54LS597 . . . FK PACKAGE
(TOP VIEW)



SN54LS598 . . . J OR W PACKAGE
LS598 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS598 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

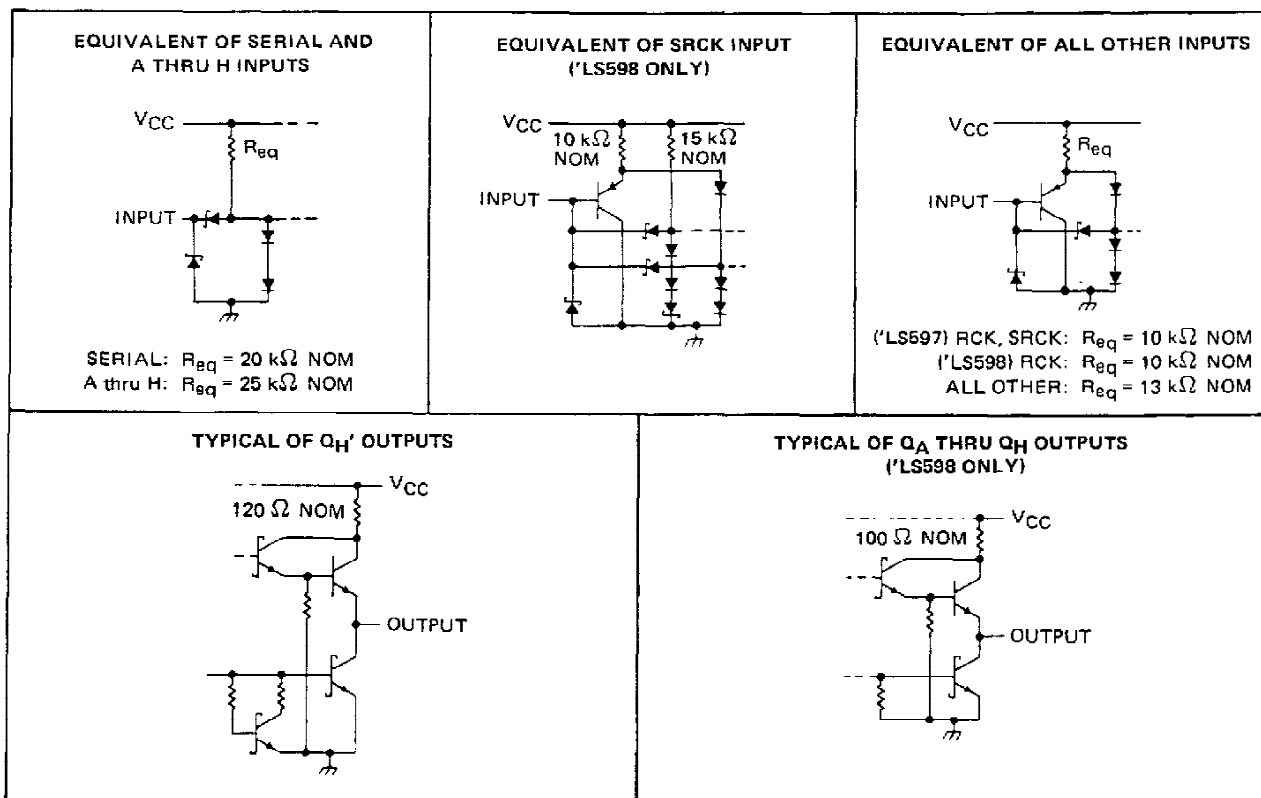
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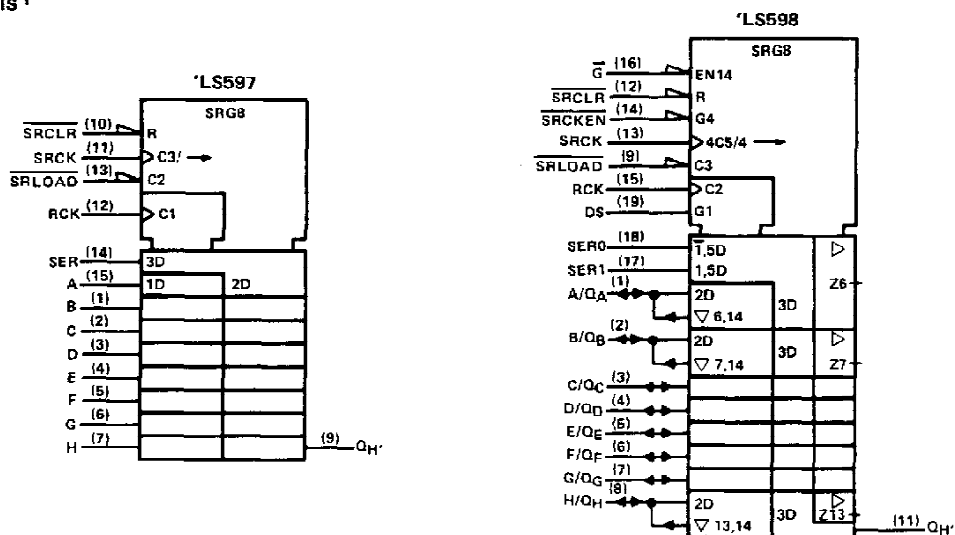
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SN54LS597, SN54LS598, SN74LS597, SN74LS598 **8-BIT SHIFT REGISTERS WITH INPUT LATCHES**

schematics of inputs and outputs



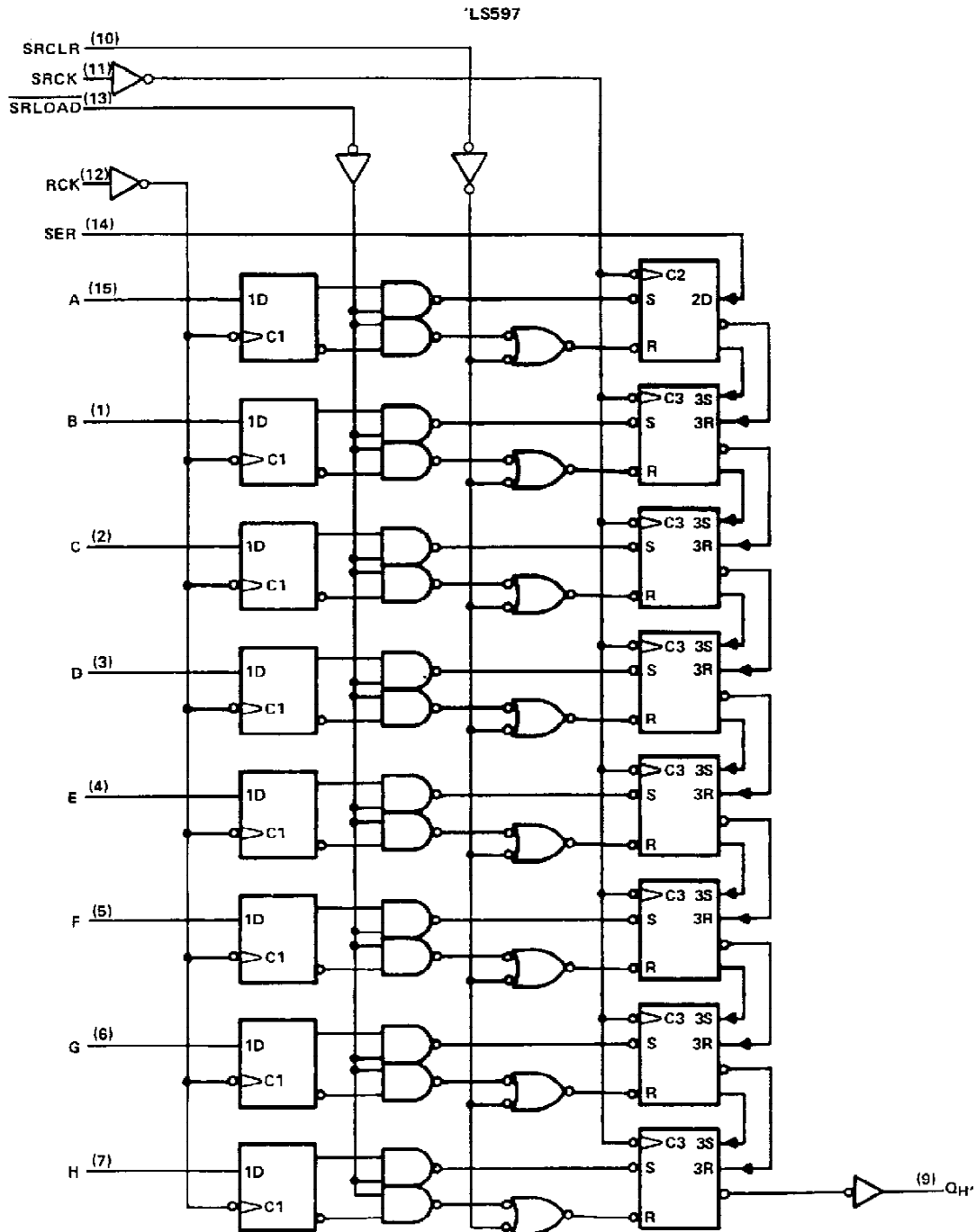
logic symbols†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

SN54LS597, SN74LS597 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

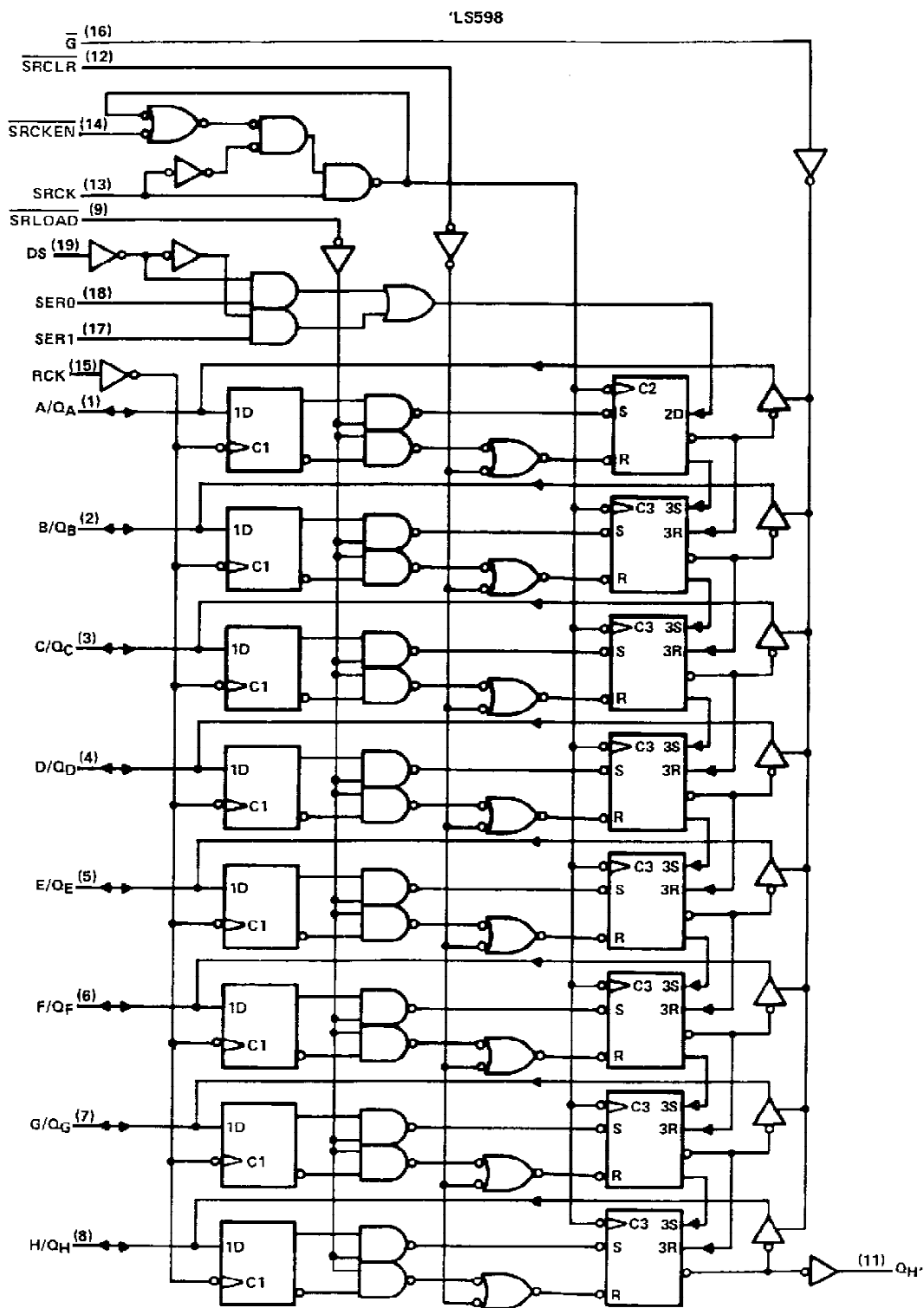
logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

SN54LS598, SN74LS598 **8-BIT SHIFT REGISTERS WITH INPUT LATCHES**

logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

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SN54LS597, SN54LS598, SN74LS597, SN74LS598

8-BIT SHIFT REGISTERS WITH INPUT LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (excluding I/O ports)	7 V
Off-state output voltage (including I/O ports)	5.5 V
Operating free-air temperature range: SN54LS597, SN54LS598	– 55°C to 125°C
SN74LS597, SN74LS598	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current	Q_H'		– 1	Q_H'		– 1	mA
		Q_A thru Q_H , 'LS598 only		– 1	Q_A thru Q_H , 'LS598 only		– 2.6	
I_{OL}	Low-level output current	Q_H'		8	Q_H'		16	mA
		Q_A thru Q_H , 'LS598 only		12	Q_A thru Q_H , 'LS598 only		24	
f_{SCK}	Shift clock frequency	0		20	0		20	MHz
t_w	Pulse duration	SRCK	high	15			15	ns
			low	35			35	
		RCK		20			20	
		SRCLR		20			20	
t_{su}	Setup time	SRLOAD		40			40	ns
		Data before RCK ↑		20			20	
		DS before SRCK ↑ ('LS598 only)		30			30	
		SRCKEN low before SRCK ↑ ('LS598 only)		20			20	
		SRCLR inactive before SRCK ↑		25			25	
		SRLOAD inactive before SRCK ↑		30			30	
t_h	Hold time	RCK ↑ before SRLOAD ↑ (see Note 2)		40			40	ns
		SER before SRCK ↑		20			20	
T_A	Operating free-air temperature	– 55		125	0		70	°C

NOTE 2: The RCK ↑ before SRLOAD ↑ setup time ensures the data saved by RCK ↑ will also be loaded into the shift register.

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SN54LS597, SN54LS598, SN74LS597, SN74LS598 **8-BIT SHIFT REGISTERS WITH INPUT LATCHES**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'		SN74LS'		UNIT
					MIN	TYP‡	MAX	MIN	
V _{IK}			V _{CC} = MIN, I _I = - 18 mA		- 1.5		- 1.5		V
V _{OH}	'LS598 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = - 1 mA	2.4	3.2			V	
	I _{OH} = - 2.6 mA				2.4	3.1			
	Q _H '		I _{OH} = - 1 mA	2.4	3.2	2.4 3.2			
V _{OL}	'LS598 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA	0.25 0.4		0.25 0.4		V	
	I _{OL} = 24 mA				0.35 0.5				
	Q _H '		I _{OL} = 8 mA	0.25 0.4		0.25 0.4			
			I _{OL} = 16 mA			0.35 0.5			
I _{OZH}	'LS598 Q	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V	V _{IL} = MAX,		20		20		μA
I _{OZL}	'LS598 Q	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V	V _{IL} = MAX,		- 0.4		- 0.4		mA
I _I	'LS598 Q	V _{CC} = MAX	V _I = 5.5 V		0.1		0.1		mA
	V _I = 7 V		0.1		0.1				
I _{IH}		V _{CC} = MAX, V _I = 2.7 V			20		20		μA
I _{IL}	'LS598 SRCK	V _{CC} = MAX, V _I = 0.4 V			- 0.8		- 0.8		mA
	SER. A Thru H				- 0.4		- 0.4		
	Others				- 0.2		- 0.2		
I _{OS} §	'LS598 Q	V _{CC} = MAX, V _O = 0 V			- 30	- 130	- 30	- 130	mA
	Q _H '				- 20	- 100	- 20	- 100	
I _{CC}	'LS597	V _{CC} = MAX, All possible inputs grounded, All outputs open	I _{CCH}	35 53		35 53		mA	
			I _{CCL}	35 53		35 53			
	'LS598		I _{CCH}	45 68		45 68			
			I _{CCL}	54 80		54 80			
			I _{CCZ}	56 85		56 85			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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8-BIT SHIFT REGISTERS WITH INPUT LATCHES

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$. (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LS597			LS598			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	SRCK	Q	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$	20	35		20	35		MHz
f_{max}	SRCK	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	20	35					MHz
t_{PLH}	SRCK↑	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$		15	23		11	17	ns
t_{PHL}	SPCK↑	Q_H'			20	30		15	23	ns
t_{PLH}	SRLOAD↓	Q_H'			38	57		28	42	ns
t_{PHL}	SRLOAD↓	Q_H'			29	44		20	30	ns
t_{PHL}	SRCLR↓	Q_H'			24	36		18	27	ns
t_{PLH}	RCK↑	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$ SRLOAD = L		41	60		32	48	ns
t_{PHL}	RCK↑	Q_H'			32	48		24	36	ns
t_{PLH}	SRCK↑	Q	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$					12	18	ns
t_{PHL}	SRCK↑	Q						19	28	ns
t_{PLH}	SRLOAD↓	Q						32	48	ns
t_{PHL}	SRLOAD↓	Q						27	40	ns
t_{PHL}	SRCLR↓	Q						25	38	ns
t_{PZH}	G↓	Q						26	31	ns
t_{PZL}	G↓	Q						29	43	ns
t_{PHZ}	G↑	Q	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$					25	38	ns
t_{PLZ}	G↑	Q						20	30	ns

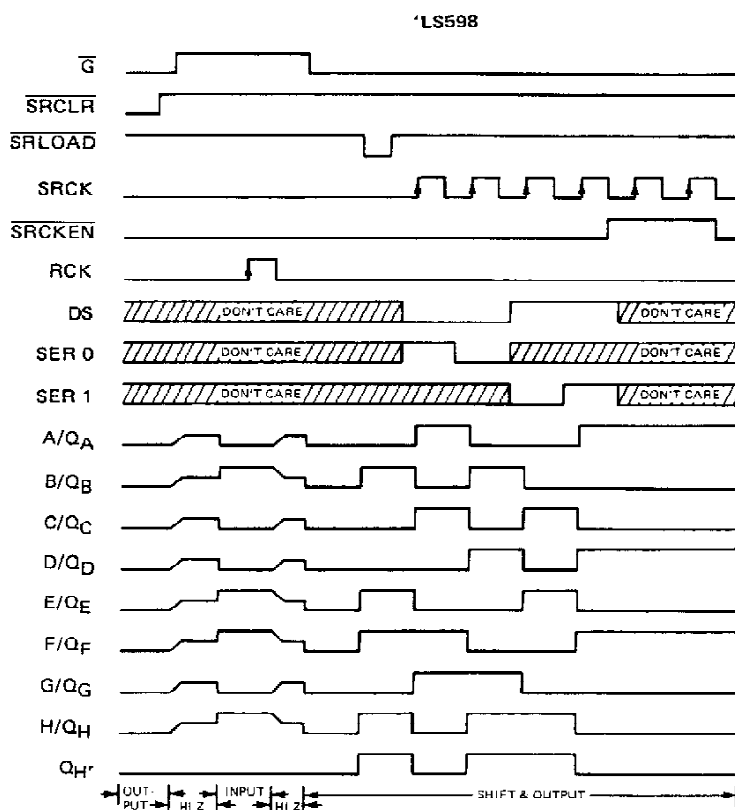
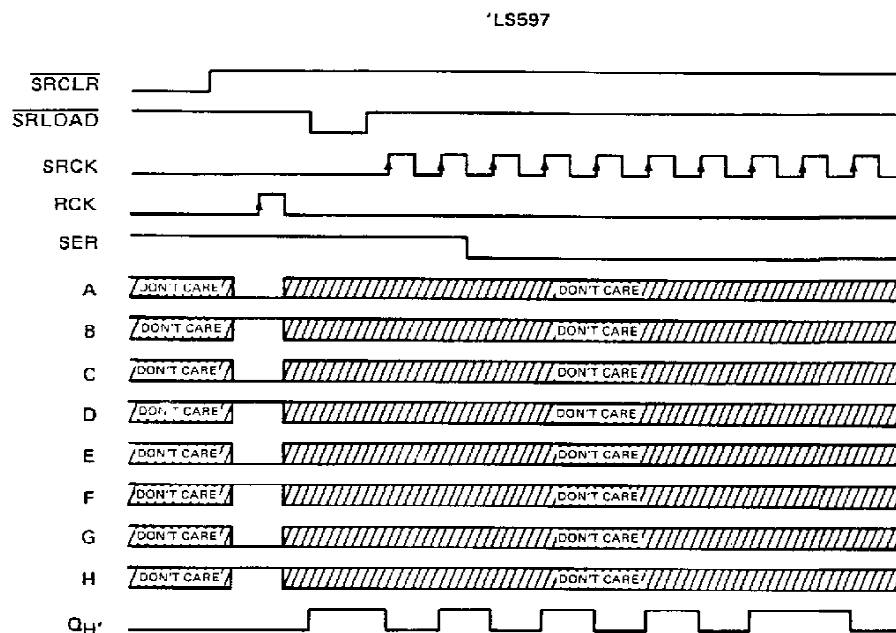
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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typical operating sequences




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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89444012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89444012A SNJ54LS 597FK	Samples
5962-8944401EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J	Samples
5962-8944401EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J	Samples
5962-8944401FA	ACTIVE	CFP	W	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W	Samples
5962-8944401FA	ACTIVE	CFP	W	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W	Samples
SN74LS597D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS597	Samples
SN74LS597D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS597	Samples
SN74LS597N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS597N	Samples
SN74LS597N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS597N	Samples
SN74LS598N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS598N	Samples
SN74LS598N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS598N	Samples
SNJ54LS597FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89444012A SNJ54LS 597FK	Samples
SNJ54LS597FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89444012A SNJ54LS 597FK	Samples
SNJ54LS597J	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS597J	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J	Samples
SNJ54LS597W	ACTIVE	CFP	W	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W	Samples
SNJ54LS597W	ACTIVE	CFP	W	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS597, SN74LS597 :

- Catalog: [SN74LS597](#)
- Military: [SN54LS597](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



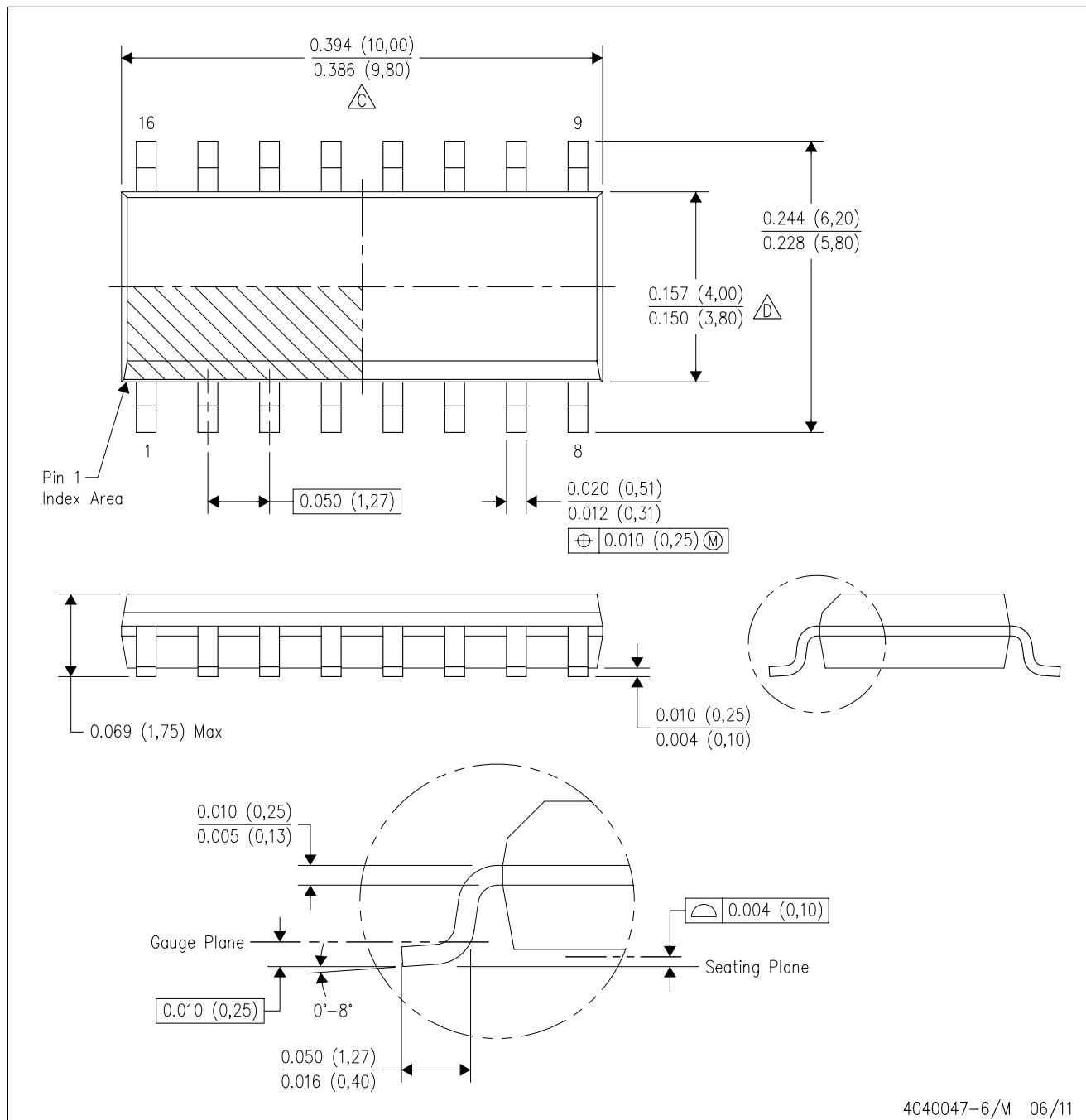
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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