

SN54HC365, SN74HC365 HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

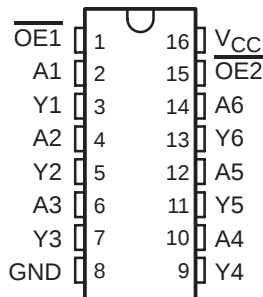
SCLS308D – JANUARY 1996 – REVISED OCTOBER 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Drive Bus Lines, Buffer-Memory Address Registers, or Drive Up To 15 LSTTL Loads
- True Outputs
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 10$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

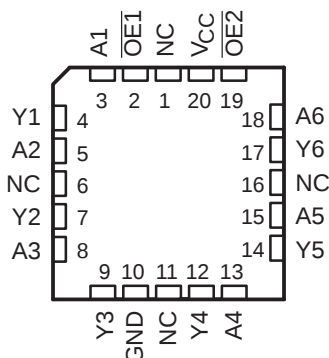
description/ordering information

These hex buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HC365 devices contain six independent buffers/drivers with dual-gated output-enable ($\overline{OE1}$ and $\overline{OE2}$) inputs. When $\overline{OE1}$ and $\overline{OE2}$ are both low, the devices pass noninverted data from the A inputs to the Y outputs. If either (or both) output-enable terminal(s) is high, the outputs are in the high-impedance state.

SN54HC365 . . . J OR W PACKAGE
SN74HC365 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC365 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC365N	SN74HC365N
	SOIC – D	Tube of 40	SN74HC365D	HC365
		Reel of 2500	SN74HC365DR	
		Reel of 250	SN74HC365DT	
	SOP – NS	Reel of 2000	SN74HC365NSR	HC365
	TSSOP – PW	Reel of 90	SN74HC365PW	HC365
		Reel of 2000	SN74HC365PWR	
		Reel of 250	SN74HC365PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC365J	SNJ54HC365J
	CFP – W	Tube of 150	SNJ54HC365W	SNJ54HC365W
	LCCC – FK	Tube of 55	SNJ54HC365FK	SNJ54HC365FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

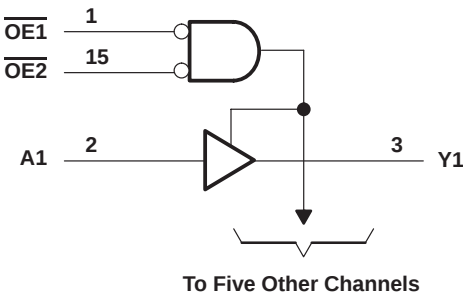
SN54HC365, SN74HC365 HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE
 (each buffer/driver)

INPUTS			OUTPUT Y
OE1	OE2	A	
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	73°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC365, SN74HC365 HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

			SN54HC365			SN74HC365			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5			1.5			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 6 V	4.2			4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5			0.5			V
		V _{CC} = 4.5 V	1.35			1.35			
		V _{CC} = 6 V	1.8			1.8			
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V	1000			1000			ns
		V _{CC} = 4.5 V	500			500			
		V _{CC} = 6 V	400			400			
T _A	Operating free-air temperature		−55	125		−40	85		°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC365		SN74HC365		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0		6 V		±0.01	±0.5		±10		±5	µA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80	µA
C _i			2 V to 6 V		3	10		10		10	pF



SN54HC365, SN74HC365

HEX BUFFERS AND LINE DRIVERS

WITH 3-STATE OUTPUTS

SCLS308D – JANUARY 1996 – REVISED OCTOBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC365		SN74HC365		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	95		145		120	ns
			4.5 V		12	19		29		24	
			6 V		10	16		25		20	
t_{en}	$\overline{OE}$	Y	2 V		100	190		285		238	ns
			4.5 V		26	38		57		48	
			6 V		21	32		48		41	
t_{dis}	$\overline{OE}$	Y	2 V		50	175		265		240	ns
			4.5 V		21	35		53		48	
			6 V		19	30		45		41	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

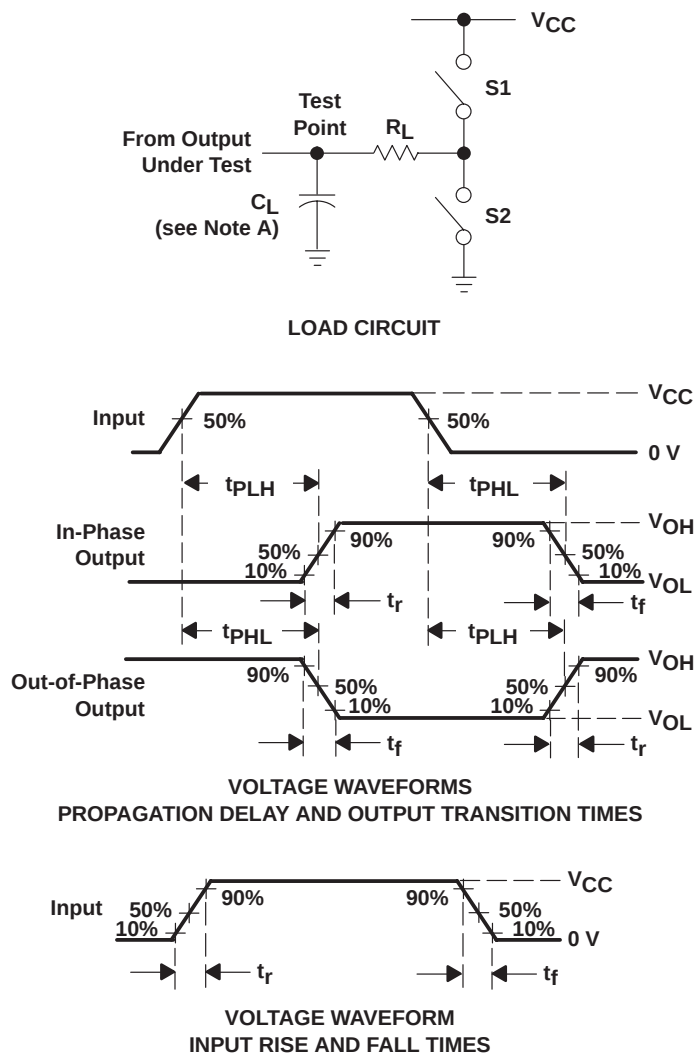
switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC365		SN74HC365		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		70	120		180		150	ns
			4.5 V		17	24		36		30	
			6 V		14	20		31		25	
t_{en}	$\overline{OE}$	Y	2 V		140	230		345		285	ns
			4.5 V		30	46		69		57	
			6 V		28	39		59		48	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

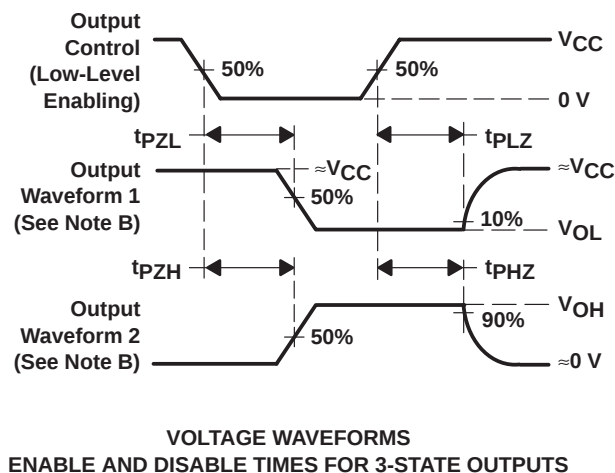
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



PARAMETER	R _L	C _L	S1	S2
t _{en}	1 kΩ	50 pF or 150 pF	Open	Closed
			Closed	Open
t _{dis}	1 kΩ	50 pF	Open	Closed
			Closed	Open
t _{pd} or t _t	--	50 pF or 150 pF	Open	Open



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd}.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - G. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8500101EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8500101EA SNJ54HC365J	Samples
JM38510/65706BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65706BEA	Samples
M38510/65706BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65706BEA	Samples
SN54HC365J	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54HC365J	Samples
SN74HC365D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	Samples
SN74HC365DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	Samples
SN74HC365DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	Samples
SN74HC365N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC365N	Samples
SN74HC365NE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC365N	Samples
SN74HC365NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	Samples
SN74HC365PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	Samples
SN74HC365PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	Samples
SN74HC365PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	Samples
SN74HC365PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	Samples
SNJ54HC365J	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8500101EA SNJ54HC365J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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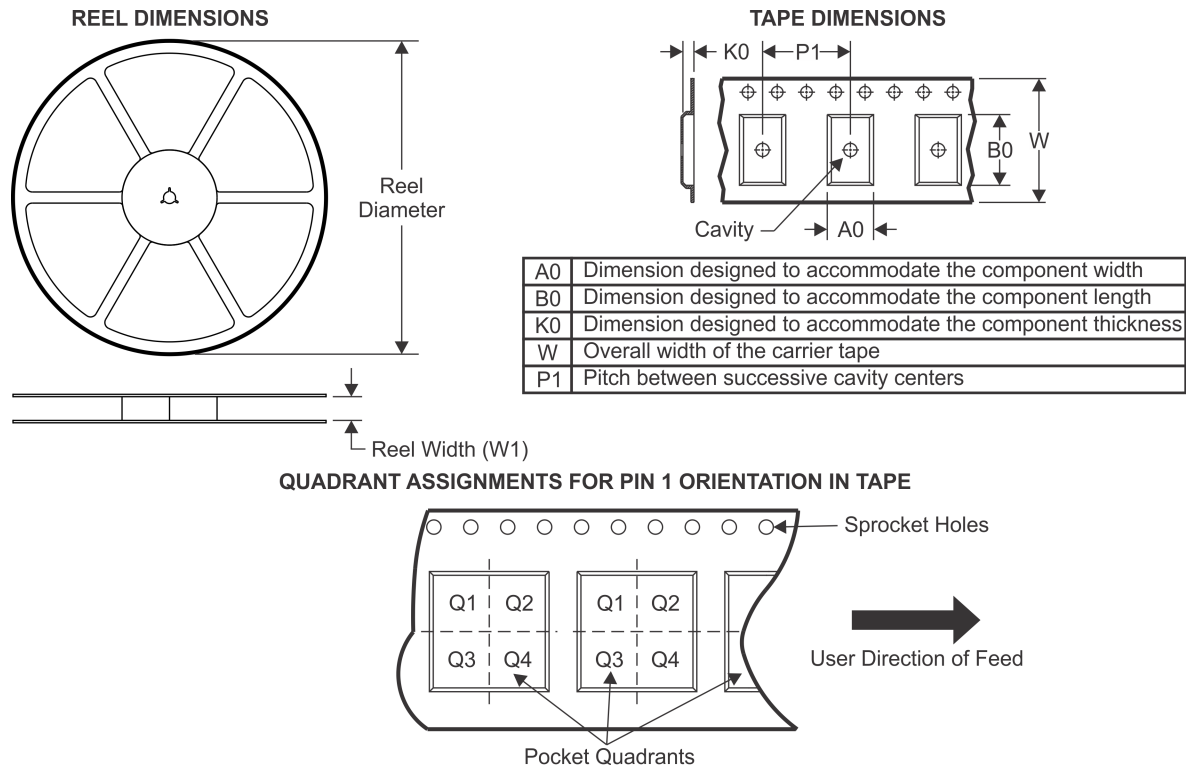
OTHER QUALIFIED VERSIONS OF SN54HC365, SN74HC365 :

- Catalog: [SN74HC365](#)

- Military: [SN54HC365](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC365DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC365NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC365PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC365PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC365DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC365NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74HC365PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74HC365PWT	TSSOP	PW	16	250	367.0	367.0	35.0

D (R-PDSO-G16)

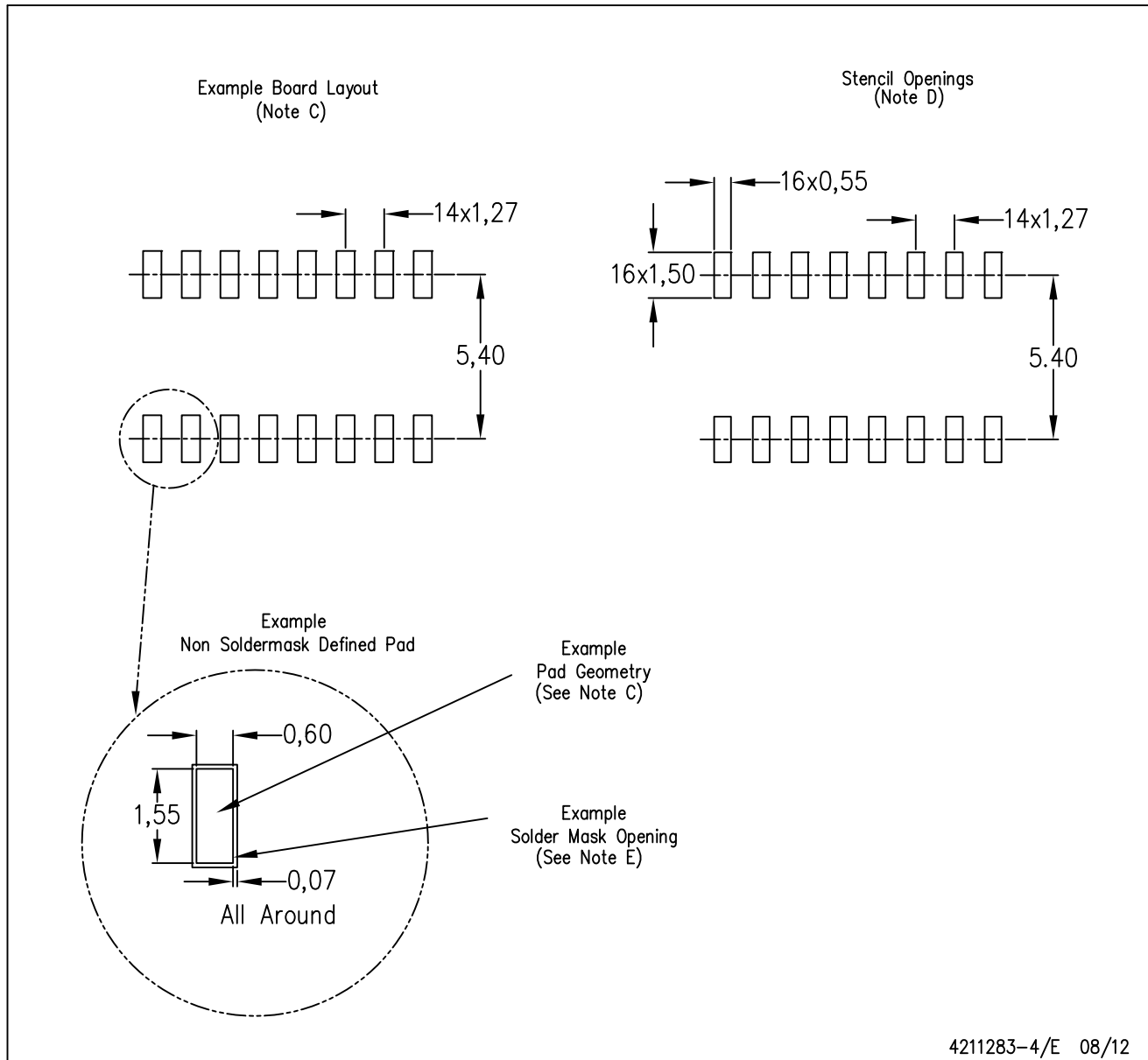
PLASTIC SMALL OUTLINE



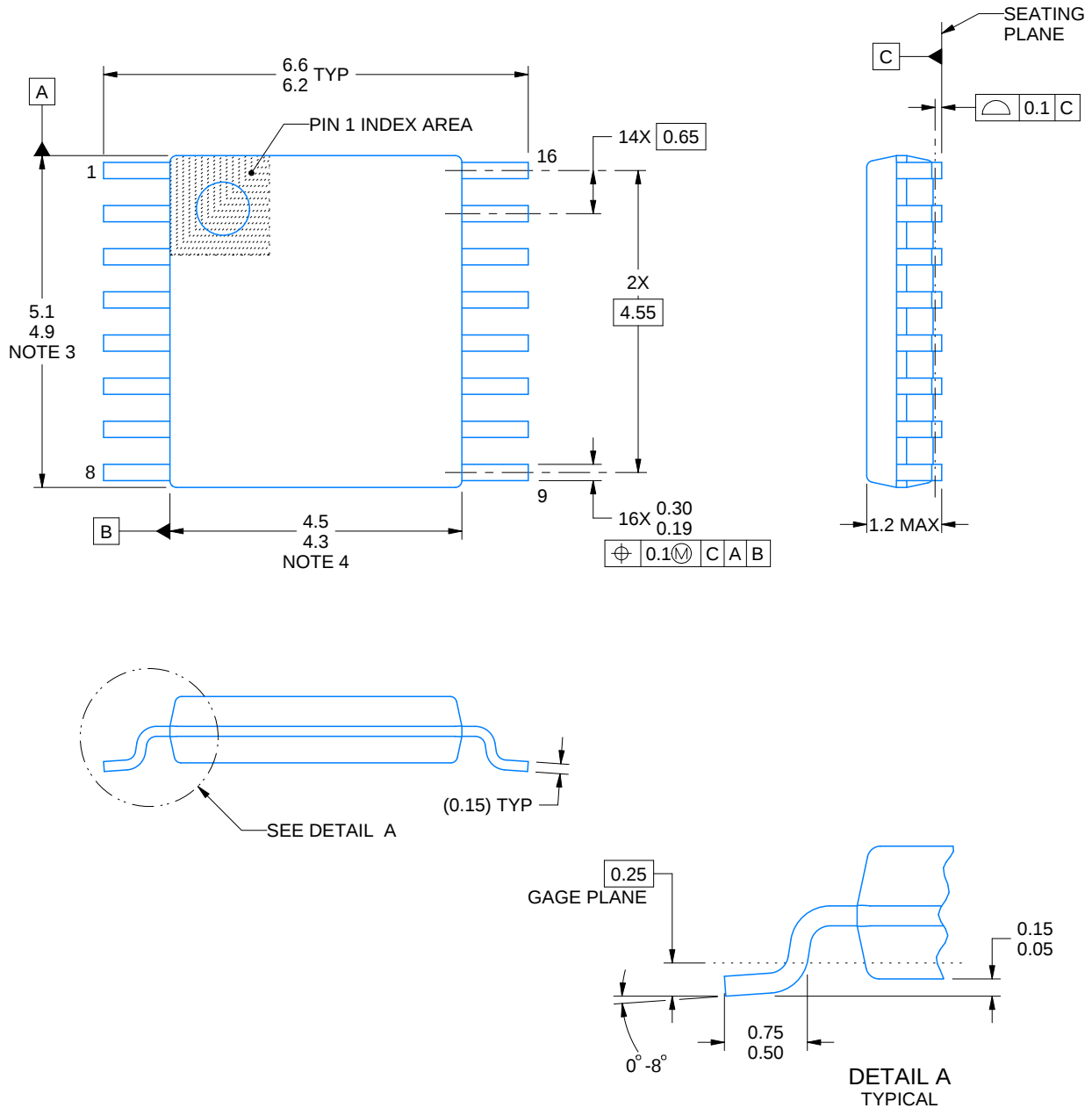
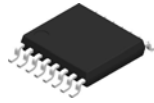
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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NOTES:

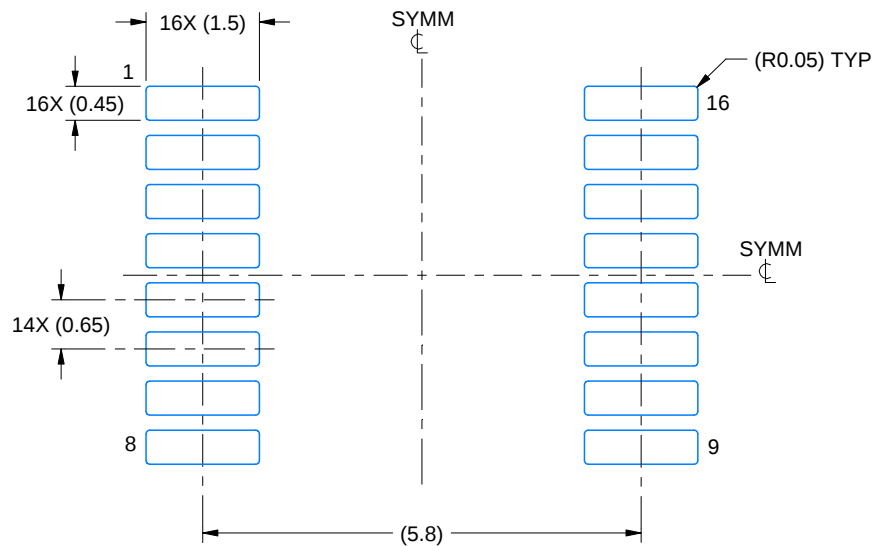
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

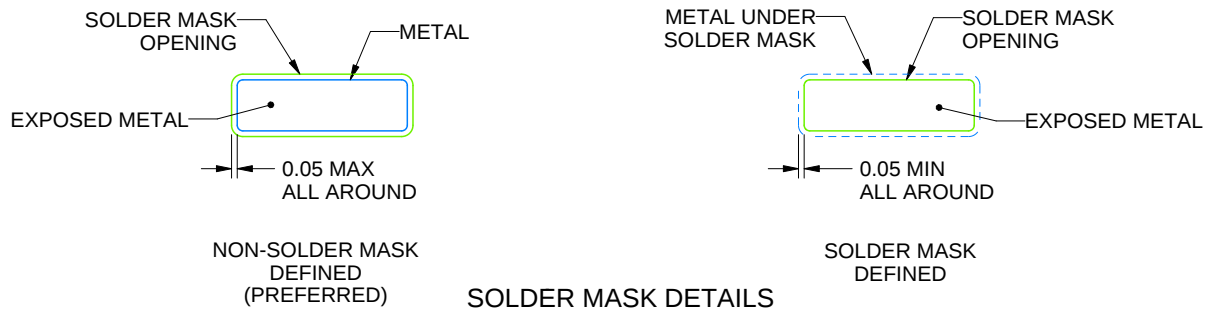
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

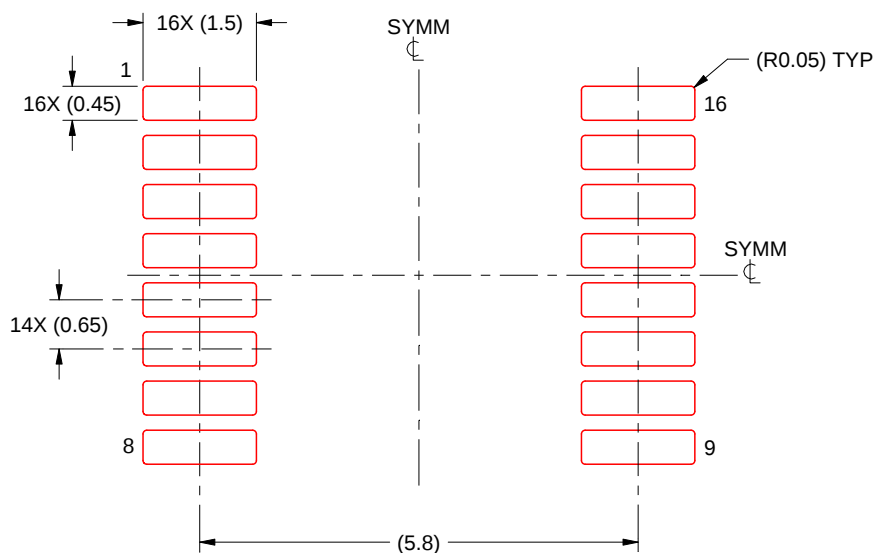
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



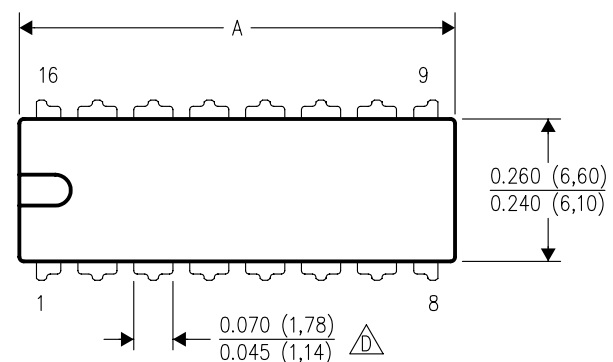
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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

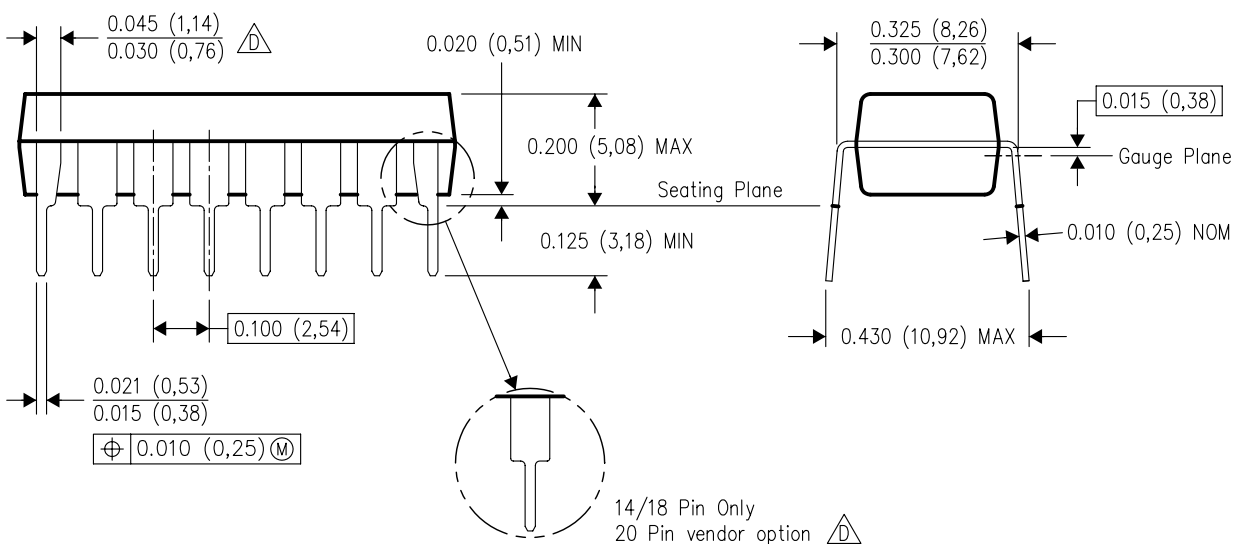
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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