



SNx4HC244 Octal Buffers and Line Drivers With 3-State Outputs

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Outputs Drive Up to 15 LSTTL Loads
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Low Power Consumption: I_{CC} , 80- μ A (Maximum)
- Typical $t_{pd} = 11$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A (Maximum)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

3 Description

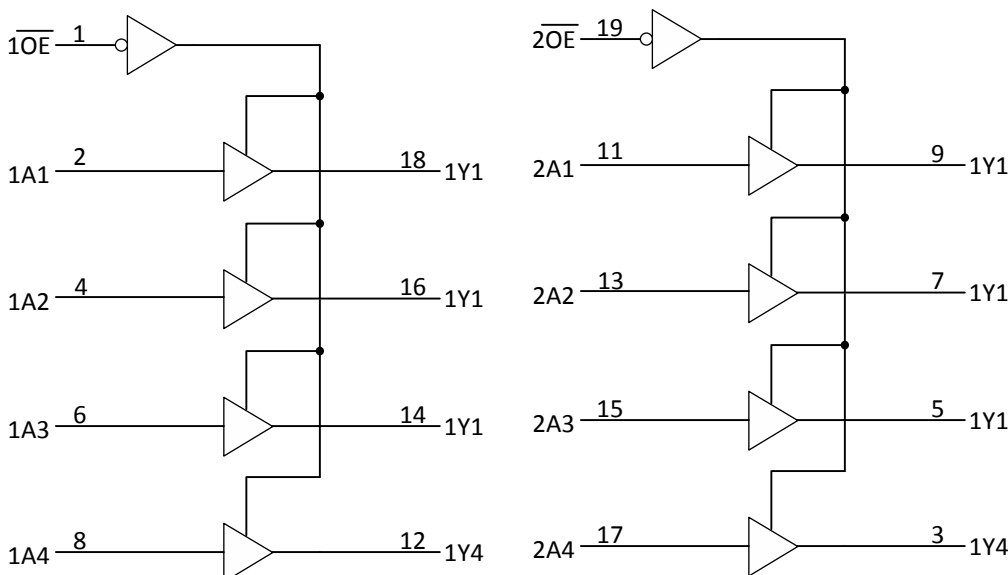
The SNx4HC244 octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The SNx4HC244 devices are organized as two 4-bit buffers and drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Device Information⁽¹⁾

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
SN54HC244	CDIP (20)	6.92 mm $\times$ 24.38 mm
	CFP (20)	6.92 mm $\times$ 13.72 mm
	LCCC (20)	8.89 mm $\times$ 8.89 mm
SN74HC244DB	SSOP (20)	5.30 mm $\times$ 7.25 mm
SN74HC244DW	SOIC (20)	7.50 mm $\times$ 12.80 mm
SN74HC244N	PDIP (20)	6.30 mm $\times$ 25.40 mm
SN74HC244NS	SOP (20)	5.30 mm $\times$ 12.60 mm
SN74HC244PW	TSSOP (20)	4.40 mm $\times$ 6.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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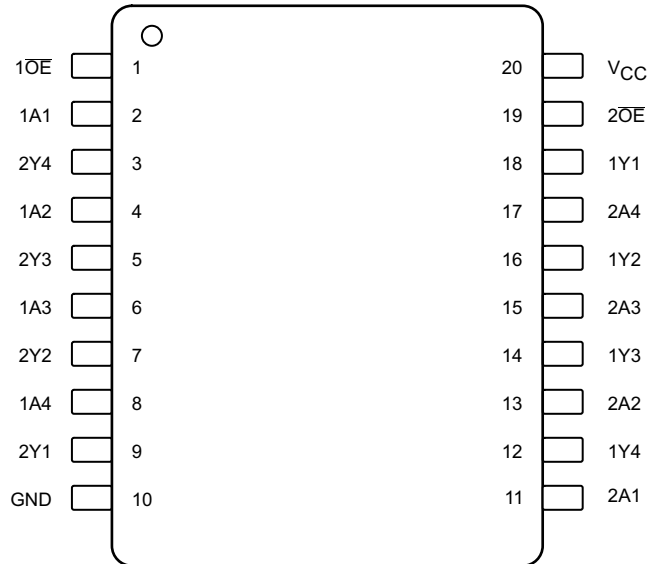
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

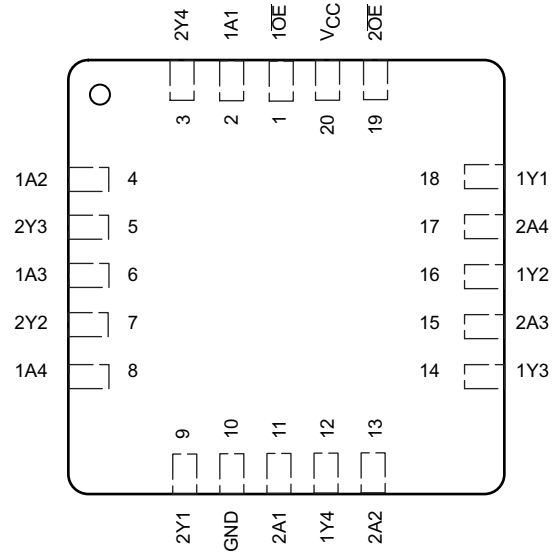
Changes from Revision D (August 2003) to Revision E	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Added Military Disclaimer to <i>Features</i> section	1
• Added <i>Applications</i> section	1
• Removed Ordering Information table	1
• Added <i>Device Information</i> table	1

5 Pin Configuration and Functions

DB, DW, J, N, NS, PW, W Package
20-Pin SSOP, SOIC, CDIP, PDIP, SOP, TSSOP, or CFP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1OE	I	Output Enable
2	1A1	I	Input
3	2Y4	O	Output
4	1A2	I	Input
5	2Y3	O	Output
6	1A3	I	Input
7	2Y2	O	Output
8	1A4	I	Input
9	2Y1	O	Output
10	GND	—	Ground
11	2A1	I	Input
12	1Y4	O	Output
13	2A2	I	Input
14	1Y3	O	Output
15	2A3	I	Input
16	1Y2	O	Output
17	2A4	I	Input
18	1Y1	O	Output
19	2OE	I	Output Enable
20	V _{CC}	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range, V_{CC}		−0.5	7	V
Input clamp current, I_{IK}	$V_I < 0$ or $V_I > V_{CC}^{(2)}$		±20	mA
Output clamp current, I_{OK}	$V_O < 0$ or $V_O > V_{CC}^{(2)}$		±20	mA
Continuous output current, I_O	$V_O = 0$ or V_{CC}		±35	mA
Continuous current through V_{CC} or GND			±70	mA
Junction Temperature, T_J			150	°C
Storage temperature, T_{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

SN74HC244		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V		1.8	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	$V_{CC} = 2$ V		1000	ns/V
		$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		400	
C_{pd}	Power dissipation capacitance per buffer or driver (no load)		35		pF
T_A	Operating free-air temperature	SN54HC244	−55	125	°C
		SN74HC244	−40	85	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the Texas Instruments application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN54HC244, SN74HC244					UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	89.5	76.8	44.9	71.9	97.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	50.9	42.2	30.9	38.2	32.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	44.6	44.6	25.8	39.3	48.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	17	15.6	16.4	14.9	1.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	44.2	44.1	25.7	39	47.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 μA	V _{CC} = 2 V	1.9	1.998	V	
			V _{CC} = 4.5 V	4.4	4.499		
			V _{CC} = 6 V	5.9	5.999		
		I _{OH} = –6 mA, V _{CC} = 4.5 V		3.98	4.3		
		I _{OH} = –7.8 mA, V _{CC} = 6 V		5.48	5.8		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	V _{CC} = 2 V	0.002		0.1	V
			V _{CC} = 4.5 V	0.001		0.1	
			V _{CC} = 6 V	0.001		0.1	
		I _{OL} = 6 mA, V _{CC} = 4.5 V		0.17		0.26	
		I _{OL} = 7.8 mA, V _{CC} = 6 V		0.15		0.26	
I _I	V _I = V _{CC} or 0, V _{CC} = 6 V			±0.1		±100	nA
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL} , V _{CC} = 6 V			±0.01		±0.5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0, V _{CC} = 6 V					8	μA
C _i	V _{CC} = 2 V to 6 V			3		10	pF

6.6 Electrical Characteristics – SN54HC244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = −20 μA	V _{CC} = 2 V	1.9			V
			V _{CC} = 4.5 V	4.4			
			V _{CC} = 6 V	5.9			
		I _{OH} = −6 mA, V _{CC} = 4.5 V		3.7			
		I _{OH} = −7.8 mA, V _{CC} = 6 V		5.2			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	V _{CC} = 2 V			0.1	V
			V _{CC} = 4.5 V			0.1	
			V _{CC} = 6 V			0.1	
		I _{OL} = 6 mA, V _{CC} = 4.5 V				0.4	
		I _{OL} = 7.8 mA, V _{CC} = 6 V				0.4	
I _I	V _I = V _{CC} or 0, V _{CC} = 6 V					±1000	nA
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL} , V _{CC} = 6 V					±10	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0, V _{CC} = 6 V					160	μA
C _i	V _{CC} = 2 V to 6 V					10	pF

SN54HC244, SN74HC244

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6.7 Electrical Characteristics – SN74HC244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = −20 μA	V _{CC} = 2 V	1.9			V
			V _{CC} = 4.5 V	4.4			
			V _{CC} = 6 V	5.9			
		I _{OH} = −6 mA, V _{CC} = 4.5 V		3.84			
		I _{OH} = −7.8 mA, V _{CC} = 6 V		5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	V _{CC} = 2 V			0.1	V
			V _{CC} = 4.5 V			0.1	
			V _{CC} = 6 V			0.1	
		I _{OL} = 6 mA, V _{CC} = 4.5 V				0.33	
		I _{OL} = 7.8 mA, V _{CC} = 6 V				0.33	
I _I	V _I = V _{CC} or 0, V _{CC} = 6 V					±1000	nA
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL} , V _{CC} = 6 V					±5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0, V _{CC} = 6 V					80	μA
C _i	V _{CC} = 2 V to 6 V					10	pF

6.8 Switching Characteristics
 $T_A = 25^\circ C$ (unless otherwise noted; see [Figure 2](#))

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	$V_{CC} = 2 V$	$C_L = 50 \text{ pF}$		40	115	ns
			$C_L = 150 \text{ pF}$		56	165	
		$V_{CC} = 4.5 V$	$C_L = 50 \text{ pF}$		13	23	
			$C_L = 150 \text{ pF}$		18	33	
		$V_{CC} = 6 V$	$C_L = 50 \text{ pF}$		11	20	
			$C_L = 150 \text{ pF}$		15	28	
t_{en}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 V$	$C_L = 50 \text{ pF}$		75	150	ns
			$C_L = 150 \text{ pF}$		100	200	
		$V_{CC} = 4.5 V$	$C_L = 50 \text{ pF}$		15	30	
			$C_L = 150 \text{ pF}$		20	40	
		$V_{CC} = 6 V$	$C_L = 50 \text{ pF}$		13	26	
			$C_L = 150 \text{ pF}$		17	34	
t_{dis}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 V$	$C_L = 50 \text{ pF}$		75	150	ns
		$V_{CC} = 4.5 V$	$C_L = 50 \text{ pF}$		15	30	
		$V_{CC} = 6 V$	$C_L = 50 \text{ pF}$		13	26	
t_t	To Y (output)	$V_{CC} = 2 V$	$C_L = 50 \text{ pF}$		28	60	ns
			$C_L = 150 \text{ pF}$		45	210	
		$V_{CC} = 4.5 V$	$C_L = 50 \text{ pF}$		8	12	
			$C_L = 150 \text{ pF}$		17	42	
		$V_{CC} = 6 V$	$C_L = 50 \text{ pF}$		6	10	
			$C_L = 150 \text{ pF}$		13	36	

6.9 Switching Characteristics – $C_L = 50 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted; see [Figure 2](#))

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		170	ns
			SN74HC244		145	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		34	
			SN74HC244		29	
		$V_{CC} = 6 \text{ V}$	SN54HC244		29	
			SN74HC244		25	
t_{en}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		225	ns
			SN74HC244		190	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		45	
			SN74HC244		38	
		$V_{CC} = 6 \text{ V}$	SN54HC244		38	
			SN74HC244		32	
t_{dis}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		225	ns
			SN74HC244		190	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		45	
			SN74HC244		38	
		$V_{CC} = 6 \text{ V}$	SN54HC244		38	
			SN74HC244		32	
t_t	To Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		90	ns
			SN74HC244		75	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		18	
			SN74HC244		15	
		$V_{CC} = 6 \text{ V}$	SN54HC244		15	
			SN74HC244		13	

6.10 Switching Characteristics – $C_L = 150 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted; see [Figure 2](#))

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		245	ns
			SN74HC244		210	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		49	
			SN74HC244		42	
		$V_{CC} = 6 \text{ V}$	SN54HC244		42	
			SN74HC244		35	
t_{en}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		300	ns
			SN74HC244		250	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		60	
			SN74HC244		50	
		$V_{CC} = 6 \text{ V}$	SN54HC244		51	
			SN74HC244		43	
t_t	To Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		315	ns
			SN74HC244		265	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		63	
			SN74HC244		53	
		$V_{CC} = 6 \text{ V}$	SN54HC244		53	
			SN74HC244		45	

6.11 Typical Characteristic

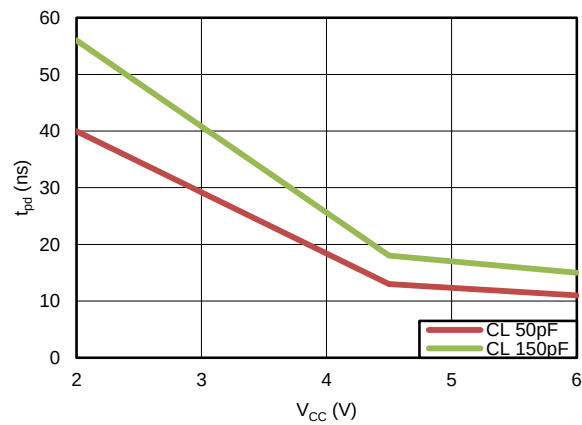


Figure 1. Propagation Delay

7 Parameter Measurement Information

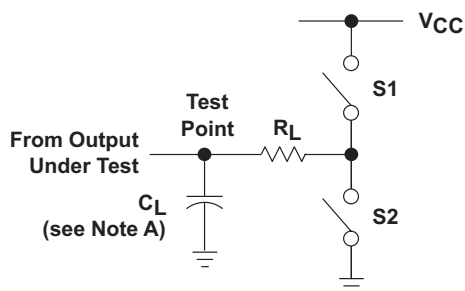


Figure 2. Load Circuit

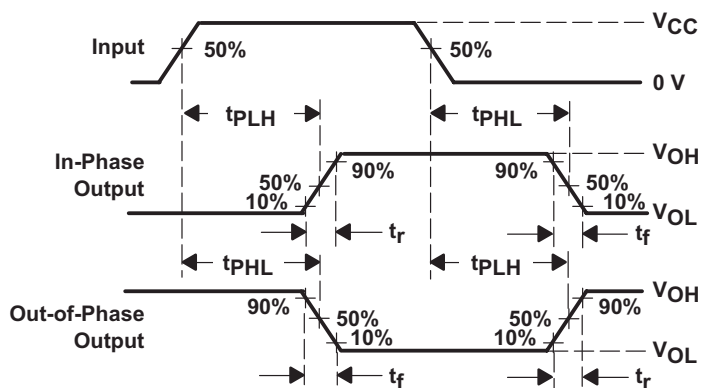


Figure 3. Propagation Delay and Output Transition Times

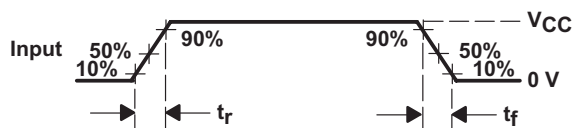


Figure 4. Input Rise and Fall Times

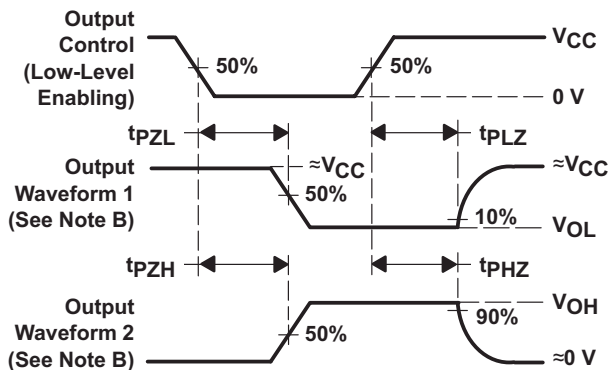


Figure 5. Enable and Disable Times for 3-State Outputs

NOTE:

A. C_L includes probe and test-fixture capacitance.

Parameter Measurement Information (continued)

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Table 1. Switching Information Table

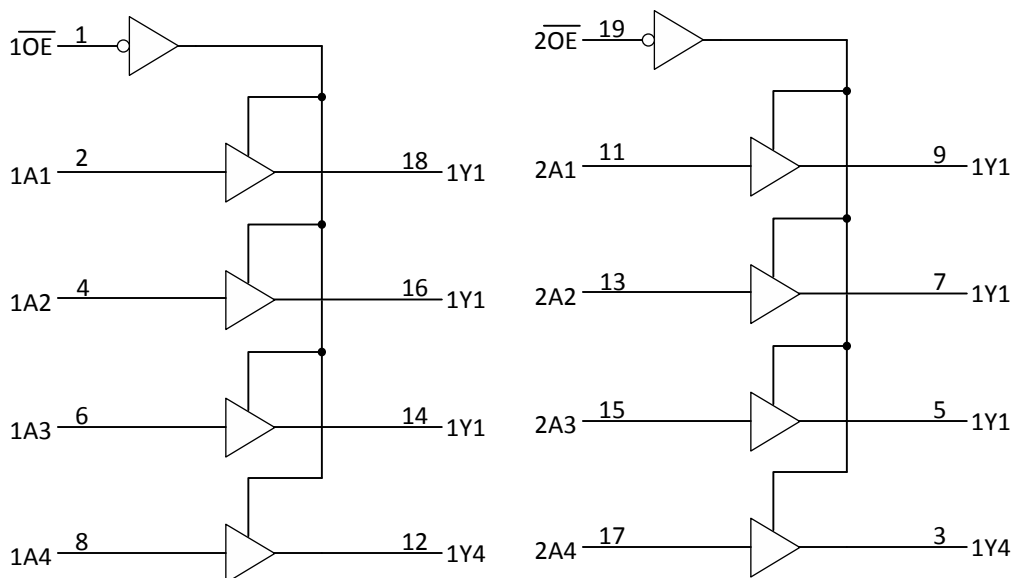
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 k Ω	50 pF or 150 pF	Open	Closed
	t_{PZL}	1 k Ω	50 pF or 150 pF	Closed	Open
t_{dis}	t_{PHZ}	1 k Ω	50 pF	Open	Closed
	t_{PLZ}	1 k Ω	50 pF	Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open

8 Detailed Description

8.1 Overview

The SNx4HC244 device is organized as two 4-bit buffers and line drivers with separate output-enable ($\overline{\text{OE}}$) inputs. When $\overline{\text{OE}}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{\text{OE}}$ is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



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8.3 Feature Description

The SNx4HC244 has a wide operating voltage of 2 V to 6 V. Inputs accept voltage levels up to V_{CC} . This device has a low power consumption of I_{CC} 80 μA (maximum). The SNx4HC244 device can drive ± 6 mA at V_{CC} of 5 V.

8.4 Device Functional Modes

Table 2 lists the functions of the SNx4HC244.

**Table 2. Function Table
(Each Buffer or Driver)**

INPUTS		OUTPUT
$\overline{\text{OE}}$	A	Y
L	H	H
L	L	L
H	X	Z

9 Application and Implementation

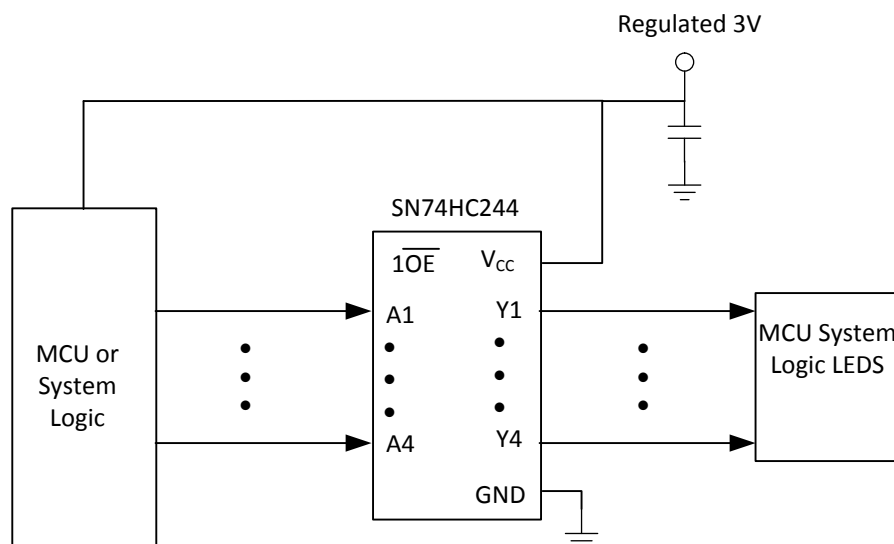
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

SN74HC244 is a high-drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

9.2 Typical Application



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Figure 6. SN74HC244 Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in [Recommended Operating Conditions](#).
 - For specified high and low levels, see V_{IH} and V_{IL} in [Recommended Operating Conditions](#).
2. Recommend output conditions:
 - Load currents should not exceed I_O max per output and should not exceed the continuous current through V_{CC} or GND total current for the part. These limits are located in [Absolute Maximum Ratings](#).
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

9.2.3 Application Curve

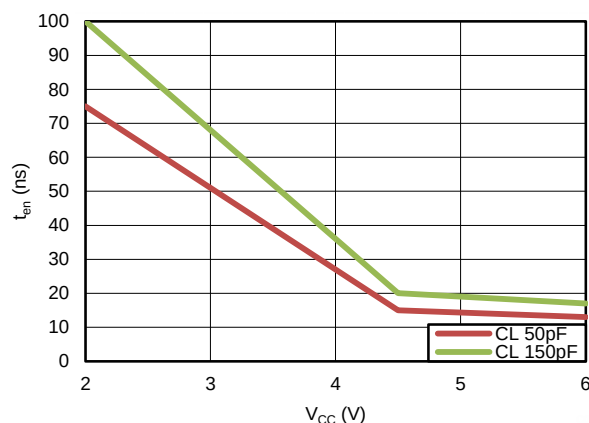


Figure 7. Enable Time

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μF capacitor. If there are multiple V_{CC} terminals, then TI recommends 0.01- μF or 0.022- μF capacitors for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input and gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 8](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

11.2 Layout Example

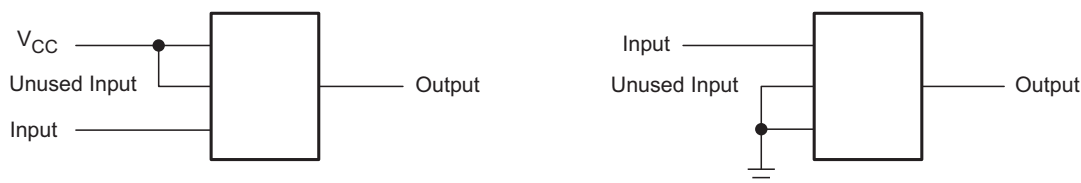


Figure 8. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

[Table 3](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC244	Click here	Click here	Click here	Click here	Click here
SN74HC244	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8409601VRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8409601VR A SNV54HC244J	Samples
5962-8409601VSA	ACTIVE	CFP	W	20	25	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8409601VS A SNV54HC244W	Samples
84096012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84096012A SNJ54HC 244FK	Samples
8409601RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8409601RA SNJ54HC244J	Samples
8409601SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8409601SA SNJ54HC244W	Samples
JM38510/65705B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 65705B2A	Samples
JM38510/65705BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65705BRA	Samples
JM38510/65705BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65705BSA	Samples
M38510/65705B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 65705B2A	Samples
M38510/65705BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65705BRA	Samples
M38510/65705BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65705BSA	Samples
SN54HC244J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54HC244J	Samples
SN74HC244ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244A	Samples
SN74HC244APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244A	Samples
SN74HC244DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC244DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC244N	Samples
SN74HC244NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC244N	Samples
SN74HC244NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244	Samples
SN74HC244QDWRG4Q1	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		HC244Q	Samples
SNJ54HC244FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84096012A SNJ54HC 244FK	Samples
SNJ54HC244J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8409601RA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54HC244J	
SNJ54HC244W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8409601SA SNJ54HC244W	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

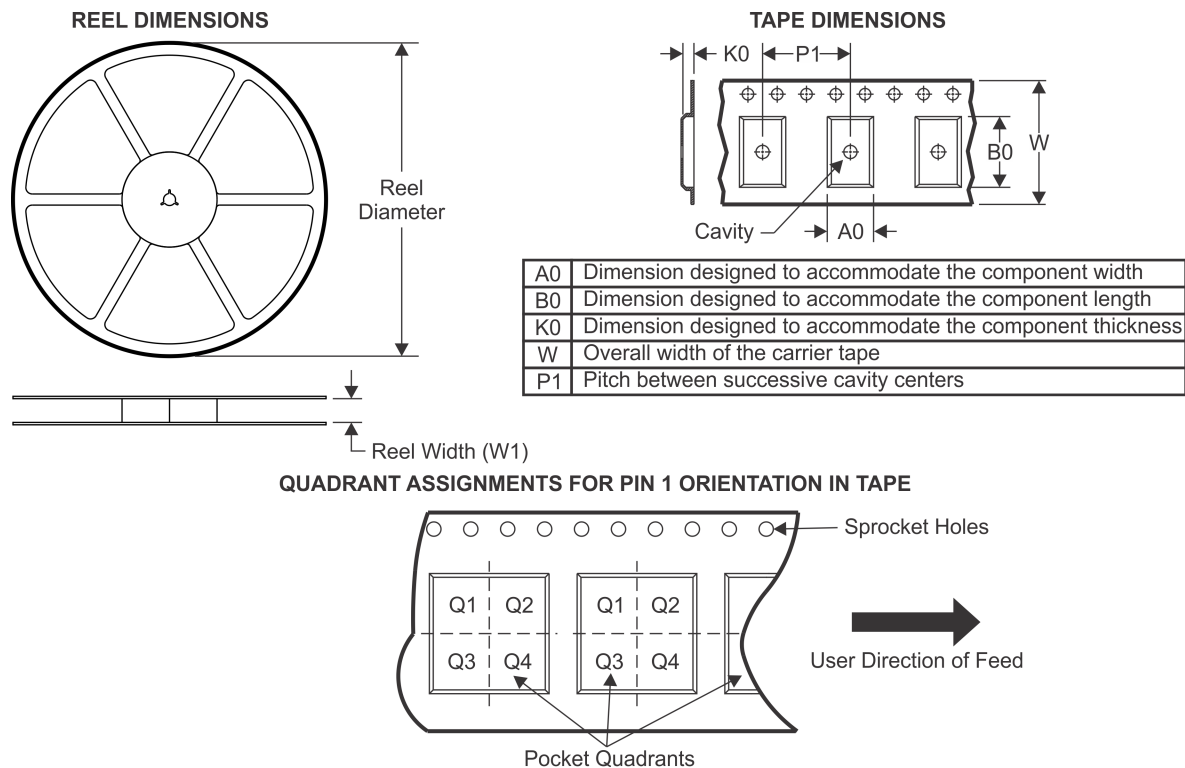
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC244, SN54HC244-SP, SN74HC244 :

- Catalog: [SN74HC244](#), [SN54HC244](#)
- Automotive: [SN74HC244-Q1](#), [SN74HC244-Q1](#)
- Enhanced Product: [SN74HC244-EP](#), [SN74HC244-EP](#)
- Military: [SN54HC244](#)
- Space: [SN54HC244-SP](#)

NOTE: Qualified Version Definitions:

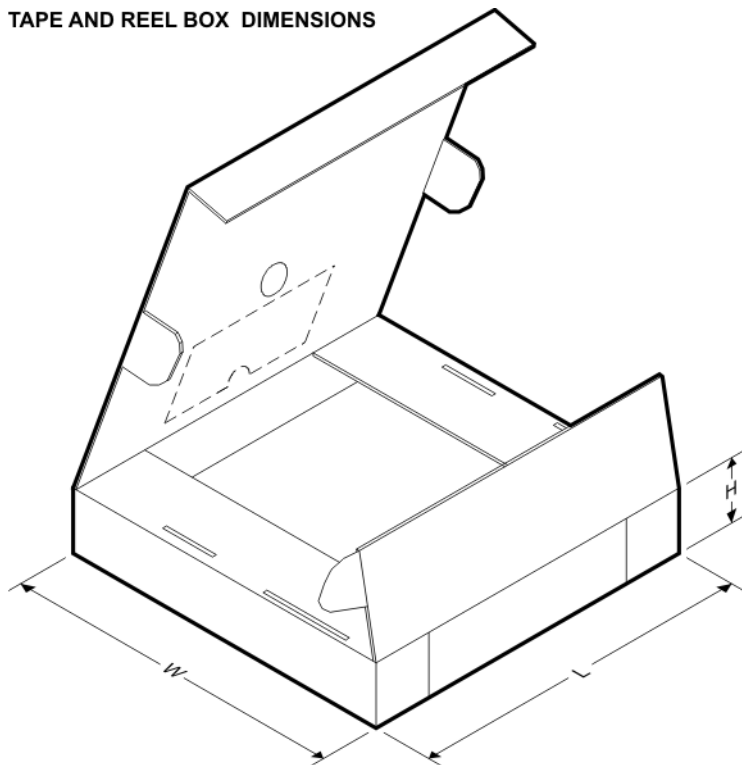
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HC244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC244DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC244NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC244PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC244QDWRG4Q1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

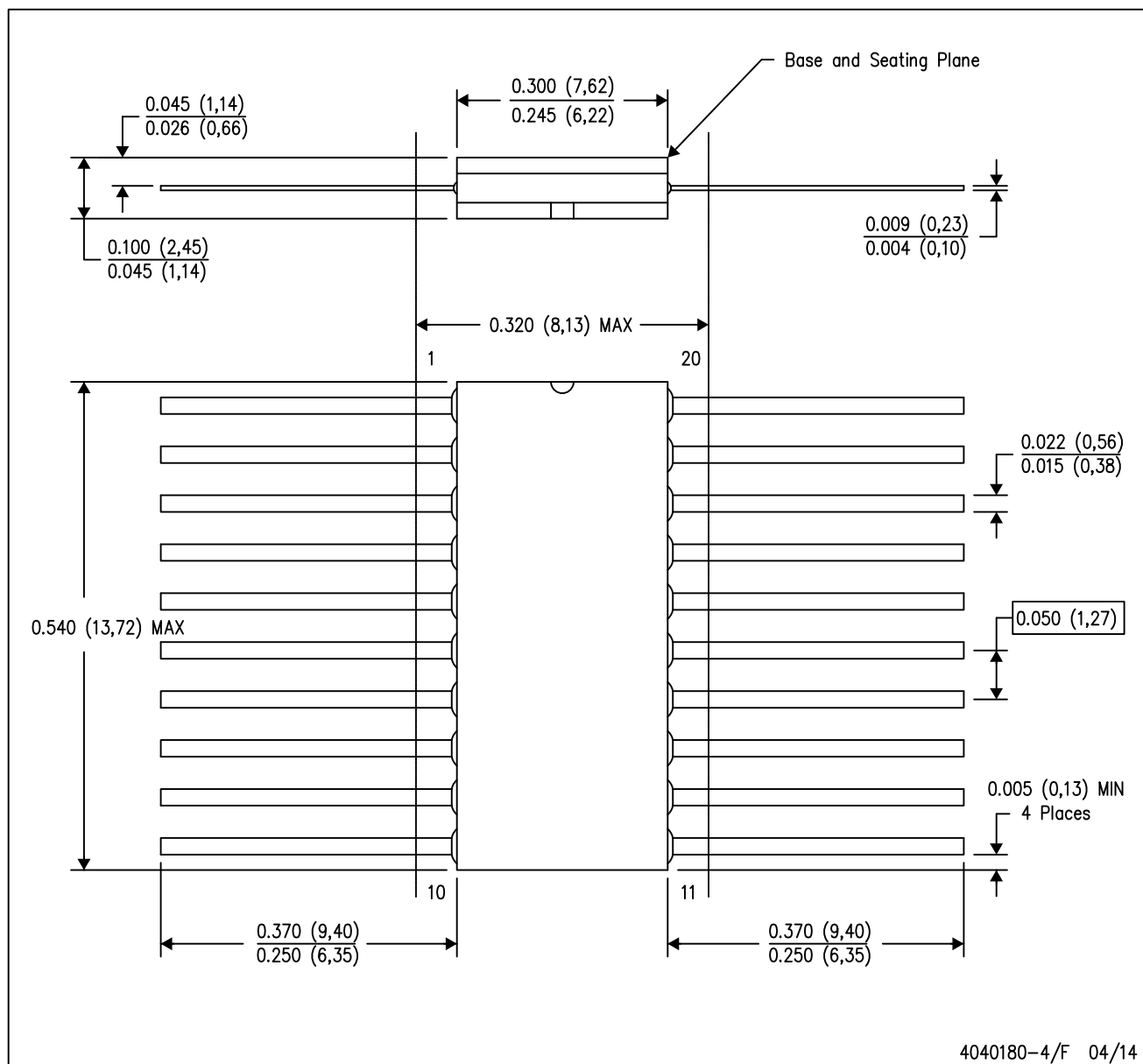


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC244ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74HC244APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74HC244DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74HC244DWR	SOIC	DW	20	2000	350.0	350.0	43.0
SN74HC244DWR	SOIC	DW	20	2000	600.0	144.0	84.0
SN74HC244DWRG4	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC244PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74HC244PWT	TSSOP	PW	20	250	367.0	367.0	38.0
SN74HC244QDWRG4Q1	SOIC	DW	20	2000	367.0	367.0	45.0

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

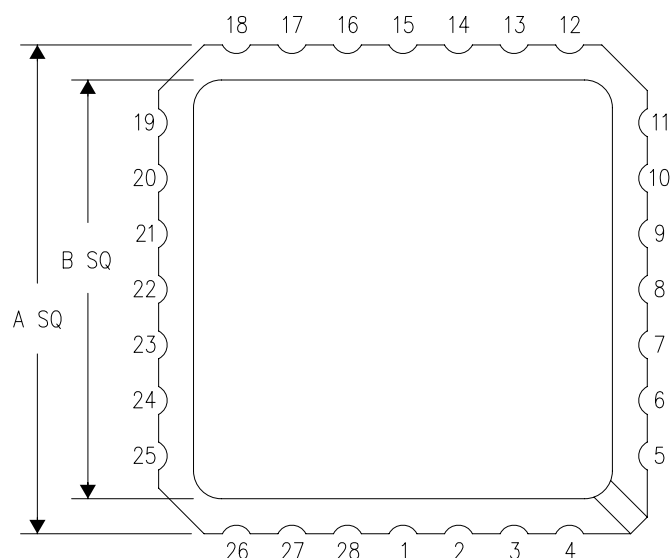


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

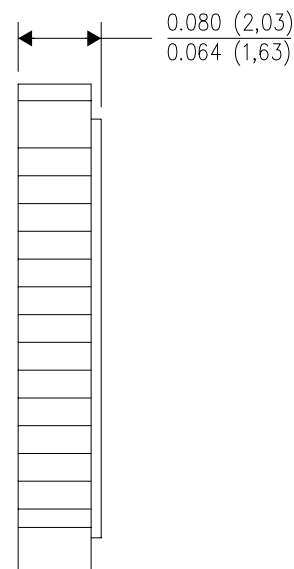
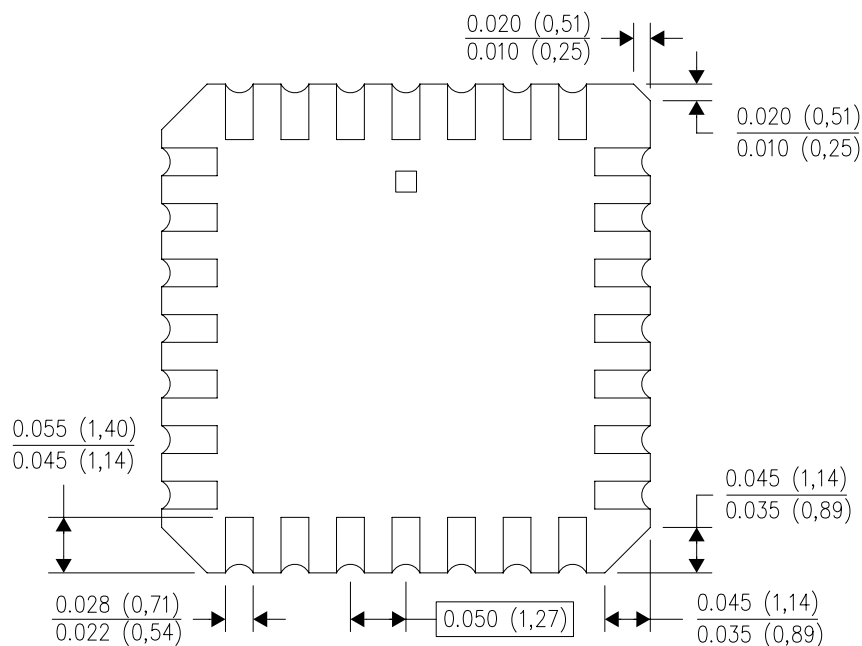
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

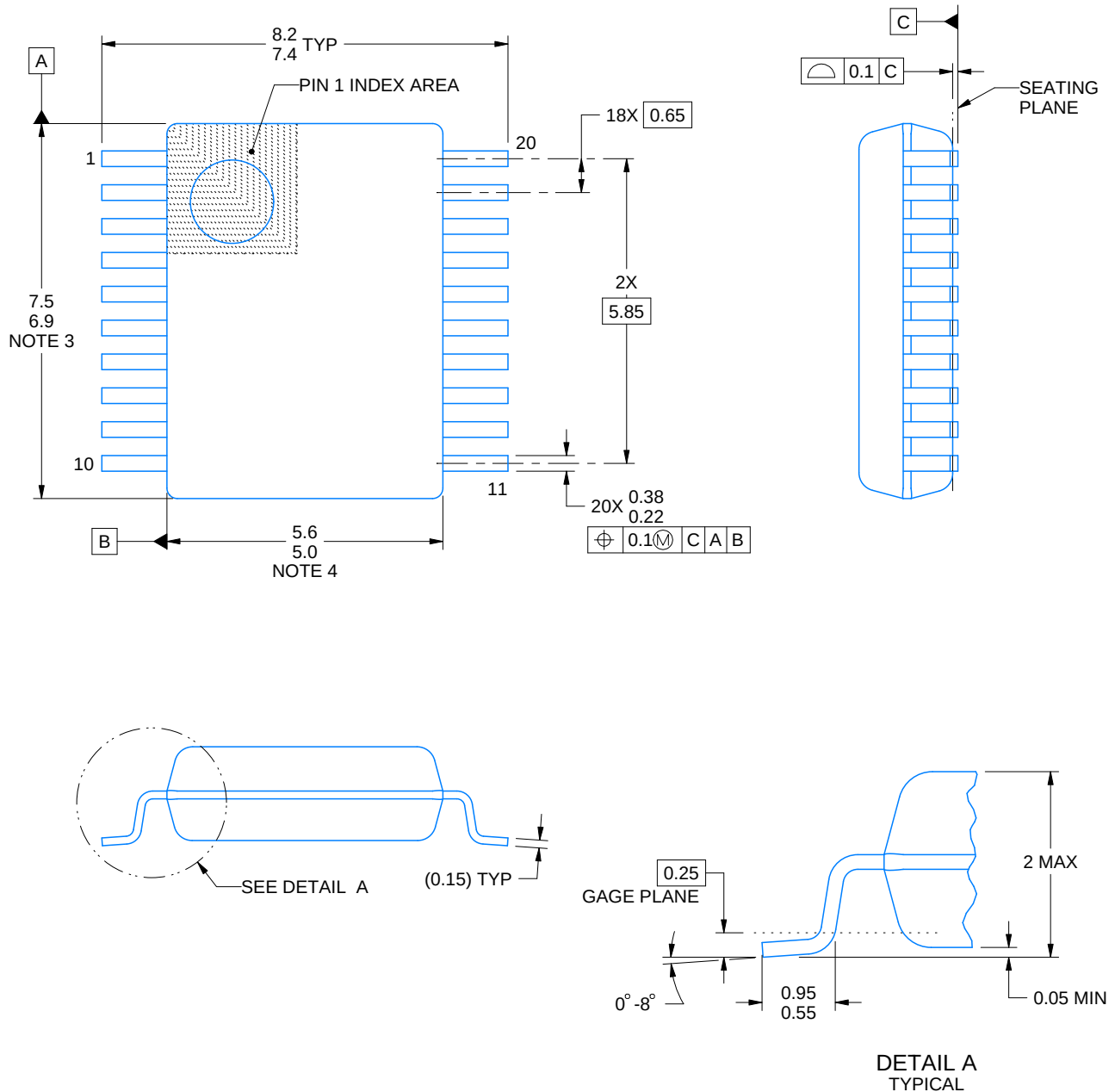
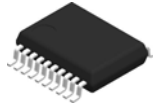


NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004



4214851/B 08/2019

NOTES:

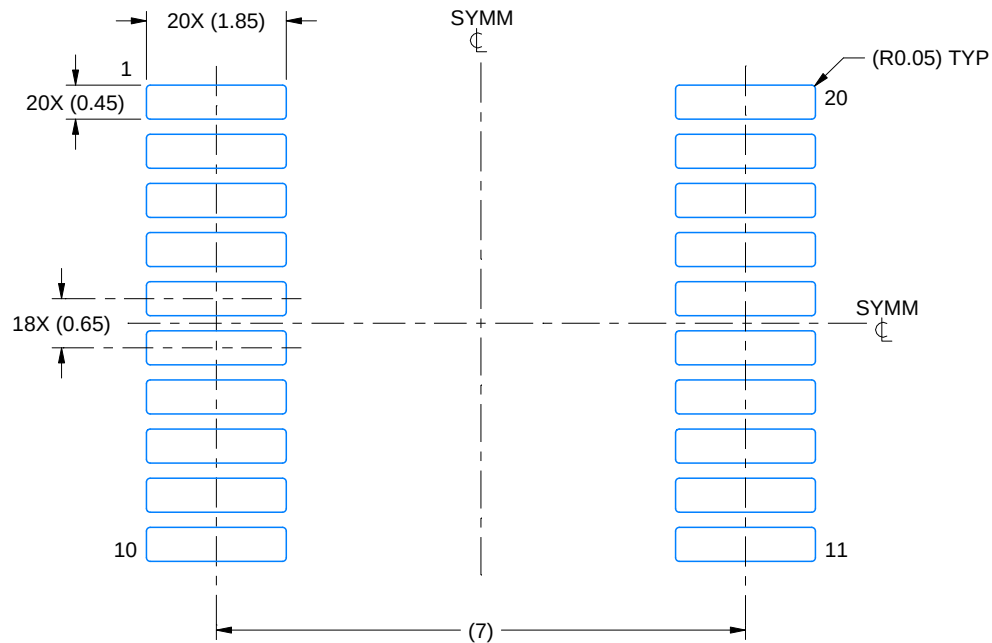
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

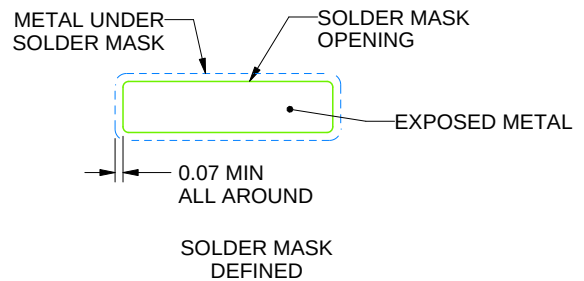
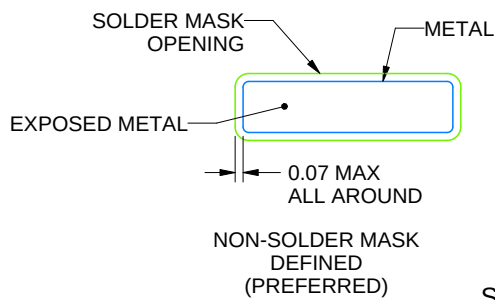
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

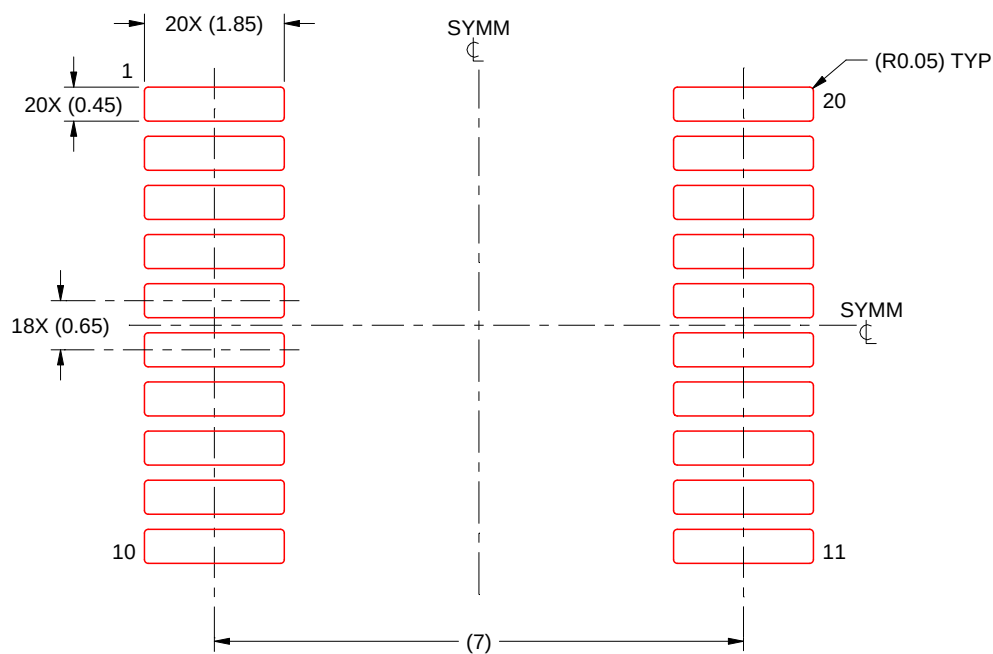
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

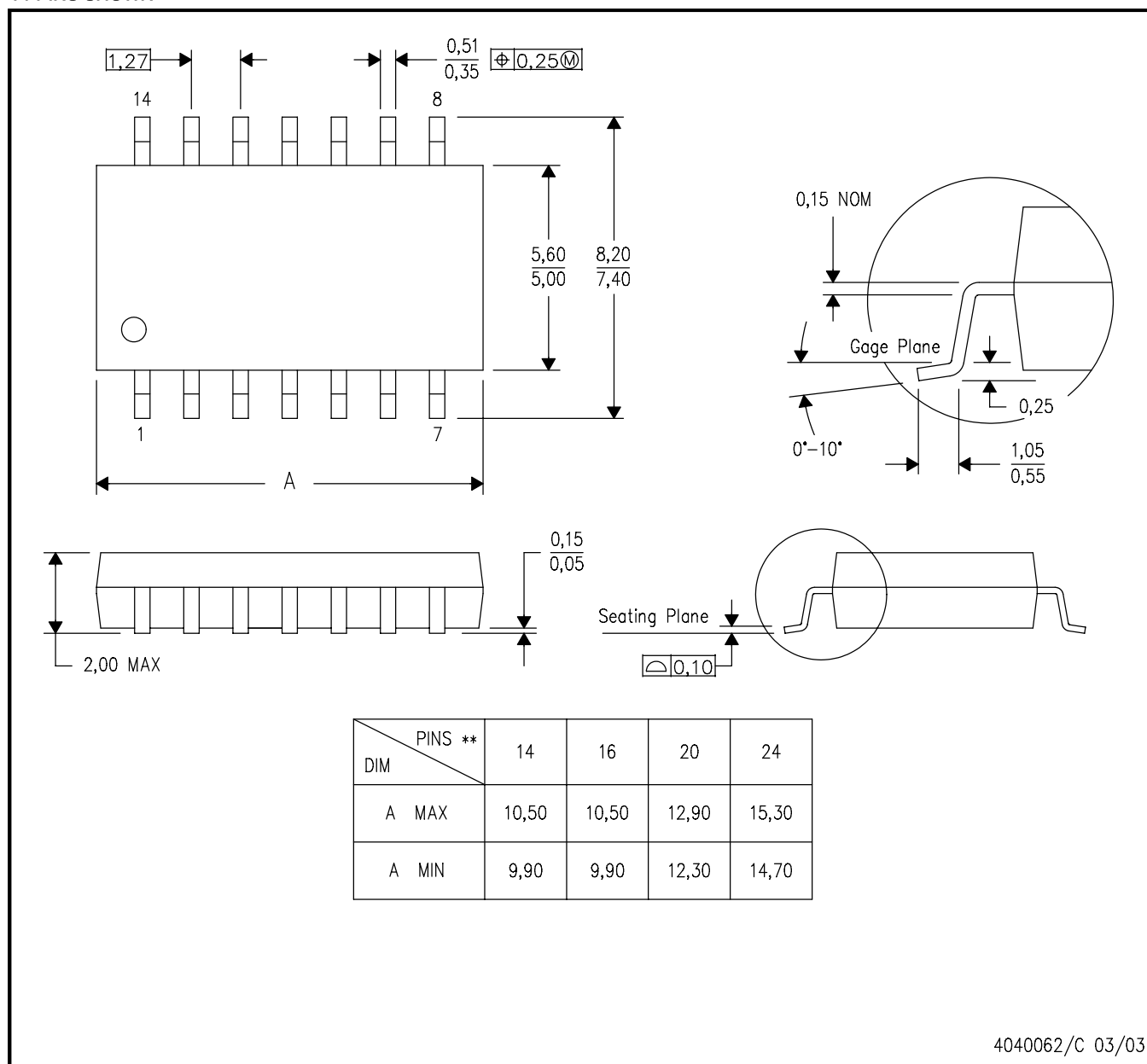
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

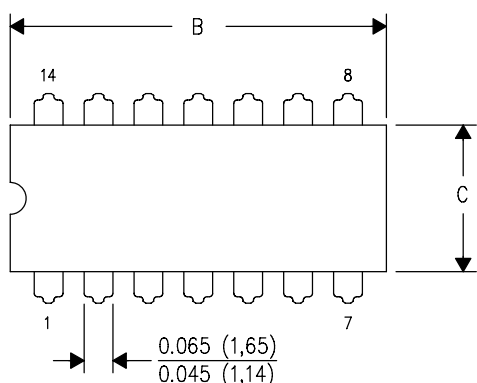


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

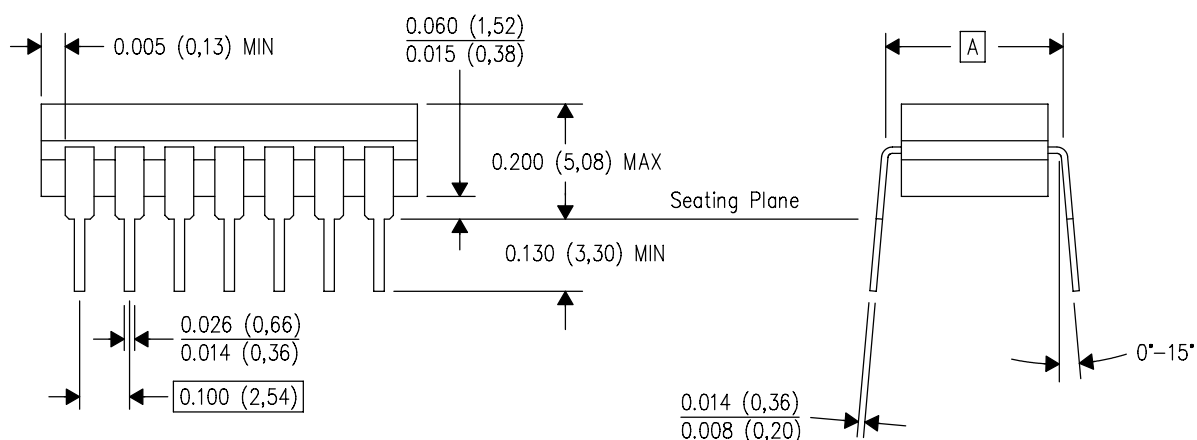
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

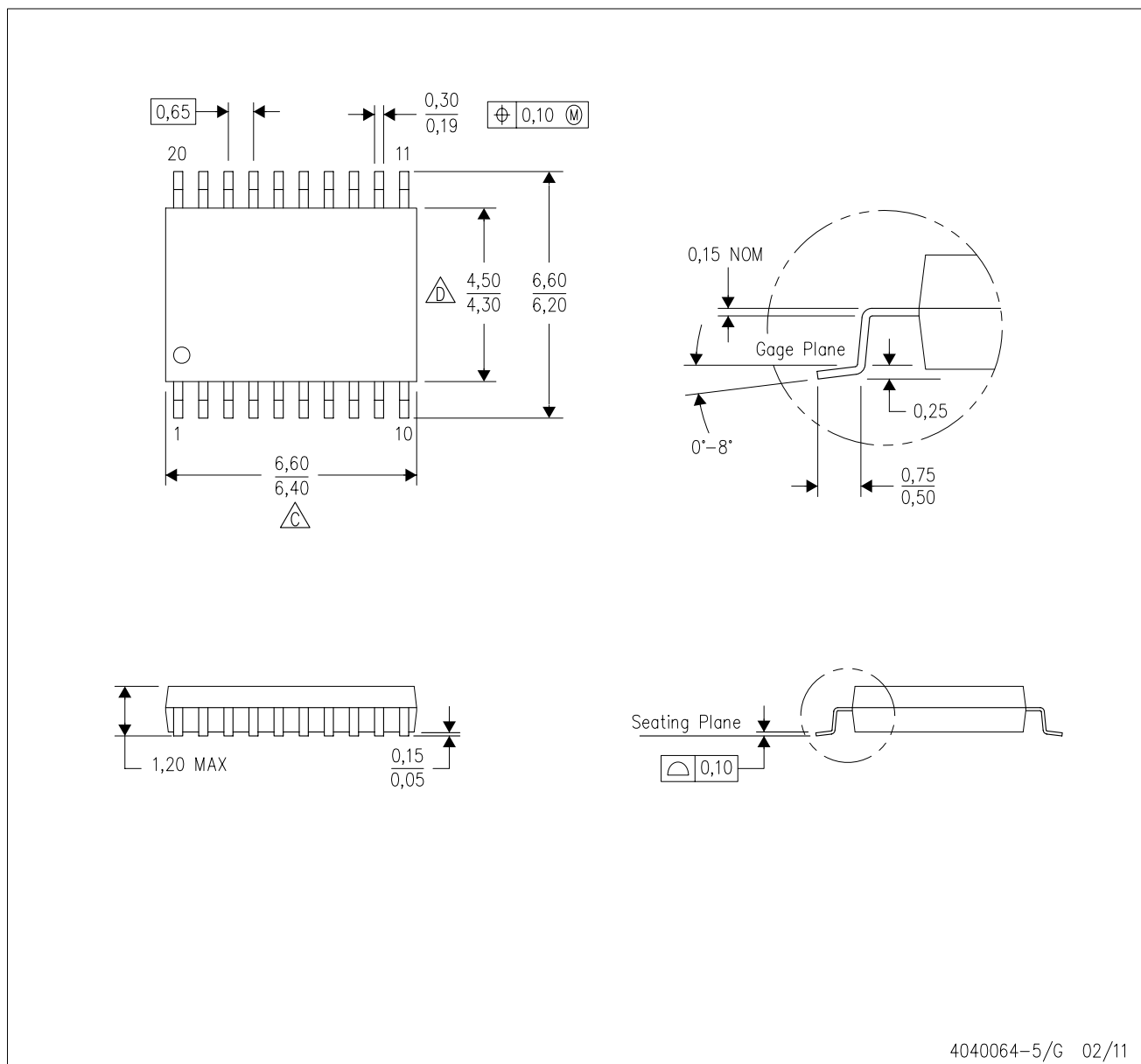


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G20)

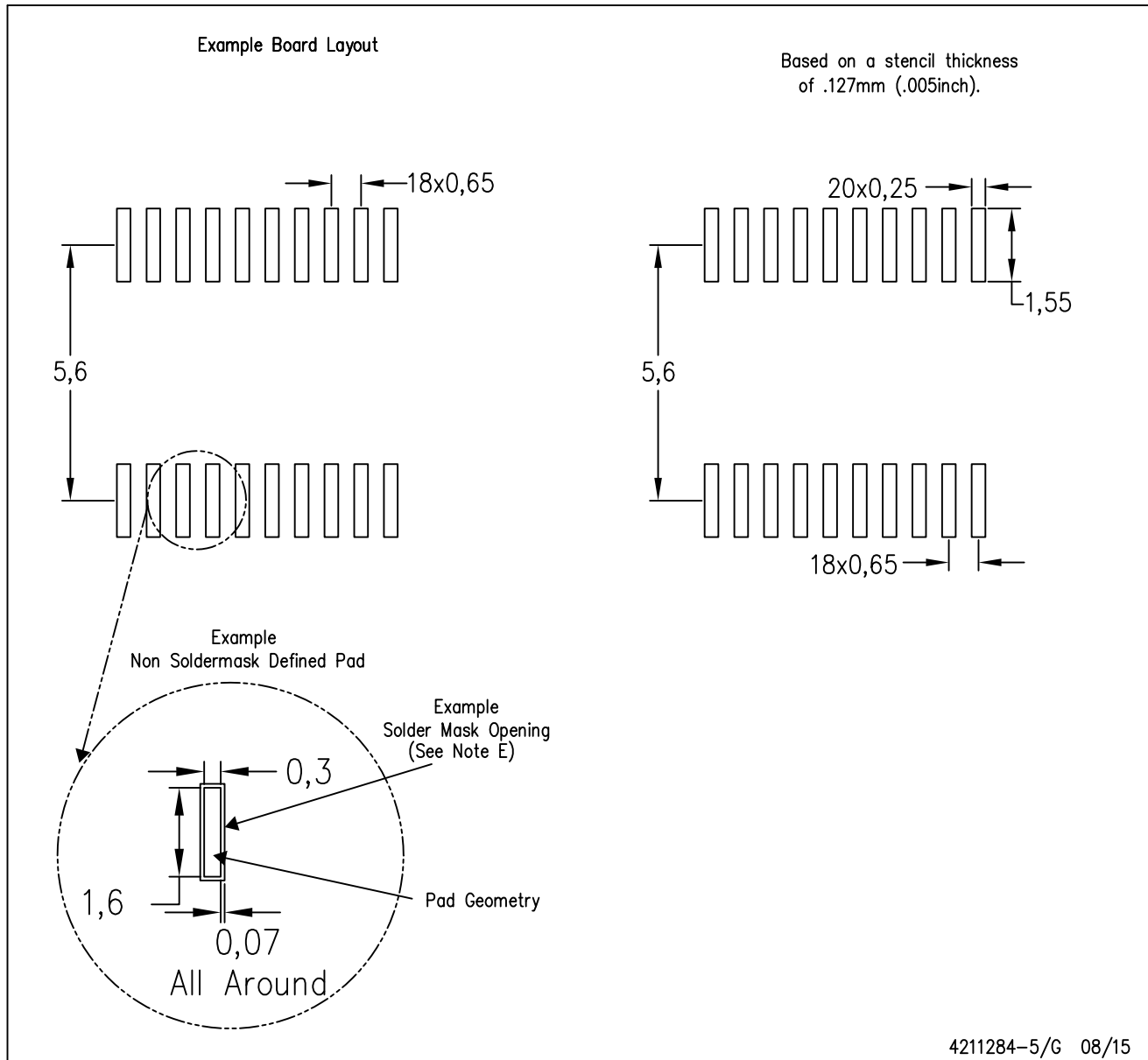
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

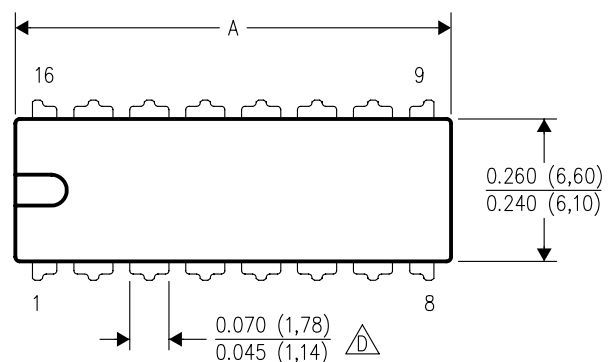


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

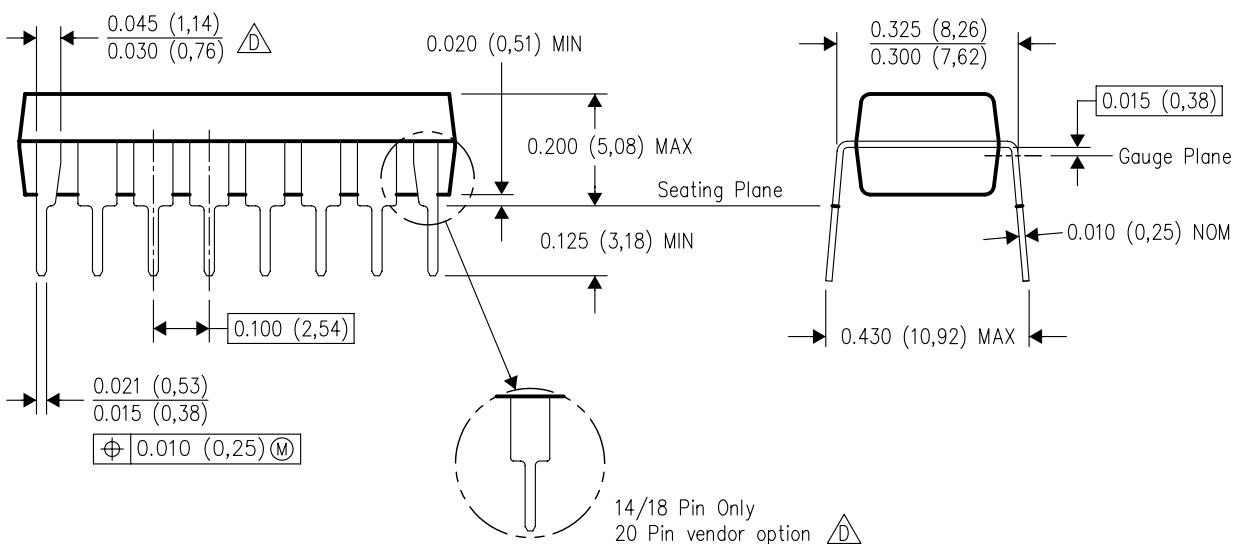
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



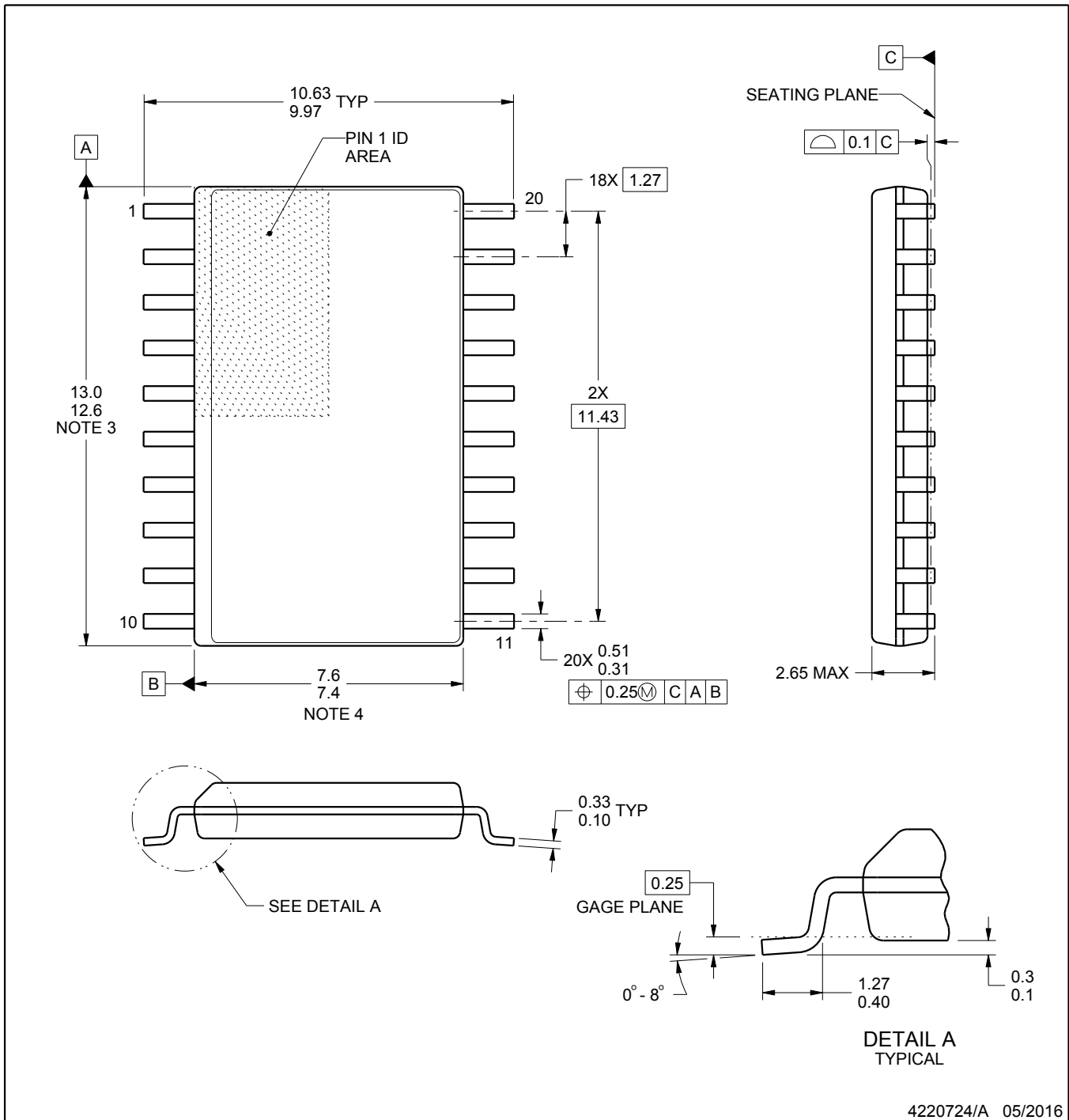
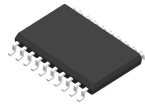
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



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NOTES:

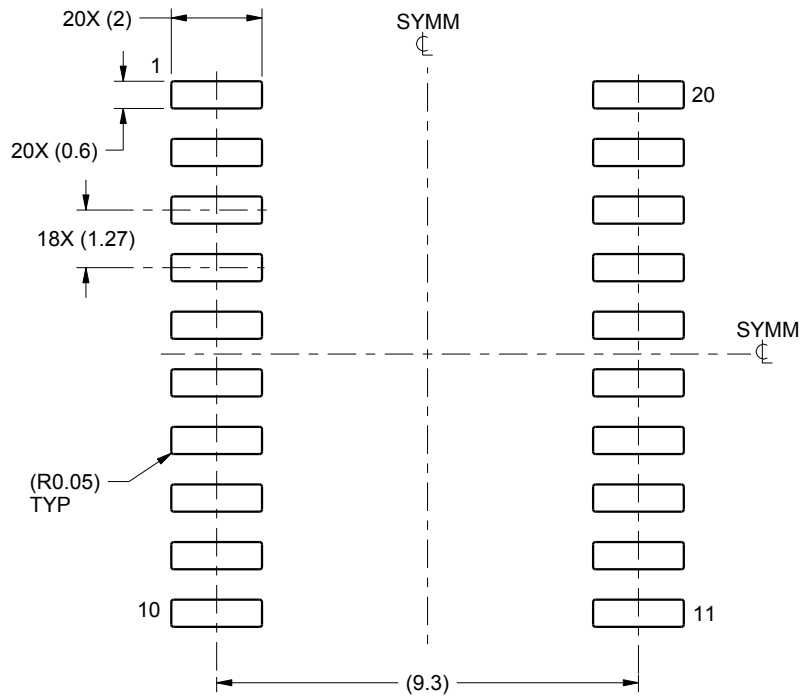
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

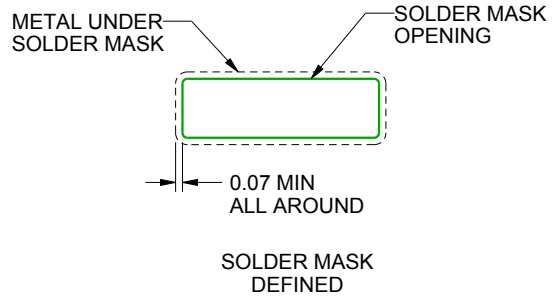
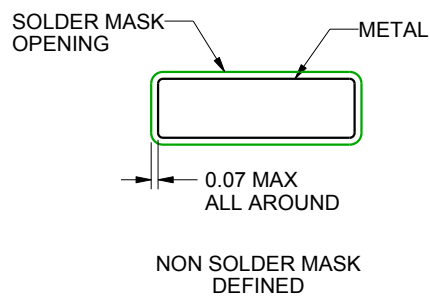
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

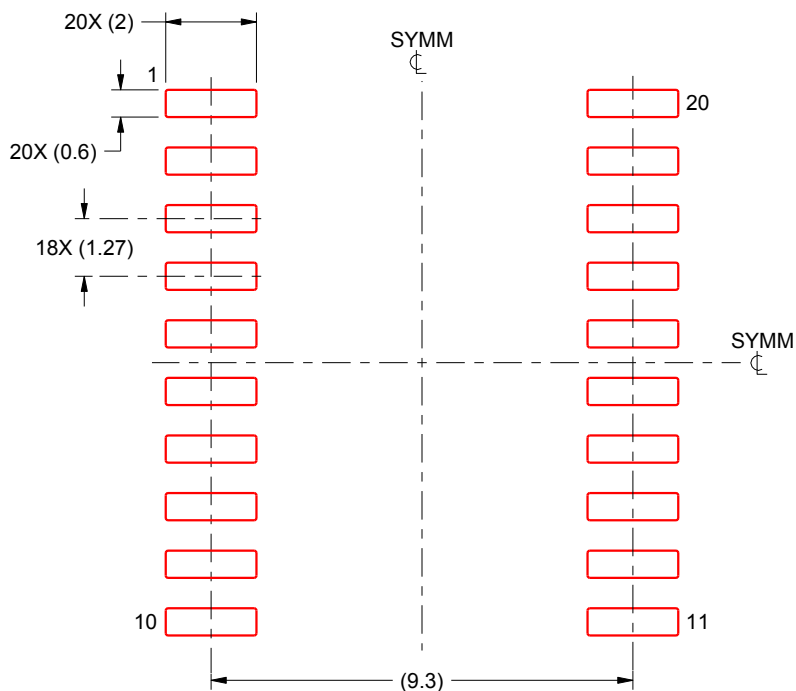
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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