

SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

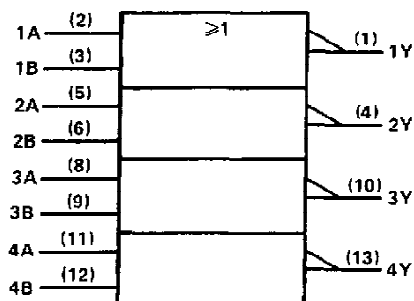
These devices contain four independent 2-input-NOR gates.

The SN5402, SN54LS02, and SN54S02 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7402, SN74LS02, and SN74S02 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

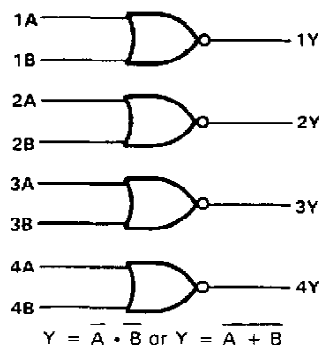
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

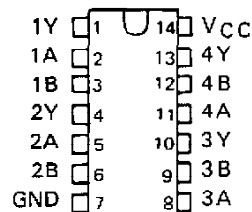
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

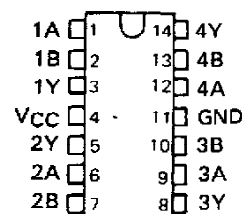


SN5402 ... J PACKAGE
SN54LS02, SN54S02 ... J OR W PACKAGE
SN7402 ... N PACKAGE
SN74LS02, SN74S02 ... D OR N PACKAGE

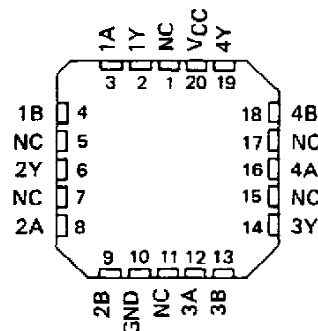
(TOP VIEW)



SN5402 ... W PACKAGE
(TOP VIEW)



SN54LS02, SN54S02 ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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schematics (each gate)



Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: '02, 'S02	5.5 V
'LS02	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54'	−55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

SN5402, SN7402

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

recommended operating conditions

	SN5402			SN7402			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			− 0.4			− 0.4	mA
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5402			SN7402			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = − 12 mA			− 1.5			− 1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = − 0.4 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40			40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			− 1.6			− 1.6	mA
I _{OS} §	V _{CC} = MAX	− 20		− 55	− 18		− 55	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		8	16		8	16	mA
I _{CCL}	V _{CC} = MAX, See Note 2		14	27		14	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 400 Ω,	C _L = 15 pF		12	22	ns
t _{PHL}						8	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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SN54LS02, SN74LS02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

recommended operating conditions

	SN54LS02			SN74LS02			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-0.4			-0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS02			SN74LS02			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		1.6	3.2		1.6	3.2	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		2.8	5.4		2.8	5.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$	10	15		ns
t_{PHL}				10	15		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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SN54S02, SN74S02 **QUADRUPLE 2-INPUT POSITIVE-NOR GATES**

recommended operating conditions

	SN54S02			SN74S02			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-1			-1	mA
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S02			SN74S02			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		17	29		17	29	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		26	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 280 Ω, C _L = 15 pF	3.5	5.5		ns
t _{PHL}				3.5	5.5		ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF	5			ns
t _{PHL}				5			ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/00401BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 00401BCA	Samples
JM38510/00401BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 00401BDA	Samples
JM38510/00401BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 00401BDA	Samples
JM38510/07301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07301BCA	Samples
JM38510/07301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07301BCA	Samples
JM38510/07301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07301BDA	Samples
JM38510/07301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07301BDA	Samples
JM38510/30301B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30301B2A	Samples
JM38510/30301B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30301B2A	Samples
JM38510/30301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301BCA	Samples
JM38510/30301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301BCA	Samples
JM38510/30301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301BDA	Samples
JM38510/30301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301BDA	Samples
JM38510/30301SDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301SDA	Samples
JM38510/30301SDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301SDA	Samples
M38510/00401BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 00401BCA	Samples
M38510/00401BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 00401BCA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/00401BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 00401BDA	Samples
M38510/00401BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 00401BDA	Samples
M38510/07301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07301BCA	Samples
M38510/07301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07301BCA	Samples
M38510/07301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07301BDA	Samples
M38510/07301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07301BDA	Samples
M38510/30301B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30301B2A	Samples
M38510/30301B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30301B2A	Samples
M38510/30301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301BCA	Samples
M38510/30301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301BCA	Samples
M38510/30301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301BDA	Samples
M38510/30301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301BDA	Samples
M38510/30301SDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301SDA	Samples
M38510/30301SDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 30301SDA	Samples
SN5402J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN5402J	Samples
SN5402J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN5402J	Samples
SN54LS02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54LS02J	Samples
SN54LS02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54LS02J	Samples
SN54S02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54S02J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN54S02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54S02J	Samples
SN7402N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN7402N	Samples
SN7402N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN7402N	Samples
SN74LS02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS02	Samples
SN74LS02N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS02N	Samples
SN74LS02N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS02N	Samples
SN74LS02NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS02N	Samples
SN74LS02NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS02N	Samples
SN74LS02NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS02	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS02NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS02	Samples
SN74LS02NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS02	Samples
SN74LS02NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS02	Samples
SN74S02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	S02	Samples
SN74S02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	S02	Samples
SN74S02N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74S02N	Samples
SN74S02N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74S02N	Samples
SNJ5402J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ5402J	Samples
SNJ5402J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ5402J	Samples
SNJ5402W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ5402W	Samples
SNJ5402W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ5402W	Samples
SNJ54LS02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 02FK	Samples
SNJ54LS02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 02FK	Samples
SNJ54LS02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54LS02J	Samples
SNJ54LS02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54LS02J	Samples
SNJ54LS02W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54LS02W	Samples
SNJ54LS02W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54LS02W	Samples
SNJ54S02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 02FK	Samples
SNJ54S02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 02FK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54S02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54S02J	Samples
SNJ54S02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54S02J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

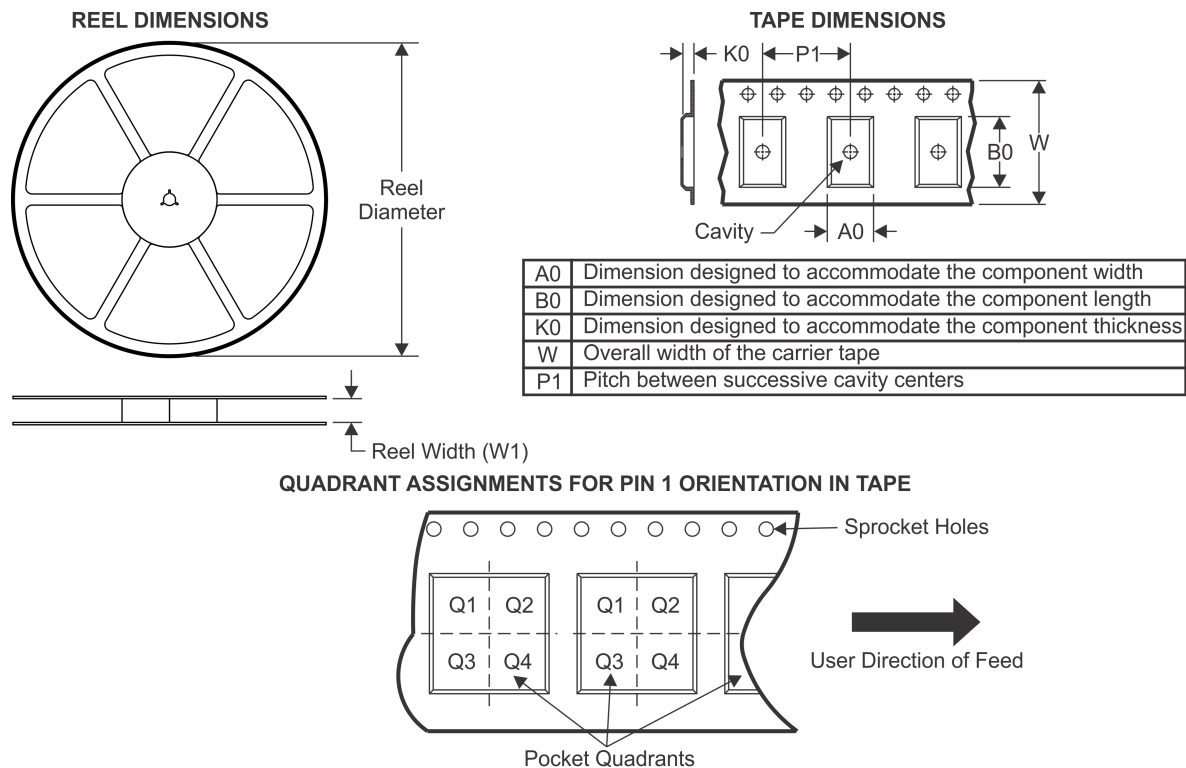
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN5402, SN54LS02, SN54LS02-SP, SN54S02, SN7402, SN74LS02, SN74S02 :

- Catalog: [SN7402](#), [SN74LS02](#), [SN54LS02](#), [SN74S02](#)
- Military: [SN5402](#), [SN54LS02](#), [SN54S02](#)
- Space: [SN54LS02-SP](#)

NOTE: Qualified Version Definitions:

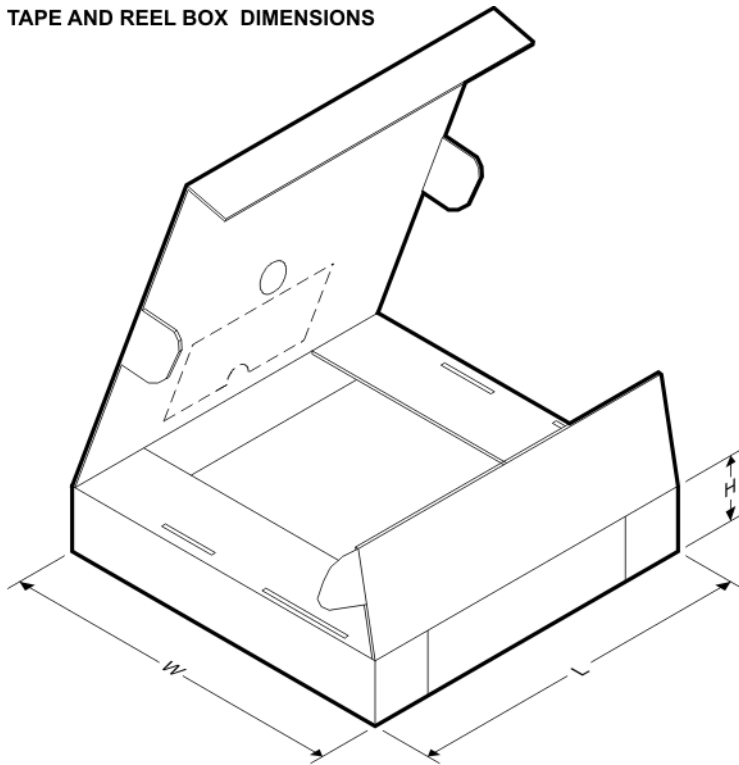
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS02DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



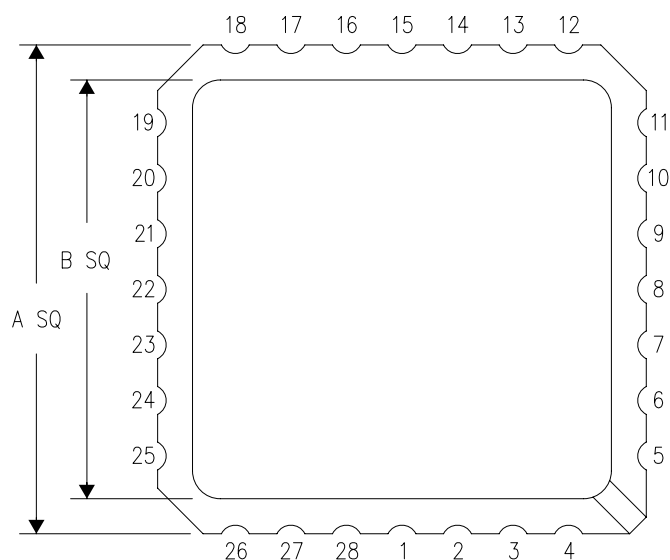
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS02DR	SOIC	D	14	2500	367.0	367.0	38.0

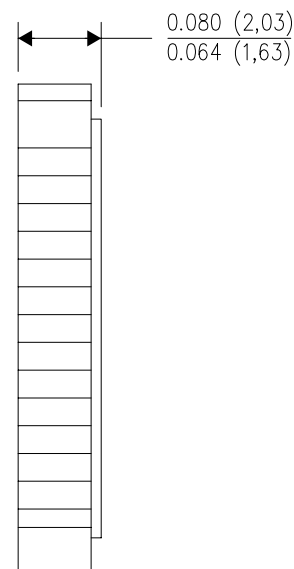
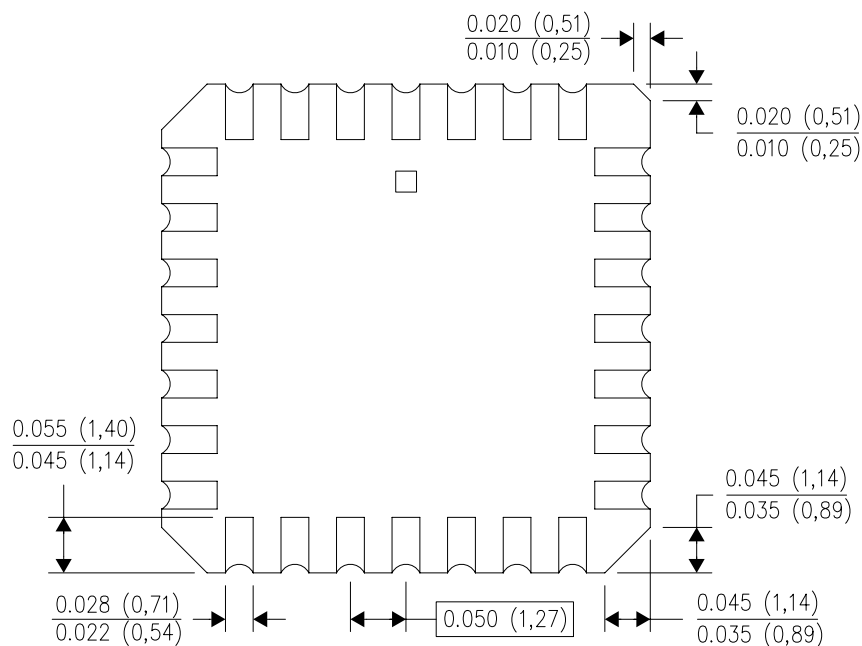
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

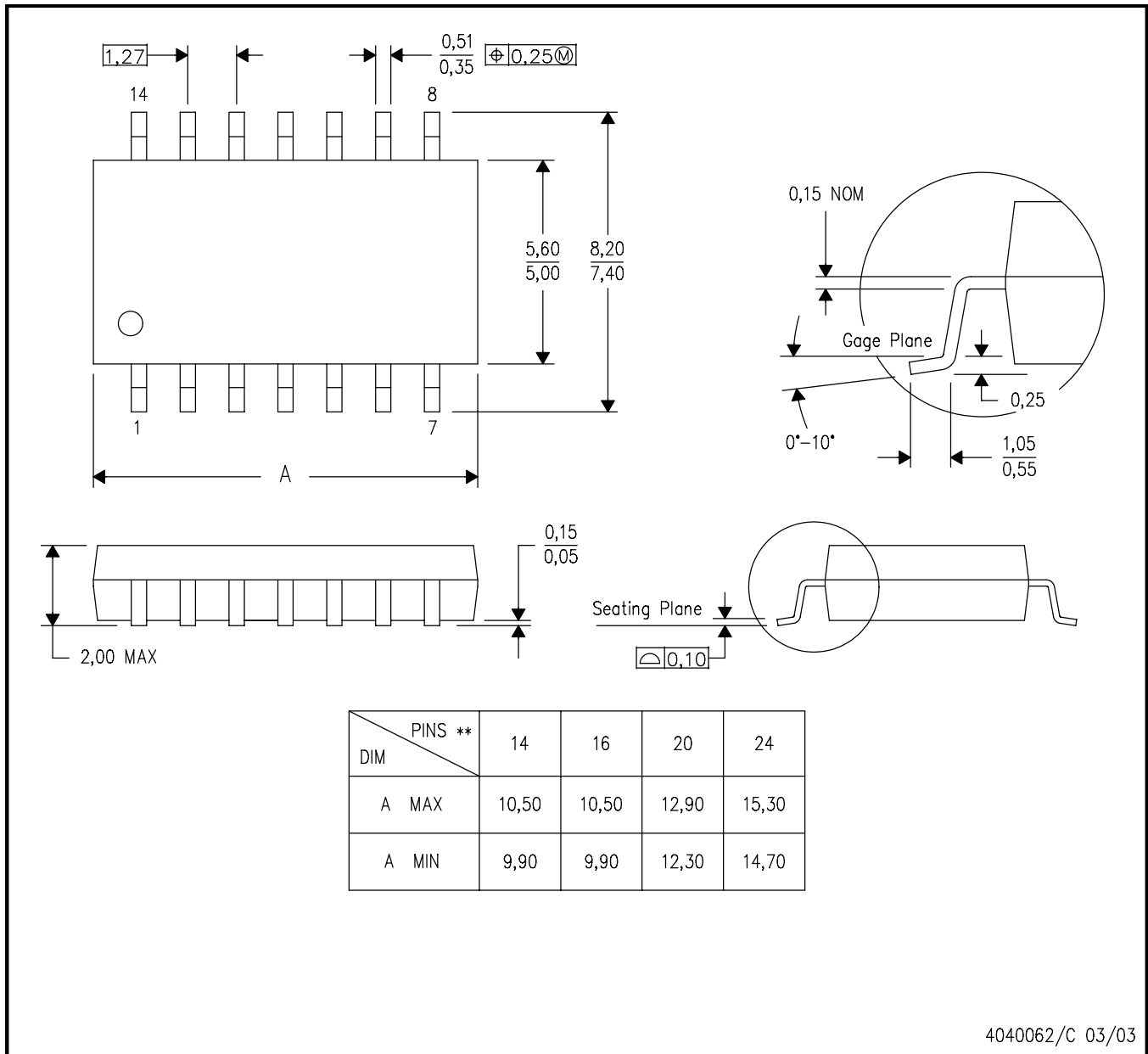
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

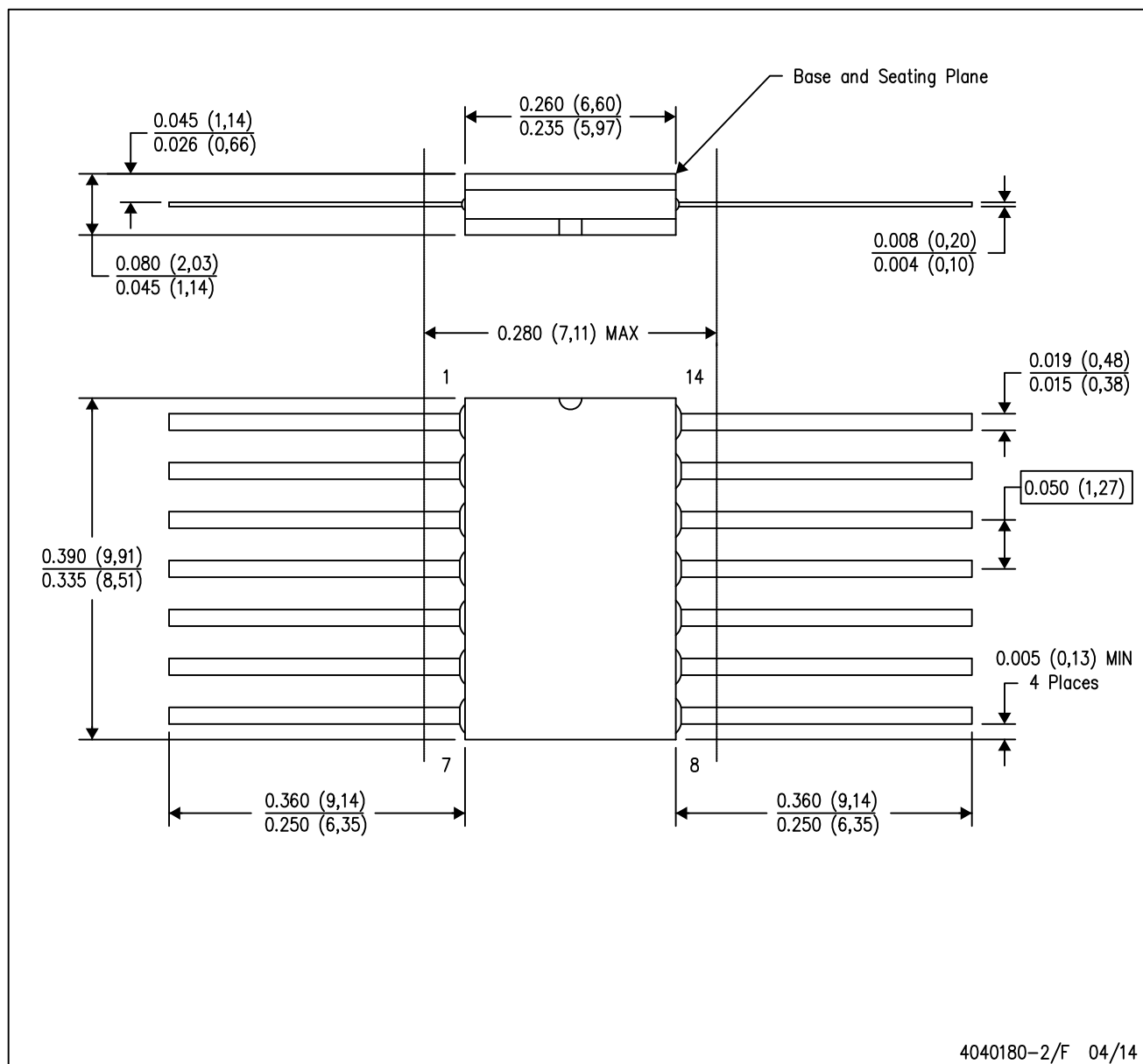
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



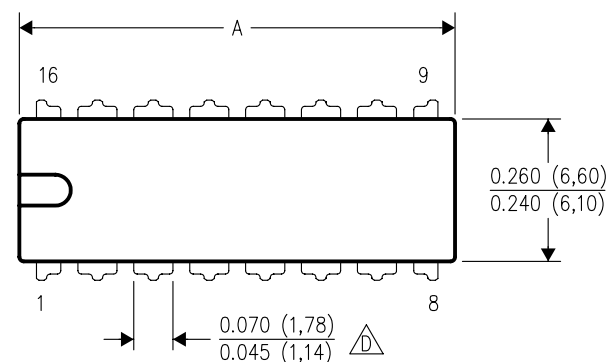
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL STD 1835 GDFP1-F14

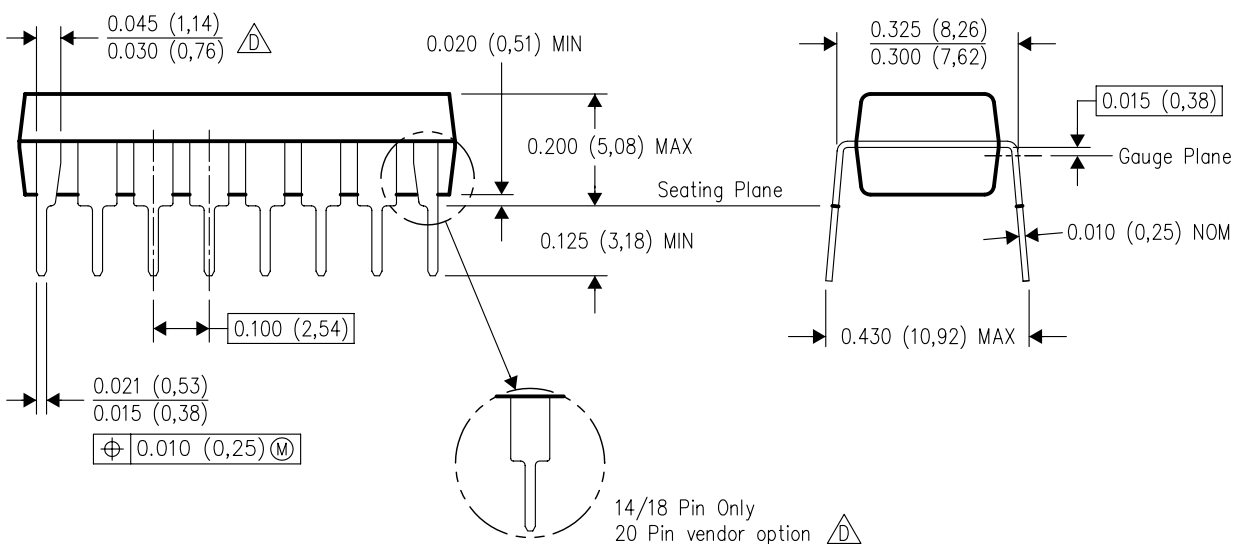
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

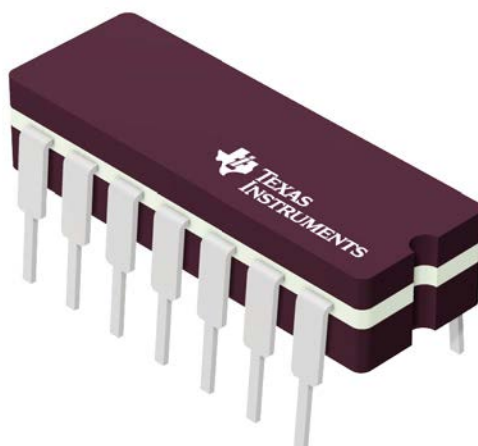
- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

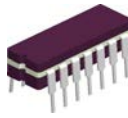
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

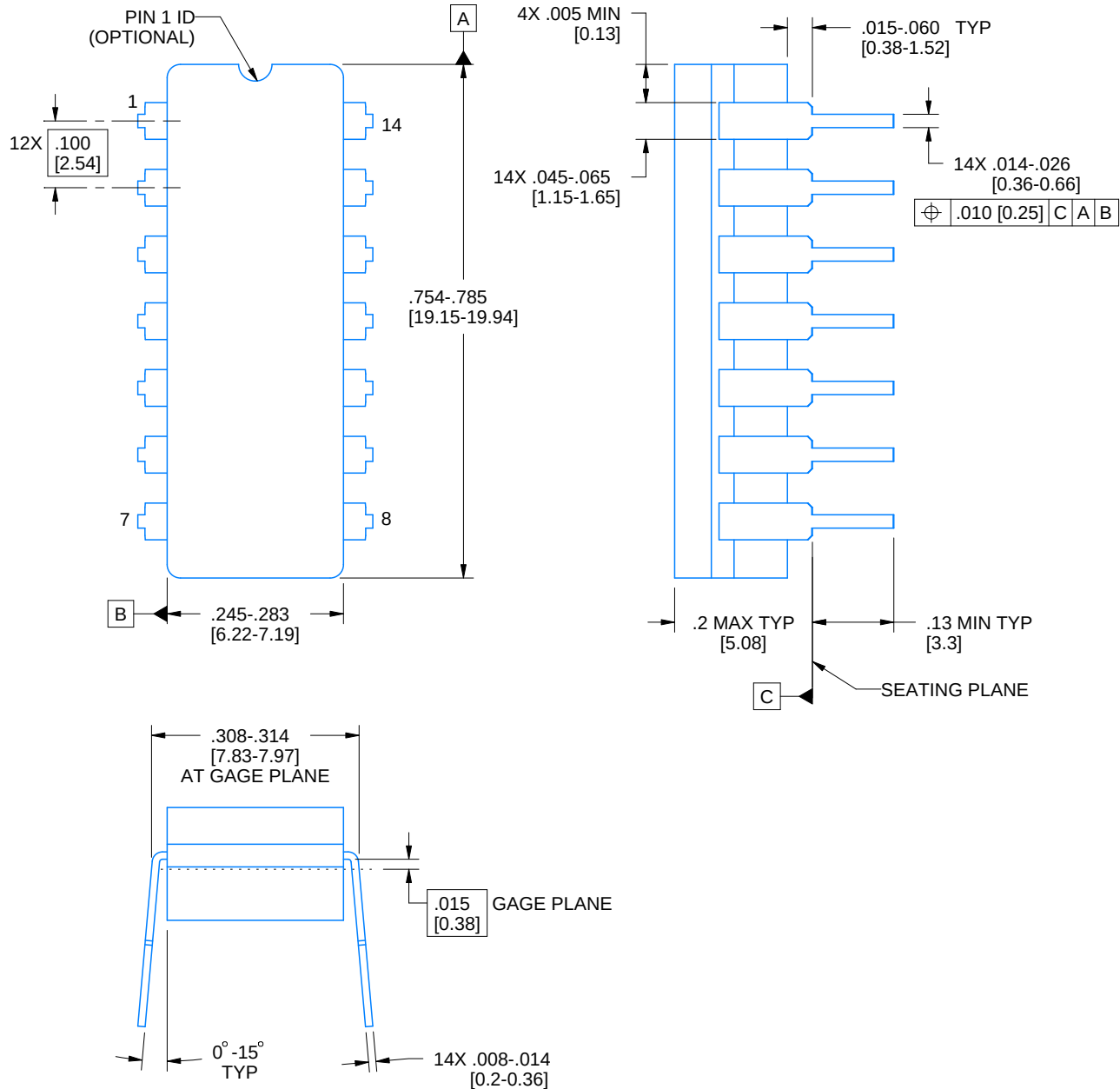
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

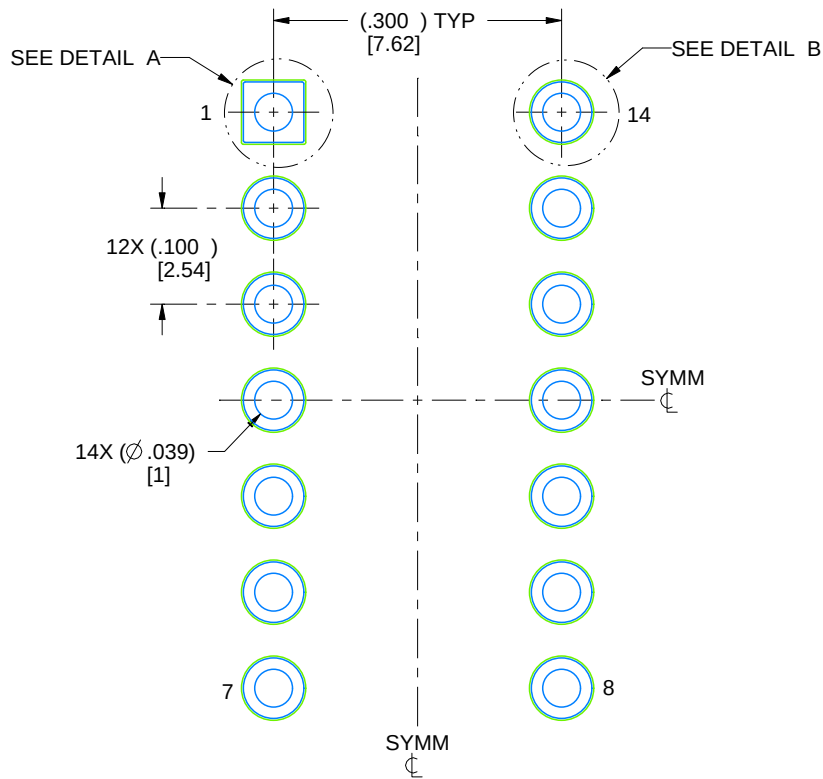
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

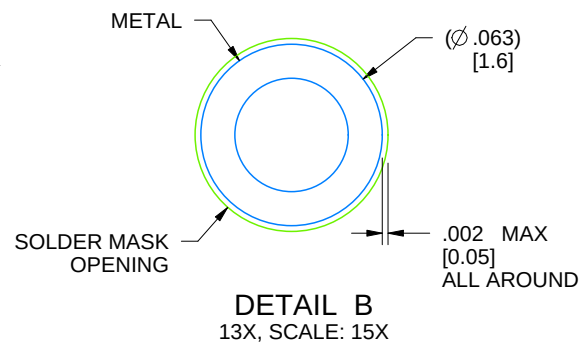
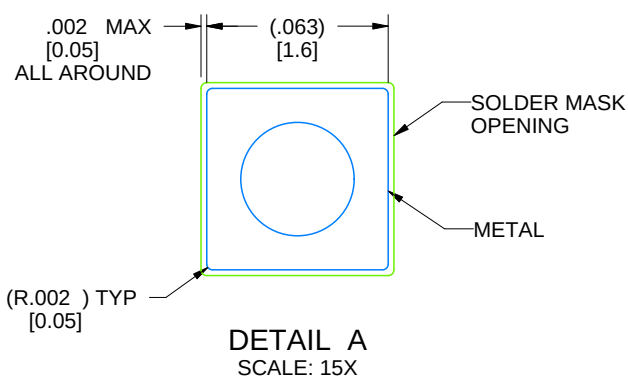
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



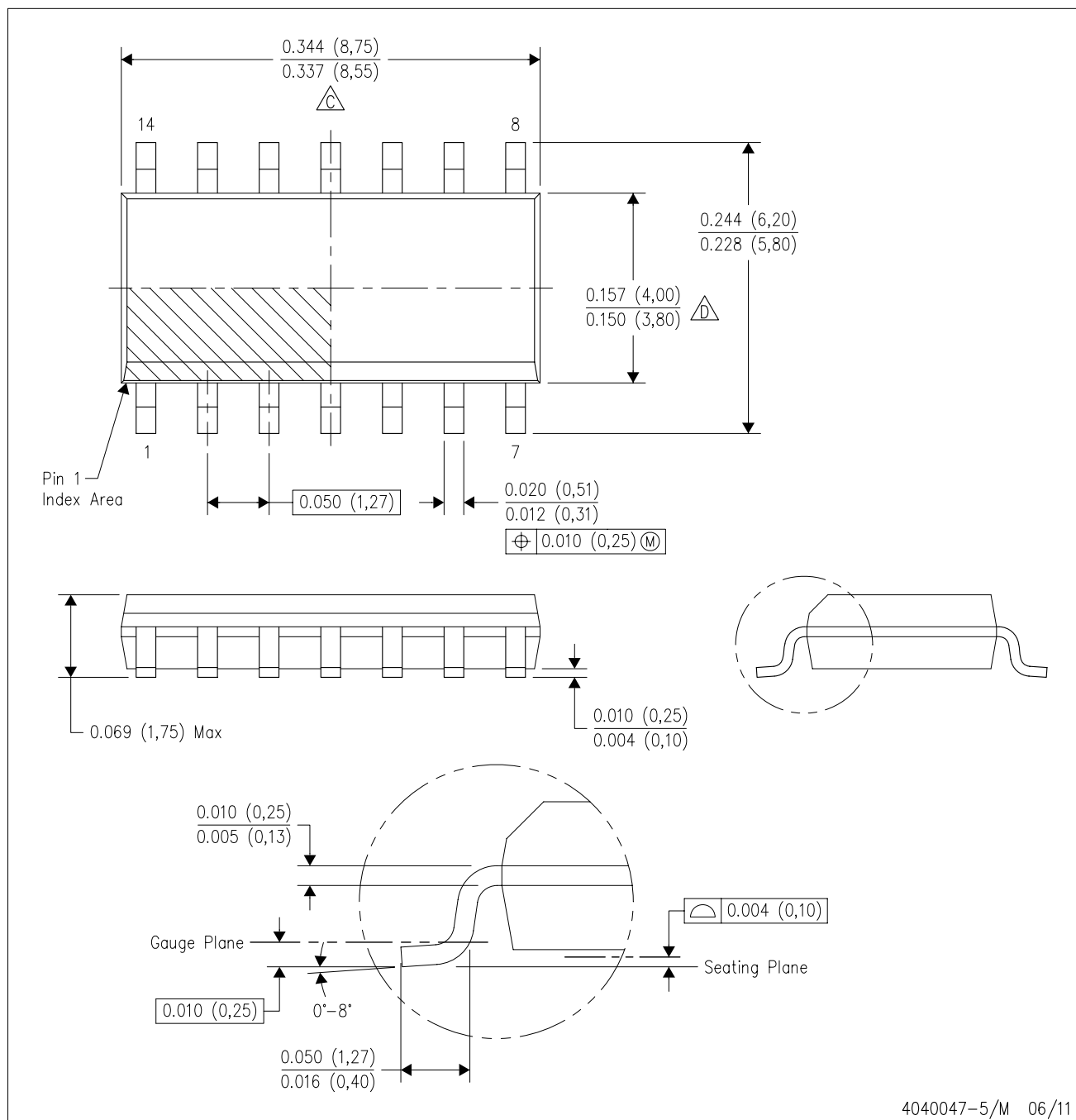
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

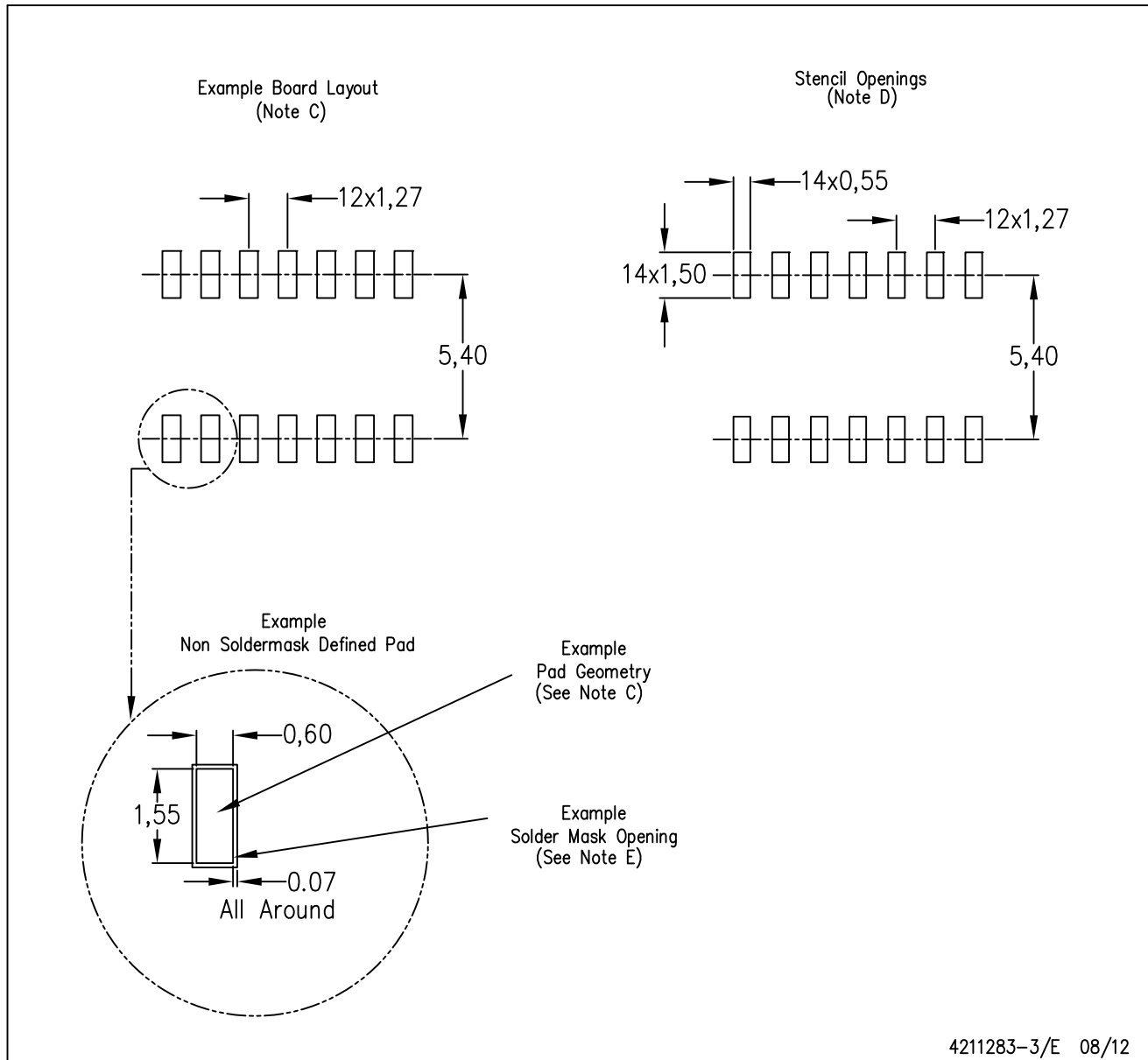


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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