KODENSHI AUK

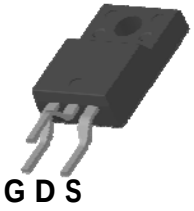
SMK0825FZ

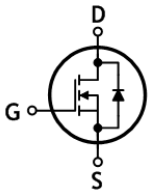
Advanced N-Ch Power MOSFET

SWITCHING REGULATOR APPLICATION

Features

- High voltage: BV_{DSS}=250V (Min.)
- Low gate charge: Q_g=14.5nC (Typ.)
- Low drain-source On resistance: $R_{DS(on)}$=0.43Ω (Max.)
- 100% avalanche tested
- RoHS compliant device



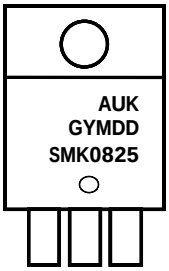


TO-220F-3L

Ordering Information

Part Number	Marking	Package
SMK0825FZ	SMK0825	TO-220F-3L (Z-Forming)

Marking Information



Column 1 : Manufacturer
Column 2 : Production Information
e.g.) GYMDD
-. G : Factory Management Code
-. YMDD : Date Code (Year, Month, Date)
Column 3 : Device Code

Absolute maximum ratings (T_C=25°C unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V_{DSS}		250	V
Repetitive Avalanche Voltage (Note 1, 2)	$V_{DS(Avalanche)}$		300	V
Gate-source voltage	V_{GSS}		±30	V
Drain current (DC) *	I_D	T_c=25°C	8	A
		T_c=100°C	5.2	A
Drain current (Pulsed) *	I_{DM}		32	A
Single pulsed avalanche energy (Note 2)	E_{AS}		356	mJ
Repetitive avalanche current (Note 1)	I_{AR}		8	A
Repetitive avalanche energy (Note 1)	E_{AR}		7.4	mJ
Power dissipation	P_D		29	W
Junction temperature	T_J		150	°C
Storage temperature range	T_{stg}		-55~150	°C

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 4.31	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	I_D=250uA, V_{GS}=0	250	-	-	V
Gate threshold voltage	$V_{GS(th)}$	I_D=250uA, V_{DS}=V_{GS}	2	-	4	V
Drain-source cut-off current	I_{DSS}	V_{DS}=250V, V_{GS}=0V	-	-	1	uA
Gate leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±30V	-	-	±100	nA
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=4A	-	0.35	0.43	Ω
Internal gate resistance	R_G	f=1MHz, V_{DS}=0V	-	4	10	Ω
Forward transfer conductance (Note 3)	g_{fs}	V_{DS}=10V, I_D=4A	-	7	-	S
Input capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1MHz	-	619	773	pF
Output capacitance	C_{oss}		-	141	176	
Reverse transfer capacitance	C_{rss}		-	33	41	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	V_{DD}=125V, I_D=8A R_G=25Ω	11	15	35	ns
Rise time (Note 3,4)	t_r		32	85	115	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		62	90	135	
Fall time (Note 3,4)	t_f		41	65	98	
Total gate charge (Note 3,4)	Q_g	V_{DS}=200V, V_{GS}=10V I_D=8A	-	14.5	18.2	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	4	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	4.5	-	

Source-Drain Diode Ratings and Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	8	A
Source current (Pulsed)	I_{SM}		-	-	32	A
Forward voltage	V_{SD}	V_{GS}=0V, I_S=8A	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	I_S=8A, V_{GS}=0V dI_F/dt=100A/us	-	178	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	1.16	-	uC

Note:
1. Repeated rating: Pulse width limited by maximum junction temperature
2. L=8.9mH, I_{AS}=8A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. Pulse test: Pulse width≤300us, Duty cycle≤2%
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristic Curves

Fig. 1 I_D - V_{DS}

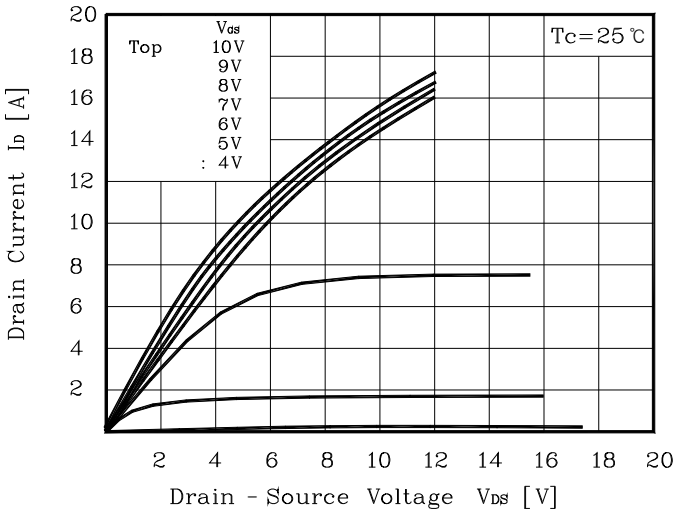


Fig. 2 I_D – V_{GS}

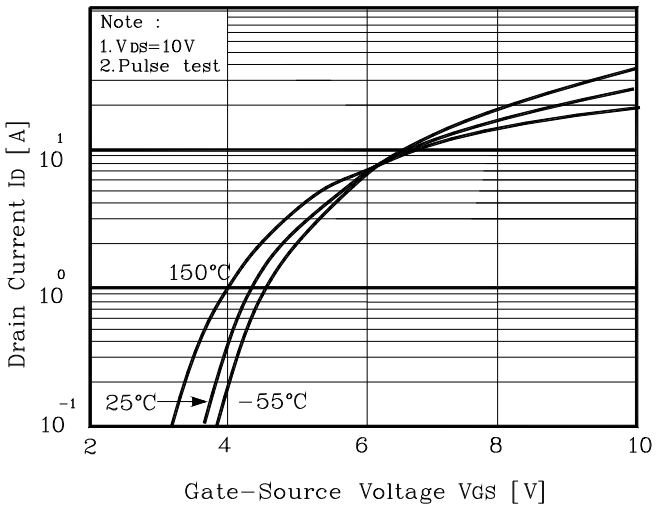


Fig. 3 $R_{DS(ON)}$ - I_D

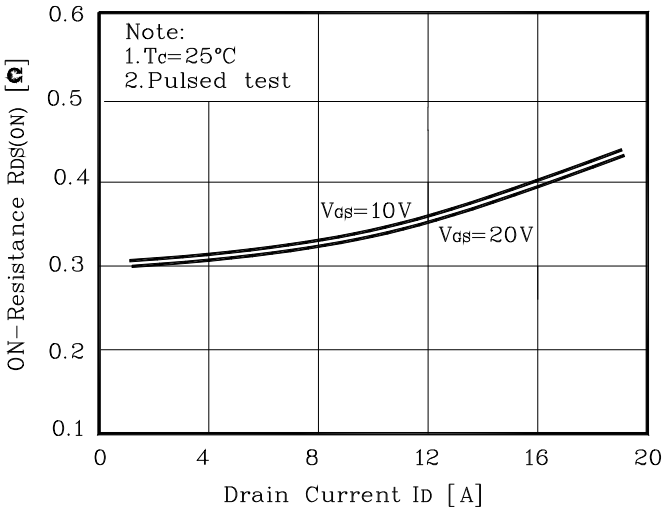


Fig. 4 I_S - V_{SD}

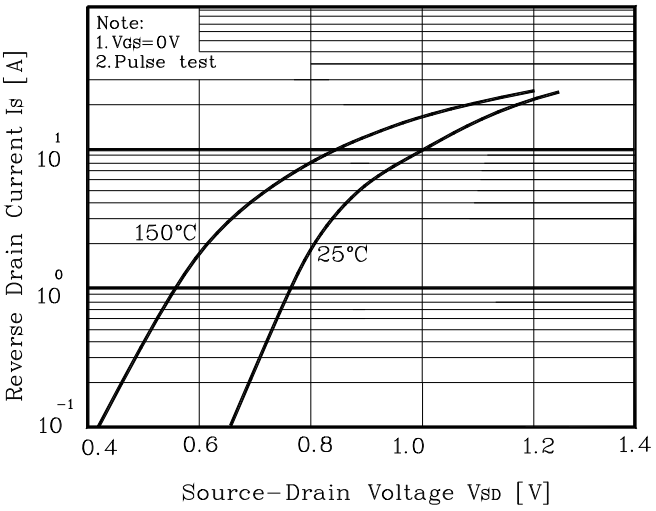


Fig. 5 Capacitance - V_{DS}

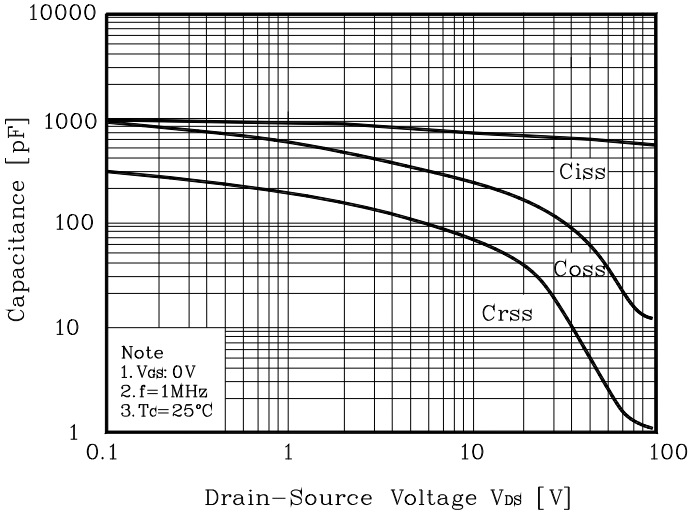
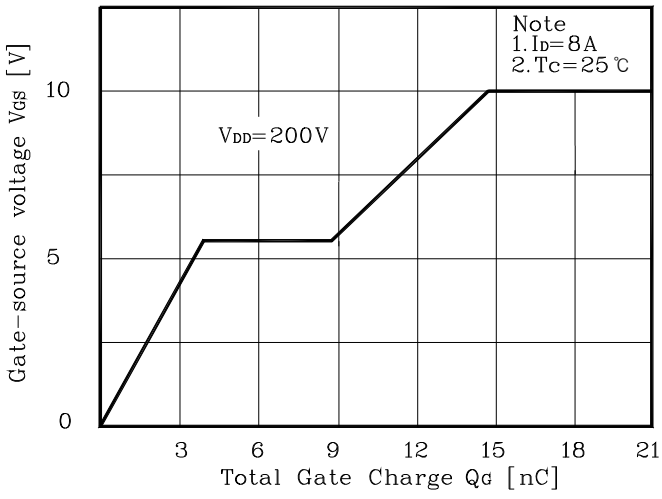


Fig. 6 V_{GS} - Q_G



Electrical Characteristic Curves (Continue)

Fig. 7 BV_{DSS} - T_J

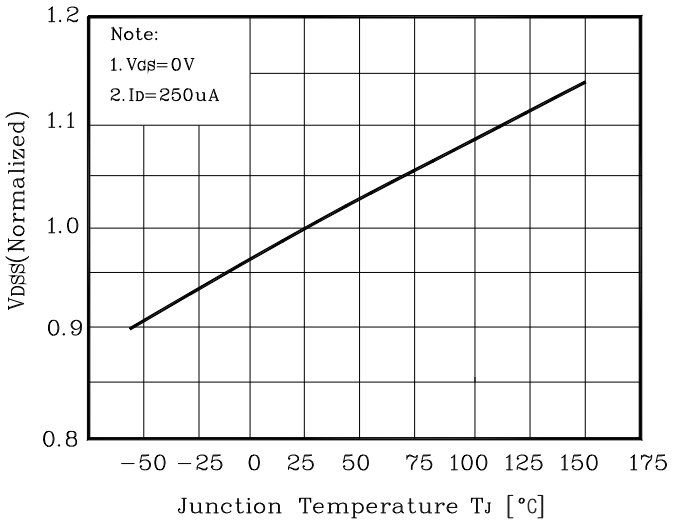


Fig. 8 $R_{DS(ON)}$ - T_J

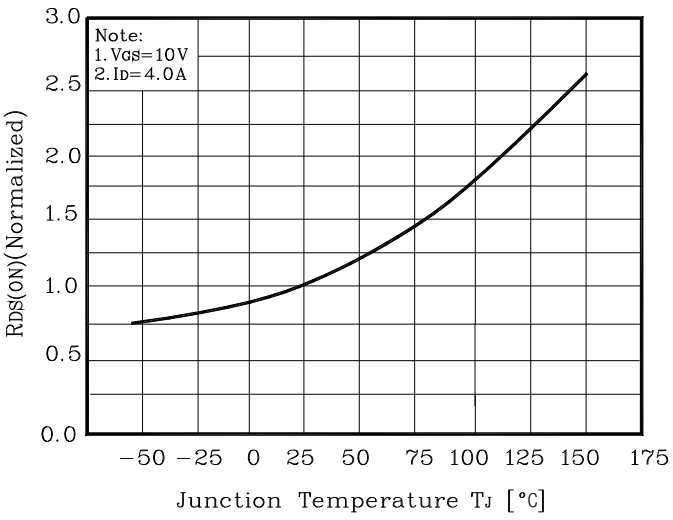


Fig. 9 I_D - T_C

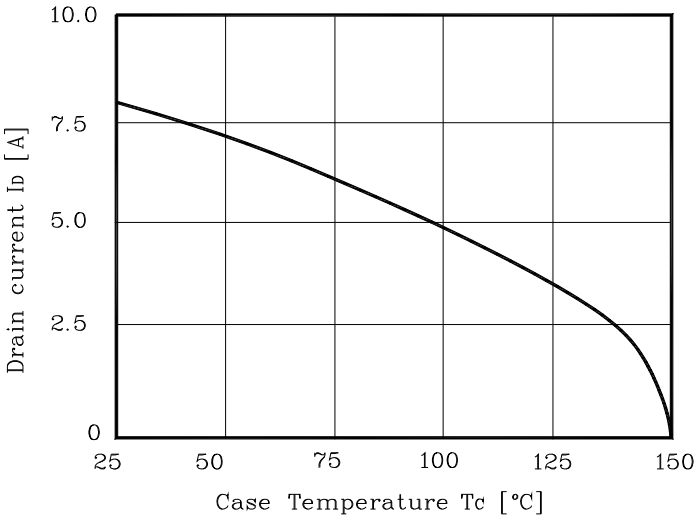


Fig. 10 Safe Operating Area

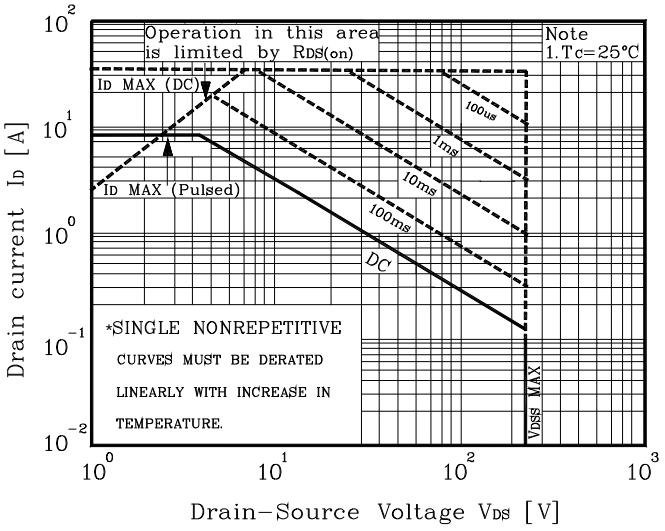
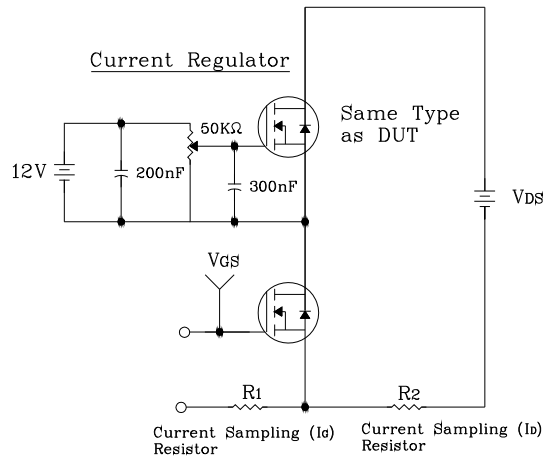


Fig. 11 Gate Charge Test Circuit & Waveform



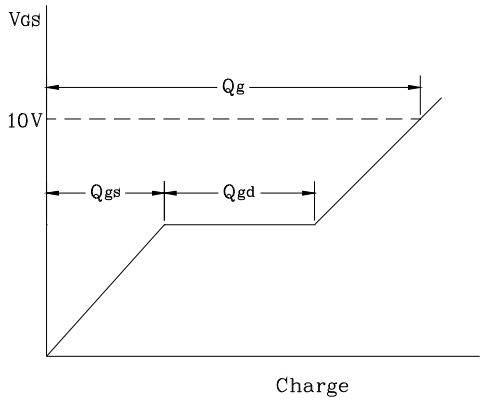
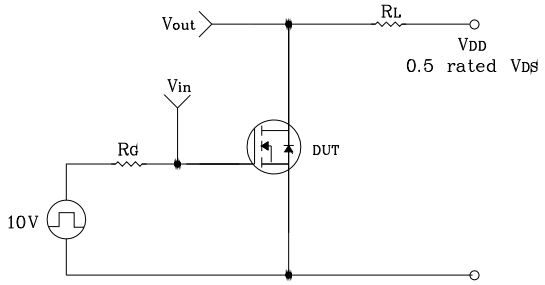


Fig. 12 Resistive Switching Test Circuit & Waveform



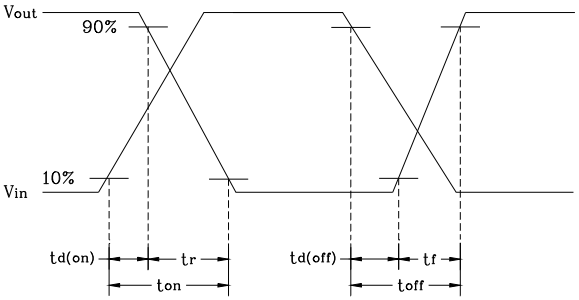
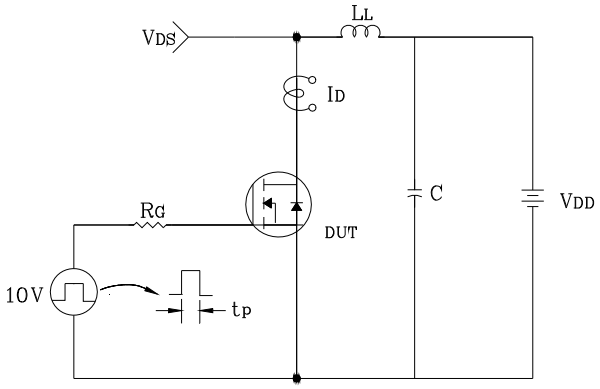


Fig. 13 E_{AS} Test Circuit & Waveform



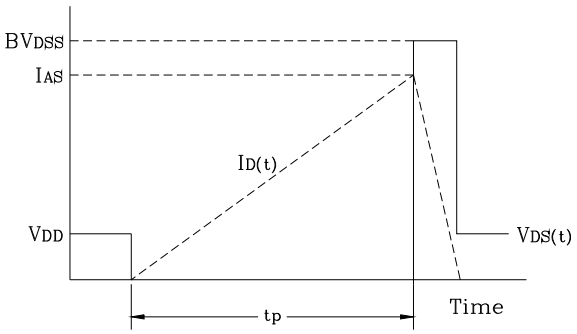
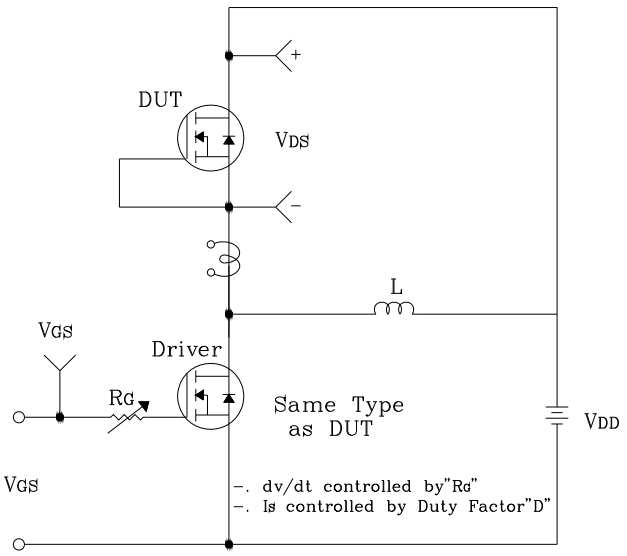
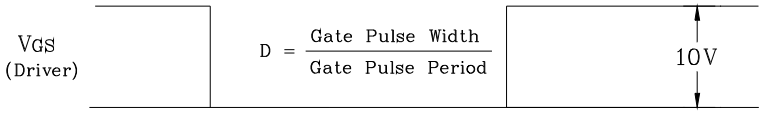
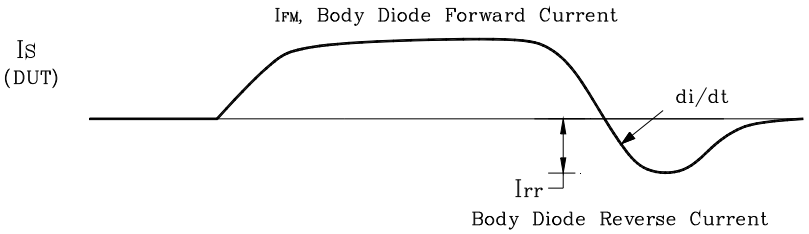
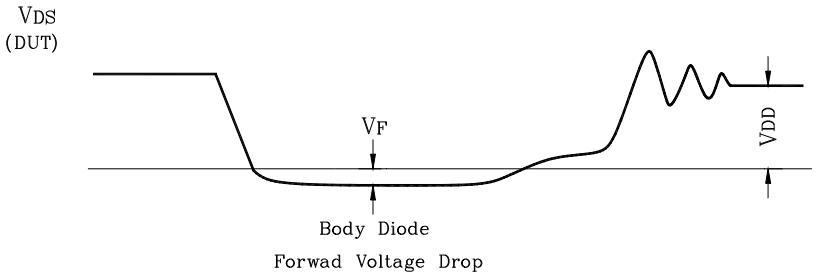


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform

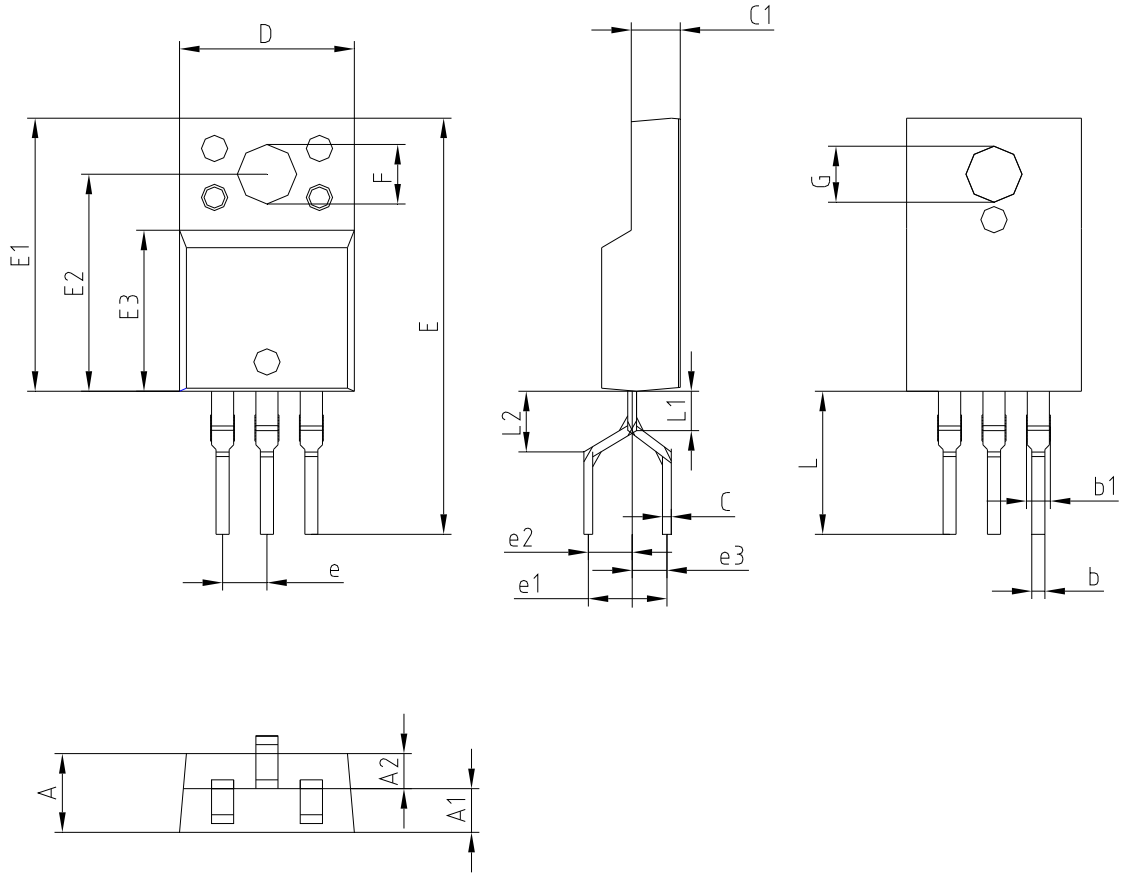








Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	–	–	4.60	
A1	2.45	2.50	2.55	
A2	1.95	2.00	2.05	
b	0.65	0.75	0.85	
b1	1.07	1.27	1.47	
C	0.40	0.50	0.60	
C1	2.70	2.80	2.90	
D	9.90	10.00	10.10	
E	22.77	–	24.77	
E1	15.50	15.60	15.70	
E2	12.30	12.40	12.50	
E3	9.15	9.20	9.25	
F	3.30	3.40	3.50	
G	3.10	3.20	3.30	
e	2.54 BSC			
e1	4.20	4.50	4.80	
e2	2.51 BSC			
e3	1.99 BSC			
L	7.17	–	9.17	
L1	2.25 BSC			
L2	3.46 BSC			

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