Preliminary

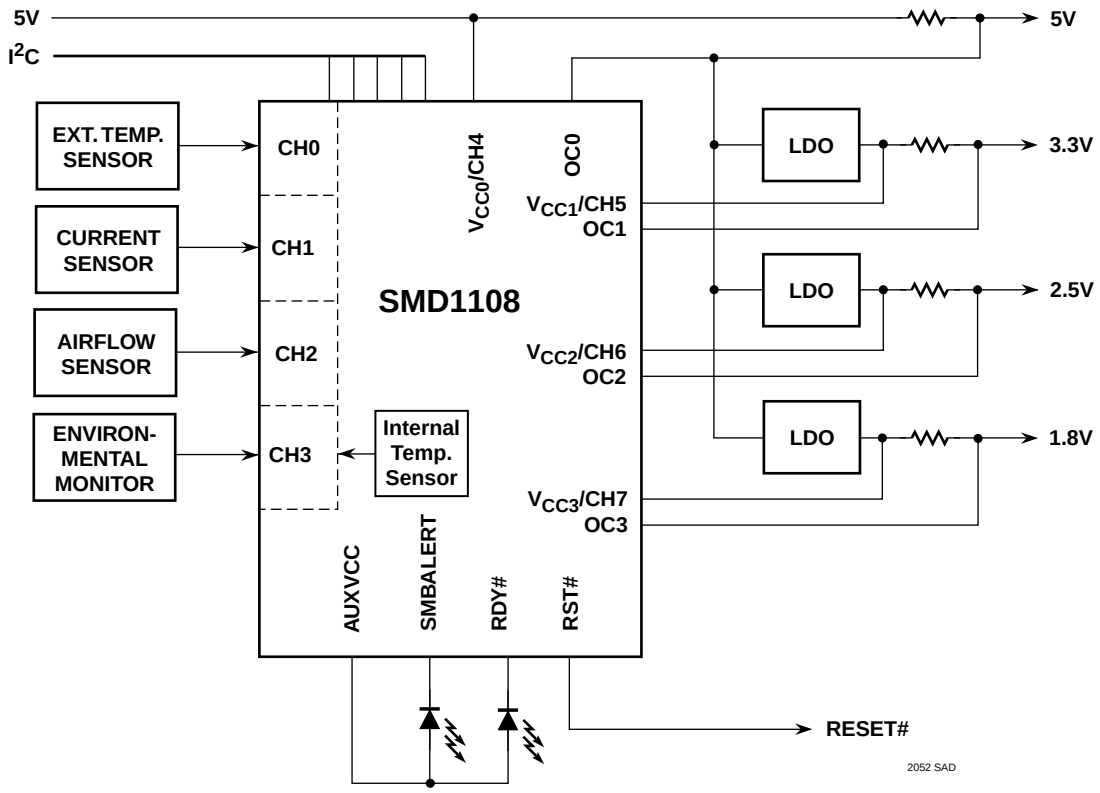
8-Channel Auto-Monitor™ ADC

In System Programmable Analog (ISPA™) Device

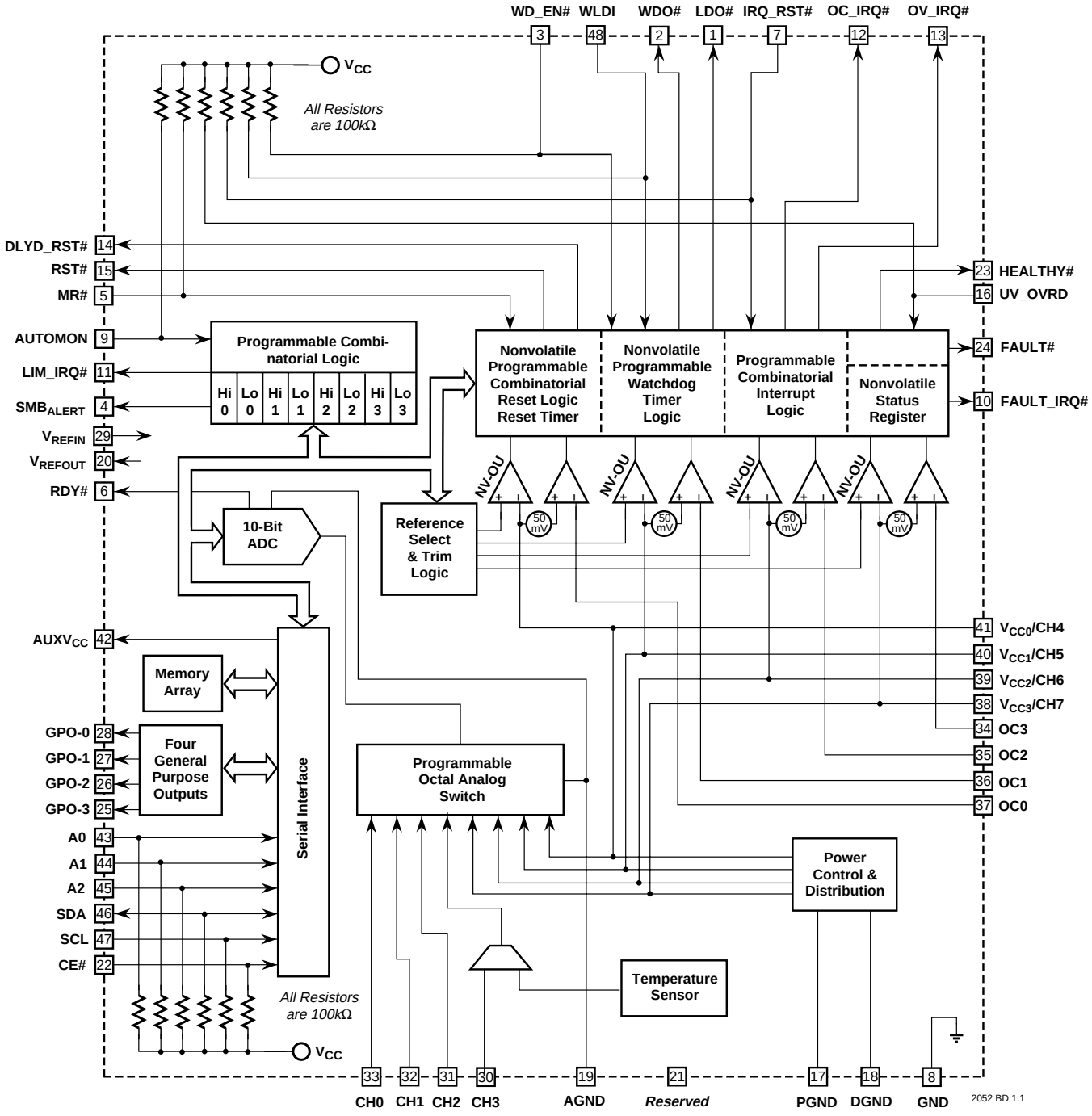
FEATURES

- Programmable 8 Channel 10-Bit A to D converter
  - Programmable Sequencing of Analog Switches in Auto-Monitor Mode
  - Resolution of 10 bits
  - Differential Non-Linearity of ±1LSB
  - Top 4 Channels Programmable, Nonvolatile Upper/Lower IRQ Limits
  - Bottom 4 Channels Tied to Matching Programmable, Nonvolatile Comparators
  - 4 Companion Over-current Comparators
- Internal Temperature Sensor
- Programmable LED Driver Outputs
- Programmable, Nonvolatile Combinatorial Reset logic
- Nonvolatile Status Capture Register
- Two Programmable, Nonvolatile Watchdog Timers
- 1K-Bit Nonvolatile Memory
- Industry Standard 2-Wire Interface
  - Nonvolatile Configuration Registers
  - ADC Conversion Results
  - Memory Array
  - Mechanism for System Level Presence Detect

SIMPLIFIED APPLICATION DRAWING



FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Temperature	–40ºC to 85ºC.
Voltage	2.7V to 5.5V

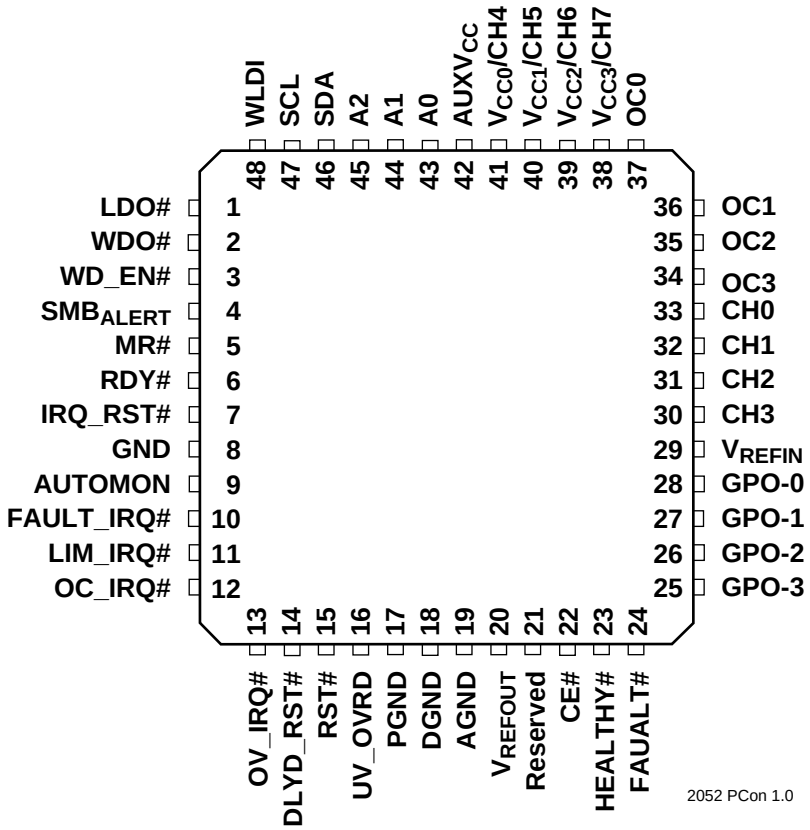
INTRODUCTION

The SMD1108 is a versatile, programmable 8-channel, 10-bit Data Acquisition System that is designed to operate autonomously, relieving the system host and logic board of the environmental monitoring tasks.

Programming of configuration, control and calibration values by the user can be simplified with the interface adapter and Windows GUI software obtainable from Summit Microelectronics.

PIN CONFIGURATION

48-Pin TQFP



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... –55°C to 125°C

Storage Temperature ..... –65°C to 150°C

Lead Solder Temperature (10s) ..... 300 °C

Output Short Circuit Current ..... ① 100mA

Terminal Voltage with Respect to GND (AGND, DGND & PGND tied):

Digital Inputs: IRQ_RST#, WD_EN#, MR#, WLDI, SCL, CE#, A0, A1, A2, and AUTOMON .... –2V to 7V

Digital Outputs: ..... LDO#, WDO#, SMB_{ALERT}#, HEALTHY#, FAULT_IRQ#, LIM_IRQ#, OC_IRQ#, RST#, OV_IRQ#, DLYD_RST#, FAULT#, RDY#, GPO-0, GPO-1, GPO-2, and GPO-3 ..... –2V to 7V

Analog Inputs: V_{CC0}/CH4, V_{CC1}/CH5, V_{CC2}/CH6, V_{CC3}/CH7, CH0, CH1, CH2, CH3, OC1, OC2, OC3, $AUXV_{CC}$, and V_{REF}IN ..... –2V to 7V

① Output shorted for no more than one second, no more than one output shorted at a time.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Conditions (Note 1)	Min.	Typ.	Max.	Units
I_{CC}	Supply Current	All outputs open	1		3	mA
I_{SB}	Standby Current	All outputs open, ADC idle, no memory in process		0.1	1	mA
I_{LI}	Input leakage current	V_{IN} = 0V to V_{CC}			2	µA
I_{LO}	Output leakage current	V_{OUT} = 0V to V_{CC}			10	µA
V_{OL1}	Output low voltage	I_{OL} = 5mA			0.4	V
		I_{OL} = 1mA			0.4	
V_{OL2}	Output low voltage	V_{CC} = 5V, I_{OL} = 2.1mA			0.4	V
		V_{CC} < 4.5V, I_{OL} = 1mA			0.2	
V_{OH}	Output high voltage	V_{CC} = 5V, I_{OL} = –400mA	2.4			V
		V_{CC} < 4.5V, I_{OL} = –100mA	V_{CC} – 0.2			
V_{IL}	Input low voltage		–0.1		$0.3 \times V_{CC}$	V
V_{IH}	Input high voltage		2		V_{CC} + 1	V
Analog Inputs						
V_{REFIN}	V_{REF} input voltage		1		5	V
V_{IN1}	Input voltage on V_{CC}0/CH0 through V_{CC}3/CH3		0		5.5	V
V_{IN2}	Input voltage on channels 4 through 7		0		$2 \times V_{REFIN}$	V
V_{IN3}	Input voltage on OC0 through OC3		0		V_{CC}	V
I_{VRO}	V_{REFOUT} current	V_{REFOUT} = 2.5V			1	mA
		V_{REFOUT} = 2.048V			1	

Note 1: Unless otherwise specified V_{CC} is the highest of the four V_{CCX}/CHX inputs.

2052 Elect Table 1.0

PIN DESCRIPTIONS

V_{CC0}/CH4 – V_{CC3}/CH7 (38, 39, 40, 41)

These 4 inputs are used as the voltage monitor inputs and the voltage supply for the SMD1108. Internally they are diode ORed and the input with the highest voltage potential will be the default supply voltage. For proper device operation at least one of the inputs must be at 2.7V or higher. V_{CC0}/CH4 to V_{CC3}/CH7 are also inputs to four programmable comparators. The under-voltage and over-voltage threshold voltage of each comparator is programmable.

V_{REFIN} (29)

A reference voltage for the ADC. The user can select either the VREFIN as the ADC reference or use the default internal reference voltage.

V_{REFOUT} (20)

The internally generated reference voltage. It is programmable and can supply either 2.048V or 2.500V.

AGND, DGND, PGND, GND (19, 18, 17, 8)

These are the analog, digital, package, and common ground inputs, respectively. They should all be tied to the same ground plane.

$AUXV_{CC}$ (42)

$AUXV_{CC}$ should be isolated from the system power supplies and tied to ground through capacitor $C_{B/U}$. During normal device operation $C_{B/U}$ will be charged by the system supplies through the SMD1108. If system power is lost the charge on $C_{B/U}$ will be used to store the status of the monitor inputs. A 10µF tantalum capacitor should be used for $C_{B/U}$.

In the system environment AUXVcc could also be connected to the front of the card (along with SDA and SCL and GND) so that power could be applied to the SMD1108 to read the contents of the NV status registers.

A0, A1 and A2 (43, 44, 45)

Address inputs. When addressing the SMD1108 either as a memory or an analog channel (or configuration register) the address inputs distinguish which one of eight possible devices sharing the common bus is being addressed.

CE# (22)

A control mechanism for the 2-wire interface. The true state polarity is programmable. When driven true the interface is active and communications channels are open. When it is driven false all communications via the bus are disabled.

SDA (46)

Serial data input/output pin. It should be tied to V_{CC} through a 10kΩ pull-up resistor.

SCL (47)

Serial clock input pin. It should be tied to V_{CC} through a 10kΩ pull-up resistor.

CH0 to CH3 (33, 32, 31, 30)

The analog channel inputs. These inputs are monitored solely through the use of the ADC.

OC0 to OC3 (37, 36, 35, 34)

Over-current sense inputs. They are paired with VCC0/CH4 to VCC3/CH7, respectively, and have a fixed 50mV offset with respect to their corresponding channel input.

MR# (5)

An active low manual reset input. When MR# is driven low the reset output will immediately be driven low. MR# is not maskable and will always generate a reset sequence. The duration of the RST# pulse will be equal to the length of the MR# input pulse plus the programmed reset time-out period value.

WD_EN# (3)

The enable input for both the Watchdog and the Longdog. It must be driven low to enable the operation of their timers. This can provide a convenient mechanism during “debug of code” or during a “power-on configuration” sequence.

WLDI (48)

The Watchdog timer interrupt input. A low to high transition on WDI will reset the Watchdog and Longdog timers. If the timer is not reset within the programmed period of time the SMD1108 will activate the WDO# output first and then the LDO# output.

RST# (15)

An active low open drain output. It will be driven low by the combination of VCC0/CH4 to VCC3/CH7 being at levels below their programmed settings and/or MR# being driven low. RST# will stay low for the duration of the fault condition or the MR# low input and remain low for the duration of t_{PURST} after the removal of the fault condition or MR# returning high.

DLYD_RESET# (14)

An active low open drain output. During normal system operation it will be driven low by the combination of VCC0/CH4 to VCC3/CH7 being at levels below their programmed settings. During the power-on sequence it will be delayed to allow the system to power-up in a controlled sequenced order. See Table 19 for the delay values.

SMB_{ALERT}# (4)

An active low open drain output. It will be driven low whenever one or more of the four auto-monitor inputs exceeds its limits. Once the SMB_{ALERT}# output is driven low the SMD1108 will respond to the industry standard SMB protocol and identify itself as the generator of the alert.

LIM_IRQ# (11)

An active low open drain output that is programmable to be driven low whenever any one of the selected auto-monitor inputs exceeds the programmed high or low value.

FAULT# (24)

An open drain output that can be programmed to drive the output low whenever a selected source is out of limits (FAULT#). Conversely it can be programmed to drive the output low (FAULT) whenever the selected sources are within limits.

HEALTHY# (23)

An open drain output that can be programmed to drive the output low whenever a selected source is out of limits (HEALTHY). Conversely it can be programmed to drive the output low whenever the selected sources are within limits (HEALTHY#).

WDO# (2)

Watchdog Timer Output is an active low open drain output that can be wire-ORed with any number of open drain outputs. Whenever the programmed time-out period of the Watchdog timer is exceeded this output will be driven low.

LDO# (1)

Longdog Timer Output is an active low open drain output that can be wire-ORed with any number of open drain outputs. Whenever the programmed time-out period of the Longdog timer is exceeded this output will be driven low.

RDY# (6)

An active low status output indicating the ADC has no conversion ongoing and the SMD1108 can be accessed via the serial interface without risk of disturbing a conversion.

GPO-0 to GPO-3 (28, 27, 26, 25)

General purpose outputs that can be accessed via the two-wire serial interface. The register controlling these outputs is located in the GFS register section. The GPx outputs are open drain and will be active when a “1” is written to the corresponding bit position in GFS Register 0x98. The SMD1108 will power-up with the GPx bits cleared; therefore, the outputs will not be actively driven.

AUTOMON (9)

This input must be high to enable the Auto Monitor function.

OV_IRQ# (13)

This is an active low open drain output that is driven low when the selected over-voltage conditions are true.

OC_IRQ# (12)

This is an active low open drain output that is driven low when the selected over-current conditions are true.

IRQ_RST# (7)

The IRQ# outputs are latched. Strobing this signal low will reset the IRQ# outputs. They can also be cleared by accessing Register 99 (see Table 29).

UV_OVRD (16)

Forcing this input high will disable Under-Voltage reset conditions.

FAULT_IRQ# (10)

This is an active low open drain output that is driven low when the selected fault conditions are true.

DEVICE OPERATION

THE ADC AND THE ANALOG SWITCH

10-bit ADC

The 10-bit ADC is a self-clocking SAR implementation. In the manual mode of conversion the sample and hold operation will begin after the SMD1108 has received the request for conversion and the channel address. See Table 1.

8 Analog Channels

The eight analog channels can be separated into two function blocks: the bottom four channels (V_{CC0}/CH4 to V_{CC3}/CH7) are primarily supply voltage monitors; the top four channels (CH0 to CH3) are primarily environmental monitors. All eight channels can be switched to the 10-bit ADC and have their inputs converted on-command. CH0 to CH3 may be placed in the Auto-Monitor mode.

V_{CC0}/CH4 to V_{CC3}/CH7 provide four inputs to the analog switch that controls the analog inputs to the ADC converter. Although these channels cannot be placed in the Auto-Monitor mode, the host can request a direct conversion.

Because these channels are designed to operate as supply voltage monitors they are each tied into a programmable comparator. The comparator threshold voltage is programmable and the polarity of the threshold is programmable. This allows very precise monitoring of under- or over-voltage conditions. Paired with each of these channels is an over-current input (OC0 to OC3) that is offset from its partner comparator by 50mV.

Signal to Noise ratio @ 25ºC.		70dB mon.
THD		–80dB min.
Peak harmonic intermodulation distortion	2nd order	–80dB min.
	3rd order	–80dB min.
Conversion time @ 25ºC.		80µs nom.
DC Accuracy		
Resolution		10 bits
Minimum resolution for which no missing codes are guaranteed		10 bits
Relative accuracy		±½LSB
DNL		±1LSB
Positive full scale error		±2LSB
Unpolar offset error	V_{CC} = 5V	±2LSB
	V_{CC} = 2.7V to 3.6V	
	V_{CC} = 1.8V to 2.7V	

2052 Table01

Table 1. Typical ADC Performance

TIMER FUNCTIONS

WATCHDOG and LONGDOG

The SMD1108 has two programmable Watchdog timers each with its own output (WDO# and LDO#) and a common reset input (WLDI). Both are independently programmable and both can be placed in an idle mode. See Register 8C.

RST#

This reset output is intended to be used to drive the backend logic. It is an active low open drain output that is driven low whenever V_{CC0}, V_{CC1}, V_{CC2} or V_{CC3} is below its programmed threshold and/or MR# is being driven low. It will stay low for the duration of the fault condition or the MR# low input and remain low for the duration of t_{PURST} (the programmed reset pulse width) after removal of the fault condition or MR# returning high. It will also be driven low whenever an over-current condition is detected. See Register 8C.

DLYD_RST#

This output is activated by the same set of conditions as RST#. However, during a power-up operation it will not be immediately asserted. As soon as power to one of the V_{CC0}/CH4 to V_{CC3}/CH7 inputs is detected a time-out sequence will be started. The time-out period is programmable and should be equal to or greater than the worst case power-on skew between all the supplies being monitored. If all of the supplies have not reached their threshold before the time-out period, DLYD_RST# will be asserted. DLYD_RST# can then be used to disable a voltage sequencer such as the SMH4803A or SMH4804. See Register 8D.

OUTPUTS

FAULT and HEALTHY

Two programmable outputs (active high or active low) that will respond to programmed source activators. See Registers 8F and 90 through 95.

IRQs

The interrupt outputs are active low open drain outputs that are driven low whenever one of the corresponding monitor inputs senses an excursion beyond its programmed value. See Registers 88, 89, and 98 through 9F.

SERIAL INTERFACE

The SMD1108 has an industry standard 2-wire serial interface. It supports four (4) device-type addresses: 1010 for reading and writing the memory array; 1001 for reading and writing the nonvolatile limit registers and initiating ADC conversions; 1011 for access to the configuration registers, and 0001 that is used for responses to the SMB_{ALERT} protocol

In order to facilitate host system presence detection techniques the SMD1108 provides A0, A1 and A2 address inputs.

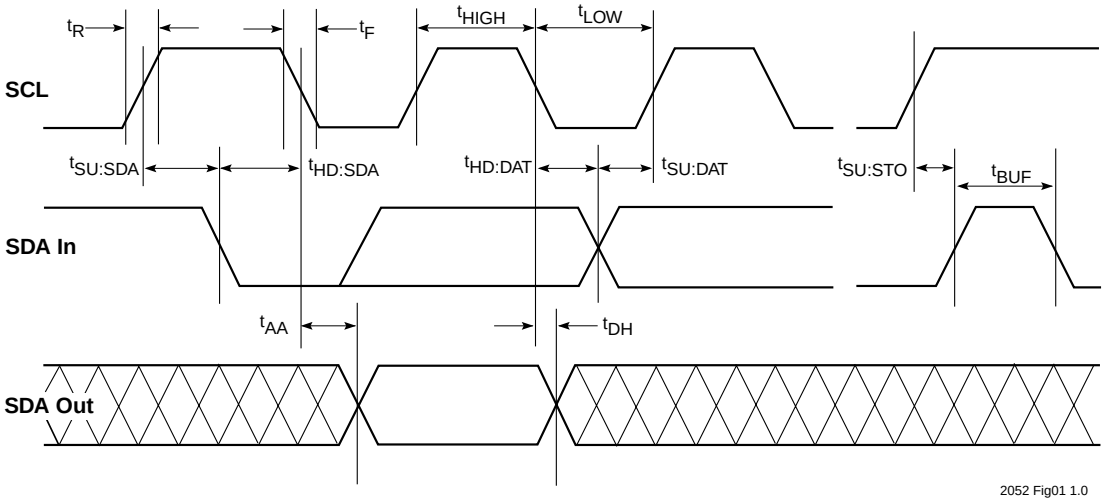


Figure 1. Memory Timing

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time (1)	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time (1)	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time (1)			1000	ns
t_F	SCL and SDA fall time (1)			300	ns
$t_{SU:DAT}$	Data In setup time (1)		250		ns
$t_{HD:DAT}$	Data In hold time (1)		0		ns
TI	Noise filter SCL and SDA (1)	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

2052 Table02 1.0

Note (1) These values are guaranteed by design.

Table 2. Memory Timing

MEMORY AND REGISTER OPERATION

The SMD1108 incorporates a memory that is configured as a 128 x 8 array. Concatenated with the memory array are the sixteen registers that hold the upper and lower limits for ADC comparison tables. Additional registers provide space for configuration usage. Another space is provided for individual channel conversion initiations and reading the conversion data.

All Read and Write operations to memory are handled via an industry standard two-wire interface. The bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus

Input Data Protocol

The protocol defines any device that sends data onto the bus as a transmitter and any device that receives data as a receiver. The device controlling data transmission is called the Master and the controlled device is called the Slave. In all cases the SMD1108 will be a Slave device since it never initiates any data transfers.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because changes on the data line while SCL is high will be interpreted as a Start or a Stop condition.

START and STOP Conditions

When both the data and clock lines are high the bus is said to be not busy. A high-to-low transition on the data line, while the clock is high, is defined as the Start condition. A low-to-high transition on the data line, while the clock is high, is defined as the Stop condition.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the Master or the Slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to Acknowledge that it received the eight bits of data.

The SMD1108 will respond with an Acknowledge after recognition of a Start condition and its Slave address byte. If both the device and a Write operation are selected, the SMD1108 will respond with an Acknowledge after the receipt of each subsequent 8-Bit word. In the Read mode the SMD1108 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no STOP condition is generated by the master, the SMD1108 will continue to transmit data. If the Master leaves the SDA line high (NACK) the SMD1108 will terminate further data transmissions and await a Stop condition before returning to the standby power mode.

Device Addressing

Following a start condition the Master must output the address of the Slave it is accessing. The most significant four bits of the Slave address are the device type identifier (DTI). For the SMD1108 the default memory DTI is 1010_{BIN}. The next three bits in the serial data stream are the device's bus address. The bus address is assigned by biasing the A0, A1 and A2 pins into any one of eight unique addresses. The last bit of the data stream defines the operation to be performed: when set to 1 a Read operation is selected; when set to 0 a Write operation is selected.

MEMORY WRITE OPERATIONS

The SMD1108 allows two types of Write operations: byte Write and page Write. A byte Write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR}.

Byte Write

After the Slave address is sent (to identify the Slave device, and a Read or Write operation), a second byte is transmitted which contains the 8-Bit address of any one of the 128 words in the array. Upon receipt of the word address the SMD1108 responds with an Acknowledge. After receiving the next byte of data it again responds with an Acknowledge. The Master then terminates the transfer by generating a Stop condition, at which time the SMD1108 begins an internal write cycle. While the internal write cycle is in progress the SMD1108 inputs are disabled, and the device will not respond to any requests from the master.

Page Write

The SMD1108 is capable of a 16-byte page Write operation. It is initiated in the same manner as the byte Write operation, but instead of terminating the Write cycle after the first data word, the Master can transmit up to 15 more bytes of data. After the receipt of each byte the SMD1108 will respond with an Acknowledge.

The SMD1108 automatically increments the address for subsequent data words. After the receipt of each word the low order address bits are internally incremented by one. The high order bits of the address byte remain constant. Should the Master transmit more than 16 bytes, prior to generating the Stop condition, the address counter will rollover, and the previously written data will be overwritten. As with the byte Write operation all inputs are disabled during the internal write cycle. Refer to Figure 2 for the address, Acknowledge, and data transfer sequence.

Acknowledge Polling

When the SMD1108 is performing an internal Write operation it will ignore any new Start conditions. Since the device will only return an acknowledge after it accepts the Start, the part can be continuously queried until an acknowledge is issued, indicating that the internal Write cycle is complete. See the flow diagram (Figure 3) for the proper sequence of operations for polling.

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to 1. There are two different Read options: (1) Current Address Byte Read; or (2) Random Address Byte Read

Current Address Read

The SMD1108 contains an internal address counter which maintains the address of the last word accessed, incre-

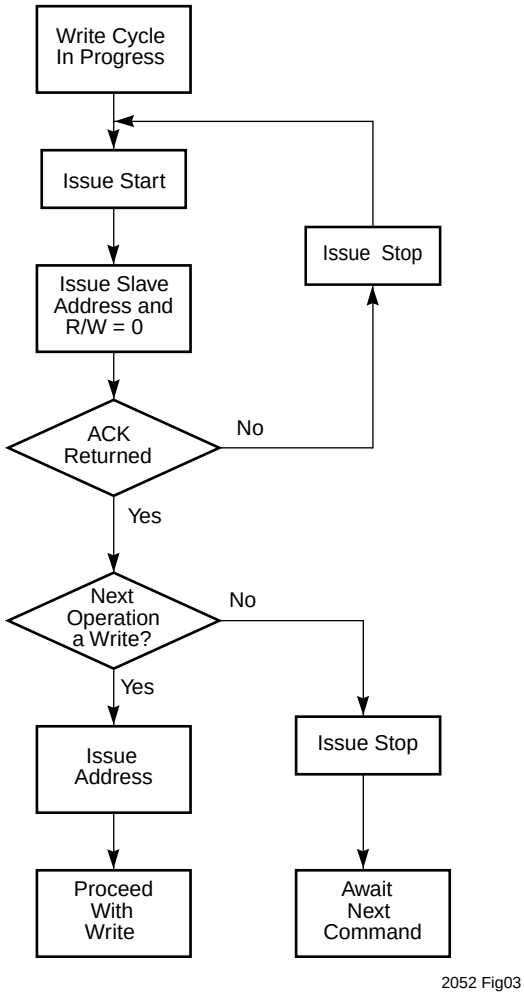


Figure 3. Polling Sequence

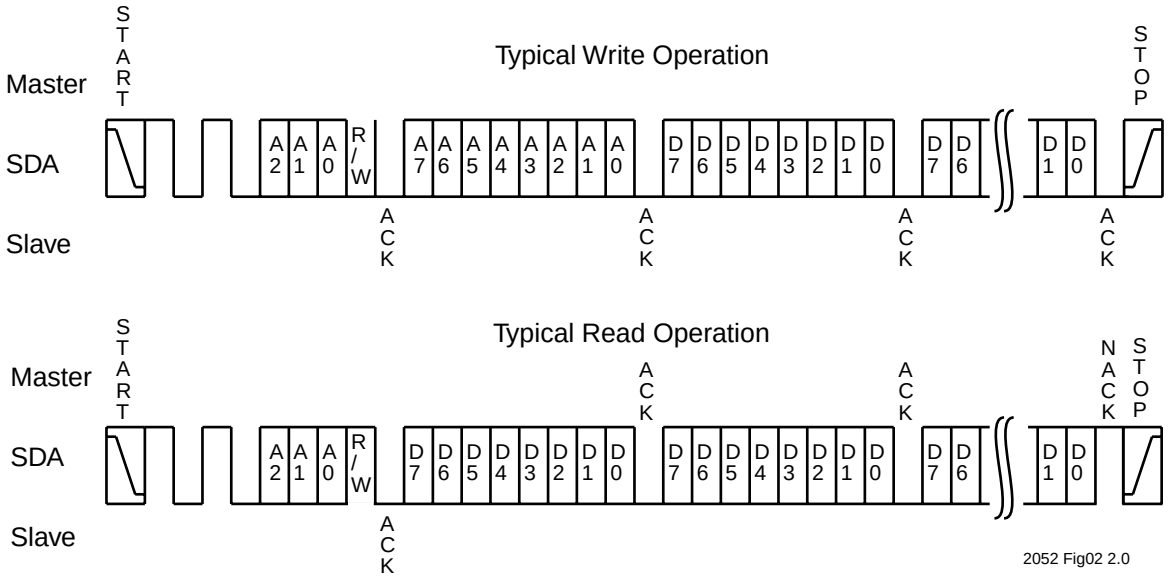


Figure 2. Address, Acknowledge and Data Transfer Sequence

mented by one. If the last address accessed (either a Read or Write) was to address location n, the next Read operation would access data from address location n+1 and increment the current address pointer. When the SMD1108 receives the Slave address field with the R/W bit set to 1 it issues an acknowledge and transmits the 8-Bit word stored at address location n+1. The current address byte Read operation only accesses a single byte of data. The Master issues a NACK and generates a Stop condition. At this point, the SMD1108 discontinues data transmission.

Random Address Read

Random address Read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a Write command which includes the Start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMD1108 to the desired address. After the word address Acknowledge is received by the master, the master immediately reissues a Start condition followed by another Slave address field with the R/W bit set to Read. The SMD1108 will respond with an Acknowledge and then transmit the 8 data bits stored at the addressed location. At this point, the Master issues a NACK and generates a Stop condition. The SMD1108 discontinues data transmission and reverts to its standby power mode.

Sequential READ

Sequential Reads can be initiated as either a current address Read or random access Read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMD1108. The SMD1108 continues to output data for each Acknowledge received. The Master terminates the sequential Read operation with NACK and issues a Stop. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal. For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter will rollover and the memory will continue to output data.

SMB_{ALERT}

The function of the SMB_{ALERT} output is similar to a standard interrupt. Whenever one of the selected channels exceeds its limits the SMB_{ALERT} pin will be driven low. This action begins an exchange of information across the 2-wire interface that establishes the source of the interrupt.

As shown in Figure 4 the SMB_{ALERT} signal is driven low and the host responds with the Alert Response Address [0001 1001]. The SMD1108 will issue an Acknowledge and then output its address, starting with the device type identifier for the PSF registers [1001]. Following this the SMD1108 outputs its bus address reflecting the biasing of the A0, A1 and A2 pins. If the response to any bus address option is selected and the pins are not biased the read back will be [111]. The last bit is undefined.

At this point the Host should not issue an ACK, but immediately generate a Stop condition. The SMD1108 will continue driving the SMB_{ALERT} output low until the Host responds back by generating a Start condition followed by the SMD1108 address. The SMD1108 will generate an ACK and release the SMB_{ALERT} pin.

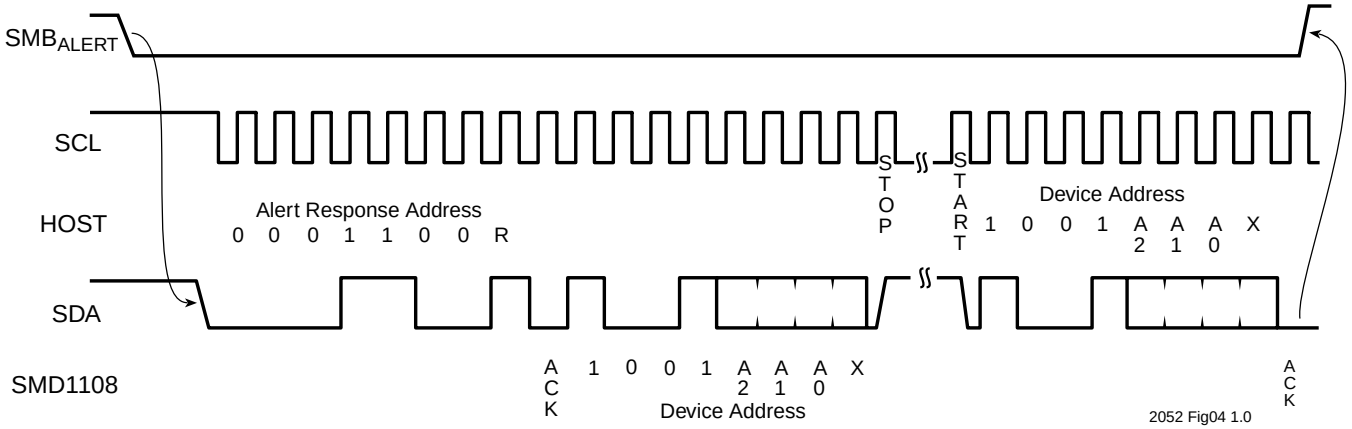


Figure 4. SMB_{ALERT} Sequence

REGISTERS

REGISTER READ/WRITE

The registers are read and written using the same 2-wire bus as the memory. The Configuration Registers and the GFS Registers are written as shown in Figure 5. Reads of the registers must be executed like a random Read operation. That is, a dummy write must be issued in order to set the address pointer for the following Read.

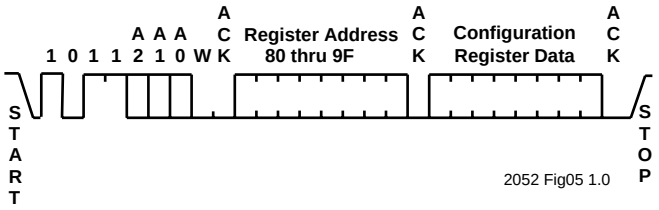


Figure 5. Writing to the Configuration Registers

The Limits Registers for channels 0 through 3 are located at the top of the ADC address space and utilize the 1001 DTI. Unlike the configuration registers that are limited to single byte Writes or Reads, the ADC limit registers can be written in page mode. The example In Figure 6 shows two byte Writes to configure the CH0 Lower Limit.

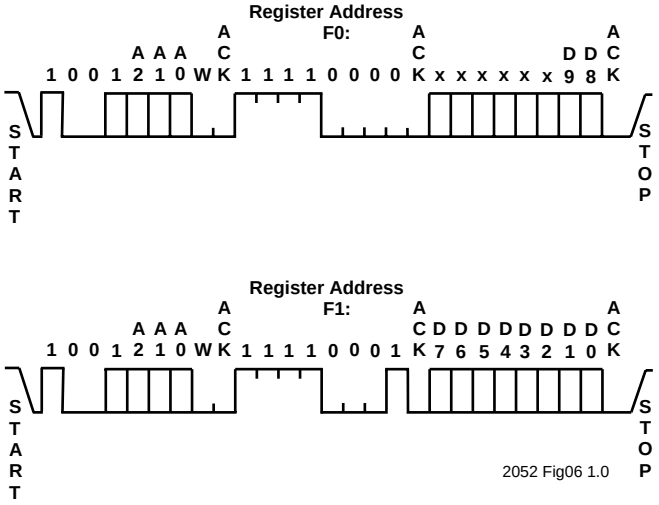


Figure 6. Writing to the Limits Registers

Even though the ADC cannot be written, performing commanded conversions (non-auto-monitor mode) requires a dummy Write operation to select the proper channel and indicate the type of conversion process that is being requested. The sequence would be: address the device using 1001 as the DTI followed by the bus address and a write bit. The next byte contains the conversion process requested and the channel or channel group to be converted.

Single Channel Conversion

The single channel Read allows the host to perform manual conversions on a single channel. The state of bits CH2, CH1 and CH0 selects one-of-eight channels. Reading DTI 1001 will return the converted data. If the host continues clocking SCL without an interim Stop command the SMD1108 will continue conversions on the selected channel and output the data as clocked. See the timing sequence diagrams in Figure 7.

Multi-Channel Conversion: 4

Command 001 will configure the channel conversion such that the MUX will switch channels 0 through 3 sequentially.

Multi-Channel Conversion: 8

Command 011 will configure the channel conversion such that the MUX will switch channels 0 through 7 sequentially.

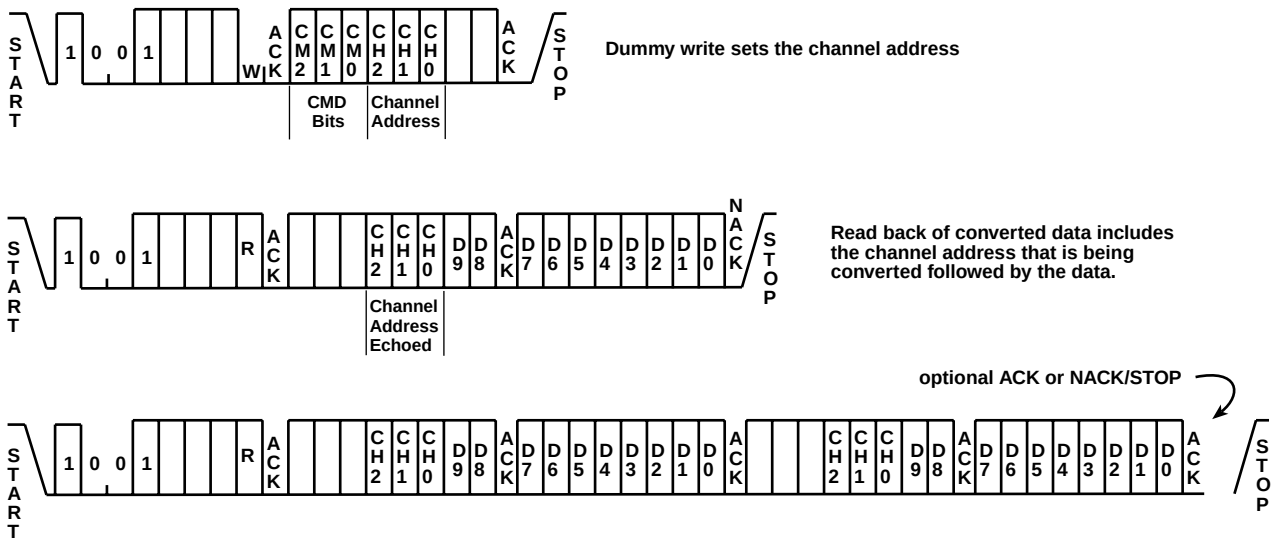
Differential Conversion

In order to provide a very accurate current sense the SMD1108 can perform a differential conversion on a selected CHx/OCx input combination. This is limited to channels 4 through 7 and their corresponding OC inputs. The measurement provides the differential voltage between the input channels (V_{CC0}/CH4 to V_{CC3}/CH7) and the over-current sense inputs (OC0 to OC3). The result is that differential noise is rejected and an accurate voltage drop across the sense resistor is measured.

7	6	5	4	3	2	1	0	Bit
CMD			**CH2**	**CH1**	**CH0**			Function
0	0	0	CH2	CH1	CH0			Single channel read mode
0	0	1	x			x	x	Continuous read mode 1
0	1	1	x					Continuous read mode 2
1	0	0	1	CH1	CH0			Differential conversion

2052 Table03 1.0

Table 3. Command/Address Byte



2052 Fig07 1.0

Figure 7. Continuous Read

M-ADD	MSB							LSB	Function
F0	x	x	x	x	x	AR01	D9	D8	Channel #0 low limit
F1	D7	D6	D5	D4	D3	D2	D1	D0	Channel #0 low limit
F2	x	x	x	x	x	AR02	D9	D8	Channel #0 high limit
F3	D7	D6	D5	D4	D3	D2	D1	D0	Channel #0 high limit
F4	x	x	x	x	x	AR11	D9	D8	Channel #1 low limit
F5	D7	D6	D5	D4	D3	D2	D1	D0	Channel #1 low limit
F6	x	x	x	x	x	AR12	D9	D8	Channel #1 high limit
F7	D7	D6	D5	D4	D3	D2	D1	D0	Channel #1 high limit
F8	x	x	x	x	x	AR21	D9	D8	Channel #2 low limit
F9	D7	D6	D5	D4	D3	D2	D1	D0	Channel #2 low limit
FA	x	x	x	x	x	AR22	D9	D8	Channel #2 high limit
FB	D7	D6	D5	D4	D3	D2	D1	D0	Channel #2 high limit
FC	x	x	x	x	x	AR31	D9	D8	Channel #3 low limit
FD	D7	D6	D5	D4	D3	D2	D1	D0	Channel #3 low limit
FE	x	x	x	x	x	AR32	D9	D8	Channel #3 high limit
FF	D7	D6	D5	D4	D3	D2	D1	D0	Channel #3 high limit

2052 Table04

Note: ARxx is the Alert Region limit. See Environmental Automonitor Blocks description in the Applications Information section.

Table 4. ADC Registers Located at the Top of 1001 Address Space

REGISTER PARTITIONING

The registers have been divided into two main functional blocks. The Configuration registers (from 0x80 through 0x95) are the primary setup registers that define the SMD1108 for its specific application. These registers can be (1) left open for both Read and Write operations, (2) locked for Write but open for Read, or (3) totally blocked for both .

The balance of the registers (the GSF registers) will frequently be used during system operation, so the lock combinations are more flexible. They can be (1) locked for Read and Writes, (2) open for Read and Write but excluding the configuration registers, (3) Read all registers but Write GSF only, or (4) Read and Write all registers.

The organization, bit patterns and functions of the registers are illustrated in Tables 6 through 33.

Registers 80 through 83 set the under-voltage threshold for the selected channel: CH4 through CH7. The register value is determined by subtracting 0.9V from the desired threshold, dividing the result by 0.02 and converting that to a hexadecimal value.

The formula is $(UV_{TH} - 0.9) / 0.02$ = Decimal value (convert to hexadecimal).

For example, if the UV threshold is to be 4.6V:

$$(4.6 - 0.9) / 0.02 = 185_{DEC} = B9_{HEX}$$

Reg. #	Reg. Name	Reg. Type
80	Channel configuration	Configuration Registers
81		
82		
83		
84		
85		
86		
87		
88		
89		
8A	Address configuration	
8B	V_{REF} configuration	
8C	Timers 1	
8D	Timers 2	
8E	Quick trip	
8F	Healthy/Fault configuration	
90	Healthy pin configuration	
91	Healthy pin configuration	
92	Fault pin configuration	
93	Fault pin configuration	
94	Fault mask	
95	Fault mask	
96	Reserved	
97	Reserved	
98	GPO register	GFS Register
99	Software reset	
9A	Status register	
9B	Status register	
9C	Reserved	
9D	Reserved	
9E	Fault latch	GFS Register
9F	Fault latch	

2052 Table05 1.0

Table 5. Register Address Map

7	6	5	4	3	2	1	0	Function
UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0	UV threshold voltage for V_{CC0}/CH4

2052 Table06

Table 6. Register 80 V_{CC0}/CH4 UV Threshold

7	6	5	4	3	2	1	0	Function
UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0	UV threshold voltage for V_{CC1}/CH5

2052 Table07

Table 7. Register 81 V_{CC1}/CH5 UV Threshold

7	6	5	4	3	2	1	0	Function
UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0	UV threshold voltage for V_{CC2}/CH6

2052 Table08

Table 8. Register 82 V_{CC2}/CH6 UV Threshold

7	6	5	4	3	2	1	0	Function
UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0	UV threshold voltage for V_{CC3}/CH7

2052 Table09

Table 9. Register 83 V_{CC3}/CH7 UV Threshold

Registers 84 through 87 set the over-voltage threshold for the selected channel: CH4 through CH7. The OV threshold minimum is equal to 120% of the channel's UV threshold. An offset of as much as 244% of the UV threshold is possible.

The formula is $[OV_{TH} – (UV_{TH} \times 1.2)] / (UV_{TH} \times 0.04)$ = Decimal value (convert to hexadecimal).

The maximum register value would be $31_{DEC} = 1F_{HEX}$.

7	6	5	4	3	2	1	0	Function
x	x	x	OV4	OV3	OV2	OV1	OV0	Over-voltage offset for V_{CC0}/CH4

2052 Table10 1.0

Table 10. Register 84 V_{CC0}/CH4 OV Threshold

7	6	5	4	3	2	1	0	Function
x	x	x	OV4	OV3	OV2	OV1	OV0	Over-voltage offset for V_{CC1}/CH5

2052 Table11 1.0

Table 11. Register 85 V_{CC1}/CH5 OV Threshold

7	6	5	4	3	2	1	0	Function
x	x	x	OV4	OV3	OV2	OV1	OV0	Over-voltage offset for V_{CC2}/CH6

2052 Table12 1.0

Table 12. Register 86 V_{CC2}/CH6 OV Threshold

7	6	5	4	3	2	1	0	Function
x	x	x	OV4	OV3	OV2	OV1	OV0	Over-voltage offset for V_{C32}/CH7

2052 Table13 1.0

Table 13. Register 87 V_{CC3}/CH7 OV Threshold

Registers 88 and 89 provide selective enabling of the channels and the channels' functions. When channels 0 through 3 are enabled any out-of-limit condition will activate the LIM_IRQ# and SMB_{ALERT}# outputs. Channels 4 through 7 are more complex in that they are inputs to three instant action measurements: under-voltage, over-voltage and over-current. Each one of these measurements can be enabled on a channel by channel basis to activate one of the three potential output reactions.

7	6	5	4	3	2	1	0	Function
x	x	x	x	UV3 (CH7)	UV2 (CH6)	UV1 (CH5)	UV0 (CH4)	A "1" enables the channel; an UV condition will cause a RESET.
OV3 (CH7)	OV2 (CH6)	OV1 (CH5)	OV0 (CH4)	x	x	x	x	A "1" enables the channel; an OV condition will cause an OV_IRQ.

2052 Table14 1.0

Table 14. Register 88 Channel Enable — Part 1

7	6	5	4	3	2	1	0	Function
x	x	x	x	LIM3 (CH3)	LIM2 (CH2)	LIM1 (CH1)	LIM0 (CH0)	A "1" enables the channel; an out-of-limit condition will cause a LM_IRQ# and a SMB_{ALERT}.
OC3 (CH7)	OC2 (CH6)	OC1 (CH5)	OC0 (CH4)	x	x	x	x	A "1" enables the channel; an over-current condition will cause an OC_IRQ#.

2052 Table15 1.1

Table 15. Register 89 Channel Enable — Part 2

Register 8A controls access to the SMD1108 with regard to the 2-wire interface and the function blocks that are accessed through the 2-wire bus.

7	6	5	4	3	2	1	0	Bits
Reg. Access		**ACK**	**Device Type**	**Device Address**	**CE**	x	x	**Function**
x	x	x	x	x	**0**	x	x	CE# input active low
					1	x	x	CE# input active high
				0	x	x	x	Responds to address pin biased address only
				1	x	x	x	Responds to any bus address
			0	x	x	x	x	EEPROM responds to 1010
			1	x	x	x	x	EEPROM responds to 1110
		0	x	x	x	x	x	ACK and access to DTI 1010
		1	x	x	x	x	x	No ACK/ no access to DTI 1010
0	**0**	x	x	x	x	x	x	All registers locked: no read, no write
0	**1**	x	x	x	x	x	x	Read and write GFS registers only (98 through 9F). All configuration registers locked.
1	**0**	x	x	x	x	x	x	Read all registers. Wrilte GFS registers.
1	**1**	x	x	x	x	x	x	Read and write all registers

2052 Table16 1.0

Table 16. Register 8A Slave Address Configuration

Register 8B controls the source for the ADC's reference, optional over-current trip values, and channel 3 vs. temp. sense enable.

7	6	5	4	3	2	1	0	Bits
V_{REF} SOURCE		**Reserved**		**T S**	**NVFL**	**OC**	**V_{REF}**	**Function**
x	x	x	x	x	x	x	**0**	**V_{REF}** = 2.048V
							1	**V_{REF}** = 2.500V
						0	x	Over-current trip = 25mV
						1	x	Over-current trip = 50mV
					0	x	x	Disable non-volatile fault latch
					1	x	x	Enable non-volatile fault latch
				0	x	x	x	Disable temp sensor
				1	x	x	x	Enable temp sensor (vs. Channel 3)
			0	x	x	x	x	Reserved function. Set to 0.
		0	x	x	x	x	x	Reserved function. Set to 0.
0	**0**	x	x	x	x	x	x	Use internally generated **V_{REF}**
0	**1**	x	x	x	x	x	x	Reserved
1	**0**	x	x	x	x	x	x	Reserved
1	**1**	x	x	x	x	x	x	Use **V_{REF}** input

2052 Table17

Table 17. Register 8B Configuration

7	6	5	4	3	2	1	0	Bits
PRT1	**PRT0**	**LD2**	**LD1**	**LD0**	**WD2**	**WD1**	**WD0**	**Function**
x	x	x	x	x	**0**	x	x	Watch dog timer disabled
					1	**0**	**0**	400ms Watch dog timer interval
					1	**0**	**1**	800ms Watch dog timer interval
					1	**1**	**0**	1600ms Watch dog timer interval
					1	**1**	**1**	3200ms Watch dog timer interval
		0	x	x	x	x	x	Long dog timer disabled
		1	**0**	**0**	x	x	x	800ms Long dog timer interval
		1	**0**	**1**	x	x	x	1600ms Long dog timer interval
		1	**1**	**0**	x	x	x	3200ms Long dog timer interval
		1	**1**	**1**	x	x	x	6400ms Long dog timer interval
0	**0**	x	x	x	x	x	x	25ms Reset interval
0	**1**	x	x	x	x	x	x	50ms Reset interval
1	**0**	x	x	x	x	x	x	100ms Reset interval
1	**1**	x	x	x	x	x	x	200ms Reset interval

2052 Table18 2.0

Table 18. Register 8C Reset Pulse Width and Timer Delays

Register 8D controls three delays. DRT2, DRT1, and DRT0 control the hold-off time period for generation of any IRQ output and define the hold-off for the DLYD_RST# output. OCD1 and OCD0 define the delay from the first sensing of an over-current condition, and how long that condition exists before taking action. FWD1 and FWD0 control the hold-off period from the first sensing of a fault condition until recording all active conditions.

7	6	5	4	3	2	1	0	Bits
FWD1	**FWD0**	**OCD1**	**OCD0**	x	**DRT2**	**DRT1**	**DRT0**	**Function**
x	x	x	x	x	**0**	x	x	Delayed reset timer disabled
					1	**0**	**0**	200ms Delayed reset timer interval
					1	**0**	**1**	400ms Delayed reset timer interval
					1	**1**	**0**	800ms Delayed reset timer interval
					1	**1**	**1**	1600ms Delayed reset timer interval
		0	**0**		x	x	x	25µs Over-current trip delay
		0	**1**		x	x	x	50µs Over-current trip delay
		1	**0**		x	x	x	100µs Over-current trip delay
		1	**1**		x	x	x	200µs Over-current trip delay
0	**0**	x	x		x	x	x	Fault write sense delay off
0	**1**	x	x		x	x	x	50µs Fault write sense delay
1	**0**	x	x		x	x	x	100µs Fault write sense delay
1	**1**	x	x		x	x	x	200µs Fault write sense delay

2052 Table19 1.0

Table 19. Register 8D Reset Pulse Width and Timer Delays

Register 8E selects the Quick Trip thresholds. The thresholds are interrelated with the value of the internal V_{REF} controlled by the state of bit 1 in Register 8B.

7	6	5	4	3	2	1	0	Bits
QT1 CH4	QT0 CH4	QT1 CH5	QT0 CH5	QT1 CH6	QT0 CH6	QT1 CH7	QT0 CH7	Function: QT threshold
x	x	x	x	x	x	0	0	Off
						0	1	50mV/75mV
						1	0	75mV/100mV
						1	1	125mV/150mV
				0	0	x	x	Off
				0	1	x	x	50mV/75mV
				1	0	x	x	75mV/100mV
				1	1	x	x	125mV/150mV
		0	0	x	x	x	x	Off
		0	1	x	x	x	x	50mV/75mV
		1	0	x	x	x	x	75mV/100mV
		1	1	x	x	x	x	125mV/150mV
0	0	x	x	x	x	x	x	Off
0	1	x	x	x	x	x	x	50mV/75mV
1	0	x	x	x	x	x	x	75mV/100mV
1	1	x	x	x	x	x	x	125mV/150mV

2052 Table20 1.0

Table 20. Register 8E Quick Trip Thresholds

Register 8F controls the function of the HEALTHY# and FAULT# outputs and the conditions that can drive them. All latched HEALTHY# or FAULT# conditions are cleared by IRQ_RST#

7	6	5	4	3	2	1	0	Bits
Healthy# & Fault#	**UV_OVRD#**	**Fault# Reset**	**Fault# Latch**	**Fault# State**	**Healthy# Reset**	**Healthy# Latch**	**Healthy# State**	**Function**
x	x	x	x	x	x	x	**0**	HEALTHY# output active low
							1	HEALTHY# outputactive high
						0	x	Do not latch HEALTHY#
						1	x	Latch HEALTHY#
					0	x	x	HEALTHY# unaffected by reset
					1	x	x	HEALTHY# goes false on reset
				0	x	x	x	FAULT# output active low
				1	x	x	x	FAULT# output active high
			0	x	x	x	x	Do not latch FAULT#
			1	x	x	x	x	Latch FAULT#
		0	x	x	x	x	x	FAULT# unaffected by reset
		1	x	x	x	x	x	FAULT# goes true on reset
	0	x	x	x	x	x	x	UV_OVRD# will override FAULT# conditions
	1	x	x	x	x	x	x	HEALTHY# & FAULT# ignore UV_OVRD#
0	x	x	x	x	x	x	x	Enabled channels affect HEALTHY# & FAULT#
1	x	x	x	x	x	x	x	Disabled channels affect HEALTHY# & FAULT#

2052 Table21

Table 21. Register 8F HEALTHY# and FAULT# Output Control

Registers 90 through 93 control the sources of activation for the HEALTHY# and FAULT# outputs. For the HEALTHY# output to be true all the selected sources must be within their limits. This is effectively an ANDing function. For the FAULT# output to be true only one of the selected sources need be out of limits (ORing). If the same sources for HEALTHY# and FAULT# are selected then only one of the two outputs can be true at one time.

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	HEALTHY# signal unaffected by condition
1	1	1	1	1	1	1	1	HEALTHY# signal goes false on condition

2052 Table22

Table 22. Register 90 HEALTHY# Deactivation Sources

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	HEALTHY# signal unaffected by condition
1	1	1	1	1	1	1	1	HEALTHY# signal goes false on condition

2052 Table23

Table 23. Register 91 HEALTHY# Deactivation Sources

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	FAULT# signal unaffected by condition
1	1	1	1	1	1	1	1	FAULT# signal goes true on condition

2052 Table24

Table 24. Register 92 FAULT# Activation Sources

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	FAULT# signal unaffected by condition
1	1	1	1	1	1	1	1	FAULT# signal goes false on condition

2052 Table25

Table 25. Register 93 FAULT# Activation Sources

Registers 94 & 95 are similar to FAULT# registers 92 and 93. If any one of the selected sources is true the fault condition will be recorded in the nonvolatile fault latches 9E and 9F. This in turn will drive the FLT_IRQ# output low.

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	FAULT# latch unaffected by condition
1	1	1	1	1	1	1	1	FAULT# latch records out of limit condition

2052 Table26

Table 26. Register 94 FAULT# Latch Mask

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	FAULT# latch unaffected by condition
1	1	1	1	1	1	1	1	FAULT# latch records out of limit condition

2052 Table27

Table 27. Register 95 FAULT# Latch Mask

THE GFS REGISTERS

The balance of the registers can be thought of as the operation registers. That is, the previous registers define the part's function and their contents will most likely be written once and never altered. The following GPO, fault, and status registers will be actively read and written during system operation.

7	6	5	4	3	2	1	0	Bit
				GPO3	GPO2	GPO1	GPO0	Function
x	x	x	x	0	0	0	0	Power on state — non-active
				1	1	1	1	Corresponding output to ground

2052 Table28 1.0

Table 28. GFS Register 98 GPO Output Control

Register 99 provides a software method for activating a RESET output or clearing an IRQ (this effectively mimics the IRQ_RST# input).

7	6	5	4	3	2	1	0	Bit
Reserved						Soft Reset	Clear IRQ	Function
0	0	0	0	0	0	x	1	Clears any IRQ except FLT_IRQ#
						1	x	Starts reset cycle, then self clears

2052 Table29 1.0

Table 29. GFS Register 99 GPO Output Control

Registers 9A and 9B are the status registers. These registers are read-only and are volatile. The Status Register is cleared by forcing the IRQ_RST# input low.

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	Condition not the cause of an IRQ
1	1	1	1	1	1	1	1	Condition the cause of an IRQ

2052 Table30 1.0

Table 30. GFS Register 9A Status Register (Read Only)

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	Condition not the cause of an IRQ
1	1	1	1	1	1	1	1	Condition the cause of an IRQ

2052 Table31 1.0

Table 31. GFS Register 9B Status Register (Read Only)

Registers 9E and 9F are the Fault registers. These registers are nonvolatile and can only be cleared by writing to the affected bit. This register is cleared by writing a 0 to the affected bit location.

7	6	5	4	3	2	1	0	Bit
OV3 CH7	OV2 CH6	OV1 CH5	OV0 CH4	UV3 CH7	UV2 CH6	UV1 CH5	UV0 CH4	Function
0	0	0	0	0	0	0	0	Condition not the cause of an IRQ
1	1	1	1	1	1	1	1	Condition the cause of an IRQ

2052 Table32 1.0

Table 32. GFS Register 9E NV Fault Latch

7	6	5	4	3	2	1	0	Bit
OC3 CH7	OC2 CH6	OC1 CH5	OC0 CH4	LIM3 CH3	LIM2 CH2	LIM1 CH1	LIM0 CH0	Function
0	0	0	0	0	0	0	0	Condition not the cause of an IRQ
1	1	1	1	1	1	1	1	Condition the cause of an IRQ

2052 Table33 1.0

Table 33. GFS Register 9F NV Fault Latch

APPLICATIONS INFORMATION

Overview

The SMD1108 Auto-Monitor ADC is designed to monitor the environmental parameters on a telecommunications line card or subsystem. Figure 9 shows the SMD1108 monitoring four dedicated supply lines — in this example: 5V, 3.3V 2.5V, and 1.8V — coming in Connector J16. For each of these 4 channels there is an associated under-voltage, over-voltage and over-current detection circuit. These voltage and current inputs are connected internally to an 'Instant Action block' (Figure 8), and, in the event of a failure, can be programmed to log the fault in an internal nonvolatile memory. The ability to log faults directly into a nonvolatile status register allows systems designers the ability to record data relating to system performance, so that data about the environment is logged immediately in the event of a failure on the subsystem. This provides the ability to fault record — which can be critical when trying to diagnose system faults — during reliability tests or field failures. The SMD1108 also allows data to be downloaded while still mounted on the line card. The SMD1108 provides out-of-limit monitoring via four environmental automonitor inputs (CH0 to CH3). Absolute measurement of the parameters via an ADC allows engineers to monitor the long term performance of the subsystem to predict system failure allowing scheduled maintenance to repair the problem before the failure occurs. For example, a current increasing over a period of months on an optical interface where a laser is aging, or the DC output of a DC-DC Converter. There are four general-purpose open collector outputs which can be used to drive low current signals such as status LEDs. They are all controlled via the serial data bus. Summit's Windows-based Graphical User Interface (GUI) Programming Software will allow the engineer to program the SMD1108 via a host PC running Windows 9*x*, 2000 or NT. The GUI is also available on the website at www.summitmicro.com.

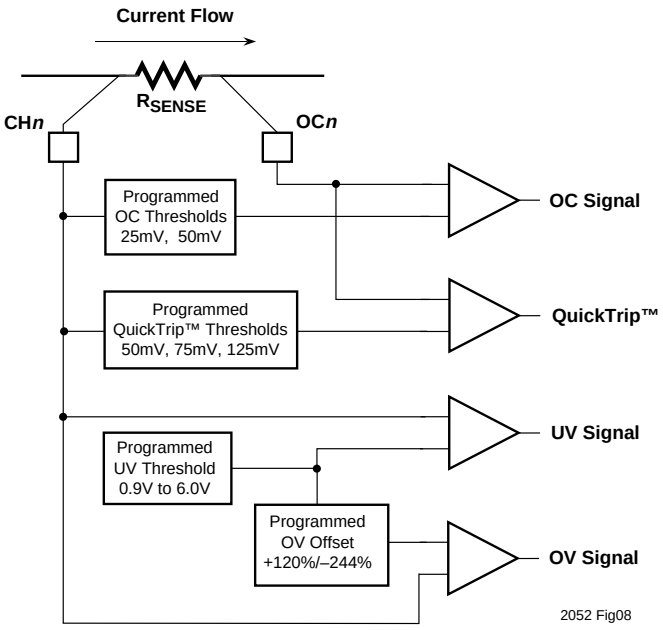


Figure 8. Instant Action Block

Power Supplies

The SMD1108 is designed to take power via the inputs V_{CC}0/Ch4 through V_{CC}3/Ch7. These 4 inputs are internally diode-ORed. Consequently the highest supply voltage actually supplies the current to the device. At least one of these supplies must be above 2.7V for correct device operation. Summit recommends 100nF decoupling capacitors across all voltage supply inputs. For more information on these inputs see Figure 8, the Instant Action Block. The AUXV_{CC} signal is provided to create a backup supply. This pin should have a 10µF capacitor to ground, and should be isolated from the main supply. AUXV_{CC} is also used to power the part to access the nonvolatile memory without having power applied to the rest of the board. See recommended connections in the Serial Interface section.

8 Channel 10 bit ADC

The SMD1108 can monitor system parameters and measure each value to an absolute level. The analog acquisition system consists of an 8-to-1 MUX, a 10-bit ADC, voltage references, and the automonitor logic. The ADC's inputs are grouped into two banks of four. The CH0 to CH3 inputs are the primary environmental automonitor channels, and the V_{CC}0/Ch4 to V_{CC}3/Ch7 inputs are the supply monitors (see Figure 8). The interface to the ADC is made via the two-wire serial data port. When the SMD1108 is in automonitor mode (signal AUTOMON high) the serial interface is disabled to prevent any noise from the serial bus disturbing the ADC conversion. During the development process the engineer can read the values of the ADC channels directly using the Windows GUI. The RDY# signal indicates when the ADC is busy in conversion. There are three sources for the reference voltage on the ADC. Two voltages are generated internally: 2.5V and 2.048V. These are doubled internally and generate full scale values of 5V and 4.096V (or 4mV/bit), respectively. In addition, it is possible to source the reference voltage externally. These three options are programmable through the GUI software.

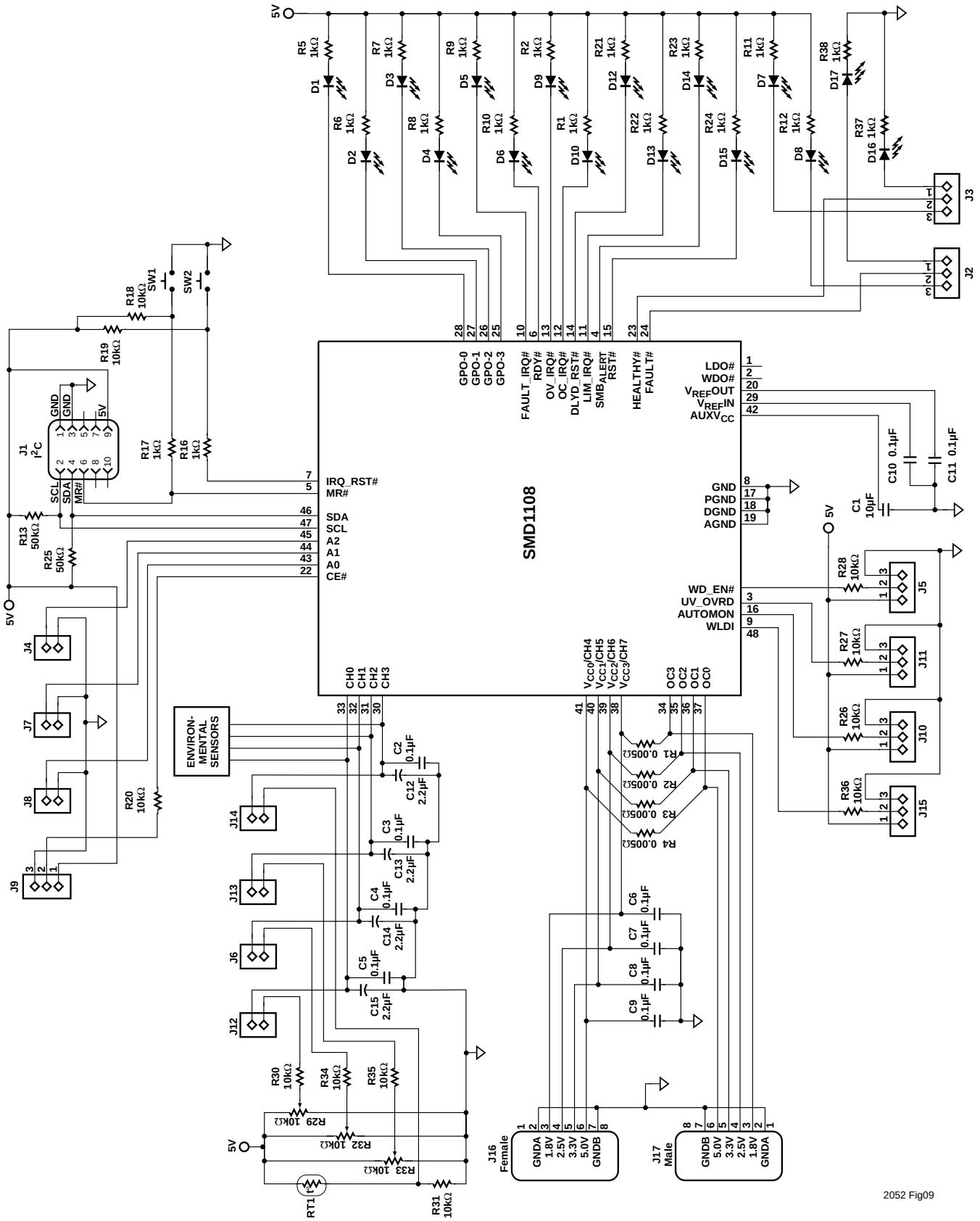


Figure 9. Typical Application Schematic

Temperature Sensor

The internal temperature sensor can be accessed as a multiplexed optional input on CH3. Channel 3 can be set to read an internal temperature dependant device with a range of ±128ºC. The 10-bit ADC converts the temperature reading to data in 2's complement format, and is accurate to ¼ºC. The GUI software can enable the Temperature Sensor and will change the displayed reading on CH3 from volts to ºC.

Instant Action Block

A single channel of the Instant Action Block is shown in Figure 8. The SMD1108 has a block of 12 nonvolatile threshold comparators dedicated to monitoring the status of the supply lines, they are arranged as:

Four Over-Voltage comparators,

Four Under-Voltage comparators, and

Four Over-Current comparators.

This structure has been adopted to ensure all supplies are continuously monitored, because if a supply interruption occurred while the ADC was sampling another channel the interruption could be missed.

Each channel can set the UV threshold anywhere in the range from 0.9V to 6V in 20mV steps. OV thresholds are offset from the UV threshold, and the value to be entered into the register can be calculated from:

$$\frac{OV_{TH} - (UV_{TH} \times 1.2)}{UV_{TH} \times 0.04}.$$

When the UV threshold is enabled it is internally ORed to the RST# signal. Please note if UV Override (UV_OVRD) is active then these thresholds are ignored. UV Override is provided to allow voltage margining during production 'burning in' of the line cards; this prevents Alarm signals from being generated during this test. The over-current comparator is offset from the input voltage by a programmable threshold, which can be set to 50, 75 or 150mV. Selection of the sense resistor is made using Ohms Law, for example:

Offset Voltage / Max Current = R sense

If a Two Amp limit using the 150mV threshold is specified, it would require a resistance of 75mΩ.

Sense resistors

Care should be taken when designing the PCB layout for the Sense resistors. A Kelvin, or 4 Wire, connection scheme should be adopted as shown in Figure 10. Circuit accuracy can be affected if the PCB trace to the resistor is not optimized. Voltage drops across copper traces due to current flow can cause additional errors.

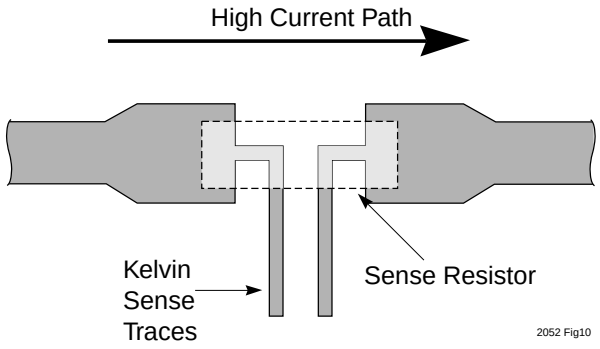


Figure 10. Kelvin-connected Sense Resistor

Each of the alarm signals can be used to change the status of the following outputs: HEALTHY#, FAULT#, FAULT_IRQ#, RST#, OV_IRQ#, and OC_IRQ#

Environmental Automonitor Blocks

The 4 environmental channels, Channels 0 through 3, are monitored autonomously by the internal logic of the SMD1108 when it is in Automonitor mode and the individual channels have been enabled. The ADC continuous samples the input and compares the value against two pre-programmed values held in a nonvolatile store.

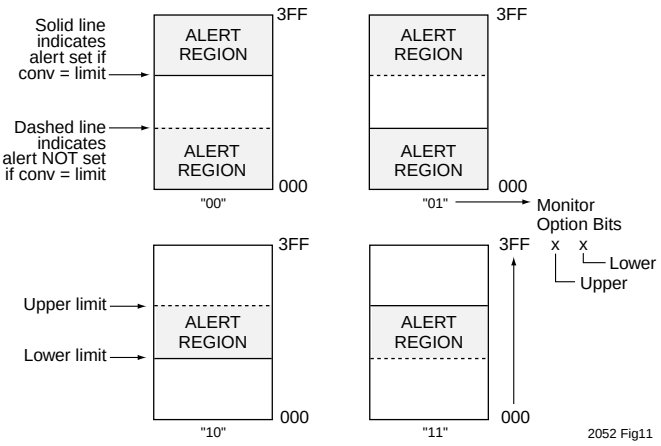


Figure 11. Alert Threshold Settings

Each Channel has two 10-bit threshold registers, one for the high threshold and one for the low threshold. The channels can be set up to measure the signals as shown in Figure 11.

If the ADC output falls into the Alert region the SMD1108 can be programmed to change any of the following signals: HEALTHY#, FAULT#, FAULT_IRQ#, and LIM_IRQ#.

In addition, the SMB Alert Output will become active. SMB_{ALERT} is a special interrupt which can be used to signal to the processor that a fault has occurred. The processor will issue a special SMB message on the serial data bus, all devices on the serial data bus will listen to the command, and the device responsible for the SMB Alert will identify its own address, as defined by the address pins (see serial data bus section). Note the processor must take the SMD1108 out of Automonitor mode prior to sending the SMB message.

General Purpose Outputs

There are 4 General Purpose Outputs which can be controlled via the serial data bus. Each signal can be controlled independently. These are open collector outputs, which are capable of sinking 5mA, suitable for driving low current LEDs. The Serial Data Bus must be active in order to control the GPO's (*i.e.*, not in Automonitor mode).

Nonvolatile Memory

In addition to programming registers the SMD1108 contains 1k bits of NV Memory, which can be accessed by a host processor using the Serial Data Bus. The NV memory looks like a conventional Serial EEPROM, using Serial Data Bus address 1010. The memory is organized as 128 × 8 bits.

Processor Supervisor Functions

Integrated into the SMD1108 are the typical functions found around a host microprocessor/microcontroller. These include reset controller, manual reset function, and a two stage watchdog timer. The RST# output signal is a function of the following inputs: Voltage Thresholds in CH4 through CH7 (can be overridden by UV_OVRD signal), the Manual Reset Input (MR#), and an Alarm from the Instant Action Block.

For each channel, which has an active UV Threshold, all channels must have a voltage above their pre-programmed UV threshold. The MR# input is intended for a front panel reset switch. This input is debounced internally and will produce a rest pulse width according to the values programmed in using the GUI. A two-stage timer is provided: the Watchdog and Longdog timers. Each timer has its own respective output (WDO and LDO), but both are triggered from a common input signal (WLDI). Normally the shorter time is programmed in the Watchdog timer. The Watchdog timer and Longdog Timer values are set in the GUI.

Serial Data Bus Interface

The SMD1108 has a serial data bus interface using clock (SCL) and data (SDA) lines. See the Serial Interface section for timing requirements. There are also three Address pins — A2, A1, A0 — which are used to select the device bus address. This allows 8 unique addresses on the bus. If the address range needs further expansion a separate CE# pin is provided. As the CE# pin enables all data bus communication with the device it must be set to the correct level for access.

The first 4 bits of the 8 bit data sent to the SMD1108 are used to access various internal functions:

0001_{BIN} — SMB Alert Protocol,

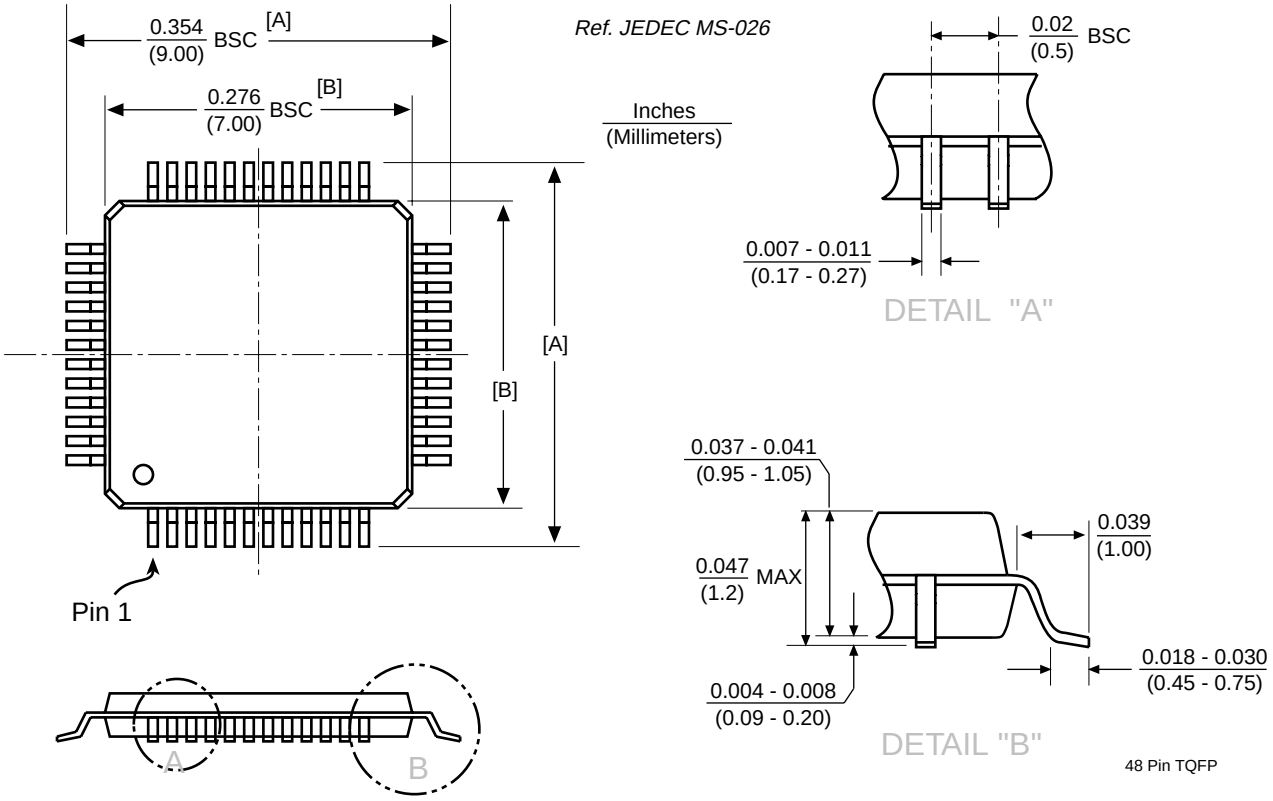
1001_{BIN} — Limit Register Access (CH0 to CH3),

1010_{BIN} — Memory Access,

1011_{BIN} — Configuration Register Access.

PACKAGE

48 PIN TQFP PACKAGE



48 Pin TQFP

ORDERING INFORMATION

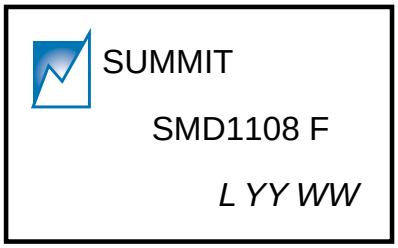
SMD1108 F

Base Part Number

Package
F = TQFP

2052 Tree 1.0

PART MARKING



F = Package type (TQFP)
L = Lot number
YY = Year
WW = Work Week

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