SM74101 Tiny 7A MOSFET Gate Driver

1 Features

- Renewable Energy Grade
- Compound CMOS and Bipolar Outputs Reduce Output Current Variation
- 7A sink/3A Source Current
- Fast Propagation Times (25 ns Typical)
- Fast Rise and Fall Times (14 ns/12 ns Rise/Fall with 2 nF Load)
- Inverting and Non-Inverting Inputs Provide Either Configuration with a Single Device
- Supply Rail Under-Voltage Lockout Protection
- Dedicated Input Ground (IN_REF) for Split Supply or Single Supply Operation
- Power Enhanced 6-Pin WSON Package (3.0mm x 3.0mm)
- Output Swings from V_{CC} to V_{EE} which can be Negative Relative to Input Ground

2 Applications

- Solar Microinverter
- AC/DC Switch-mode Power Supply
- DC/DC Switch-mode Power Supply
- Solenoid and Motor Drivers

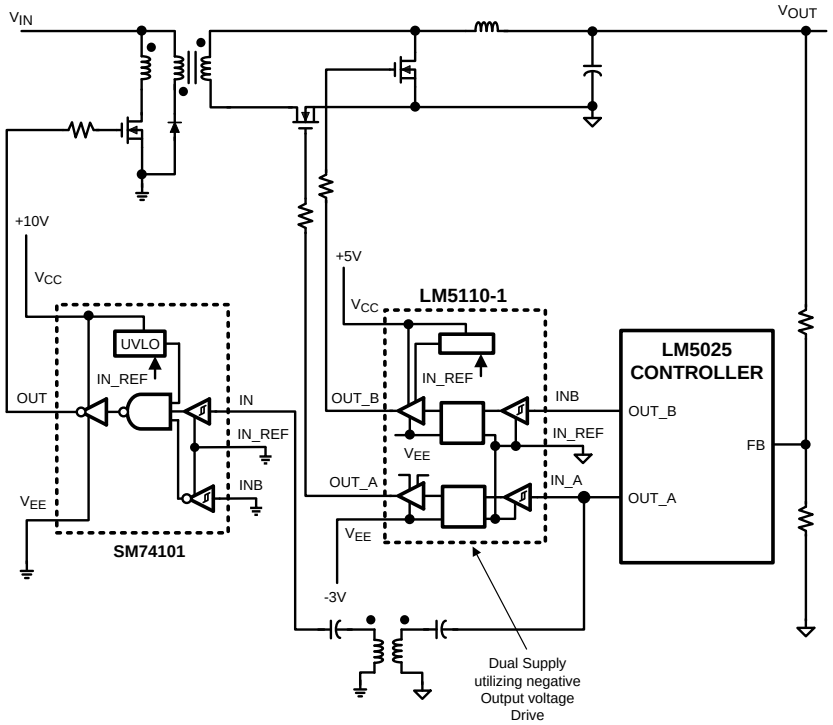
3 Description

The SM74101 MOSFET gate driver provides high peak gate drive current in the tiny WSON-6 package (SOT23 equivalent footprint), with improved power dissipation required for high frequency operation. The compound output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 7A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is provided to prevent damage to the MOSFET due to insufficient gate turn-on voltage. The SM74101 provides both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive with a single device type.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SM74101	WSON (6)	3.0 mm x 3.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



SM74101 in a DC/DC Forward Topology Power Supply

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2013) to Revision B — **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (April 2013) to Revision A — **Page**

- Changed layout of National Data Sheet to TI format ... 11

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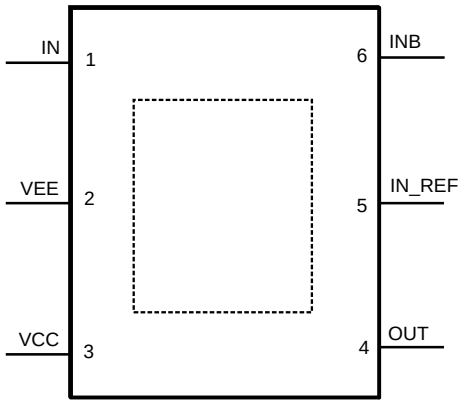
5 Pin Configuration and Functions

WSON
6-Pin
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	TTL compatible thresholds. Pull up to VCC when not used.
VEE	2	-	Connect to either power ground or a negative gate drive supply for positive or negative voltage swing.
VCC	3	I	Locally decouple to VEE. The decoupling capacitor should be located close to the chip.
OUT	4	O	Capable of sourcing 3A and sinking 7A. Voltage swing of this output is from VEE to VCC.
IN_REF	5	-	Connect to power ground (VEE) for standard positive only output voltage swing. Connect to system logic ground when VEE is connected to a negative gate drive supply.
INB	6	I	TTL compatible thresholds. Connect to IN_REF when not used.
- - -	Exposed Pad	-	Internally bonded to the die substrate. Connect to VEE ground pin for low thermal impedance.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
V_{CC} to V_{EE}	−0.3	15	V
V_{CC} to IN_REF	−0.3	15	V
IN/INB to IN_REF	−0.3	15	V
IN_REF to V_{EE}	−0.3	5	V
T_{stg} Storage temperature	−55	150	°C
Maximum Junction Temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Operating Junction Temperature		-40	125	°C
V_{CC} Operating Range	V_{CC} – IN_REF and V_{CC} - V_{EE}	3.5	14	V

6.4 Thermal Information

THERMAL METRIC (1)		SM74101 NGG 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, 0 LFPM Air Flow	40.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	
ψ_{JT}	Junction-to-top characterization parameter	0.7	
ψ_{JB}	Junction-to-board characterization parameter	29.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating junction temperature range, V_{CC} = 12 V, INB = IN_REF = V_{EE} = 0V, No Load on output, unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY						
UVLO	V_{CC} Under-voltage Lockout (rising)	V_{CC} – IN_REF	2.4	3.0	3.5	V
V_{CCH}	V_{CC} Under-voltage Hysteresis			230		mV
I_{CC}	V_{CC} Supply Current			1.0	2.0	mA
CONTROL INPUTS						
V_{IH}	Logic High		2.3			V
V_{IL}	Logic Low				0.8	V
V_{thH}	High Threshold		1.3	1.75	2.3	V

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Electrical Characteristics (continued)

Over operating junction temperature range, V_{CC} = 12 V, INB = IN_REF = V_{EE} = 0V, No Load on output, unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{thL}	Low Threshold		0.8	1.35	2.0	V
HYS	Input Hysteresis			400		mV
I_{IL}	Input Current Low	IN = INB = 0V	-1	0.1	1	µA
I_{IH}	Input Current High	IN = INB = V_{CC}	-1	0.1	1	µA
OUTPUT DRIVER						
R_{OH}	Output Resistance High	I_{OUT} = -10mA (1)		30	50	Ω
R_{OL}	Output Resistance Low	I_{OUT} = 10mA (1)		1.4	2.5	Ω
I_{SOURCE}	Peak Source Current	OUT = V_{CC}/2, 200ns pulsed current		3		A
I_{SINK}	Peak Sink Current	OUT = V_{CC}/2, 200ns pulsed current		7		A
LATCHUP PROTECTION						
	AEC–Q100, METHOD 004	T_J = 150°C		500		mA

(1) The output resistance specification applies to the MOS device only. The total output current capability is the sum of the MOS and Bipolar devices.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
td1	Propagation Delay Time Low to High, IN/ INB rising (IN to OUT)	C_{LOAD} = 2 nF, see Figure 11 and Figure 12		25	40	ns
td2	Propagation Delay Time High to Low, IN / INB falling (IN to OUT)	C_{LOAD} = 2 nF, see Figure 11 and Figure 12		25	40	ns
tr	Rise time	C_{LOAD} = 2 nF , see Figure 11 and Figure 12		14		ns
tf	Fall time	C_{LOAD} = 2 nF , see Figure 11 and Figure 12		12		ns

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6.7 Typical Characteristics

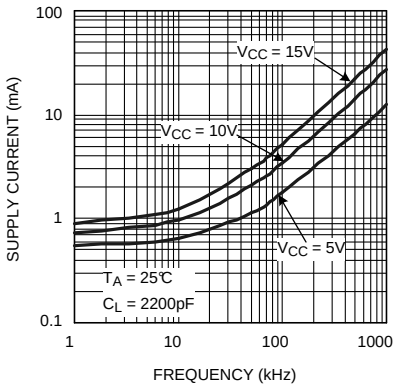

Figure 1. Supply Current vs Frequency

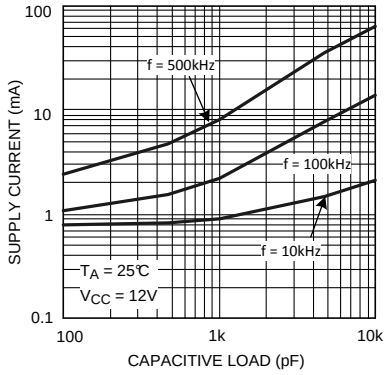

Figure 2. Supply Current vs Capacitive Load

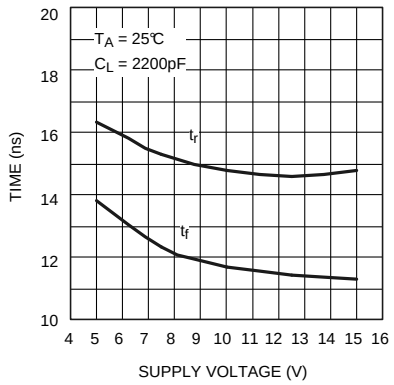

Figure 3. Rise and Fall Time vs Supply Voltage

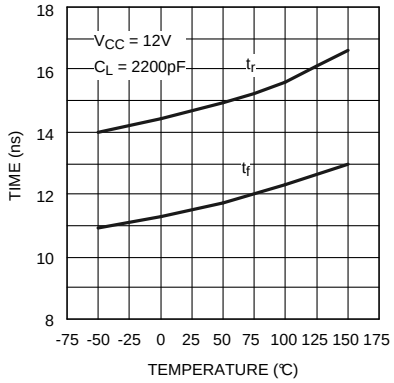

Figure 4. Rise and Fall Time vs Temperature

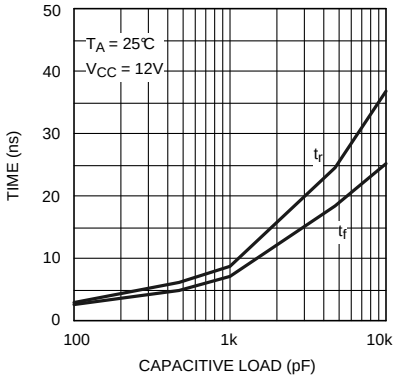

Figure 5. Rise and Fall Time vs Capacitive Load

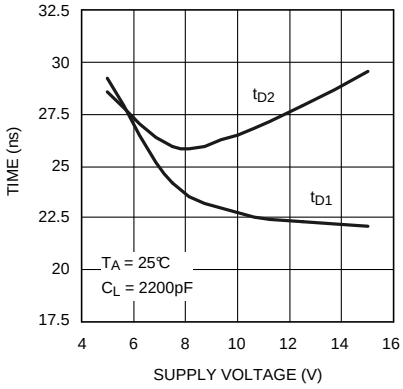

Figure 6. Delay Time vs Supply Voltage

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Typical Characteristics (continued)

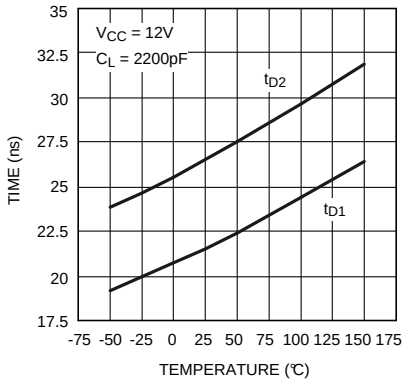


Figure 7. Delay Time vs Temperature

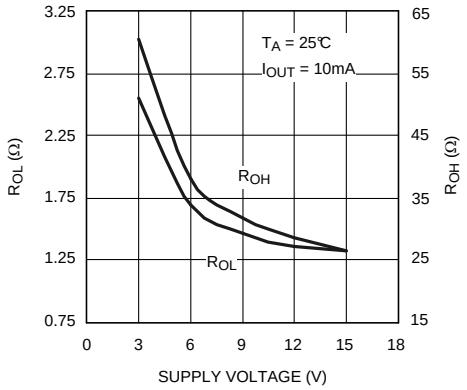


Figure 8. RDSON vs Supply Voltage

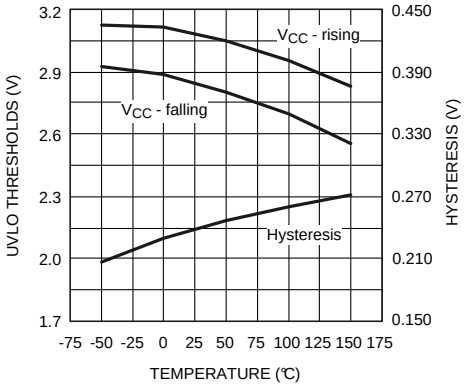


Figure 9. UVLO Thresholds and Hysteresis vs Temperature

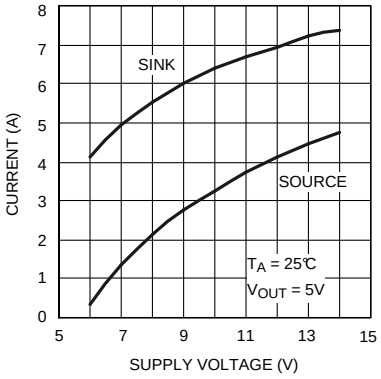


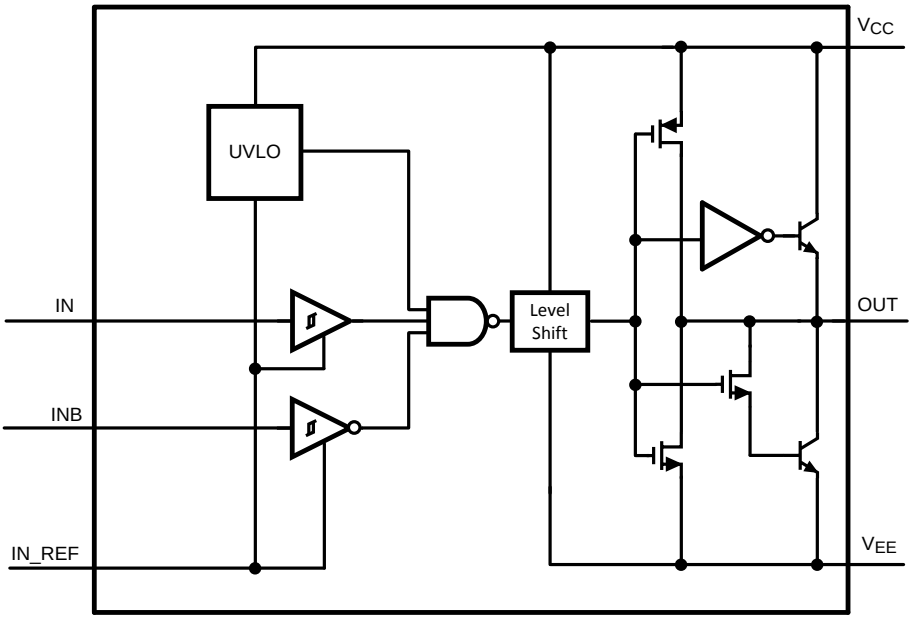
Figure 10. Peak Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The SM74101 is a high speed, high peak current (7A) single channel MOSFET driver. The high peak output current of the SM74101 will switch power MOSFET's on and off with short rise and fall times, thereby reducing switching losses considerably. The SM74101 includes both inverting and non-inverting inputs that give the user flexibility to drive the MOSFET with either active low or active high logic signals. The driver output stage consists of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical Miller plateau region of the MOSFET V_{GS} , while the MOS device provides rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage V_{CC} and the power ground potential at the V_{EE} pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Detailed Operating Description

The control inputs of the driver are high impedance CMOS buffers with TTL compatible threshold voltages. The negative supply of the input buffer is connected to the input ground pin IN_REF. An internal level shifting circuit connects the logic input buffers to the totem pole output drivers. The level shift circuit and the separate input/output ground pins provide the option of single supply or split supply configurations. When driving the MOSFET gate from a single positive supply, the IN_REF and V_{EE} pins are both connected to the power ground.

The isolated input and output stage grounds provide the capability to drive the MOSFET to a negative V_{GS} voltage for a more robust and reliable off state. In split supply configuration, the IN_REF pin is connected to the ground of the controller which drives the SM74101 inputs. The V_{EE} pin is connected to a negative bias supply that can range from the IN_REF potential to as low as 14 V below the Vcc gate drive supply. For reliable operation, the maximum voltage difference between V_{CC} and IN_REF or between V_{CC} and V_{EE} is 14V.

The minimum recommended operating voltage between Vcc and IN_REF is 3.5V. An Under Voltage Lock Out (UVLO) circuit is included in the SM74101 which senses the voltage difference between V_{CC} and the input ground pin, IN_REF. When the V_{CC} to IN_REF voltage difference falls below 2.8V the driver is disabled and the output pin is held in the low state. The UVLO hysteresis prevents chattering during brown-out conditions; the driver will resume normal operation when the V_{CC} to IN_REF differential voltage exceeds 3.0V.

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7.4 Device Functional Modes

7.4.1 Inverting Mode of Operation

During the inverting mode of operation, INB is used as the control input and the polarity of OUT is reversed with respect to INB. A timing diagram of this mode is shown in Figure 11. The IN pin is not used in this mode of operation and should be pulled up to VCC.

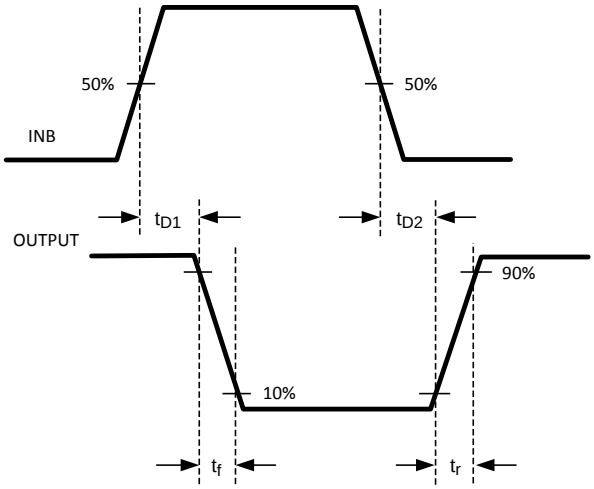

Figure 11. Inverting

7.4.2 Non-inverting Mode of Operation

During the non-inverting mode of operation, IN is used as the control input and the polarity of OUT is the same with respect to IN. A timing diagram of this mode is shown in Figure 12. The INB pin is not used in this mode of operation and should be connected to IN_REF.

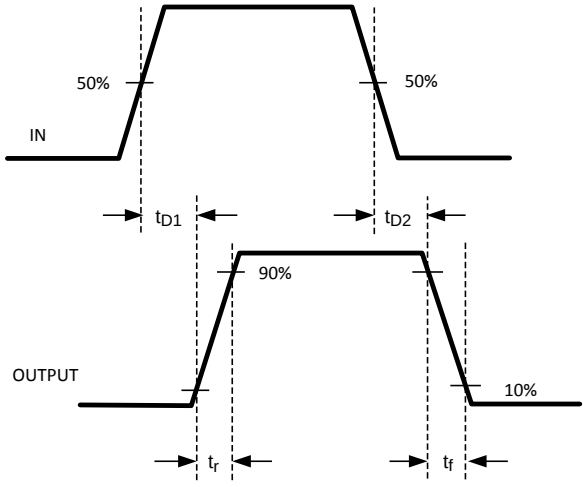

Figure 12. Non-Inverting

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7.5 Thermal Considerations

The primary goal of the thermal management is to maintain the integrated circuit (IC) junction temperature (Tj) below a specified limit to ensure reliable long term operation. The maximum T_J of IC components should be estimated in worst case operating conditions. The junction temperature can be calculated based on the power dissipated on the IC and the junction to ambient thermal resistance θ_{JA} for the IC package in the application board and environment. The θ_{JA} is not a given constant for the package and depends on the PCB design and the operating environment.

7.5.1 Drive Power Requirement Calculations In SM74101

SM74101 is a single low side MOSFET driver capable of sourcing / sinking 3A / 7A peak currents for short intervals to drive a MOSFET without exceeding package power dissipation limits. High peak currents are required to switch the MOSFET gate very quickly for operation at high frequencies.

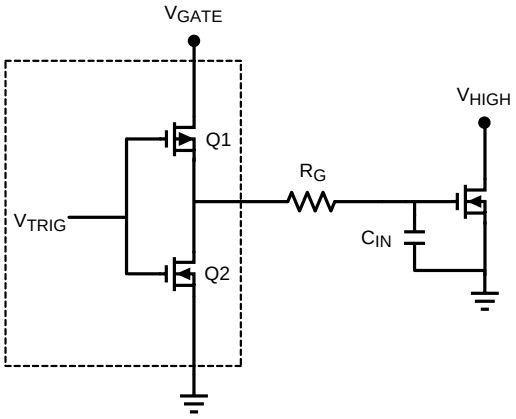

Figure 13.

The schematic above shows a conceptual diagram of the SM74101 output and MOSFET load. Q1 and Q2 are the switches within the gate driver. Rg is the gate resistance of the external MOSFET, and Cin is the equivalent gate capacitance of the MOSFET. The equivalent gate capacitance is a difficult parameter to measure as it is the combination of Cgs (gate to source capacitance) and Cgd (gate to drain capacitance). The Cgd is not a constant and varies with the drain voltage. The better way of quantifying gate capacitance is the gate charge Qg in coloumbs. Qg combines the charge required by Cgs and Cgd for a given gate drive voltage Vgate. The gate resistance Rg is usually very small and losses in it can be neglected. The total power dissipated in the MOSFET driver due to gate charge is approximated by:

$$P_{DRIVER} = V_{GATE} \times Q_G \times F_{SW}$$

Where

- F_{SW} = switching frequency of the MOSFET. (1)

For example, consider the MOSFET MTD6N15 whose gate charge specified as 30 nC for V_{GATE} = 12V.

Therefore, the power dissipation in the driver due to charging and discharging of MOSFET gate capacitances at switching frequency of 300 kHz and V_{GATE} of 12V is equal to

$$P_{DRIVER} = 12V \times 30\ nC \times 300\ kHz = 0.108W. \quad (2)$$

In addition to the above gate charge power dissipation, - transient power is dissipated in the driver during output transitions. When either output of the SM74101 changes state, current will flow from V_{CC} to V_{EE} for a very brief interval of time through the output totem-pole N and P channel MOSFETs. The final component of power dissipation in the driver is the power associated with the quiescent bias current consumed by the driver input stage and Under-voltage lockout sections.

Characterization of the SM74101 provides accurate estimates of the transient and quiescent power dissipation components. At 300 kHz switching frequency and 30 nC load used in the example, the transient power will be 8 mW. The 1 mA nominal quiescent current and 12V V_{GATE} supply produce a 12 mW typical quiescent power.

Therefore the total power dissipation

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Thermal Considerations (continued)

$$P_D = 0.118 + 0.008 + 0.012 = 0.138W. \quad (3)$$

We know that the junction temperature is given by

$$T_J = P_D \times \theta_{JA} + T_A \quad (4)$$

Or the rise in temperature is given by

$$T_{RISE} = T_J - T_A = P_D \times \theta_{JA} \quad (5)$$

For WSON-6 package, the integrated circuit die is attached to leadframe die pad which is soldered directly to the printed circuit board. This substantially decreases the junction to ambient thermal resistance (θ_{JA}). By providing suitable means of heat dispersion from the IC to the ambient through exposed copper pad, which can readily dissipate heat to the surroundings, θ_{JA} as low as 40°C / Watt is achievable with the package. The resulting Trise for the driver example above is thereby reduced to just 5.5 degrees.

Therefore T_{RISE} is equal to

$$T_{RISE} = 0.138 \times 40 = 5.5°C \quad (6)$$

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SM74101 can be used to drive a low side MOSFET with very low switching losses. Either one of the control input pins, IN or INB, can be used to control the gate drive to the MOSFET. The choice of the control input pin used will depend on the polarity of operation.

8.2 Typical Application

The SM74101 is utilized in a DC/DC forward topology power supply as shown in Figure 14. The high peak gate drive current of the SM74101 allows for short rise and fall times on the primary side MOSFET, thereby improving overall efficiency of the system and reducing switching losses. It is used in conjunction with the LM5025 Active Clamp Voltage Mode PWM Controller to provide drive capability to the primary side MOSFET after isolation.

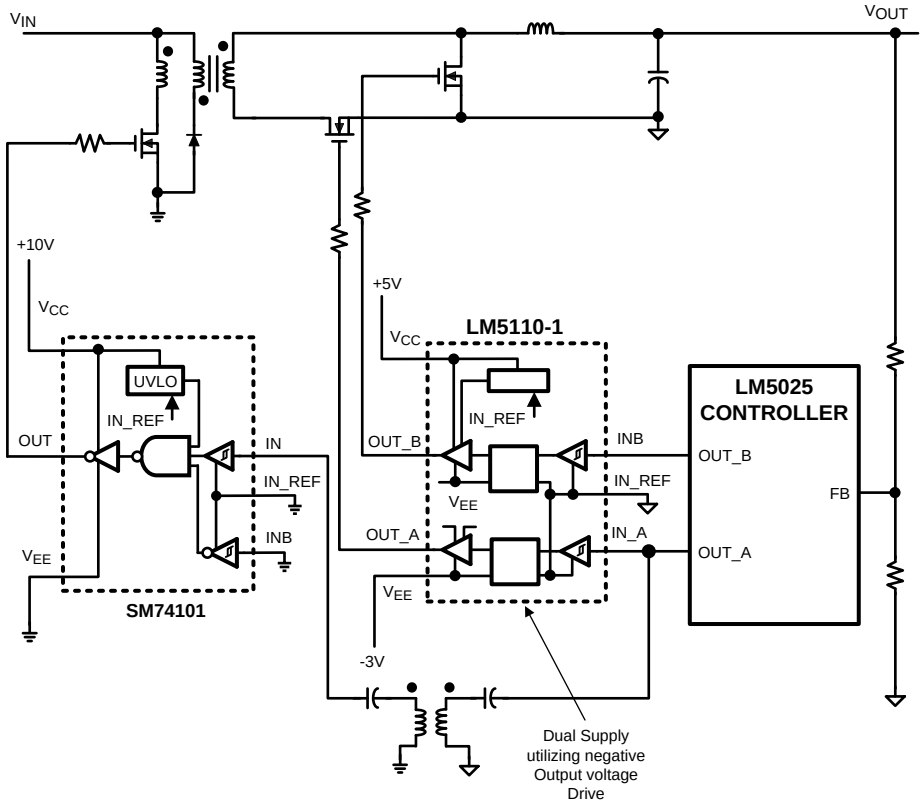

Figure 14. DC/DC Forward Topology Power Supply

8.2.1 Design Requirements

The SM74101 is used in the non-inverting mode of operation. The IN pin is used to control the OUT signal to the primary side MOSFET. The signal that travels from OUT_A and through the isolation transformer should be compatible with the high and low threshold voltages of the IN pin. INB is not used in this mode and is therefore connected to IN_REF, which is also the primary side ground.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

See Power Supply Recommendations, Layout, and Thermal Considerations for key design considerations regarding the input supply, grounding, and thermal calculations specific to the SM74101.

8.2.3 Application Curve

The rise and fall times of the OUT signal will depend on the capacitance of the MOSFET gate. Therefore, an appropriate MOSFET should be selected to meet the switching speed and efficiency requirements of the system.

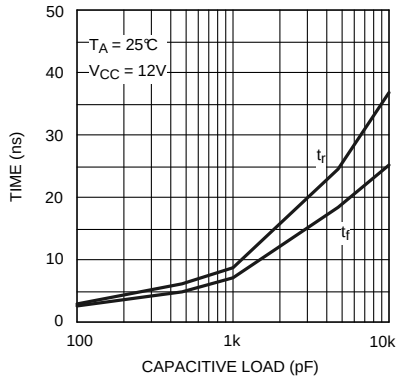

Figure 15. Rise and Fall Time vs Capacitive Load

9 Power Supply Recommendations

A Low ESR/ESL capacitor must be connected close to the IC and between the V_{CC} and V_{EE} pins to support high peak currents being drawn from V_{CC} during turn-on of the MOSFET. Also, if either channel is not being used, the respective input pin (IN or INB) should be connected to either V_{EE} or V_{CC} to avoid spurious output signals.

10 Layout

10.1 Layout Guidelines

Attention must be given to board layout when using the SM74101. Proper grounding is crucial. The driver needs a very low impedance path for current return to ground avoiding inductive loops. Two paths for returning current to ground are a) between SM74101 IN_REF pin and the ground of the circuit that controls the driver inputs and b) between SM74101 V_{EE} pin and the source of the power MOSFET being driven. Both paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. These ground paths should be distinctly separate to avoid coupling between the high current paths (VCC, VEE, and OUT) and the logic signal paths (IN, INB, and IN_REF) of the SM74101. With rise and fall times in the range of 10 to 30 ns, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated when driving large capacitive loads.

10.2 Layout Example

Figure 16 shows an example layout for the SM74101 configured in the non-inverting mode of operation. In this mode, the INB pin is not used and is connected to IN_REF. Two low ESR/ESL capacitors, C1 and C2, are used for input decoupling purposes and are placed as close as possible to the IC.

The level shift circuit and the separate input/output ground pins provide the option of single supply or split supply configurations. When driving the MOSFET gate from a single positive supply, the control ground should be connected to the power ground in an area of the board where the least amount of noise will exist. Otherwise, when using a split supply configuration, the control ground and power ground paths should be distinctly separate to avoid noise coupling between the two paths.

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Layout Example (continued)

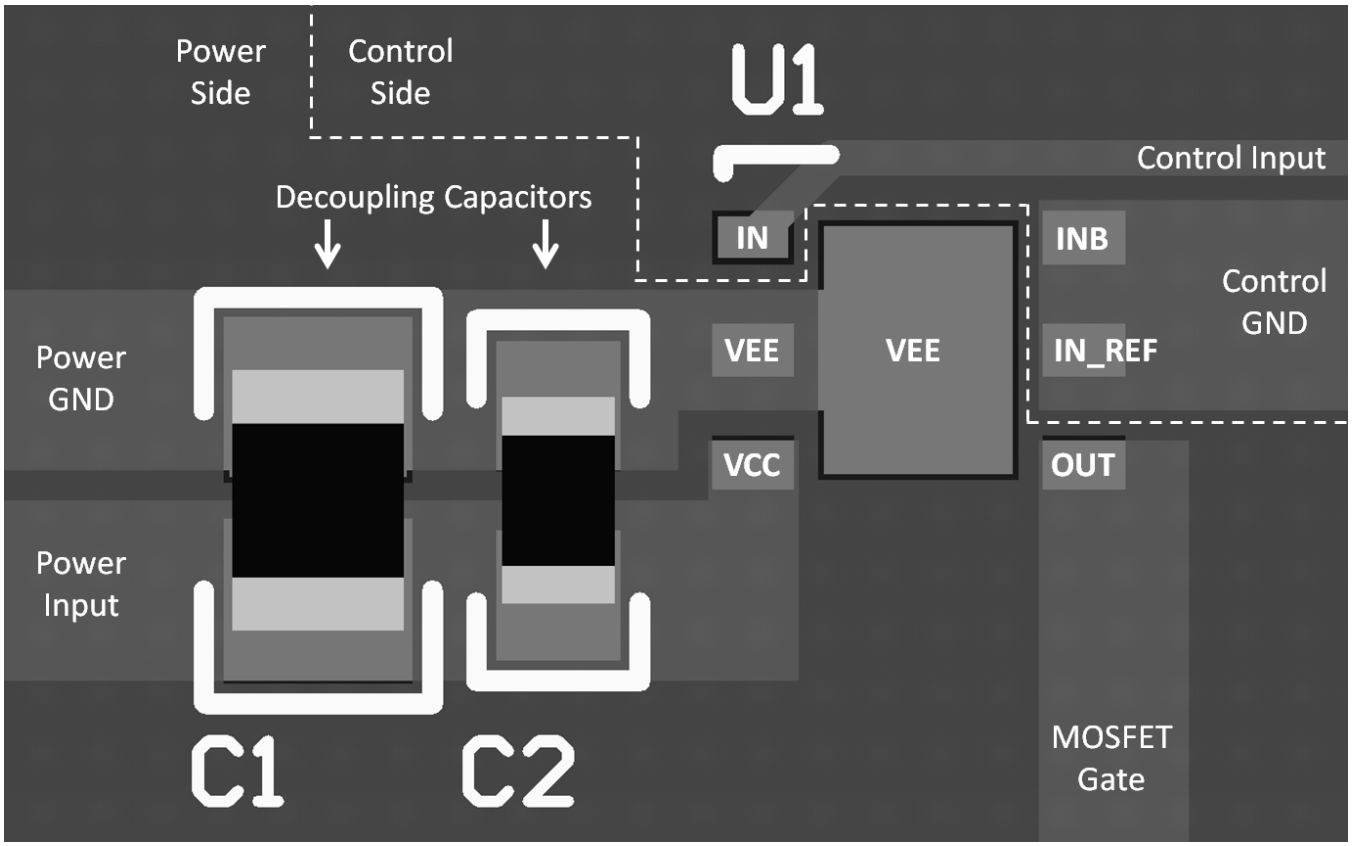

Figure 16. SM74101 Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SM74101SD/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L264B	Samples
SM74101SDX/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L264B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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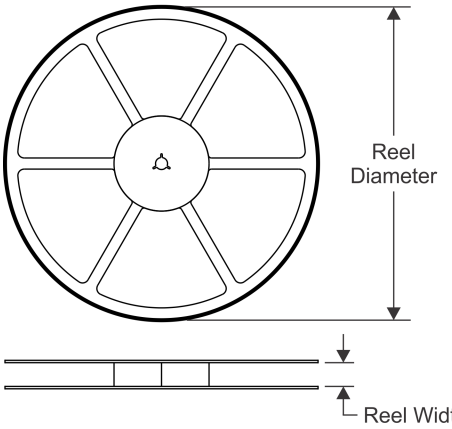
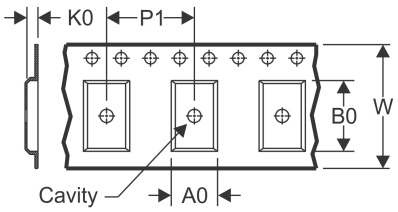
TAPE AND REEL INFORMATION

REEL DIMENSIONS

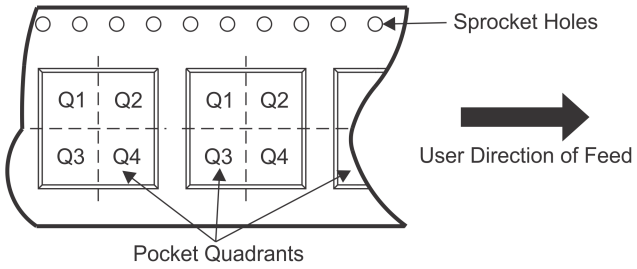


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

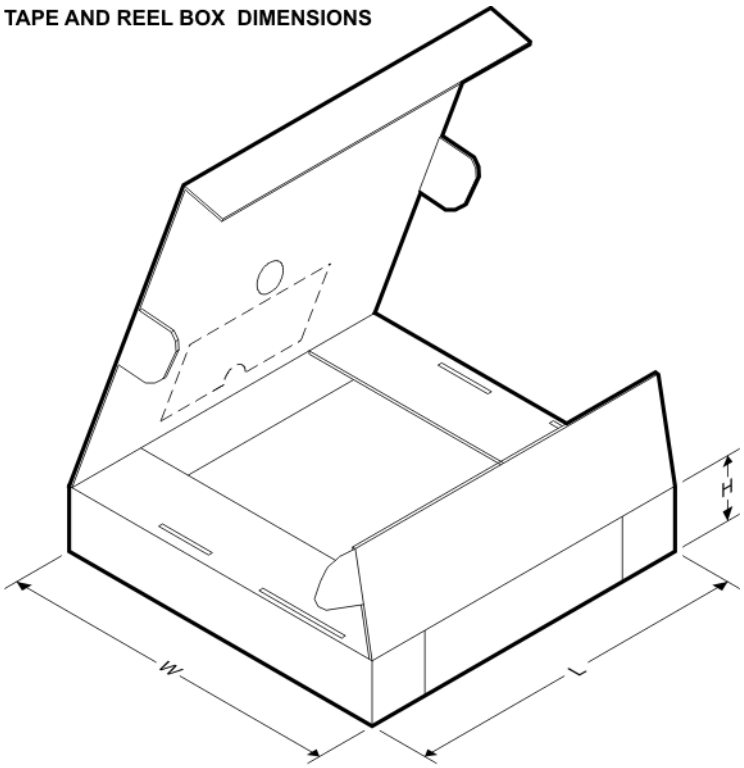
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM74101SD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
SM74101SDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

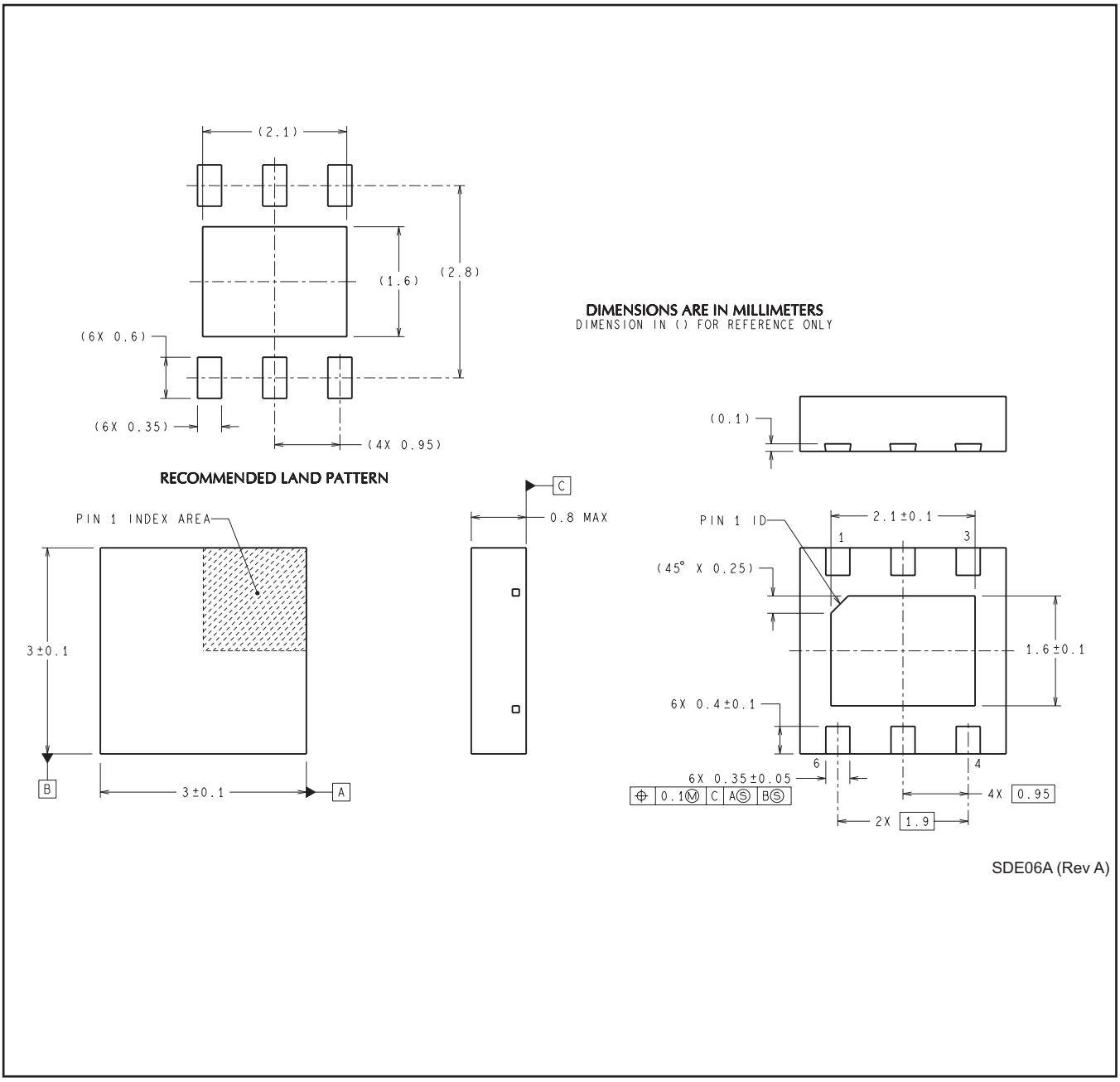
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM74101SD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
SM74101SDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0

NGG0006A



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