SL811HS
Embedded USB Host/Slave Controller

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Document #: 38-08008 Rev. *A Revised March 14, 2002

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1.0 Conventions

1,2,3,4	Numbers without annotations are decimals.
Dh, 1Fh, 39h	Hexadecimal numbers are followed by an “h.”
0101b, 010101b	Binary numbers are followed by a “b.”
bRequest, n	Words in *italics* indicate terms defined by USB Specification or by this Specification.

2.0 Definitions

USB	**U**niversal **S**erial **B**us
SL811HS	The SL811HS is a Cypress USB Host/Slave Controller, providing multiple functions on a single chip. This part is offered in both a 28-pin PLCC package (SL811HS) and a 48-pin TQFP package (SL811HST-AC). Throughout this document, “SL811HS” refers to both packages unless otherwise noted.
	Note: This chip does not include CPU.
SL11	The SL11 is a Cypress **USB** Peripheral Device Controller, providing multiple functions on a single chip. This part is offered in both a 28-pin PLCC package (SL11) and a 48-pin TQFP package (SL11T-AC). Throughout this document, “SL11” refers to both packages unless otherwise noted.
	Note: This chip does not include a CPU.
SL11H	The SL11H is a Cypress **USB** Host/Slave Controller, providing multiple functions on a single chip. This part is offered in both a 28-Pin PLCC package (SL11H) and a 48-Pin TQFP package (SL11HT-AC). Throughout this document, “SL11H” refers to both packages unless otherwise noted.
	Note: This chip does not include CPU.
LSB	**L**east **S**ignificant **B**it
MSB	**M**ost **S**ignificant **B**it
R/W	**R**ead/**W**rite
PLL	**P**hase **L**ock **L**oop
RAM	**R**andom **A**ccess **M**emory
SIE	**S**erial **I**nterface **E**ngine
ACK	Handshake packet indicates a positive acknowledgment.
NAK	Handshake packet indicating a negative acknowledgment
USBD	**U**niversal **S**erial **B**us **D**river
SOF	**S**tart **o**f **F**rame is the first transaction in each frame. It allows endpoints to identify the start of the frame and synchronize internal endpoint clocks to the host.
CRC	**C**yclic **R**edundancy **C**heck
HOST	The host computer system on which the USB Host Controller is installed

3.0 References

[Ref 1] USB Specification 1.1: http://www.usb.org.

4.0 Introduction

4.1 Block Diagram

The SL811HS is an Embedded USB Host/Slave Controller capable of communicate with either full-speed or low-speed USB peripherals. The SL811HS can interface to devices such as microprocessors, microcontrollers, DSPs, or directly to a variety of buses such as ISA, PCMCIA, and others. The SL811HS USB Host Controller conforms to USB Specification 1.1.

The SL811HS USB Host/Slave Controller incorporates USB Serial Interface functionality along with internal full-/low-speed transceivers. The SL811HS supports and operates in USB full-speed mode at 12 Mbps, or at low-speed 1.5-Mbps mode.

The SL811HS data port and microprocessor interface provide an 8-bit data path I/O or DMA bidirectional, with interrupt support to allow easy interface to standard microprocessors or microcontrollers such as Motorola or Intel CPUs and many others. Internally, the SL811HS contains a 256-byte RAM data buffer which is used for control registers and data buffer.

The available package types offered are a 28-pin PLCC (SL811HS) and a 48-pin TQFP package (SL811HST-AC). Both packages operate at 3.3 VDC. The I/O interface logic is 5V-tolerant.

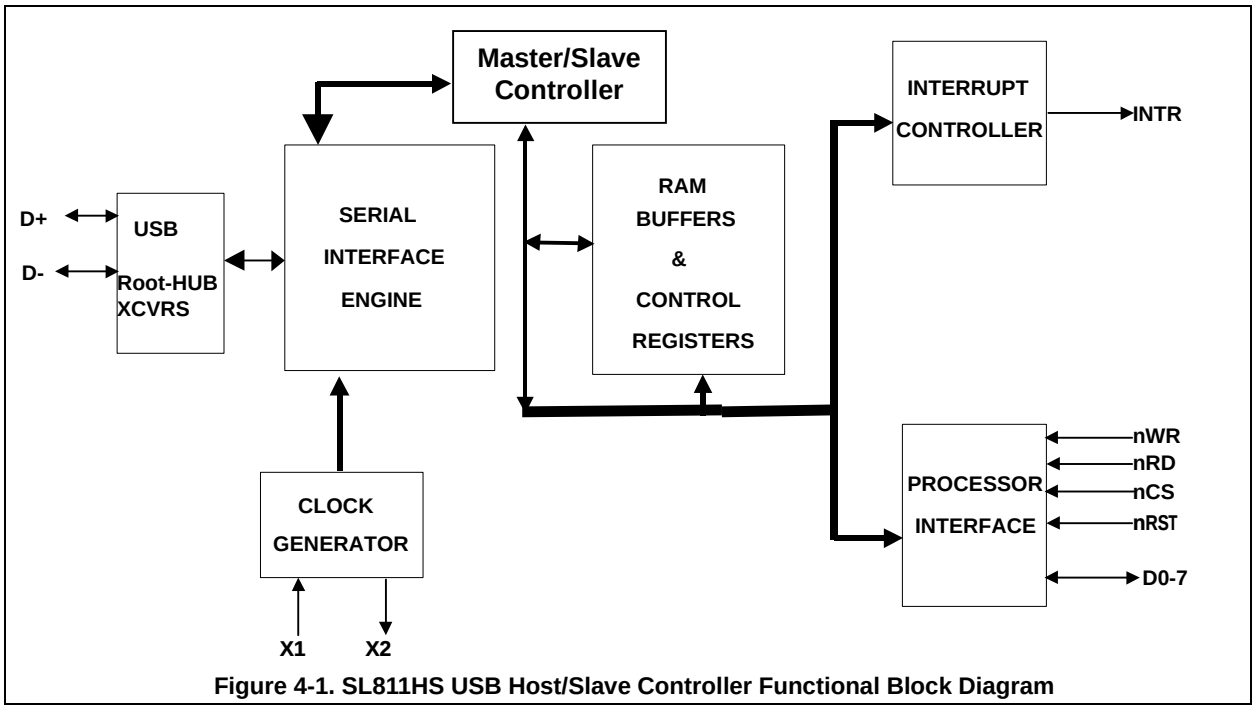


Figure 4-1. SL811HS USB Host/Slave Controller Functional Block Diagram

4.2 SL811HS Host or Slave Mode Selection [Master/Slave Mode]

SL811HS can work in two modes—host or slave. **For slave-mode operation and specification, please refer to the SL811S specification. This data sheet only covers host-mode operation.**

4.3 Features

- The only USB Host/Slave controller for embedded systems in the market with a standard microprocessor bus interface.
- Supports both full-speed (12 Mbps) and low-speed (1.5 Mbps) USB transfer

4.3.1 USB Specification Compliance

- Conforms to USB Specification 1.1

4.3.2 CPU Interface

- Operates as a single USB host or slave under software control
- Low-speed 1.5 Mbps, and full speed 12 Mbps, in both master and slave modes
- Automatic detection of either low- or full-speed devices
- 8-bit bidirectional data, port I/O (DMA supported in slave mode)
- On-chip SIE and USB transceivers
- On-chip single root HUB support
- 256-byte internal SRAM buffer, ping-pong operation
- Operates from 12- or 48-MHz crystal or oscillator (built-in DPLL)
- 5 V-tolerant interface
- Suspend/resume, wake up, and low-power modes are supported
- Auto-generation of SOF and CRC5/16
- Auto-address increment mode, saves memory Read/Write cycles
- Development kit including source code drivers is available
- Backward-compatible with SL11H, both pin and functionality
- 3.3V power source, 0.35 micron CMOS technology
- Available in both a 28-pin PLCC package (SL811HS) and a 48-pin TQFP package (SL811HST-AC).

4.4 Data Port, Microprocessor Interface

The SL811HS microprocessor interface provides an 8-bit bidirectional data path along with appropriate control lines to interface to external processors or controllers. The control lines, Chip Select, Read and Write input strobes and a single address line, A0, along with the 8-bit data bus, support programmed I/O or memory mapped I/O designs.

Access to memory and control register space is a simple two step process, requiring an address Write with A0 set = “0,” followed by a register/memory Read or Write cycle with address line A0 set = “1.”

In addition, DMA bidirectional interface in slave mode is available with handshake signals such as DREQ, ACK, WR, RD, CS and INTR. Please refer to the SL811S spec.

The SL811HS Write or Read operation terminates when either nWR or nCS goes inactive. For devices interfacing to the SL811HS, that deactivate the Chip Select nCS before the Write nWR, the data hold timing should be measured from the nCS and will be the same value as specified. Thus, both Intel®– and Motorola-type CPUs can work easily with the SL811HS without any external glue logic requirements.

4.5 Interrupt Controller

The SL811HS interrupt controller provides a single output signal (INTRQ) that can be activated by a number of events that may occur as result of USB activity. Control and status registers are provided to allow the user to select single or multiple events, which will generate an interrupt (assert INTRQ), and lets the user view interrupt status. The interrupts can be cleared by writing to the appropriate register (the Status Register at address 0x0d).

4.6 Buffer Memory

The SL811HS contains 256 bytes of internal buffer memory. The first 16 bytes of memory represent control and status registers for programmed I/O operations. The remaining memory locations are used for data buffering (max. 240 Bytes).

Access to the registers and data memory is through an external microprocessor, 8-bit data bus, in either of two addressing modes, indexed or, if used with multiplexed address/data bus interfaces, direct access. With indexed addressing, the address is first written to the device with the A0 address line LOW, then the following cycle with A0 address line HIGH is directed to the specified address. USB transactions are automatically routed to the memory buffer. Control registers are provided, so that pointers and block sizes in buffer memory can be can set up.

4.6.1 Auto Address Increment Mode

The SL811HS supports auto-increment mode for Read or Write Cycles, A0 mode. In A0 mode, the Micro Controller sets up the address only once. On any subsequent DATA Read or Write access, the internal address pointer will advance to the next DATA location.

4.6.1.1 For example

Write 0x10 to SL811HS in address cycle (A0 is set LOW)

Write 0x55 to SL811HS in data cycle (A0 is set HIGH) -> Write 0x55 to location 0x10

Write 0xaa to SL811HS in data cycle (A0 is set HIGH) -> Write 0xaa to location 0x11

Write 0xbb to SL811HS in data cycle (A0 is set HIGH) -> Write 0xbb to location 0x12

The advantage of auto address increment mode is that it reduces the number of SL811HS memory Read/Write cycles required to move data to/from the device. For example, transferring 64-bytes of data to/from SL811HS using auto increment mode, will reduce the number of cycles to 1 Address Write and 64 Read/Write Data cycles, compared to 64 Address Writes and 64 Data Cycles for Random Access.

4.7 PLL Clock Generator

Either a 12-MHz or a 48-MHz external crystal can be used with the SL811HS. Two pins, X1 and X2, are provided to connect a low-cost crystal circuit to the device as shown in *Figure 4-2* and *Figure 4-3*. If an external 48-MHz clock source is available in the application, it can be used instead of the crystal circuit by connecting the source directly to the X1 input pin. When a clock is used, the X2 pin is left unconnected.

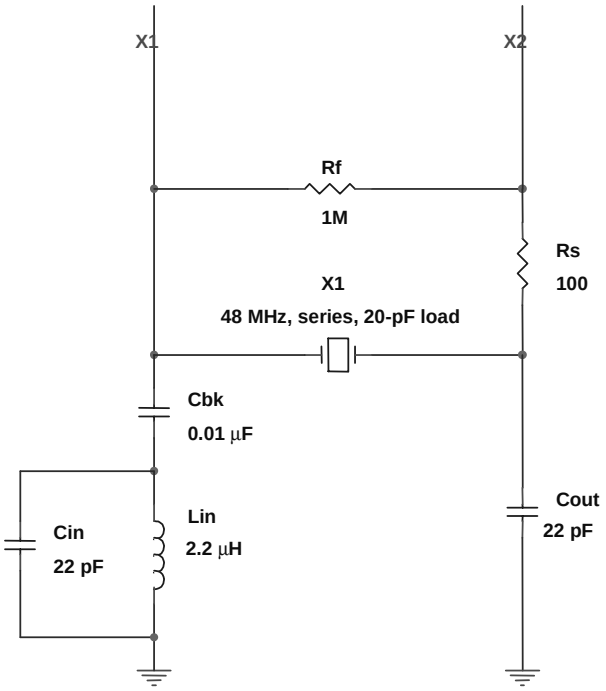


Figure 4-2. Full-Speed 48-MHz Crystal Circuit

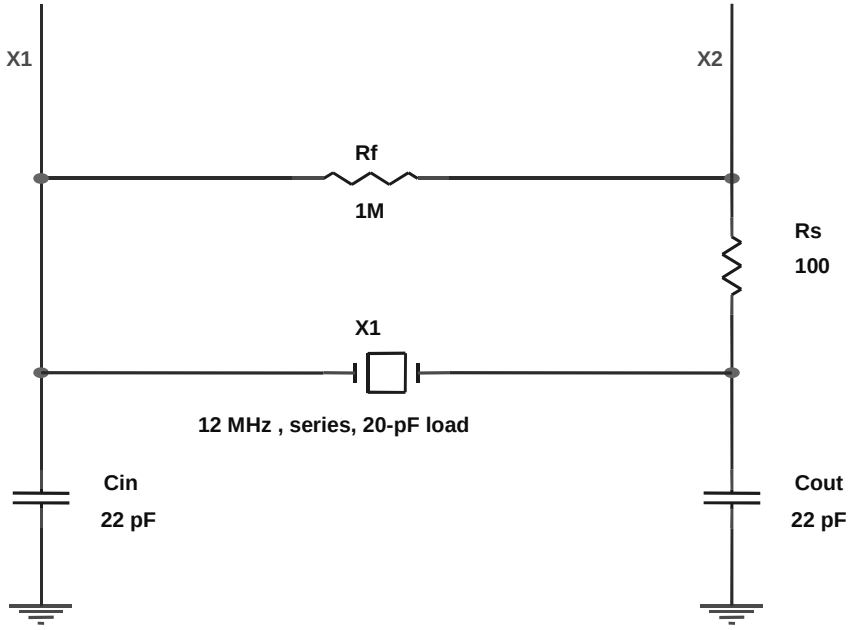


Figure 4-3. Optional 12-MHz Crystal Circuit

Note:
1. CM (Clock Mode) pin of the SL811HS should be tied to GND when 48-MHz Xtal circuit or 48-MHz clock source is used.

4.7.1 Typical Crystal Requirements

The following are examples of “typical requirements”. Please note that these specifications are generally found as standard crystal values and are therefore less expensive than custom values. If crystals are used in series circuits, load capacitance is not applicable. Load capacitance of parallel circuits is a requirement.

12-MHz Crystals:

Frequency Tolerance:	±100 ppm or better
Operating Temperature Range:	0°C to 70°C
Frequency:	12 MHz
Frequency Drift over Temperature:	± 50 ppm
ESR (Series Resistance):	60Ω
Load Capacitance:	10 pF min.
Shunt Capacitance:	7 pF max.
Drive Level:	0.1–0.5 mW
Operating Mode:	fundamental

48-MHz Crystals:

Frequency Tolerance:	±100 ppm or better
Operating Temperature Range:	0°C to 70°C
Frequency:	48 MHz
Frequency Drift over Temperature:	± 50 ppm
ESR (Series Resistance):	40 Ω
Load Capacitance:	10 pF min.
Shunt Capacitance:	7 pF max.
Drive Level:	0.1–0.5 mW
Operating Mode:	third overtone

4.8 USB Transceiver

The SL811HS has a built in transceiver that meets USB Specification 1.1. The transceiver is capable of transmitting and receiving serial data at USB full speed (12 Mbits) and low speed (1.5 Mbits). The driver portion of the transceiver is differential while the receiver section is comprised of a differential receiver and two single-ended receivers. Internally, the transceiver interfaces to the Serial Interface Engine (SIE) logic. Externally, the transceiver connects to the physical layer of the USB.

5.0 SL811HS Registers

Operation of the SL811HS is controlled through 16 internal registers. A portion of the internal RAM is devoted to the control register space, and access is through the microprocessor interface. The registers provide control and status information for transactions on the USB, microprocessor interface, and interrupts.

Any Write to control register 0FH will enable the SL811HS full features bit. This is an internal bit of the SL811HS that enables additional features not supported by the SL11H. For SL11H hardware backward compatibility, this register should not be accessed.

The table below shows the memory map and register mapping of both the SL11H and SL811HS. The SL11H is shown for users upgrading to the SL811HS.

Register Name SL11H and SL811HS	SL11H (hex) Address	SL811HS (hex) Address
USB-A Host Control Register	00H	00H
USB-A Host Base Address	01H	01H
USB-A Host Base Length	02H	02H
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03H	03H
USB-A Host Device Address (Write)/Transfer Count (Read)	04H	04H
Control Register1	05H	05H
Interrupt Enable Register	06H	06 H
Reserved Register	Reserved	Reserved
USB-B Host Control Register	Reserved	08H
USB-B Host Base Address	Reserved	09H
USB-B Host Base Length	Reserved	0AH
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	Reserved	0BH
USB-B Host Device Address (Write)/Transfer Count (Read)	Reserved	0CH
Status Register	0DH	0DH
SOF Counter LOW (Write)/HW Revision Register (Read)	0EH	0E H
SOF Counter HIGH and Control Register2	Reserved	0F H
Memory Buffer	10H-FFH	10H-FFH

The registers in the SL811HS are divided into two major groups. The first group is referred to as USB Control registers. These registers enable and provide status for control of USB transactions and data flow. The second group of registers provides control and status for all other operations.

5.1 Register Values on Power-up and Reset

The following registers initialize to zero on power-up and reset:

- USB-A/USB-B Host Control Register [00H, 08H] bit 0 only
- Control Register 1 [05H]
- USB Address Register [07H]
- Current Data Set/Hardware Revision/SOF Counter LOW Register [0EH]

All other registers power-up and reset in an unknown state and should be initialized by firmware.

5.2 USB Control Registers

Communication and data flow on the USB uses the SL811HS's USB A-B Control Registers. The SL811HS can communicate with any USB Device functions and any specific endpoints via the USBA or USBB register sets.

The USB A-B Host Control Registers can be used in a Ping-Pong arrangement to manage traffic on the USB. The USB Host Control Register also provides a means to interrupt an external CPU or Micro Controller when one of the USB protocol transactions is completed. The table above shows the two sets of USB Host Control Registers, the "A" set and "B" set. The two register sets allow for overlapped operation. When one set of parameters is being set up, the other is transferring. On completion of a transfer to an endpoint, the next operation will be controlled by the other register set.

Note. On the SL11H, the USB-B set control registers are not used. The USB-B register set can be used only when SL811HS mode is enabled by initializing register 0FH.

The SL811HS USB Host Control has two groups of five registers each, which map in the SL811HS memory space. These registers are defined in the following tables.

5.2.1 SL811HS Host Control Registers

Register Name SL11H and SL811H	SL11H (hex) Address	SL811HS (hex) Address
USB-A Host Control Register	00H	00H
USB-A Host Base Address	01H	01H
USB-A Host Base Length	02H	02H
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03H	03H
USB-A Host Device Address (Write)/Transfer Count (Read)	04H	04H
USB-B Host Control Register	Reserved	08H
USB-B Host Base Address	Reserved	09H
USB-B Host Base Length	Reserved	0AH
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	Reserved	0BH
USB-B Host Device Address (Write)/Transfer Count (Read)	Reserved	0CH

5.2.2 USB-A/USB-B Host Control Registers [00H, 08H]

Bit Position	Bit Name	Function
0	Arm	Allows enabled transfers when set = “1.” Cleared to “0” when transfer is complete.
1	Enable	When set = “1” allows transfers to this endpoint. When set “0” USB transactions are ignored. If Enable = “1” and Arm = '0' the endpoint will return NAKs to USB transmissions.
2	Direction	When set = “1” transmit to Host. When “0” receive from Host.
3	Reserved	
4	ISO	When set to “1” allows Isochronous mode for this endpoint.
5	SOF	“1” = Synchronize with the SOF transfer
6	Data Toggle Bit	“0” if DATA0, “1” if DATA1.
7	Preamble	If set = “1” a preamble token is transmitted prior to transfer of low-speed packet. If set = “0,” preamble generation is disabled.

- Bit 3 is reserved for future usage.
- The SL811HS uses bit 5 to enable transfer of a data packet after a SOF packet is transmitted. When this bit set “1,” the next enabled packet will be sent after next SOF. If set = “0” the next packet is sent immediately if the SIE is free.
- The SL811HS automatically generates preamble packets when bit 7 is set. This bit is only used to send packets to a low-speed device through a hub. To communicate to a full speed device, this bit is set to zero. For example, when SL811HS communicates to a low-speed device via the HUB:
  - SL811HS SIE should set to operate at 48 MHz, i.e., bit 5 of register 05H should be set = “0.”
  - Bit 6 of register 0FH should be set = “0,” set correct polarity of DATA+ and DATA– state for Full Speed.
  - Bit 7, Preamble Bit, should be set = “1” in Host Control register.
- When SL811HS communicates directly to low-speed device:
  - SL811HS. Bit 5 of register 05H should be set = “1.”
  - Bit 6 of register 0FH should be set = “1,” DATA+ and DATA– polarity for low speed.
  - The state of bit 7 is ignored in this mode.

5.2.3 Example of SL811HS USB Packet Transfer

SL811HS memory set-up as shown:

03h-04h Register will contain PID and Device endpoint and Device Address.

10h-FFh USB Data as required.

5.2.4 SOF Packet Generation

The SL811HS automatically computes CRC5 by hardware. No CRC or SOF is required to be generated by external firmware for SL811HS.

5.2.5 USB-A/USB-B Host Base Address [01H, 09H]

The USB-A/USB-B Base Address is a Pointer to the SL811HS memory buffer location for USB reads and writes. When transferring data OUT (Host to Device), the USB-A and USB-B can be set up prior to setting ARM on the USB-A or USB-B Host Control register. See the software implementation example.

5.2.6 USB-A/USB-B Host Base Length [02H, 0AH]

The USB A/B host base register contains the maximum packet size to be transferred between the SL811HS and a slave USB peripheral. Essentially, this designates the largest packet size that can be transferred by the SL811HS. Base Length designates the size of data packet to be sent. For example, in Bulk mode the maximum packet length is 64 bytes. In ISO mode, the maximum packet length is 1023, since the SL811HS only has an 8-bit length; the maximum packet size for the ISO mode using the SL811HS is 255 – 16 bytes. When the Host Base Length register is set to zero, a Zero-Length packet will be transferred.

5.2.7 USB-A/USB-B Host PID, Device Endpoint (Write)/USB Status (Read) [03H, 0BH]

This register has two modes. When read, this register provides packet status and it contains information relative to the last packet that has been received or transmitted. The register is defined as follows.

Bit Position	Bit Name	Function
0	ACK	Transmission Acknowledge
1	Error	Error detected in transmission
2	Time-out	Time-out occurred
3	Sequence	Sequence Bit. “0” if DATA0, “1” if DATA1
4	Setup	“1” indicates Setup Packet
5	Overflow	Overflow condition - maximum length exceeded during receives
6	NAK	Slave returns NAK
7	STALL	Slave set STALL bit

When written, this register provides the PID and Endpoint information to the USB SIE engine to be used in the next transaction. All sixteen Endpoints can be addressed by the SL811HS.

D7	D6	D5	D4	D3	D2	D1	D0
PID3	PID2	PID1	PID0	EP3	EP2	EP1	EP0

PID3-0 4-bit PID Field (See Table Below)

EP3-0 4-bit Endpoint Value in Binary.

PID TYPE	D7-D4
SETUP	1101 (D Hex)
IN	1001 (9 Hex)
OUT	0001 (1 Hex)
SOF	0101 (5 Hex)
PREAMBLE	1100 (C Hex)
NAK	1010 (A Hex)
STALL	1110 (E Hex)
DATA0	0011 (3 Hex)
DATA1	1011 (B Hex)

5.2.8 USB-A/USB-B Host Transfer Count Register (Read), USB Address (Write) [04H, 0CH]

This register has two functions. When read, this register contains the number of bytes left over (from “Length” field) after a packet is transferred. If an overflow condition occurs, i.e., the received packet from slave USB device was greater than the Length field specified, a bit is set in the Packet Status Register indicating the condition. When written, this register will contain the USB Device Address to which the Host wishes to communicate.

D7	D6	D5	D4	D3	D2	D1	D0
0	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA6-DA0 Device address, up to 127 devices can be addressed

DA7 Reserved bit should be set zero.

5.3 SL811HS Control Registers

Register Name SL11H and SL811H	SL11H (hex) Address	SL811HS (hex) Address
Control Register1	05H	05H
Interrupt Enable Register	06H	06 H
Reserved Register	07H	07 H
Status Register	0DH	0DH
SOF Counter LOW (Write)/HW Revision Register (Read)	0EH	0E H
SOF Counter HIGH and Control Register2	Reserved	0F H
Memory Buffer	10H-FFH	10H-FFH

5.3.1 Control Register 1, Address [05H]

The Control Register 05H enables/disables USB transfer operation with control bits defined as follows.

Bit	Bit Name	Function
0	SOF ena/dis	“1” enable auto Hardware SOF generation, “0”= disable
1	Reserved	
2	Reserved	
3	USB Engine Reset	USB Engine reset = “1.” Normal set “0”
4	J-K state force	See the table below
5	USB Speed	“0” set-up for full speed, “1” set-up LOW-SPEED
6	Suspend	“1” enable, “0” = disable
7	Reserved	

- At power-up this register will be cleared to all zeros.
- In the SL811HS, bit 0 is used to enable HW SOF auto-generation (bit 0 was not used in the SL11H).

5.3.2 J-K Programming States [bits 3 and 4 of Control Register 05H]

The J-K force state control and USB Engine Reset bits can be used to generate USB reset condition on the USB. Forcing K-state can be used for Peripheral device remote wake-up, Resume and other modes. These two bits are set to zero on power-up.

Bit 4	Bit 3	Function
0	0	Normal operating mode
0	1	Force USB Reset, D+ and D– are set LOW (SE0)
1	0	Force J-State, D+ set HIGH, D– set LOW[2]
1	1	Force K-State, D– set HIGH, D+ set LOW[3]

5.3.3 Low-speed/Full Speed Modes [bit 5 Control Register 05H]

The SL811HS is designed to communicate with either full or low-speed devices. At power-up bit 5 will be set LOW, i.e., for full speed. There are two cases when communicating with a low-speed device. When a low-speed device is connected directly to the SL811HS, bit 5 of Register 05H should be set to logic “1” and bit 6 of register 0FH, Output-Invert, needs to be set to “1” in order to change the polarity of D+ and D–. When a low-speed device is connected via a HUB to SL811HS, bit 5 of Register 05H should be set to logic “0” and bit 6 of register 0FH should be set to logic “0” in order to keep the polarity of D+ and D– for full speed. In addition, make sure that bit 7 of USB-A/USB-B Host Control Registers [00H, 08H] is set to “1.”

5.3.4 Low-power Modes [bit 6 Control Register 05H]

When bit-6 (Suspend) is set to “1,” the power of the transmit transceiver will be turned off, the internal RAM will be in the suspend mode, and the internal clocks will be disabled. **Note**. Any activity on the USB bus (i.e., K-State, etc.) will resume normal operation. To resume normal operation from the CPU side, a data Write cycle (i.e., A0 set HIGH for a data Write cycle) should be done.

5.3.5 Interrupt Enable Register, Address [06H]

The SL811HS provides an Interrupt Request Output, which can be activated on a number of conditions. The Interrupt Enable Register allows the user to select conditions that will result in an Interrupt being issued to an external CPU. A separate Interrupt Status Register is provided. It can be polled in order to determine those conditions that initiated the interrupt. (See Interrupt Status Register description.) When a bit is set to “1” the corresponding interrupt is enabled.

Bit Position	Bit Name	Function
0	USB-A	USB-A Done Interrupt
1	USB-B	USB-B Done Interrupt
2	Reserved	
3	Reserved	
4	SOF Timer	1 = Enable Interrupt on 1-ms SOF Timer
5	Inserted/Removed	Slave Insert/Remove Detection
6	Device Detect/Resume	Enable Device Detect/Resume Interrupt

- Bits 0–1 are used for the USB A/B controller interrupt.
- Bit 4 is used to enable/disable the SOF timer. To utilize this bit function, bit 0 of register 05H must be enabled and the SOF counter registers 0EH and 0FH must be initialized.
- Bit 5 is used to enable/disable the device inserted/removed interrupt.
- When bit-6 of register 05H is set = “1,” bit 6 of this register enables the Resume Detect Interrupt. Otherwise, this bit is used to enable Device detection status as defined in the Interrupt Status Register bit definitions.

Note:
2. Force K-State for low speed.
3. Force J-State for low speed.

5.3.6 USB Address Register, Reserved, Address [07H]

This register is reserved for the device USB Address in Slave operation. It should not be written by the user.

5.3.7 Interrupt Status Register, Address [0DH]

The ISR is a Read/Write register providing interrupt status. Interrupts can be cleared by writing to this register. To clear a specific interrupt, the register is written with corresponding bit set to “1.”

Bit Position	Bit Name	Function
0	USB-A	USB-A Done Interrupt
1	USB-B	USB-B Done Interrupt
2	Reserved	
3	Reserved	
4	SOF timer	1 = Interrupt on 1-ms SOF Timer
5	Insert/Remove	Slave Insert/Remove Detection
6	Device Detect/Resume	Device Detect/Resume Interrupt
7	D+	Value of the Data+ Pin

- Bit 5 is provided to support USB cable Insertion/Removal for the SL811HS in Host Mode. This bit is set when a transition from SE0 to IDLE (device inserted) or IDLE to SE0 (device removed) occurs on the bus.
- Bit 6 is shared between Device Detection status and Resume detection interrupt. When bit-6 of register 05H is set to one, this bit will be the Resume detection Interrupt bit. Otherwise, this bit is used to indicate the presence of a Device, “1” = device “Not present” and “0” = device “Present.” In this mode this bit should be checked along with bit 5 to determine whether a device has been inserted or removed.
- Bit 7 provides continuous USB Data+ line status. Once it has been determined that a device has been inserted as described above with bits 5 and 6, bit 7 can be used to detect if the inserted device is low- or full-speed.

5.3.8 Current Data Set Register/Hardware Revision/SOF Counter LOW, Address [0EH]

- This register has two modes: a Read from this register indicates the current SL811HS silicon revision.

Bit Position	Bit Name	Function
0	Reserved	Reserved for slave
1	Reserved	Reserved for slave
2	Reserved	Read will be zero
3	Reserved	Read will be zero
4–7	HW Revision	SL11H Read = 0H, SL811HS rev1.2 Read = 1H, SL811HS rev1.5 Read = 2

- Writing to this register will set up auto generation of SOF to all connected peripherals. This counter is based on the 12-MHz clock. To set up a 1-ms timer interval, the software must set up both SOF counter registers to the proper values.

Bit Position	Bit Name	Function
0–7	SOF LOW Counter Register	Write-only to set SOF LOW Counter Register, OEH

- **Example**. To set up SOF for 1-ms interval, SOF counter register 0EH should be set to E0H.

5.3.9 SOF Counter HIGH/Control2 Register, Address [0FH, READ/WRITE]

When writing to this register the bits definition are defined as follows.

Bit Position	Bit Name	Function
0–5	SOF HIGH Counter Register	Write a value or read it back to SOF HIGH Counter Register
6	SL811HS D+/D– Data Polarity Swap	Write/Read, set “1” change polarity, “0” no change of polarity
7	SL811HS Master/Slave selection	Write/Read, “1” is master, else Slave

Note. Any Write to control register 0FH will enable the SL811HS full features bit. This is an internal bit of the SL811HS which enables additional features not supported by the SL11H. For SL11H hardware backward compatibility, this register should not be accessed.

The USB-B register set can be used when SL811HS full feature bit is enabled. **Example**. To set up for 1-ms SOF time:

The register 0FH contains the upper 6 bits of the SOF timer. Register 0EH contains the lower 8 bits of the SOF timer. The timer is based on a 12-MHz clock and uses a counter, which counts down to zero from an initial value. To set the timer for 1 ms time, the register 0EH should be loaded with value E0H, register 0F, Bits 0–5 should be loaded with 2EH. To start the timer, bit 0 of register 05H should be set to “1.” To load both HIGH and LOW registers with the proper values the user must follow this sequence:

- Write E0H to register 0EH.
- Write 2EH to register 0FH, bits 0–5. Bits 6 and 7 should be set for appropriate function: polarity and Master/Slave.
- Enable bit 0 in register 05H.

Note. Any Write to the 0FH register will clear the internal frame counter. Register 0FH must be written at least once after power-up. The internal frame counter is incremented after every SOF timer tick. The internal frame counter is an 11-bit counter, which is used to track the frame number. The frame number is incremented after each timer tick. Its contents are transmitted to the slave every millisecond in a SOF packet.

D7	D6	D5	D4	D3	D2	D1	D0
C13	C12	C11	C10	C9	C8	C7	C6

C13–C6 Top 8 bits of 14-bit SOF counter.

When read, this register will return the value of the SOF counter divided by 64. The software should use this register to determine the available bandwidth in the current frame before initiating any USB transfer. In this way, the user will be able to avoid babble conditions on the USB. For example, to determine the available bandwidth left in a frame:

Maximum number of clock ticks in 1-ms time frame is 12000(1 count per 12-MHz clock period, or approximately 84 ns.) The value read back in Register 0FH is the (count × 64) × 84 ns = time remaining in current frame. USB bit time = one 12-MHz period.

Value of register 0FH	Available bit times left are between
BBH	12000 bits to 11968 (187 × 64) bits
BAH	11968 bits to 11904 (186 × 64) bits

6.0 SL811HS and SL811HST-AC Physical Connections

This part is offered in both a 28-pin PLCC package (SL811HS) and a 48-pin TQFP package (SL811HST-AC).

6.1 SL811HS Physical Connections

6.1.1 SL811HS Pin Layout

Pins 2 and 3 should be No Connect in Host Mode. See Pin and Signal Description.

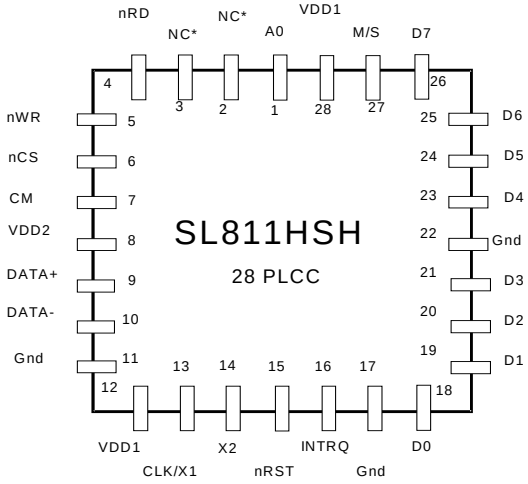
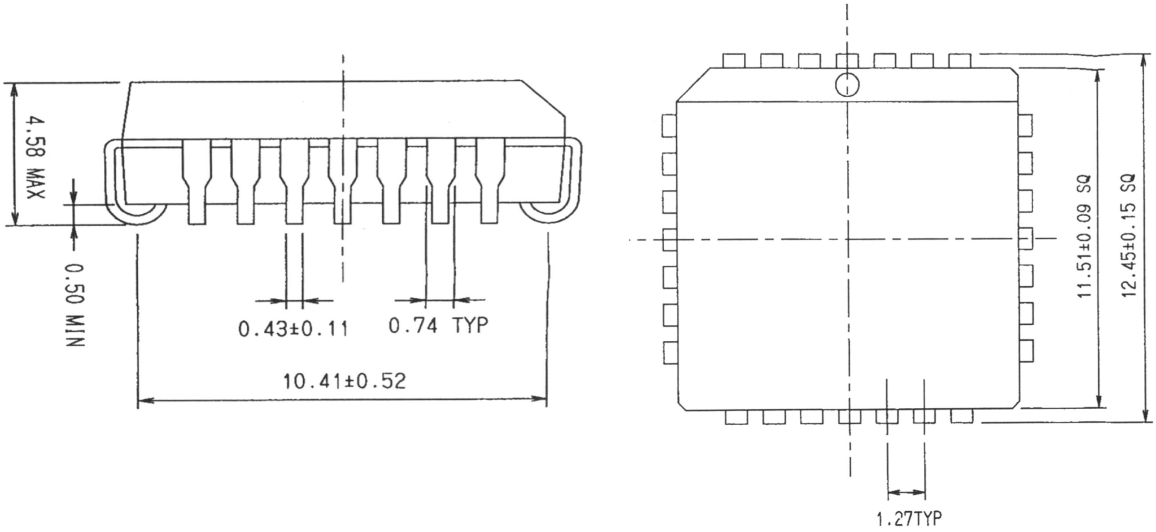


Figure 6-1. SL811HS USB Host/Slave Controller—Pin Layout

6.1.2 28-Pin PLCC Mechanical Dimensions



6.1.3 SL811HS USB Host Controller Pins Description

The SL811HS package is a 28-pin PLCC. The device requires 3.3 VDC. Average typical current consumption is less then 20 mA for 3.3V.

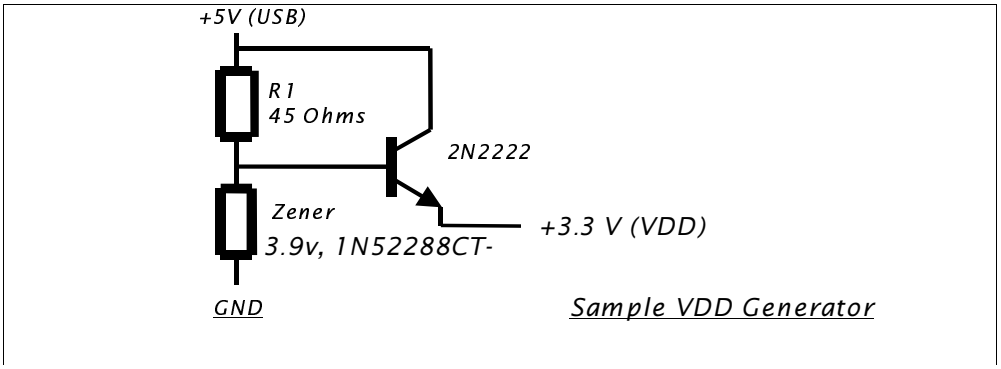
Table 6-1. SL811HS Pin Assignments and Definitions

Pin No.	Pin Type	Pin Name	Pin Description
1	IN	A0	**A0 = "0." Selects Address Pointer**. Reg. Write Only. Selects Data Buffer or Register. R/W.[4]
2	IN	nDACK	**DMA Acknowledge**. An active LOW input used to interface to an external DMA controller. This works only in slave mode. In host mode, pin should be tied to Logic "1" in Host Mode.
3	OUT	nDRQ	**DMA Request**. An active LOW output used with an external DMA controller. nDRQ and nDACK form the handshake for DMA data transfers. In host mode, pin must be left unconnected in Host Mode.
4	IN	nRD	**Read Strobe Input**. An active LOW input used with nCS to Read registers/data memory.
5	IN	nWR	**Write Strobe Input**. An active LOW input used with nCS to Write to registers/data memory.
6	IN	nCS	**Active LOW Chip Select**. Used with nRD and nWD when accessing SL811HS.
7	IN	CM	**Clock Mode**. Select Internal 4 X Clock Multiplier. "1" enables 4X clock multiplier. "0" Disables.[5]
8	VDD1	+3.3 VDC	Power for USB Transceivers
9	BIDIR	DATA +	USB Differential Data Signal HIGH Side
10	BIDIR	DATA -	USB Differential Data Signal LOW Side
11	GND	USB GND	Ground Connection for USB
12	VDD	+3.3 VDC	SL811HS Device V_{DD} Power[6]
13	IN	CLK/X1	12-/48-MHz Clock or External Crystal X1 Connection[7]
14	OUT	X2	External Crystal X2 Connection
15	IN	nRST	SL811HS Device Active LOW Reset Input
16	OUT	INTRQ	Active HIGH Interrupt Request Output to External Controller
17	GND	GND	SL811HS Device Ground
18	BIDIR	D0	Data 0. Microprocessor Data/(Address) Bus
19	BIDIR	D1	Data 1. Microprocessor Data/(Address) Bus
20	BIDIR	D2	Data 2. Microprocessor Data/(Address) Bus
21	BIDIR	D3	Data 3. Microprocessor Data/(Address) Bus
22	GND	GND	SL811HS Device Ground
23	BIDIR	D4	Data 4. Microprocessor Data/(Address) Bus
24	BIDIR	D5	Data 5. Microprocessor Data/(Address) Bus
25	BIDIR	D6	Data 6. Microprocessor Data/(Address) Bus
26	BIDIR	D7	Data 7. Microprocessor Data/(Address) Bus
27	IN	M/S	Master/Slave Select. Host = "0," Slave = "1"
28	VDD	+3.3 VDC	SL811HS Device V_{DD} Power

Notes:

4. The A0 Address bit is used to access address or data registers in I/O-mapped or memory-mapped applications.
5. The CM Clock Multiplier pin should be tied HIGH for a 12-MHz clock source and tied to ground for a 48-MHz clock source. In SL11H, this pin was designated as an ALE input pin.
6. V_{DD} can be derived from the USB supply. The diagram below shows a simple method to provide 3.3V/30 mA. Another option is to use a Torex Semiconductor, Ltd. 3.3V SMD regulator (part number XC62HR3302MR).
7. The X1/X2 clock requires external 12- or 48-MHz matching crystal or clock source.

The Diagram below illustrates a simple +3.3V voltage source.



6.1.4 Package Markings (SL811HS)

YYWW = Date code

XXXX = Product code

X.X = Silicon revision number

6.2 SL811HST-AC Physical Connections

6.2.1 SL811HST-AC Pin Layout

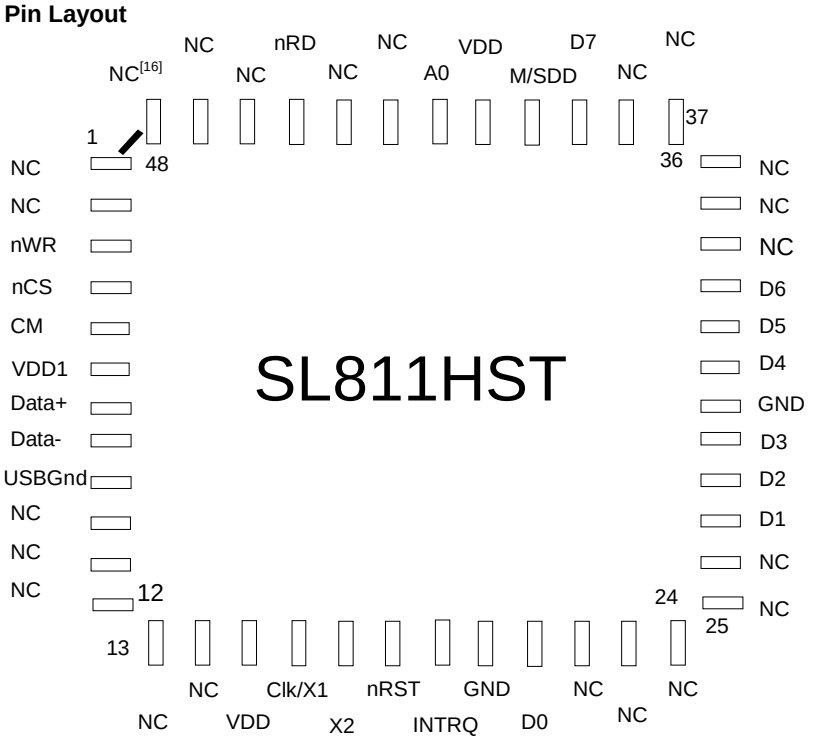
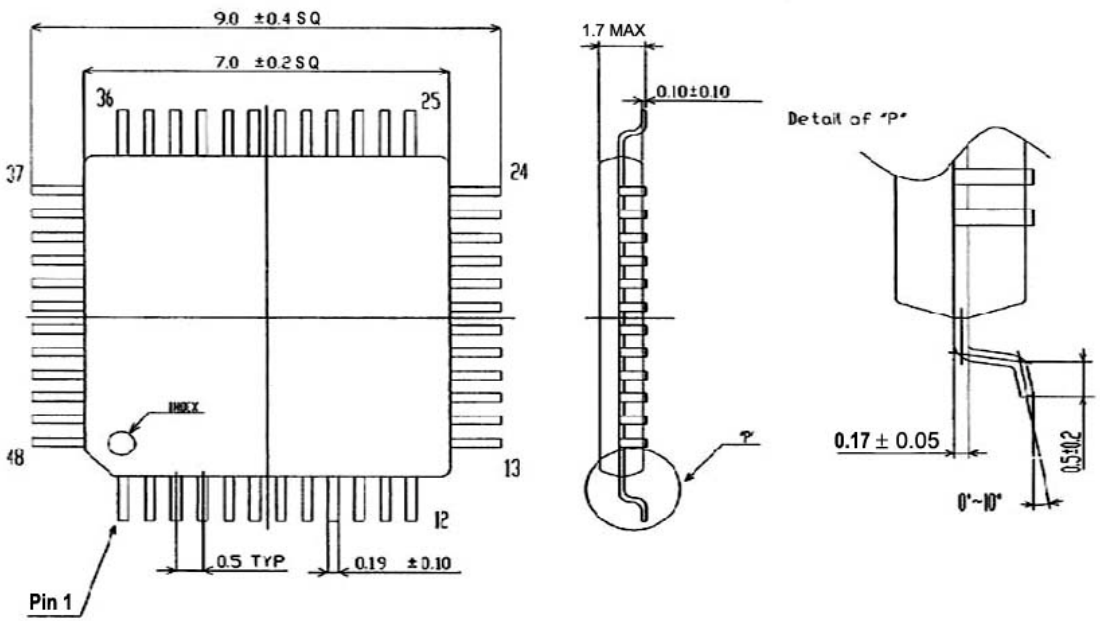


Figure 6-2. SL811HST-AC USB Host/Slave Controller Pin Layout

6.2.2 Mechanical Dimensions 48-Pin TQFP



Note:

8. NC. Indicates No Connection. NC Pins should be left unconnected.

6.2.3 SL811HST-AC USB Host Controller Pins Description

The SL811HST-AC is packaged in a 48-pin TQFP. The device requires a 3.3VDC power source. The SL811HST-AC requires an external 12 or 48 MHz crystal or Clock.

Table 6-2. SL811HST-AC Pin Assignments and Definitions

Pin No.	Pin Type	Pin Name	Pin Description
1	NC	NC	NC
2	NC	NC	NC
3	IN	nWR	**Write Strobe Input**. An active LOW input used with nCS to Write to registers/data memory.
4	IN	nCS	**Active LOW SL811HST-AC Chip select**. Used with nRD and nWr when accessing SL811HT.
5	IN	CM	**Clock Mode**. Select 12-MHz/48-MHz Clock Source.[9]
6	VDD1	+3.3 VDC	**Power for USB Transceivers**. V_{DD1} may be connected to V_{DD}.
7	BIDIR	DATA +	USB Differential Data Signal HIGH Side
8	BIDIR	DATA -	USB Differential Data Signal LOW Side
9	GND	USB GND	Ground Connection for USB
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	NC	NC	NC
14	NC	NC	NC
15	VDD	+3.3 VDC	SL811HST-AC Device V_{DD} Power[10]
16	IN	CLK/X1	Clock or External Crystal X1 connection[11]
17	OUT	X2	External Crystal X2 connection
18	IN	NRST	SL811HST-AC Device active low reset input
19	OUT	INTRQ	Active HIGH Interrupt Request output to external controller
20	GND	GND	SL811HST-AC Device Ground
21	BIDIR	D0	**Data 0**. Microprocessor Data/(Address) Bus.
22	NC	NC	NC
23	NC	NC	NC
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	BIDIR	D1	**Data 1**. Microprocessor Data/(Address) Bus.
28	BIDIR	D2	**Data 2**. Microprocessor Data/(Address) Bus.
29	BIDIR	D3	**Data 3**. Microprocessor Data/(Address) Bus.
30	GND	GND	SL811HST-AC Device Ground
31	BIDIR	D4	**Data 4**. Microprocessor Data/(Address) Bus.
32	BIDIR	D5	**Data 5**. Microprocessor Data/(Address) Bus.

Notes:

9. The CM Clock Multiplier pin should be tied HIGH for a 12-MHz clock source and tied to ground for a 48-MHz clock source. In SL11H, this pin was designated as ALE input pin.
10. VDD can be derived from the USB supply. See diagram.
11. The X1/X2 Clock requires external 12- or 48-MHz matching crystal or clock source.

Table 6-2. SL811HST-AC Pin Assignments and Definitions (continued)

Pin No.	Pin Type	Pin Name	Pin Description
33	BIDIR	D6	**Data 6**. Microprocessor Data/(Address) Bus.
34	NC	NC	NC
35	NC	NC	NC
36	NC	NC	NC
37	NC	NC	NC
38	NC	NC	NC
39	BIDIR	D7	**Data 7**. Microprocessor Data/(Address) Bus.
40	IN	M/S	**Master/Slave Mode Select**. “1” selects Slave. “0” = Master.
41	VDD	+3.3 VDC	SL811HST-AC Device V_{DD} Power.
42	IN	A0	**A0 = “0.”** Selects address pointer. Reg.A0 = “1.” Selects data buffer or register.[12]
43	IN	nDACK	**DMA Acknowledge**. An active LOW input used to interface to an external DMA controller. DMA is enabled only in slave mode. In host mode, pin should be tied HIGH (logic “1”) .
44	OUT	nDRQ	**DMA Request**. An active LOW output used with an external DMA controller. nDRQ and nDACK form the handshake for DMA data transfers. In host mode, pin must be left unconnected .
45	IN	NRD	**Read Strobe Input**. An active LOW input used with nCS to Read registers/data memory.
46	NC	NC	NC
47	NC	NC	NC
48	NC	NC	NC

Notes:
12. The A0 Address bit is used to access address register or data registers in I/O Mapped or Memory Mapped applications.

6.2.4 Package Markings (SL811HST-AC)



YYWW = Date code

XXXX = Product code

X.X = Silicon revision number

7.0 Electrical Specifications

7.1 Absolute Maximum Ratings

This section lists the absolute maximum ratings of the SL811HS. Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can affect device operation and reliability.

Storage Temperature	–40°C to 125°C
Voltage on any pin with respect to ground	–0.3V to 6.0V
Power Supply Voltage (V_{DD})	4.0 V
Power Supply Voltage (V_{DD1})	4.0 V
Lead Temperature (10 seconds)	180°C

7.2 Recommended Operating Condition

Parameter	Min.	Typical	Max.
Power Supply Voltage, VDD	3.0V	3.3 V	3.45V
Power Supply Voltage, VDD1	3.0V		3.45V
Operating Temperature	0°C		65°C

Crystal Requirements, (X1, X2)	Min.	Typical	Max.
Operating Temperature Range	0°C		65°C
Parallel Resonant Frequency[13]		48 MHz	
Frequency Drift over Temperature			±50 ppm
Accuracy of Adjustment			±30 ppm
Series Resistance			100 ohms
Shunt Capacitance	3 pF		6 pF
Load Capacitance		20 pF	
Drive Level	20 µW		5 mW
Mode of Vibration Third Overtone[14]			

7.3 External Clock Input Characteristics (X1)

Parameter	Min.	Typical	Max.
Clock Input Voltage @ X1 (X2 Open)	1.5 V		
Clock Frequency[15]		48 MHz	

Notes:

13. The SL811HS can use a 12-MHz Crystal Oscillator or 12-MHz Clock Source.
14. Fundamental mode for 12-MHz Crystal.
15. The SL811HS can use a 12-MHz Clock Source.

7.4 DC Characteristics

Parameter	Description	Min.	Typ.	Max.
V_{IL}	Input Voltage LOW	–0.3 V		0.8V
V_{IH}	Input Voltage HIGH (5V Tolerant I/O)	2.0 V		6.0V
V_{OL}	Output Voltage LOW (I_{OL} = 4 mA)			0.4V
V_{OH}	Output Voltage HIGH (I_{OH} = –4 mA)	2.4 V		
I_{OH}	Output Current HIGH	4 mA		
I_{OL}	Output Current LOW	4 mA		
I_{LL}	Input Leakage			±1 µA
C_{IN}	Input Capacitance			10 pF
I_{CC}[16]	Supply Current (V_{DD}) inc USB @FS		21 mA	25 mA
I_{CCsus1}[17]	Supply Current (V_{DD}) Suspend w/Clk & Pll Enb		4.2 mA	5 mA
I_{CCsus2}[18]	Supply Current (V_{DD}) Suspend no Clk & Pll Dis		50 µA	60 µA
I_{USB}	Supply Current (V_{DD1})			10 mA
I_{USBSUS}	Transceiver Supply Current in Suspend			10 µA

7.5 USB Host Transceiver Characteristics

Parameter	Description	Min.	Typ.[19]	Max.
V_{IHYS}	Differential Input Sensitivity (Data+, Data–)	0.2V		200 mV
V_{USBIH}	USB Input Voltage HIGH Driven	2.0		
V_{USBIL}	USB Input Voltage LOW	0.8V		
V_{USBOH}	USB Output Voltage HIGH	2.0V		
V_{USBOL}	USB Output Voltage LOW	0.0V		0.3 V
Z_{USBH}[20]	Output Impedance HIGH STATE	36 Ohms		42 Ohms
Z_{USBL}[20]	Output Impedance LOW STATE	36 Ohms		42 Ohms
I_{USB}	Transceiver Supply p-p Current (3.3V)			10 mA @ FS

Every V_{DD} pin, including USB V_{DD}, has to have a decoupling capacitor to ensure clean V_{DD} (free of high-frequency noise) at the chip input point (pin) itself.

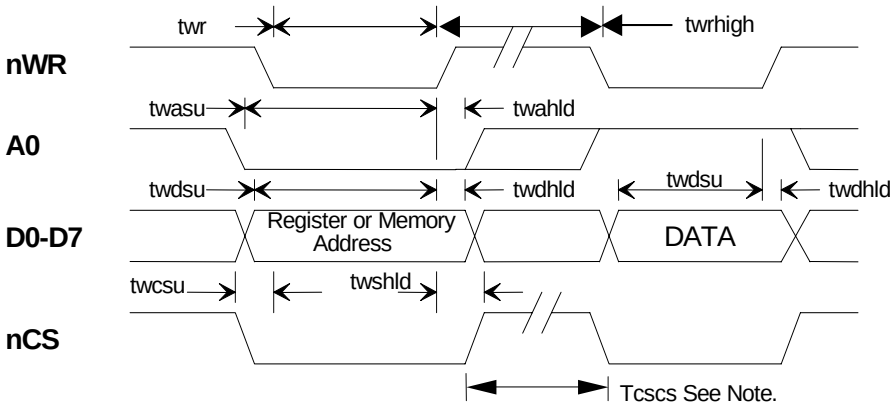
The best way to do this is to connect a ceramic capacitor (0.1 µF, 6V) between the pin itself and a good ground. Capacitor leads must be kept as short as possible. Use surface mount capacitors with the shortest traces possible (the use of a ground plane is strongly recommended).

Notes:

16. I_{CC} measurement includes USB Transceiver current (I_{USB}) operating at Full Speed.
17. I_{CCsus1} measured with 12-MHz Clock Input and Internal PLL enabled. Suspend set –(USB transceiver and internal Clocking disabled).
18. I_{CCsus2} measured with external Clock, PLL disabled, and Suspend set. For absolute minimum current consumption, ensure that all inputs to the device are at static logic level.
19. All typical values are V_{DD} = 3.3V and T_{AMB}= 25°C.
20. Z_{USBX} impedance values includes an external resistor of 24 Ohms ± 1% (SL811HS revision 1.2 requires external resistor values of 33 Ohms ±1%).

7.6 Bus Interface Timing Requirements

7.6.1 I/O Write Cycle



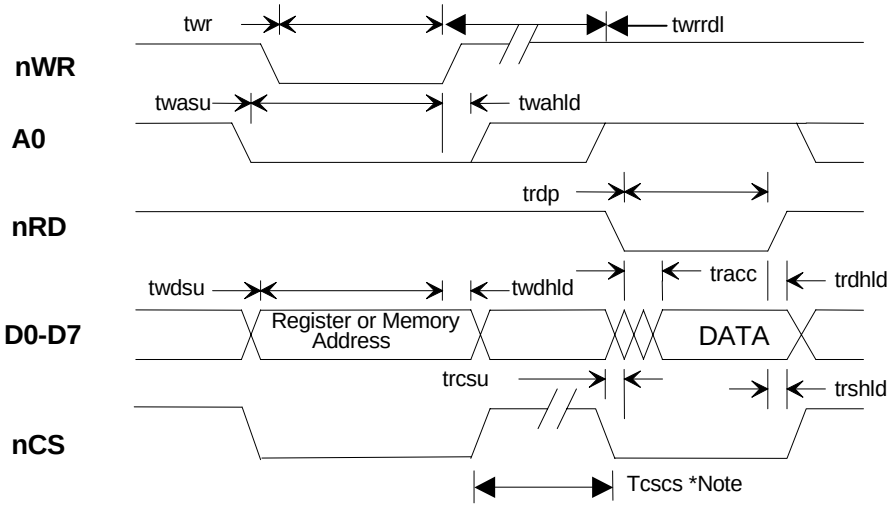
I/O Write Cycle to Register or Memory Buffer

Note: nCS an be held LOW for multiple Write cycles provided nWR is cycled.

Parameter	Description	Min.	Typ.	Max.
t_{WR}	Write pulse width	65 ns		
t_{WCSU}	Chip select set-up to nWR LOW	0 ns		
t_{WSHLD}	Chip select hold time After nWR HIGH	0 ns		
t_{WASU}	A0 address set-up time	65 ns		
t_{WAHLD}	A0 address hold time	10 ns		
t_{WDSU}	Data to Write HIGH set-up time	60 ns		
t_{WDHLD}	Data hold time after Write HIGH	5 ns		
t_{CSCS}	nCS inactive to nCS* asserted	85 ns		
t_{WRHIGH}	NWR HIGH	85 ns		

Write Cycle Time for Auto Inc Mode Writes is 150 ns minimum.

7.6.2 I/O Read Cycle



I/O Read Cycle from Register or Memory Buffer

Parameter	Description	Min.	Typ.	Max.
t_{WR}	Write pulse width	65 ns		
t_{RD}	Read pulse width	65 ns		
t_{WCSU}	Chip select set-up to nWR	0 ns		
t_{WASU}	A0 address set-up time	65 ns		
t_{WAHLD}	A0 address hold time	10 ns		
t_{WDSU}	Data to Write HIGH set-up time	60 ns		
t_{WDHLD}	Data hold time after Write HIGH	5 ns		
t_{RACC}	Data valid after Read LOW	20 ns		25 ns
t_{RDHLD}	Data hold after Read HIGH	5 ns		
t_{RCSU}	Chip select LOW to Read LOW	0 ns		
t_{RSHLD}	NCS hold after Read HIGH	0 ns		
T_{CSCS}*	nCS inactive to nCS *asserted	85 ns		
t_{WRRDL}	nWR HIGH to nRD LOW	85ns		

Note. NCS can be kept LOW during multiple Read cycles provided nRD is cycled. Rd Cycle Time for Auto Inc Mode Reads is 150 ns minimum.

7.6.3 Reset Timing

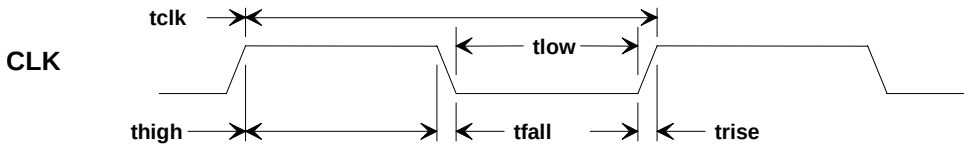


RESET TIMING

Parameter	Description	Min.	Typ.	Max.
t_{RESET}	nRst Pulse width	16 clocks		
t_{IOACT}	nRst HIGH to nRD or nWR active	16 clocks		

Note. Clock is 48-MHz nominal.

7.6.4 Clock Timing Specifications

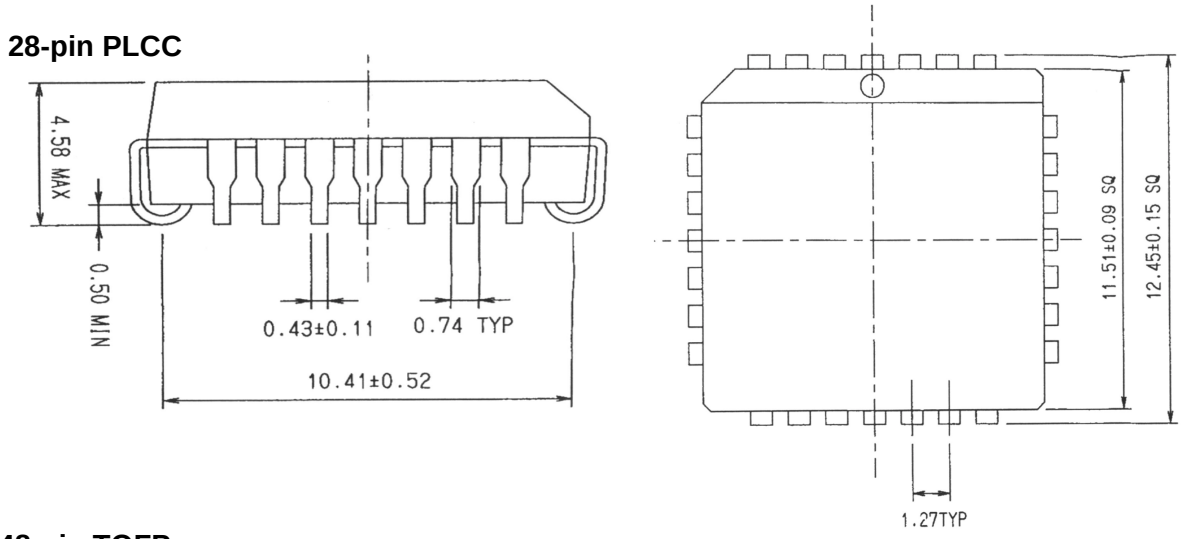


CLOCK TIMING

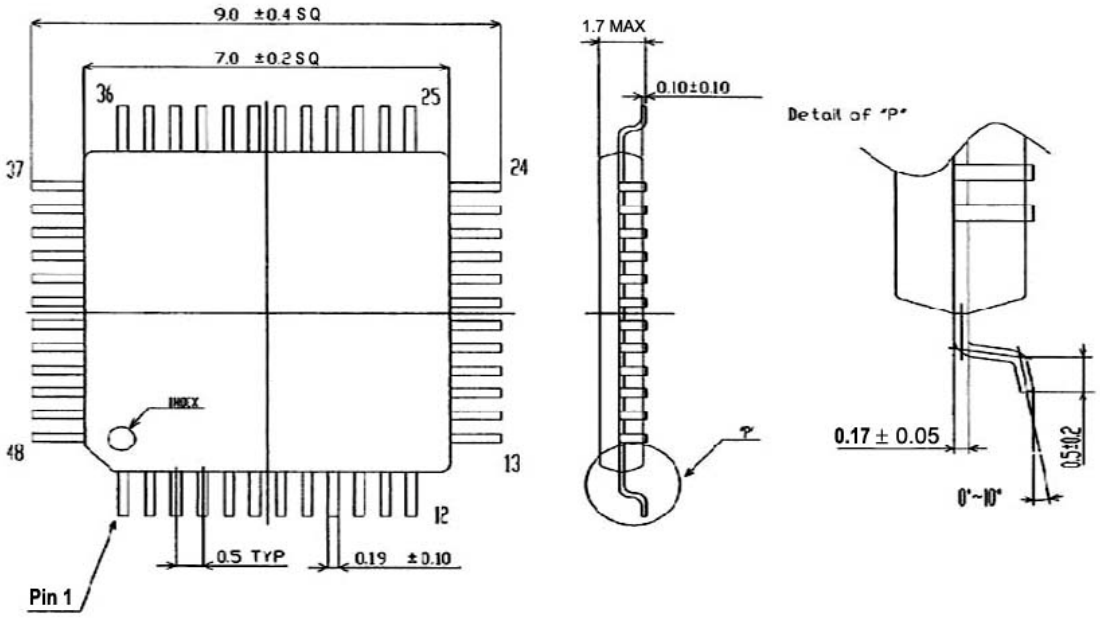
Parameter	Description	Min.	Typ.	Max.
t_{CLK}	Clock Period (48 MHz)	20.0 ns	20.8 ns	
t_{HIGH}	Clock HIGH Time	9 ns		11 ns
t_{LOW}	Clock LOW Time	9 ns		11 ns
t_{RISE}	Clock rise Time			5.0 ns
t_{FALL}	Clock fall Time			5.0 ns
	Clock Duty Cycle	45%		55%

8.0 Package Diagrams

28-pin PLCC



48-pin TQFP



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Document Title: SL811HS USB Host/Slave Controllers Hardware Specification Document Number: 38-08008				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110850	12/14/01	BHA	Converted to Cypress format from ScanLogic
*A	112687	03/22/02	MUL	1) Changed power supply voltage to 4.0V in section 7.1 2) Changed value of twdsu in section 7.6.2 3) Changed max. power supply voltage to 3.45 V in section 7.2 4) Changed accuracy of adjustment in section 7.2 5) Changed bits 0 and 1 to reserved in section 5.3.8 6) Changed bit 2 to reserved in section 5.3.5 and 5.3.7 7) Changed bit 2 to reserved in section 5.3.1 8) Changed definition of bit 6 in section 5.3.5 & 5.3.7 9) Added section 5.1, Register Values on Power-up and Reset 10) Changed bit description notes in section 5.3.7 11) Changed note about series termination resistors in section 7.5 12) Changed example in section 5.3.9 13) Changed J-K Programming States table in section 5.3.2 14) Added and removed comments for low-power modes in section 5.3.4 15) Removed sections specific to slave operation and SL11H 16) Removed duplicate tables 17) General formatting changes to section headings 18) Fixed all part number references 19) Added comments to section 7.5 and new definitions to section 2.0