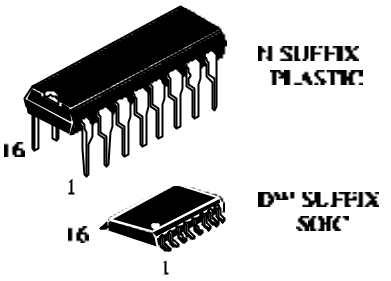
Presettable Up/Down Counter

High-Voltage Silicon-Gate CMOS



ORDERING INFORMATION
SL4029BN Plastic
SL4029BDW SOIC
T_A = -55° to 125° C for all packages

The SL4029B consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consists of a single CLOCK, CARRY IN,(CLOCK ENABLE), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a CARRY OUT signal are provided as outputs.

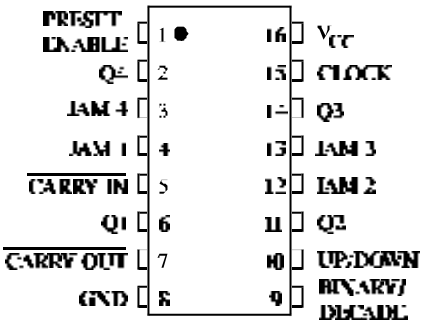
A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY IN or PRESET ENABLE signals are high. The CARRY OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY IN signal is low. The CARRY IN signal in the low state can thus be considered a CLOCK ENABLE. The CARRY IN terminal must be connected to GND when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts up when the UP/DOWN input is high, and down when the UP/DOWN input is low.

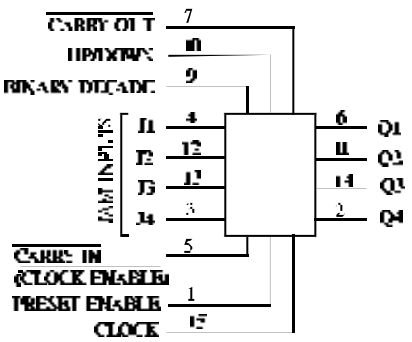
Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10.0 V supply
  2.5 V min @ 15.0 V supply

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16=V_{CC}
PIN 8= GND

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125 °C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}= 0.5 V or V_{CC} - 0.5V	5.0	3.5	3.5	3.5	V
		V_{OUT}= 1.0 V or V_{CC} - 1.0 V	10	7	7	7	
		V_{OUT}= 1.5 V or V_{CC} - 1.5V	15	11	11	11	
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}= 0.5 V or V_{CC} - 0.5V	5.0	1.5	1.5	1.5	V
		V_{OUT}= 1.0 V or V_{CC} - 1.0 V	10	3	3	3	
		V_{OUT}= 1.5 V or V_{CC} - 1.5V	15	4	4	4	
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0	5	5	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC}					mA
		U_{OL}=0.4 V	5.0	0.64	0.51	0.36	
		U_{OL}=0.5 V	10	1.6	1.3	0.9	
		U_{OL}=1.5 V	15	4.2	3.4	2.4	
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC}					mA
		U_{OH}=2.5 V	5.0	-2	-1.6	-1.15	
		U_{OH}=4.6 V	5.0	-0.64	-0.51	-0.36	
		U_{OH}=9.5 V	10	-1.6	-1.3	-0.9	
		U_{OH}=13.5 V	15	-4.2	-3.4	-2.4	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=200kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
t_{max}	Maximum Clock Frequency (Figure 1)	5.0 10 15	2 4 5.5	2 4 5.5	1 2 2.75	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q (Figure 1)	5.0 10 15	500 240 180	500 240 180	1000 480 360	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Carry Output (Figure 1)	5.0 10 15	560 260 190	560 260 190	1120 520 380	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset Enable to Q (Figure 1)	5.0 10 15	470 200 160	470 200 160	940 400 320	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset Enable to Carry Output (Figure 1)	5.0 10 15	640 290 210	640 290 210	1280 580 420	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Carry Input to Carry Output (Figure 1)	5.0 10 15	340 140 100	340 140 100	680 280 200	ns
t_{THL}, t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

FUNCTION TABLE

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	H L	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	H L	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	H L	JAM IN NO JAM
$\overline{\text{CARRY IN (CI)}}$ (CLOCK ENABLE)	H L	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION ADVANCE COUNTER AT POS. CLOCK TRANSITION

TIMING REQUIREMENTS (C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	25°C	≤125°C	Unit
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	180 90 60	180 90 60	360 180 120	ns
t_w	Minimum Pulse Width, Preset Enable (Figure 1)	5.0 10 15	130 70 50	130 70 50	260 140 100	ns
t_{su}*	Minimum Setup Time, Clock to B/D or U/D (Figure 1)	5.0 10 15	340 140 100	340 140 100	680 280 200	ns
t_{rem}*	Minimum Removal Time, Preset Enable (Figure 1)	5.0 10 15	200 110 80	200 110 80	400 220 160	ns
t_h**	Minimum Hold Time, Clock to Carry In (Figure 2)	5.0 10 15	50 30 25	50 30 25	100 60 50	ns
t_{su}	Minimum Setup Time, Carry In to Clock (Figure 1)	5.0 10 15	200 70 60	200 70 60	400 140 120	ns
t_r, t_f**	Maximum Input Rise and Fall Times,Clock (Figure 2)	5.0 10 15	15 15 15	15 15 15	30 30 30	μs

* From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.
** From Carry In to Clock Edge

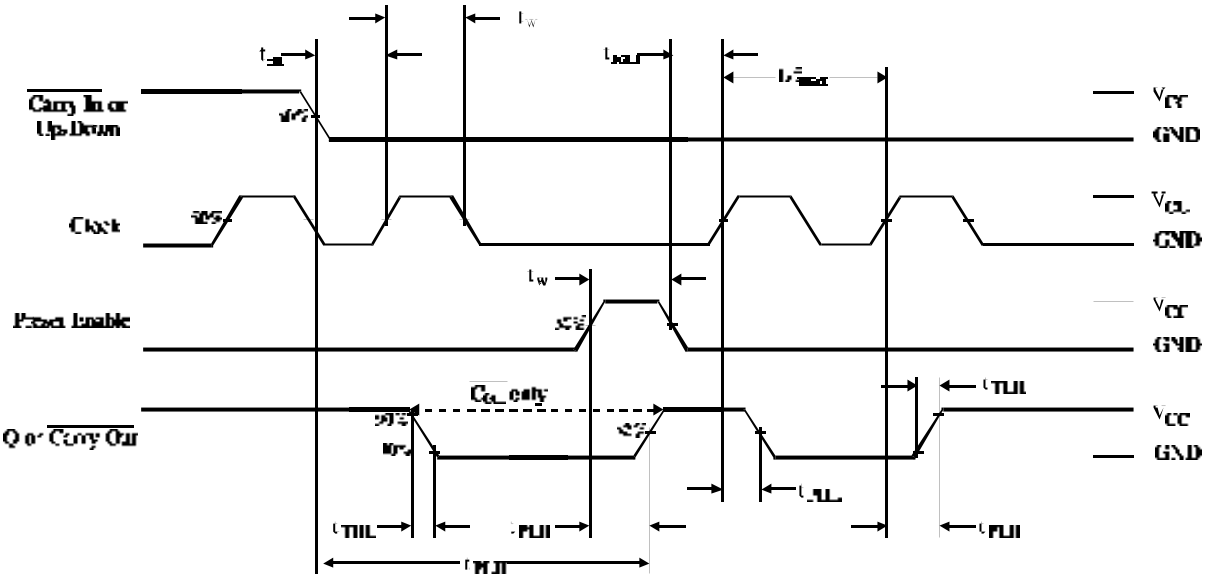


Figure 1. Switching Waveforms

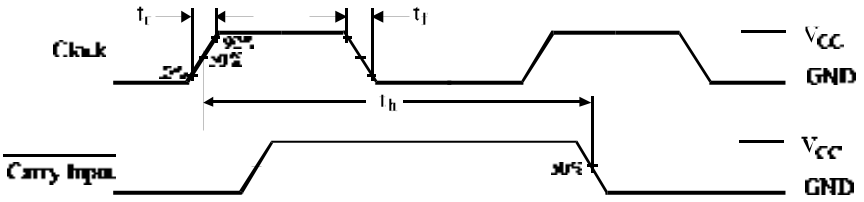
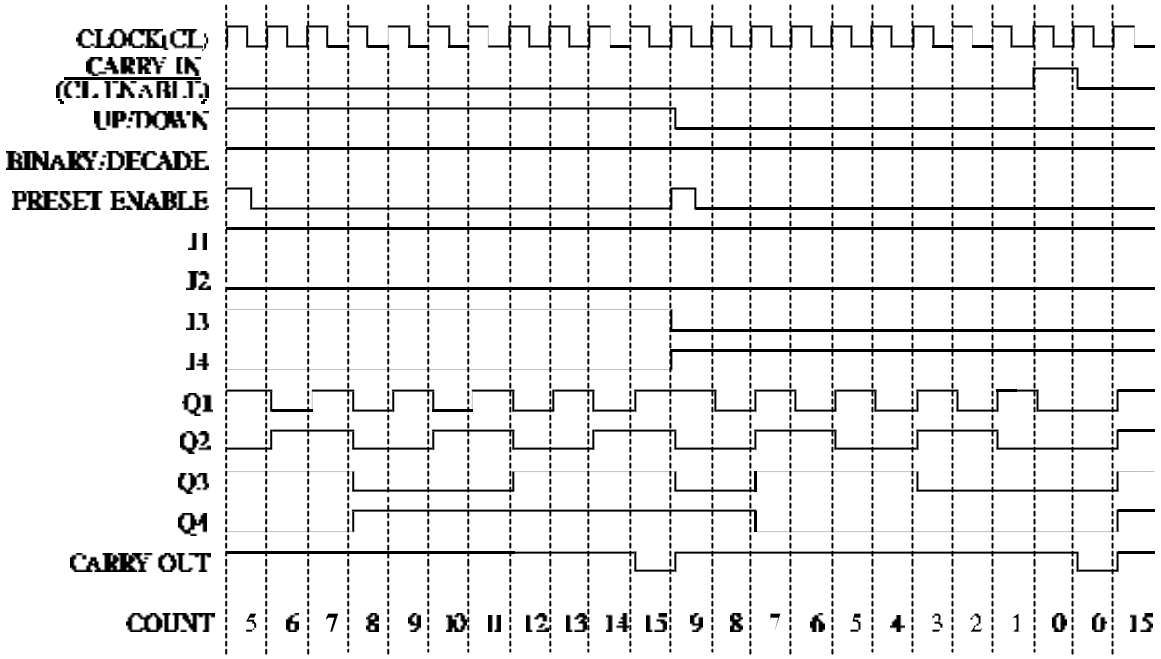
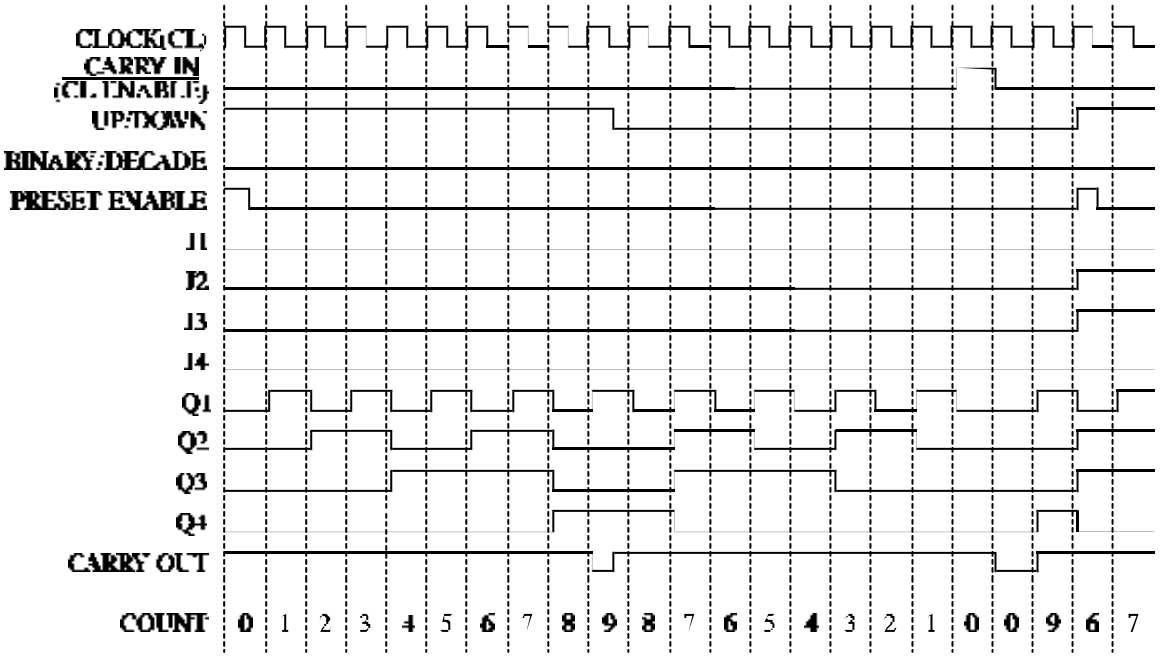


Figure 2. Switching Waveforms

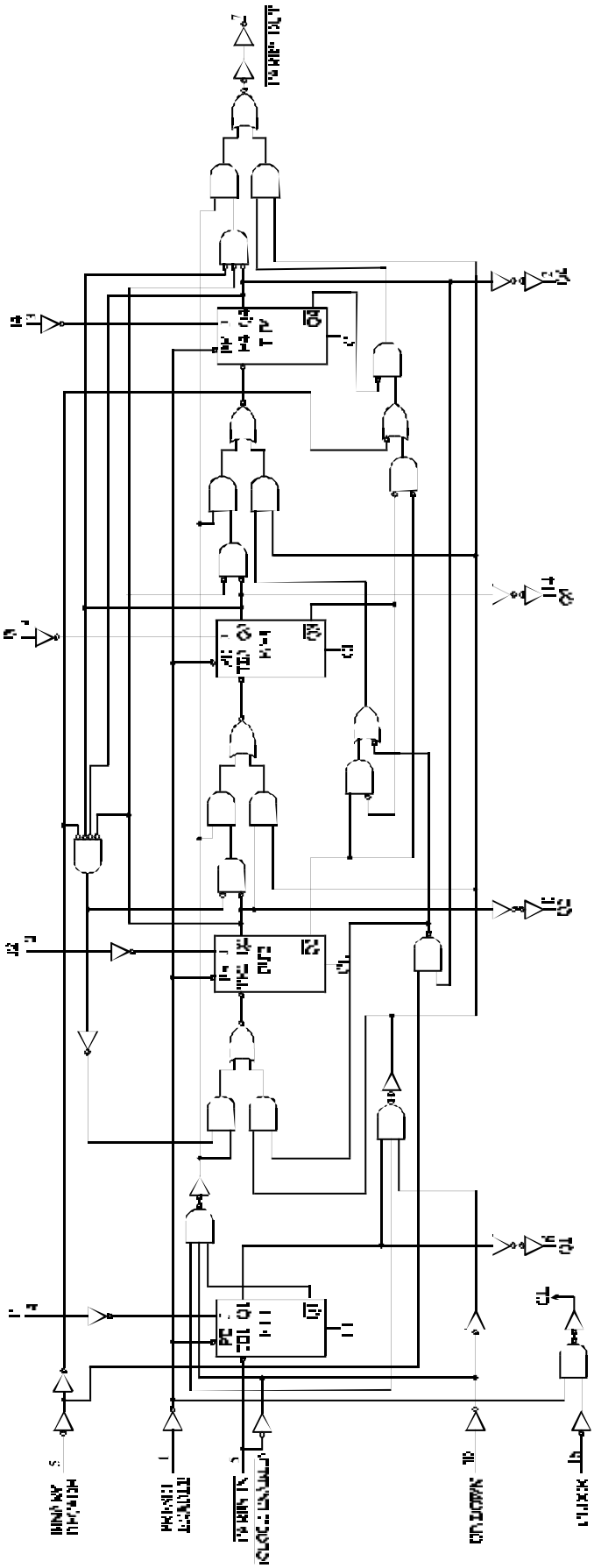
TIMING DIAGRAM; binary mode; J1=HIGH; J2=LOW; BIN/DEC=HIGH



TIMING DIAGRAM; decade mode; J1=LOW; J4=LOW; BIN/DEC=LOW



EXPANDED LOGIC DIAGRAM



TRUTH TABLE

CLOCK	TE	PE	J	Q	$\overline{Q}$
X	X	L	L	L	H
↓	L	H	X	Q	Q
X	X	L	H	H	L
↓	H	H	X	Q	$\overline{Q}$ NC
↑	X	H	X	Q	$\overline{Q}$ NC

