SL2 ICS53

Wafer addendum

Rev. 3.0 — 21 March 2007
135830

Product data sheet
PUBLIC

1. General description

This specification describes the electrical, physical and dimensional properties of Au-bumped sawn wafers on FFC of I•CODE SLI-S Label ICs on an NXP C075EE process and is the base for delivery of tested I•CODE SLI-S Label ICs.

2. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Ordering Code
SL2 ICS5301EW/V7		bumped sawn wafer on UV-tape	9352 837 46005

3. Mechanical specification

3.1 Wafer

- Diameter: 8”
- Thickness: 150 μm ± 15 μm

3.2 Wafer backside

- Material: Si
- Treatment: ground + stress releave
- Roughness: R_a max. 0.5 μm

  R_t max. 5 μm

3.3 Chip dimensions

- Chip size: 940 x 900μm^2
- Scribe lines: 50 / 50 μm

3.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride (on top)
- Thickness: 500 nm / 600 nm

3.5 Au bump

- Bump material: > 99.9 % pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 μm
- Bump height uniformity:
  - within a die: ± 2 μm
  - within a wafer: ± 3 μm
  - wafer to wafer: ± 4 μm
- Bump flatness: ± 1.5 μm
- Bump size:
  - LA, LB: 60 x 60 μm^2
  - VSS[1], TEST[1]: 60 x 60 μm^2
- Bump size variation: ± 5 μm
- Under bump metallization: sputtered TiW

1.Pads VSS and TEST are disconnected when wafer is sawn.

3.6 Reference die definition (SECS II Wafer map format)

- Physical appearance: no chip structure, full die size
- Local coordinates: x=-67, y= -20

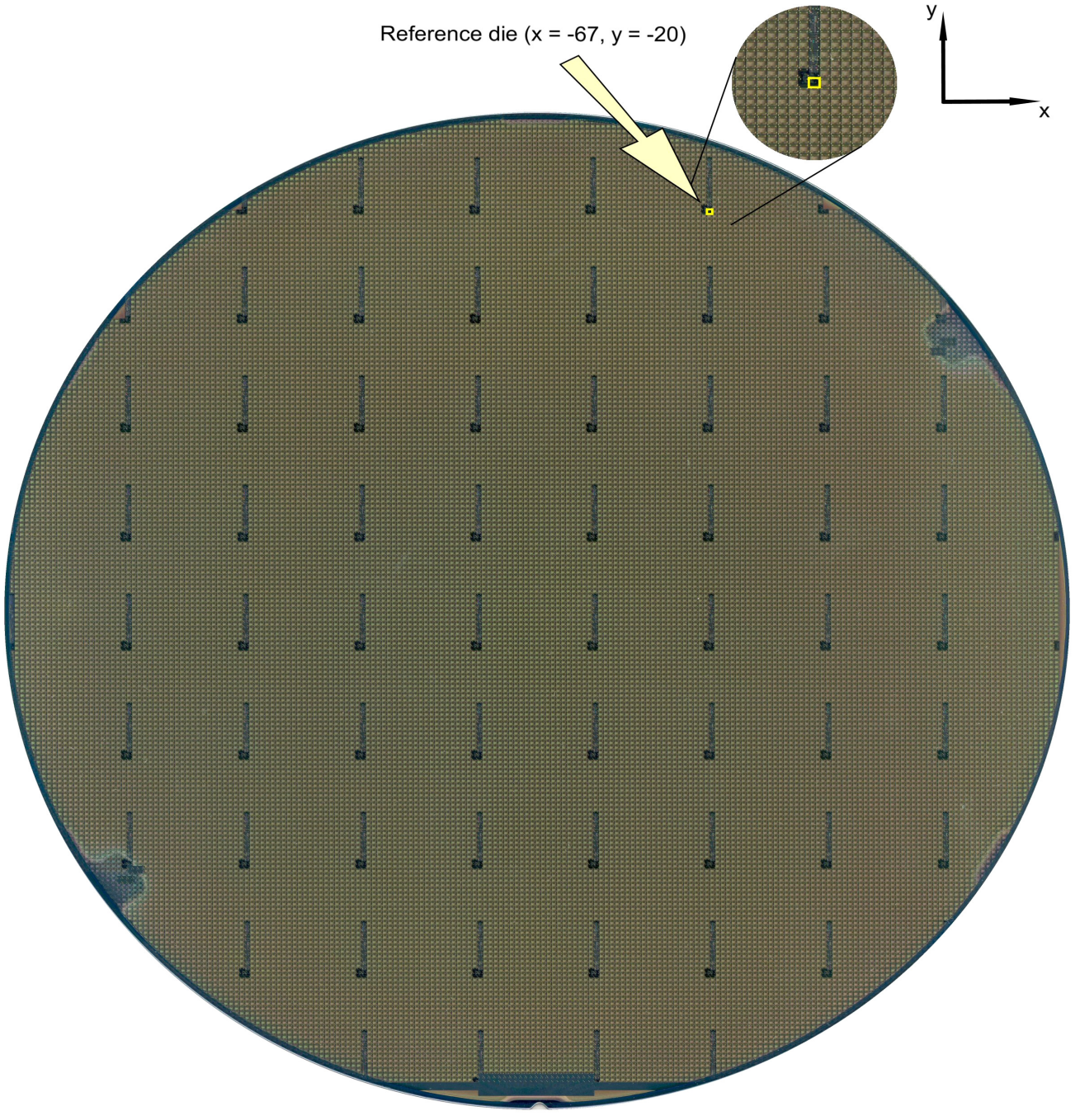


Fig 1. Wafer layout with reference die

4. Fail die identification

4.1 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

4.2 Wafer mapping

Wafer mapping for failed die information is available on floppy-disk.

Format: SECS II format

5. Limiting values

Table 2. Limiting values[1][2]

Absolute Maximum Ratings

Symbol	Parameter		Min	Type	Max	Unit
T_{STOR}	Storage temperature range		-55		+140	°C
Tj	Junction temperature		-55		+140	°C
V_{ESD}	Electrostatic discharge voltage	[3]			±2	kV_{peak}
$I_{max\ LA-LB}$	Maximum input peak current				±60	mA_{peak}
T_{jop}	Operating junction temperature		-25		+85	°C
I_{LA-LB}	Input current	[4]			30	mA_{rms}

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

[3] MIL-STD-883D, Method 3015.7, Human Body Model

[4] The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter I_{LA-LB})

6. Characteristics

6.1 Electrical characteristics

T_{op}= -25 to 85° C

Table 3. Characteristics [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{LA-LB}	Minimum Supply Voltage for READ/WRITE				2.5	2.7	V_{rms}
f_{op}	Operating Frequency		[2]	13.553	13.560	13.567	MHz
C_{res}	Input Capacitance between LA – LB	V_{LA-LB} = 2 V_{rms}	[3]	22.3	23.5	24.7	pF
P_{min}	Minimum Operating Supply Power		[4]		280		µW
m	Modulation of RF Voltage for Demodulator Response	$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$	[5]				%
tP_{sm}	Modulation Pulse Length of RF Voltage		[5]				µs
tD	Demodulator Response Time	m ≥ 10 %, 100 %	[5]				µs
Rmod	Load Modulation		[5]				Ω
t_{ret}	EEPROM Data Retention	T_{amb} ≤ 55 °C		10			Years
n_{write}	EEPROM Write Endurance			100000			Cycles

[1] Typical ratings are not guaranteed. These values listed are at room temperature.

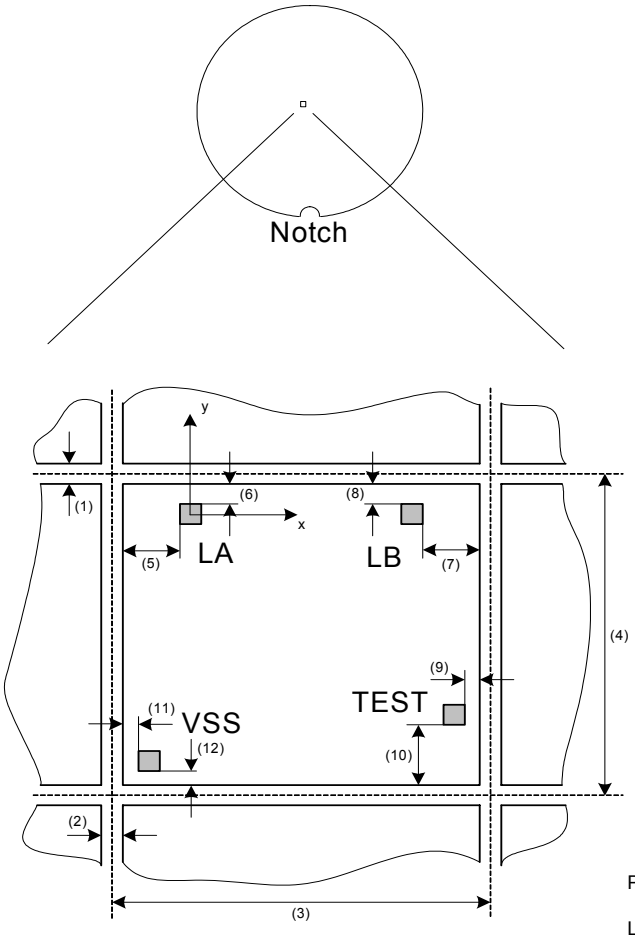
[2] Bandwidth limitation (±7 kHz) according to ISM band regulations.

[3] Measured with an HP4285A LCR meter at 13.56 MHz

[4] Including losses in resonant capacitor and rectifier

[5] refer to ISO/IEC 15693-2 and 15693-3 including pulse shapes and tolerances; proper coil design assumed

7. Chip orientation and bond pad locations



PAD coordinates	(center) x [µm]	y
LA	0	0
LB	630	0
TEST	515	–600
VSS	–105	–760

(1) X-Scribeline width: 50 µm
(2) Y-Scribeline width: 50 µm
(3) Chip step, x-length: 990 µm
(4) Chip step, y-length: 950 µm
(5) LA bump edge to chip edge, x-length: 135 µm
(6) LA bump edge to chip edge, y-length: 50 µm
(7) LB bump edge to chip edge, x-length: 115 µm
(8) LB bump edge to chip edge, y-length: 50 µm
(9) TEST bump edge to chip edge, x-length: 30 µm
(10) TEST bump edge to chip edge, y-length: 190 µm
(11) VSS bump edge to chip edge, x-length: 30 µm
(12) VSS bump edge to chip edge, y-length: 30 µm

Fig 2. Chip orientation and bond pad locations

8. Final wafertest specification

- Minimum yield per wafer: 30 % of 29941 potential good dies.
- Minimum yield per lot: 30 %

9. References

- Data sheet ’General specification for 8” wafers on UV-tape’
- Data sheet ’General quality specification’
- Application note ’SECS II wafer map format’
- Data sheet ’I•CODE SLI-S/I•CODE SLI-S HC, Functional Specification’
- Application note ’I•CODE coil design guide’

10. Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
135830	21 March 2007	Product data sheet		Revision 3.0
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name.			

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 21 March 2007
Document identifier: 135830