SPECTRALINEAR

SL15100

Programmable Spread Spectrum Clock Generator (SSCG)

Key Features

- Low power dissipation
  - 7.7mA-typ at 66MHz and VDD=3.3V
  - 6.8mA-typ at 66MHz and VDD=2.5V
- Wide 2.5V to 3.3V +/-10% power supply range
- Programmable outputs from 3 to 200MHz
- Low Jitter
  - 110ps at 66MHz
- Programmable Center or Down Spread Modulation from 0.25 to 5.0%
- 8 to 48 MHz external crystal range
- 8 to 166 MHz external clock range
- Integrated internal voltage regulator
- Programmable PD#/OE/SSON#/FS functions
- Programmable CL at XIN and XOUT pins
- Programmable output rise and fall times
- Programmable modulation frequency from 30 to 120 kHz

Applications

- Printers, MFPs
- Digital Copiers
- NBPCs and LCD Monitors
- Routers, Servers and Switchers
- HDTV and DVD-R/W

Description

The SL15100 a programmable low power Spread Spectrum Clock Generator (SSCG) used for reducing Electromagnetic Interference (EMI). The product is designed using SpectraLinear proprietary **EProClock™** programmable phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the input clock. The modulated clock can significantly reduce the measured EMI levels, and leading to the compliance with regulatory agency requirements.

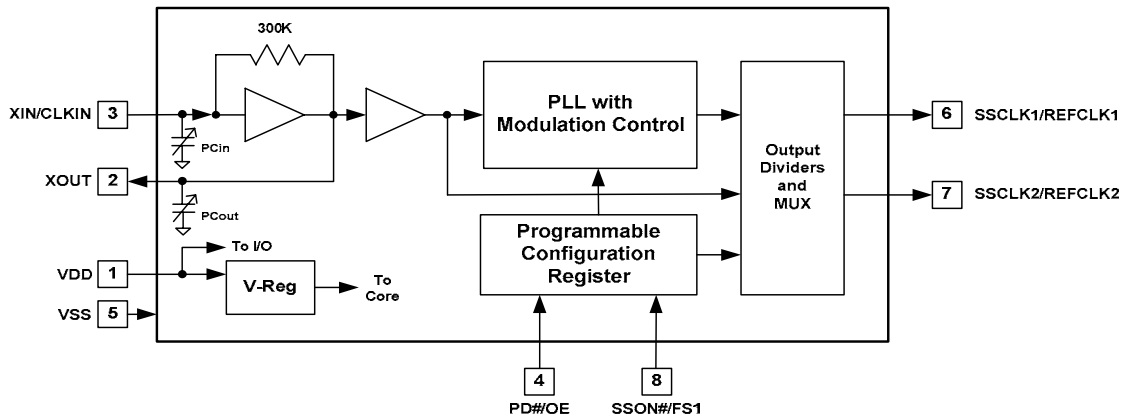
The output clock frequency, Spread %, output rise and fall times, crystal load, modulation frequency and PD#/OE/SSON#/FS functions can be programmed to meet the needs of wide range of applications. The SL15100 operates from 2.5V to 3.3V power supply voltage range. The product is offered in 8-pin TSSOP package with commercial and industrial grades.

Refer to SL15101 for up to four (4) programmable clock outputs and SL15L100/101 Programmable SSCG products for 1.8V power supply operation.

Benefits

- Peak EMI reduction of 8 to 16 dB
- Fast time-to-market
- Cost Reduction
- Reduction of PCB layers
- Eleminates the need for higher order crystals (Xtals) and crystal oscillators (XOs)

Block Diagram



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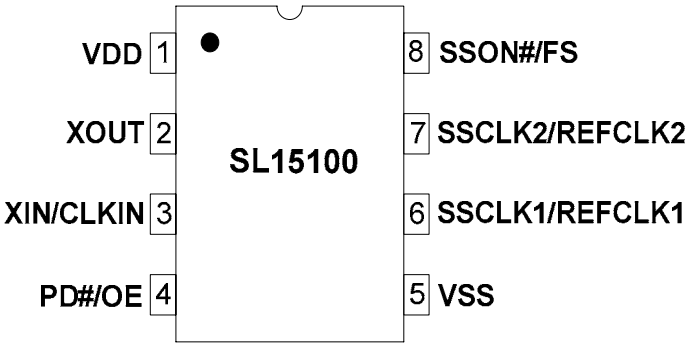
Pin Configuration



8-Pin TSSOP

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	VDD	Power	Positive power supply.
2	XOUT	Output	Crystal or ceramic resonator output pin. Leave this pin unconnected (floating) if external clock is used at Pin-3.
3	XIN/CLKIN	Input	Crystal, ceramic resonator or external clock input pin.
4	PD#/OE	Input	User Programmable PD# or OE control pin. Power Down (PD#-Active Low): If PD#=0(Low), the device is powered down and both SSCLK and REFOUT outputs are weakly pulled low to VSS. Output Enable (OE-Active High): If OE=1(High), the SSCLK and REFOUT outputs are enabled. PD# or OE is weakly pulled high to VDD.
5	VSS	Power	Power supply ground.
6	SSCLK1 or REFCLK1	Output	This pin can be programmed as SSCLK1 or REFCLK1.
7	SSCLK2 or REFCLK2	Output	This pin can be programmed as SSCLK2 or REFCLK2.
8	SSON#/FS	Input	Programmable SSON# or Frequency Select (FS) Control pin. If SSCG# function is programmed: Spread-on=0(Low) or Spread-off=1(High). If FS function is programmed: The clock frequencies can be switched between two sets of frequencies as programmed. SSON# or FS is weakly pulled low to VSS.

General Description

The primary source of EMI from digital circuits is the system clock and all the other synchronous clocks and control signals derived from the system clock. The well know techniques of filtering (suppression) and shielding (containment), while effective, can cost money, board space and longer development time.

A more effective and efficient technique to reduce EMI is Spread Spectrum Clock Generator (SSCG) technique. Instead of using constant clock frequency, the SSCG technique modulates (spreads) the system clock with a much smaller frequency, to reduce EMI emissions at its source: The System Clock.

The SL15100 is designed using SpectraLinear proprietary programmable **EProClock™** phase-locked loop (PLL) and Spread Spectrum Technologies (SST) to synthesize and modulate (spread) the system clock such that the energy is spread out over a wider bandwidth. This reduces the peak value of the radiated emissions at the fundamental and the harmonics. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements and improve time-to-market without degrading system performance.

The SL15100 operates with both 3.3V and 2.5V power supply voltages. Refer to SL15L100 for 1.8V power supply operation.

The SL15100 is available in 8-pin TSSOP package with Extended Commercial Temperature range of 0 to +85°C and Industrial Temperature range of –40 to +85°C.

Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals and ceramic resonators. If an external clock is used, the input frequency range is from 8 to 166 MHz.

Output Frequency Range and Outputs

The two (2) outputs can be programmed as SSCLK or REFCLK. SSCLK output can be synthesized to any value from 3 to 200 MHz with spread based on valid input frequency. The spread at SSCLK pins can be stopped by SSON# input control pin, If SSON# pin is HIGH (VDD), the frequency at this pin is the synthesized nominal value of the input frequency and there is no spread.

REFOUT is the buffered output of the oscillator and is the same frequency as the input frequency without spread. However, REFOUT value can also be divided by using the output dividers from 2 to 32. The second programmable output (SSCLK2) can be used to generate a copy of SSCLK1 (fanout of 2) or the same SSCLK frequency can be divided from 2 to 32. In this case, the spread % value is the same as the original programmed spread % value. By using only first order crystals, SL15100 can synthesize output frequency up to 200 MHz, eliminating the need for higher order Crystals (Xtals) and Crystal Oscillators (XOs). This reduces the cost while improving the system clock accuracy, performance and reliability.

Programmable CL (Crystal Load)

The SL15100 provides programmable on-chip capacitors at XIN/CLKIN (Pin-3) and XOUT (Pin-2). The resolution of this programmable capacitor is 6-bits with LSB value of 0.5pF. When all bits are off the pin capacitance is CXIN=CXOUT =8.5pF (minimum value). When all bits are on the pin capacitance is CXIN=CXOUT=40pF (maximum value). The values of C_{XIN} and C_{XOUT} based on the C_L (Crystal Load Capacitor) can be calculated as: $C_{XIN}=C_{XOUT}=2C_L-C_{PCB}$. Refer to the Page-13 for additional information on crystal load (C_L).

In addition, if an external clock is used, the capacitance at Pin-3 (CLKIN) can programmed to control the edge rate of this input clock, providing additional EMI control.

Programmable Modulation Frequency

The Spread Spectrum Clock (SSC) modulation default value is 31.5 kHz. The higher value of up to120 kHz can also be programmed. Less than 30 kHz modulation frequency is not recommended to stay out of the range audio frequency bandwidth since this frequency could be detected as a noise by the audio receivers within the vicinity.

Programmable Spread Percent (%)

The spread percent (%) value is programmable from +/-0.25% to +/-2.5% (center spread) or -0.5% to -5.0% (down spread) for all SSCLK frequencies. It is possible to program smaller or larger non-standard values of spread percent. Contact SLI if these non-standard spread percent values are required in the application.

SSON# or Frequency Select (FS)

The SL15100 Pin-8 can be programmed as either SSON# to enable or disable the programmed spread percent value or as Frequency Select (FS). If SSON# is used, when this pin is pulled high (VDD), the spread is stopped and the frequency is the nominal value without spread. If low (GND), the frequency is the nominal value with the spread.

If FS function is used, the output pins can be programmed for different set of frequencies as selected by FS. SSCLK value can be any frequency from 3 to 200MHz, but the spread % is the same percent value. REFOUT is the same frequency as the input reference clock or divide by from 2 to 32 without spread. The set of frequencies in Table 1 is given as en example, using 48MHz crystal. The SL15100 also allows a fan-out of 2, meaning that Pins 6 and 7 can be programmed to the same frequencies with or without spread such that F1=F2 and F3=F4.

FS (Pin-8)	SSCLK1 (Pin-6)	REFCLK2 (Pin-7)
0	F1= 66MHz, +/-1%	F2= 48MHz
1	F3 =125MHz,+/-3%	F4= 24MHz

Table 1. Frequency Selection (FS)

Power Down (PD#) or Output Enable (OE)

The SL15100 Pin-4 can be programmed as either PD# or OE. PD# powers down the entire chip whereas OE only disables the output buffers to Hi-Z.

Absolute Maximum Ratings

Description	Condition	Min	Max	Unit
Supply voltage, VDD		-0.5	4.6	V
All Inputs and Outputs		-0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	85	°C
Ambient Operating Temperature	In operation, I-Grade	-40	85	°C
Storage Temperature	No power is applied	-65	150	°C
Junction Temperature	In operation, power is applied	-	125	°C
Soldering Temperature		-	260	°C
ESD Rating (Human Body Model)	JEDEC22-A114D	-4,000	4,000	V
ESD Rating (Charge Device Model)	JEDEC22-C101C	-1,500	1,500	V
ESD Rating (Machine Model)	JEDEC22-A115D	-250	250	V
Latch-up	125°C	-200	200	mA

DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +85 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Input Low Voltage	VIL	CMOS Level, Pins 4 and 8	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, Pins 4 and 8	0.7VDD	-	VDD	V
Output High Voltage	VOH1	IOH=10mA , Pins 6 and 7	VDD-0.5	-	-	V
Output Low Voltage	VOL1	IOL=10mA, Pins 6 and 7	-	-	0.5	V
Input High Current	IIH	VIN=VDD, Pins 4 and 8 If no pull-up/down resister used	-	-	10	µA
Input Low Current	IIL	VIN=GND, Pins 4 and 8 If no pull-up/down resister used	-	-	10	µA
Operating Supply Current	IDD	FIN=30MHz, REFCLK=30MHz SSCLK=66MHz, PD#/OE=VDD SSON#=GND, CL=0	-	7.7	9.2	mA
Standby Current	ISBC	PD#=GND	-	70	90	µA
Output Leakage Current	IOL	Pins 6 and 7	-10	-	10	µA
Programmable Input Capacitance at Pins 2 and 3	PCin PCout	Minimum setting value	-	8.5	-	pF
		Maximum setting value	-	40	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Input Capacitance	CIN2	Pins 4 and 8	-	4	6	pF
Load Capacitance	CL	SSCLK/REFCLK , Pins 6 and 7	-	-	15	pF

AC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +85 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	8	-	166	MHz
Output Frequency Range	FOUT1	SSCLK	3	-	200	MHz
Output Frequency Range	FOUT2	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Frequency Range	FOUT3	REFCLK, clock input	0.25	-	166	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%
Output Duty Cycle	DC2	REFCLK	45	50	55	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Output Rise/Fall Time	tr/f1	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	4.00	4.80	ns
Output Rise/Fall Time	tr/f2	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	2.00	2.40	ns
Output Rise/Fall Time	tr/f3	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	1.40	1.70	ns
Output Rise/Fall Time	tr/f4	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	1.10	1.35	ns
Output Rise/Fall Time	tr/f5	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	0.85	1.00	ns
Output Rise/Fall Time	tr/f6	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	0.70	0.85	ns
Output Rise/Fall Time	tr/f7	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	0.55	0.67	ns
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ1	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=Off	-	90	120	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ2	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=Off	-	100	130	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ3	CLKIN=SSCLK=33MHz, 2%Spread REFCLK=Off	-	120	160	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ4	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=On	-	100	130	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ5	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=On	-	105	140	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ6	CLKIN=SSCLK=33MHz, 2%Spread REFCLK=On	-	180	240	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ7	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=On	-	80	100	ps

Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ8	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=On	-	100	130	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ9	CLKIN=SSCLK=33MHz, 2%Spread REFCLK=On	-	135	180	ps
Power-down Time	tPD	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	150	350	ns
Power-up Time (Crystal or Resonator)	tPU1	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	3.5	5.0	ms
Power-up Time (Clock)	tPU2	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	2.0	3.0	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Spread Percent Range	SPR	SSCLK-1/2 Outputs	0.25	-	5.0	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	-15	-	15	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	30	31.5	120	kHz

DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +85 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.25	2.5	2.75	V
Input Low Voltage	VIL	CMOS Level, Pins 4 and 8	0	-	$0.3V_{DD}$	V
Input High Voltage	VIH	CMOS Level, Pins 4 and 8	$0.7V_{DD}$	-	V_{DD}	V
Output High Voltage	VOH1	IOH=6mA , Pins 6 and 7	V_{DD}-0.5	-	-	V
Output Low Voltage	VOL1	IOL=6mA, Pins 6 and 7	-	-	0.5	V
Input High Current	IIH	VIN=VDD, Pins 4 and 8 If no pull-up/down resister used	-	-	10	µA
Input Low Current	IIL	VIN=GND, Pins 4 and 8 If no pull-up/down resister used	-	-	10	µA
Pull-up/Down Resistors	RPU/D	VIN=VDD or GND	90	160	230	kΩ
Operating Supply Current	IDD	FIN=30MHz, REFCLK=30MHz SSCLK=66MHz, PD#/OE=VDD SSON#=GND, CL=0	-	6.8	8.1	mA
Standby Current	ISBC	PD#=GND	-	70	90	µA
Output Leakage Current	IOL	Pins 6 and 7	-10	-	10	µA
Programmable Input Capacitance at Pins 2 and 3	CXIN CXOUT	Minimum programming value	-	8.5	-	pF
		Maximum programming value	-	40	-	pF
		Resolution (programming steps)	-	0.5	-	pF

Input Capacitance	CIN2	Pins 4 and 8	-	4	6	pF
Load Capacitance	CL	SSCLK/REFCLK , Pins 6 and 7	-	-	15	pF

AC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +85 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	8	-	166	MHz
Output Frequency Range	FOUT1	SSCLK	3	-	200	MHz
Output Frequency Range	FOUT2	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Frequency Range	FOUT3	REFCLK, clock input	0.25	-	166	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%
Output Duty Cycle	DC2	REFCLK	45	50	55	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Output Rise/Fall Time	tr/f1	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	4.80	5.80	ns
Output Rise/Fall Time	tr/f2	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	2.60	3.10	ns
Output Rise/Fall Time	tr/f3	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.80	2.20	ns
Output Rise/Fall Time	tr/f4	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.40	1.70	ns
Output Rise/Fall Time	tr/f5	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.10	1.35	ns
Output Rise/Fall Time	tr/f6	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	0.90	1.10	ns
Output Rise/Fall Time	tr/f7	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	0.70	0.85	ns
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ1	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=Off	-	100	130	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ2	CLKIN=SSCLK=66MHz, 2%Spread, REFCLK=Off	-	110	140	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ3	CLKIN=SSCLK=33MHz, 2%Spread, REFCLK=Off	-	130	170	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ4	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=On	-	110	140	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ5	CLKIN=SSCLK=66MHz, 2%Spread, REFCLK=On	-	115	150	ps

Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ6	CLKIN=SSCLK=33MHz, 2%Spread, REFCLK=On	-	200	260	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ7	CLKIN=SSCLK=166MHz, 2%Spread, REFCLK=On	-	90	110	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ8	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=On	-	110	140	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ9	CLKIN=SSCLK=33MHz, 2%Spread REFCLK=On	-	150	200	ps
Power-down Time	tPD	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Power-up Time (Crystal or Resonator)	tPU1	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	3.5	5.0	ms
Power-up Time (Clock)	tPU2	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	2.0	3.0	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Spread Percent Range	SPR	SSCLK-1/2	0.25	-	5.0	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	-15	-	15	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	30	31.5	120	kHz

DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Input Low Voltage	VIL	CMOS Level, Pins 4 and 8	0	-	$0.3V_{DD}$	V
Input High Voltage	VIH	CMOS Level, Pins 4 and 8	$0.7V_{DD}$	-	V_{DD}	V
Output High Voltage	VOH1	IOH=8mA , Pins 6 and 7	V_{DD}-0.5	-	-	V
Output Low Voltage	VOL1	IOL=8mA, Pins 6 and 7	-	-	0.5	V
Input High Current	IIH	VIN=VDD, Pins 4 and 8 If no pull-up/down resister used	-	-	15	µA
Input Low Current	IIL	VIN=GND, Pins 4 and 8 If no pull-up/down resister used	-	-	15	µA
Pull-up or Down Resistor	RPU/D	VIN=VDD or GND	100	160	220	kΩ
Operating Supply Current	IDD	FIN=30MHz, REFCLK=30MHz SSCLK=66MHz, PD#/OE=VDD SSON#=GND, CL=0	-	8.0	9.6	mA

Standby Current	ISBC	PD#=GND	-	80	100	µA
Output Leakage Current	IOL	Pins 6 and 7	-15	-	15	µA
Programmable Input Capacitance at Pins 2 and 3	CXIN CXOUT	Minimum setting value	-	8.5	-	pF
		Maximum setting value	-	40	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Input Capacitance	CIN2	Pins 4 and 8	-	4	7	pF
Load Capacitance	CL	SSCLK/REFCLK , Pins 6 and 7	-	-	15	pF

AC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	8	-	166	MHz
Output Frequency Range	FOUT1	SSCLK	3	-	200	MHz
Output Frequency Range	FOUT2	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Frequency Range	FOUT3	REFCLK, clock input	0.25	-	166	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%
Output Duty Cycle	DC2	REFCLK	45	50	55	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Output Rise/Fall Time	tr/f1	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	4.00	4.80	ns
Output Rise/Fall Time	tr/f2	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	2.00	2.40	ns
Output Rise/Fall Time	tr/f3	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	1.40	1.70	ns
Output Rise/Fall Time	tr/f4	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	1.10	1.35	ns
Output Rise/Fall Time	tr/f5	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	0.85	1.00	ns
Output Rise/Fall Time	tr/f6	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	0.70	0.85	ns
Output Rise/Fall Time	tr/f7	Programmable, VDD=3.3 CL=15pF, 20 to 80% of VDD	-	0.55	0.67	ns
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ1	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=Off	-	100	135	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ2	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=Off	-	110	145	ps
Cycle-to-Cycle Jitter	CCJ3	CLKIN=SSCLK=33MHz, 2%Spread	-	130	175	ps

(SSCLK – Pin 7)		REFCLK=Off				
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ4	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=On	-	110	145	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ5	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=On	-	115	155	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ6	CLKIN=SSCLK=33MHz, 2%Spread REFCLK=On	-	190	255	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ7	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=On	-	90	115	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ8	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=On	-	110	145	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ9	CLKIN=SSCLK=33MHz, 2%Spread REFCLK=On	-	145	195	ps
Power-down Time	tPD	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	150	350	ns
Power-up Time (Crystal or Resonator)	tPU1	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	3.5	5.0	ms
Power-up Time (Clock)	tPU2	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	2.0	3.0	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	150	350	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	150	350	ns
Spread Percent Range	SPR	SSCLK-1/2	0.25	-	5.0	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	-20	-	20	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	30	31.5	120	kHz

DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.25	2.5	2.75	V
Input Low Voltage	VIL	CMOS Level, Pins 4 and 8	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, Pins 4 and 8	0.7VDD	-	VDD	V
Output High Voltage	VOH1	IOH=6mA , Pins 6 and 7	VDD-0.4	-	-	V
Output Low Voltage	VOL1	IOL=6mA, Pins 6 and 7	-	-	0.4	V
Input High Current	IIH	VIN=VDD, Pins 4 and 8 If no pull-up/down resister used	-	-	15	µA
Input Low Current	IIL	VIN=GND, Pins 4 and 8 If no pull-up/down resister used	-	-	15	µA
Pull-up or Down Resistors	RPU/D	Vin=VDD or GND	90	160	230	kΩ

Operating Supply Current	IDD	FIN=30MHz, REFCLK=30MHz SSCLK=66MHz, PD#/OE=VDD SSON#=GND, CL=0	-	7.0	8.4	mA
Standby Current	ISBC	PD#=GND	-	80	100	µA
Output Leakage Current	IOL	Pins 6 and 7	-10	-	10	µA
Programmable Input Capacitance at Pins 2 and 3	CXIN CXOUT	Minimum setting value	-	8.5	-	pF
		Maximum setting value	-	40	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Input Capacitance	CIN2	Pins 4 and 8	-	4	7	pF
Load Capacitance	CL	SSCLK/REFCLK , Pins 6 and 7	-	-	15	pF

AC Electrical Characteristics (I-Grade)

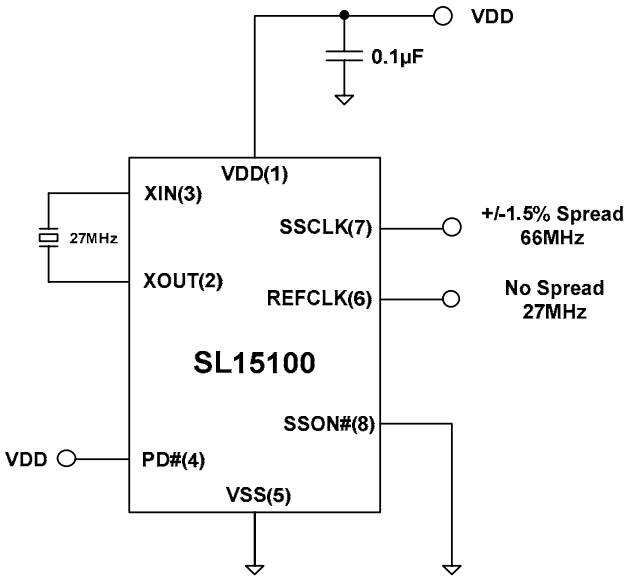
Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	8	-	166	MHz
Output Frequency Range	FOUT1	SSCLK	3	-	200	MHz
Output Frequency Range	FOUT2	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Frequency Range	FOUT3	REFCLK, clock input	0.25	-	166	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%
Output Duty Cycle	DC2	REFCLK	45	50	55	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Output Rise/Fall Time	tr/f1	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	4.80	5.80	ns
Output Rise/Fall Time	tr/f2	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	2.60	3.10	ns
Output Rise/Fall Time	tr/f3	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.80	2.20	ns
Output Rise/Fall Time	tr/f4	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.40	1.70	ns
Output Rise/Fall Time	tr/f5	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.10	1.35	ns
Output Rise/Fall Time	tr/f6	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	0.90	1.10	ns
Output Rise/Fall Time	tr/f7	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	0.70	0.85	ns
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ1	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=Off	-	115	150	ps

Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ2	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=Off	-	125	160	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ3	CLKIN=SSCLK=33MHz, 2%Spread REFCLK=Off	-	125	160	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ4	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=On	-	145	185	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ5	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=On	-	125	160	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 7)	CCJ6	CLKIN=SSCLK=33MHz, 2%Spread REFCLK=On	-	215	280	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ7	CLKIN=SSCLK=166MHz, 2%Spread REFCLK=On	-	105	130	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ8	CLKIN=SSCLK=66MHz, 2%Spread REFCLK=On	-	125	160	ps
Cycle-to-Cycle Jitter (SSCLK – Pin 6)	CCJ9	CLKIN=SSCLK=33MHz, 2%Spread REFCLK=On	-	165	220	ps
Power-down Time	tPD	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Power-up Time (Crystal or Resonator)	tPU1	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	3.5	5.0	ms
Power-up Time (Clock)	tPU2	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	2.0	3.0	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Spread Percent Range	SPR	SSCLK-1/2	0.25	-	5.0	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	-20	-	20	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	30	31.5	120	kHz

External Components & Design Considerations

Typical Application Schematic



Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS on the pins 1 and 5. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible Do not use vias between the decoupling capacitor and the VDD pin.

Series Termination Resistor: A series termination resistor is recommended if the distance between the output (SSCLK) and the load is over 1 ½ inch. The nominal impedance of the SSCLK output is about 30 Ω. Use 20 Ω resistor in series with the output to terminate 50Ω trace impedance and place 20 Ω resistor as close to the SSCLK output as possible.

Crystal and Crystal Load: Use only parallel resonant fundamental crystals. DO NOT USE higher overtone crystals. To meet the crystal initial accuracy specification (in ppm); the internal on-chip programmable capacitors PCin and PCout must be programmed to match the crystal load requirement. These values are given by the formula below:

$$PCin(pF) = PCout(pF) = [(CL(pF) - Cp(pF)/2)] \times 2$$

Where CL is crystal load capacitor as given by the crystal datasheet and Cp(pF) is the compensation factor for the total parasitic capacitance at XIN or XOUT pin including PCB related parasitic capacitance.

As an example; if a crystal with CL=18pF is used and Cp=4pF, by using the above formula, PCin=PCout=[(18-(4/2)] x 2 = 32pF. Programming PCin and PCout to 32pF assures that this crystal sees an equivalent load of 18pF and no other external crystal load capacitor is needed. Deviating from the crystal load specification could cause an increase in frequency accuracy in ppm. Refer to the Table 5 for the recommended crystal specifications.

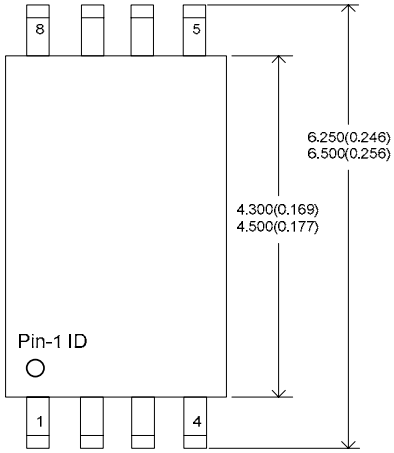
Recommended External Crystal Specifications

Parameter	Description	Min	Typ	Max	Unit	Comments
FNOM	Nominal Crystal Frequency Range	8	-	48	MHz	Fundamental Mode – AT Cut
CL	Nominal Crystal Load	6	12	18	pF	Load for +/-0 ppm Fo resonance value
R1,1	Equivalent Series Resistance	20	40	100	Ohm	F-Range: 8.0 to 12.999 MHz
R1,2	Equivalent Series Resistance	12.5	25	60	Ohm	F-Range: 13.0 to 19.999 MHz
R1,3	Equivalent Series Resistance	10	20	50	Ohm	F-Range: 20.0 to 48.000 MHz
DL1,1	Crystal Drive Level	-	-	200	µW	F-Range: 8.0 to 19.999 MHz
DL1,2	Crystal Drive Level	-	-	150	µW	F-Range: 20.0 to 48.000 MHz
Co1	Shunt Capacitance	-	4	5.4	pF	SMD Xtals
Co2	Shunt Capacitance	-	5	7.2	pF	Through Hole (Leaded) Xtals

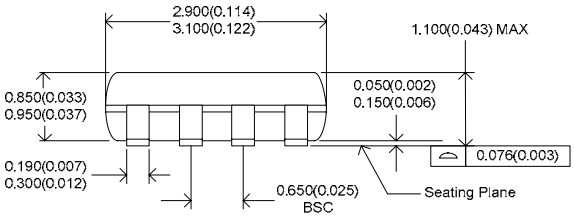
Table 5. Recommended Crystal Specifications

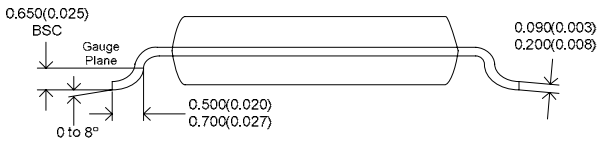
Package Outline and Package Dimensions

8-Pin TSSOP Package (173 Mil)



Dimensions are in milimeters(inches).
Top line: (MIN) and Bottom line: (Max)





Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA1}	Still air	-	110	-	°C/W
	θ_{JA2}	1m/s air flow	-	100	-	°C/W
	θ_{JA3}	3m/s air flow	-	80	-	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Independent of air flow	-	35	-	°C/W

Ordering Information [1]

Ordering Number [2]	Marking	Shipping Package	Package	Temperature
SL15100ZC-XXX	TBD	Tube	8-pin TSSOP	0 to 85°C
SL15100ZCT-XXX	TBD	Tape and Reel	8-pin TSSOP	0 to 85°C
SL15100ZI-XXX	TBD	Tube	8-pin TSSOP	-40 to 85°C
SL15100ZIT-XXX	TBD	Tape and Reel	8-pin TSSOP	-40 to 85°C

Notes:

1. All SLI products are RoHS compliant.
2. “XXX” is “Dash” number and will be assigned by SLI for the final programmed samples or production the units based on the each customer programming requirements.

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