DATA SHEET

SKYA21004: Three-Channel LCD Bias Power Management IC with Three-Channel High-Efficiency White LED Driver

Applications

- Automotive displays
- Digital photo frames
- Digital still cameras
- Tablets
- Notebooks

Features

LCD bias power (AVDD boost)

- Input supply range: 2.8 V to 5.5 V
- 1.3 MHz fixed frequency boost regulator
- Adjustable voltage up to 14.5 V (±1% typical accuracy)
- Short-circuit, over-voltage, and over-temperature protection

Positive/negative gate drive (V_{GH}/V_{GL})

- Up to 13.2 V input supply (V_{DD})
- Adjustable voltage up to 30 V @ 20 mA (V_{GH})
- Adjustable voltage down to –30 V @ 20 mA (V_{GL})

LED driver

- Input supply range: 2.8 V to 5.5 V
- Adjustable operating frequency: 600 kHz to 2 MHz
- Dimming control options:
  - 8-bit resolution on LED current control – I^2C interface
  - Direct PWM dimming (10-bit resolution of PWM duty control)
  - Analog PWM dimming (9-bit resolution of PWM duty control)
  - Programmable maximum LED current (30 mA to 120 mA) per channel
- Up to 28 V, 120 mA per channel
- Accuracy matching: ±2.5% @ 60 mA
- Fade in/out feature for current control
- PWM input range: 100 Hz to 25 kHz
- LED open/short detection, boost over-voltage/current protection, over-temperature protection
- AEC-Q100 qualified
- QFN (36-pin, 7 mm × 4 mm, 0.5 mm pitch) package (MSL3, 260 ºC per JEDEC J-STD-020)

Description

The SKYA21004 consists of a power management block supplying LCD bias rails and a three-channel backlight driver.

The LCD bias power management block of the SKYA21004 includes a boost converter that supplies main analog voltage (AVDD) of the panel, two charge-pump controllers supplying a gate-on voltage (V_{GH}), and a gate-off voltage (V_{GL}) to the LCD panel. The boost converter uses a 1.3-MHz fixed frequency to generate AVDD voltage up to 14.5 V. Two charge-pump controllers can generate up to +30 V and down to –30 V from the charge-pump stages configured by diodes and capacitors. A proprietary regulation algorithm can minimize the output ripple.

The backlight driver of the SKYA21004 integrates the boost converter to drive the LED voltage up to 28 V. The switching frequency is adjustable from 600 kHz to 2 MHz for system integration flexibility, which optimizes the efficiency and controls EMI. Three precision current sinks are programmable to drive LED current up to 120 mA per string.

The backlight driver of the SKYA21004 supports Analog Pulse Width Modulation (APWM) dimming, Direct Pulse Width Modulation (DPWM) dimming, and analog dimming (through I^2C).

In the DPWM dimming mode, the output waveform follows the duty and the frequency of control input signal from the PWM pin. In the APWM dimming mode, the LED current of each channel is controlled by the input duty of PWM input signal, the I^2C programmed brightness level, and the external R_{ISET} resistor.

The PWM pin can accept the frequency range from 100 Hz to 25 kHz with 10-bit resolution of duty control and 8-bit resolution of current control. When the PWM pin is not used, it needs to be pulled high.

The SKYA21004 is available in a 7 mm × 4 mm, 36-pin QFN package.

A typical application circuit is shown in Figure 1. The pin configurations are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

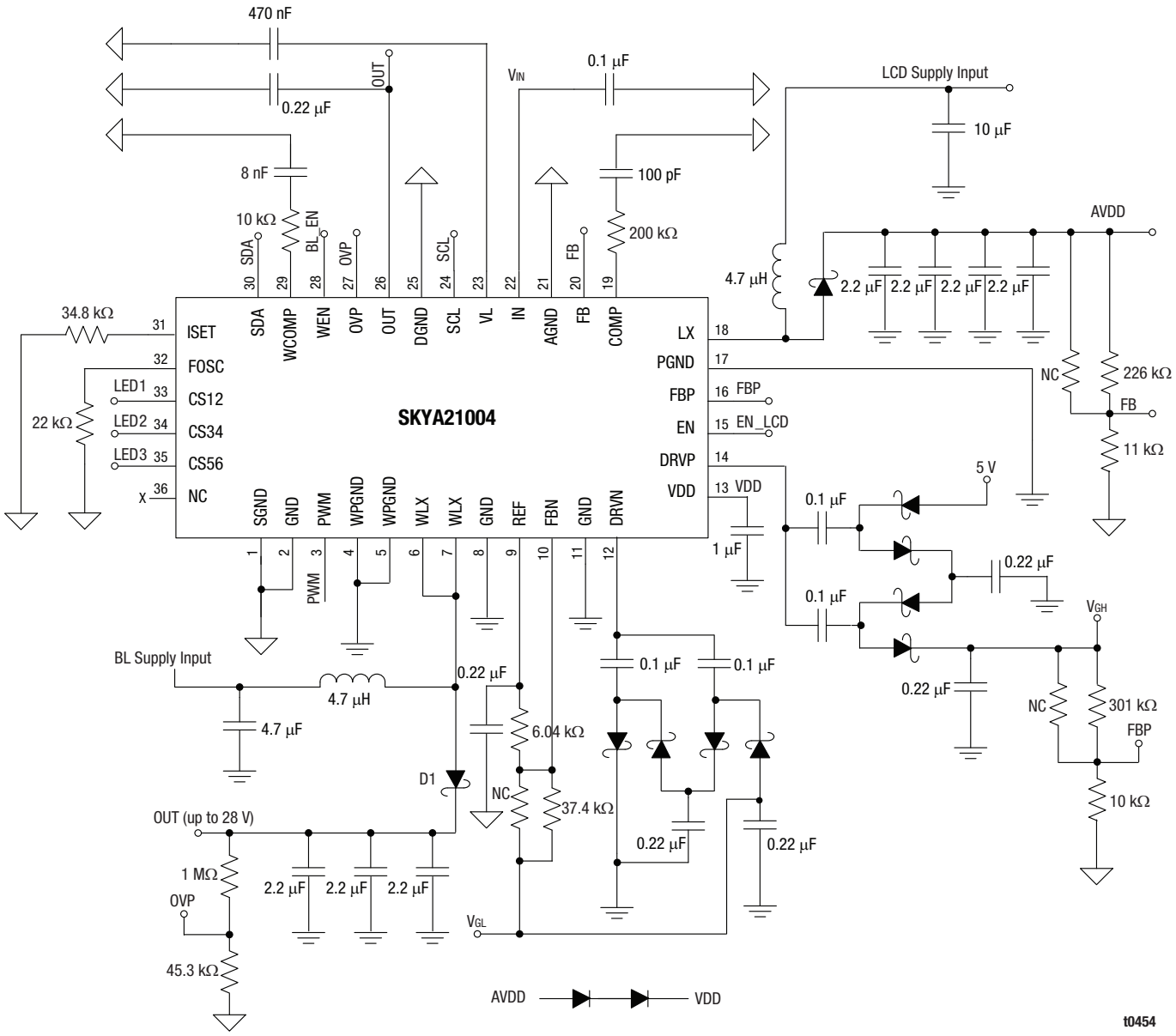


Figure 1. SKYA21004 Typical Application Circuit

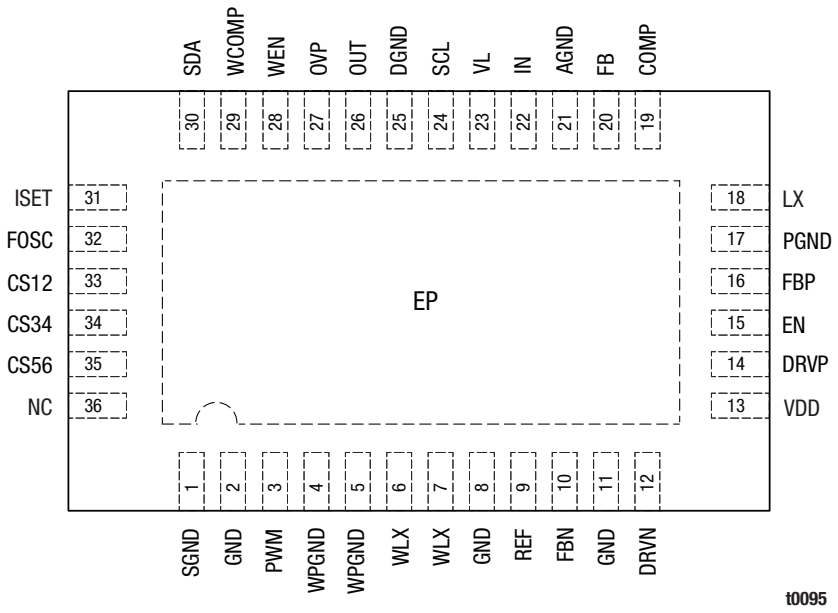


Figure 2. SKYA21004 Pinout – 7 mm × 4 mm, 36-Pin QFN (Top View)

Table 1. SKYA21004 Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	SGND	Ground connection for current sinks.	19	COMP	LCD bias boost external compensation.
2	GND	Ground.	20	FB	LCD bias boost feedback input.
3	PWM	External PWM dimming signal input. When this is not used, it should be pulled high.	21	AGND	Analog ground.
4	WPGND	LED driver boost converter power ground.	22	IN	IC supply input.
5	WPGND	LED driver boost converter power ground.	23	VL	LED driver internal regulator bypass output. Bypass with 16 V, X7R 470 nF capacitor to the ground.
6	WLX	LED driver boost converter switch node.	24	SCL	I^2C serial interface clock input.
7	WLX	LED driver boost converter switch node.	25	DGND	LED driver digital ground. Connect to the analog ground.
8	GND	Ground.	26	OUT	LED driver boost output sense pin.
9	REF	Internal reference bypass pin. Bypass with 0.1 μF ceramic capacitor to the AGND.	27	OVP	LED driver OVP set pin. Connect to the LED driver boost output using high-impedance resistor voltage divider.
10	FBN	Negative charge-pump feedback input.	28	WEN	LED driver enable pin.
11	GND	Ground.	29	WCOMP	LED driver boost external compensation pin.
12	DRVN	Negative charge-pump driver output.	30	SDA	I^2C serial interface data.
13	VDD	Charge-pump driver supply voltage. Bypass with 1 μF ceramic capacitor to the AGND.	31	ISET	LED channel current set-up pin. Connect a set resistor between this pin and analog ground to program the max LED current.
14	DRVP	Positive charge-pump driver output.	32	FOSC	LED driver boost switching frequency setting pin. Connect an external resistor to set the frequency from 600 kHz to 2 MHz.
15	EN	LCD bias power block enable pin.	33	CS12	LED current sink 12. Connect to AGND to disable the channel.
16	FBP	Positive charge-pump feedback input.	34	CS34	LED current sink 34. Connect to AGND to disable the channel.
17	PGND	LCD bias boost converter power ground.	35	CS56	LED current sink 56. Connect to AGND to disable the channel.
18	LX	LCD bias boost converter switch node.	36	NC	No connect.
			EP		Exposed paddle.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKYA21004 are provided in Table 2. The recommended operating conditions are listed in Table 3. The electrical specifications are provided in Table 4.

Safe operating area characteristics are shown in Figures 3 through 6. Typical performance characteristics of the SKYA21004 are illustrated in Figures 7 through 47.

Table 2. SKYA21004 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Typical	Maximum	Units
IN and VL to SGND, AGND, DGND, (W)PGND	V_{IN}, V_{VL}	–0.3		+6.5	V
LX, CS12, CS34, CS56, WLX and OUT to SGND, AGND, (W)PGND, DGND	V_{LX}, V_{CS12}, V_{CS34}, V_{CS56}, V_{WLX}, V_{OUT}	–0.3		+30.0	V
WEN, ISET, WCOMP, OVP, FOSC, SDA, SCL, and PWM to SGND, AGND, (W)PGND, DGND	V_{WEN}, V_{ISET}, V_{WCOMP}, V_{OVP}, V_{FOSC}, V_{SDA}, V_{SCL}, V_{PWM}	–0.3		V_{IN} + 0.3	V
VDD	V_{DD}	–0.3		+14	V
COMP, FB, FBP, FBN, and REF to AGND, PGND	V_{COMP}, V_{FB}, V_{FBP}, V_{FBN}, V_{REF}	–0.3		V_{IN} + 0.3	V
DRVP, DRVN	V_{DRV}	–0.3		V_{DD} + 0.3	V
Maximum junction operating temperature	T_J	–40		+150	ºC
Maximum power dissipation (Notes 2 and 3)	P_D		1.257		W
Thermal resistance (Note 2)	θ_{JA}		16.5		ºC/W

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed may result in permanent damage to the device.

Note 2: The thermal resistance is measured in accordance with EIA/JESD 51 series.

Note 3: When T_A = 25 ºC.

CAUTION: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. SKYA21004 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Input voltage range	V_{IN}	2.8	5.5	V
Charge-pump drivers supply voltage	V_{DD}	2.8	13.2	V
Input PWM frequency	f_{PWM}	0.1	25.0	kHz
Storage temperature	T_S	–40	+150	ºC
Operating ambient temperature	T_A	–40	+105	ºC

Table 4. SKYA21004 Electrical Specifications (1 of 2) (Notes 1 and 2)
(V_{IN} = 5 V, V_{DD} = 12 V, AVDD = 13.2 V, L1 = 4.7 µH, L2 = 4.7 µH, C_{IN} = 10 µF, C_{WIN} = 4.7 µF, C_{WOUT} = 3 × 2.2 µF, C_{OUT} = 4 × 2.2 µF, T_A = –40 °C to +105 °C, Typical Values are T_A = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
General						
Input voltage	V_{IN}		2.8		5.5	V
Quiescent supply current	I_Q	V_{EN} = V_{WEN} = high, V_{IN} = 3.6 V		4.7		mA
Input shutdown current	I_{SHDN}	V_{EN} = V_{WEN} = 0 V, V_{IN} = 3.6 V			2	µA
Reference voltage	V_{REF}	No load, V_{IN} = 3.6 V	1.18	1.2	1.22	V
Over-temperature shutdown threshold	T_{SD}			140		ºC
Maximum input logic low	V_{IL}				0.4	V
Minimum input logic high	V_{IH}		1.4			V
LCD Bias Boost Section (AVDD)						
Output voltage	V_{AVDD}		V_{IN} + 1		14.5	V
Operating frequency	f_{OSC}		910	1300	1690	kHz
Maximum duty cycle	D_{MAX}		86	90		%
FB regulation voltage	V_{FB}	No load	0.588	0.6	0.612	V
FB fault trip level		V_{FB} falling	0.528	0.548	0.568	V
FB load regulation	$\Delta V_{AVDD}/\Delta I_{AVDD}$	0 < I_{AVDD} < full load		0.01		%/mA
FB input bias current	I_{FB}	V_{FB} = 0.7 V	–1		+1	µA
LX on resistance	$R_{LX(ON)}$	I_{LX} = 200 mA		350	700	mΩ
LX leakage current	I_{LX_LEAK}	V_{LX} = 13.2 V		0.01	20	µA
LX current limit	I_{LIM}		1			A
Soft-start time	tss	No load		1.3		ms
Gate On Charge-Pump Driver (V_{GH})						
VDD input voltage range	V_{DD}		2.8		13.2	V
FBP regulation voltage	V_{FBP}		0.588	0.6	0.612	V
FBP fault trip level	V_{FBP}	V_{FBP} rising	0.457	0.487	0.517	V
DRVP P-Ch on resistance	DRVPPRDS			3	6	Ω
DRVP N-Ch on resistance	DRVPNRDS	V_{FBP} = 0.585 V		1.5	3	Ω
Gate Off Charge-Pump Driver (V_{GL})						
VDD input voltage	V_{DD}		2.8		13.2	V
FBN regulation	V_{FBN}		–50	0	50	mV
FBN fault trip level	V_{FBN}	V_{FBN} rising	0.403	0.43	0.457	V
DRVN P-Ch on resistance	$DRVNP_{RDS}$			3	6	Ω
DRVN N-Ch on resistance	$DRVNN_{RDS}$	V_{FBN} = 0.035 V		1.5	3	Ω
LED Driver Boost Converter						
Over-voltage threshold	V_{OVP}	V_{IN} = 3.6 V	0.91	1.00	1.09	V
Over-voltage hysteresis	V_{OVP_HYS}	V_{IN} = 3.6 V		100		mV
Soft-start time	t_{SS}			2.5		ms
Oscillator frequency	f_{OSC}	V_{IN} = 3.6 V	600		2000	kHz
Switch on resistance	R_{DSON}	V_{IN} = 3.6 V		150		mΩ

Table 4. SKYA21004 Electrical Specifications (2 of 2) (Notes 1 and 2)
(V_{IN} = 5 V, V_{DD} = 12 V, AVDD = 13.2 V, L1 = 4.7 µH, L2 = 4.7 µH, C_{IN} = 10 µF, C_{WIN} = 4.7 µF, C_{WOUT} = 3 × 2.2 µF, C_{OUT} = 4 × 2.2 µF, T_A = –40 °C to +105 °C, Typical Values are T_A = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Switch current limit	I_{LIM}	ILIM = 0, V_{IN} = 3.6 V	2.6		3.7	A
		ILIM = 1, V_{IN} = 3.6 V	2.1		3.1	A
Switch off time	t_{OFF}		55			ns
FOSC voltage	V_{FOSC}	V_{IN} = 3.6 V		0.6		V
LED Driver Current Sink						
ISET voltage	V_{ISET}	V_{IN} = 3.6 V		0.6		V
Current sink leakage	I_{CS_LEAK}	V_{CSx} = 28 V, WEN = logic low, V_{IN} = 3.6 V			1	µA
Maximum channel current	I_{LED_MAX}	R_{ISET} program	30		120	mA
Current sink accuracy	I_{CSX}	I_{CS} = 60 mA, V_{IN} = 3.6 V	–2.5		2.5	%
Current sink matching	$I_{CSX\_MATCHING}$	I_{CS} = 60 mA, V_{IN} = 3.6 V	–2.5		2.5	%
Current sink voltage	V_{CSX}	I_{CS} = 60 mA		0.5		V
Shorted LED detection threshold	$V_{CSX(SHORT)}$	VSHRT = 00		7		V
Open LED detection threshold	$V_{CSX(OPEN)}$			100		mV
PWM input frequency range	f_{PWM}	V_{IN} = 3.6 V	0.1		25	kHz
PWM duty hysteresis	D_{PWM_HYS}	Duty direction change		0.5		%
Current sink brightness changing time	t_{SLEW}	From one dimming level to another level		4		ms/step
Current sink brightness changing time at startup or dimming mode change	t_{SLEW_START}	From one dimming level to another level		30		µs/step
DPWM propagation delay	t_{PWM_PROP}			1		cycle
PWM leakage current	I_{PWM_LEAK}	V_{PWM} = 3.3 V, V_{IN} = 3.6 V			15	µA
I²C Interface						
Input logic low	V_{IL}	V_{IN} = 3.6 V			0.4	V
Input logic high	V_{IH}	V_{IN} = 3.6 V	1.4			V
SDA output low voltage	V_{OL}	I_{PULL_UP} = 3 mA, V_{IN} = 3.6 V			0.4	V
SDA, SCL input leakage current	I_{IN}	V_{SDA} = V_{SCL} = 5 V, V_{IN} = 3.6 V	–1		+1	µA
SCL clock frequency	f_{SCL}				400	kHz
SCL low clock period	t_{LOW}	V_{IN} = 3.6 V	1.3			µs
SCL high clock period	t_{HIGH}	V_{IN} = 3.6 V	0.6			µs
Hold time start condition	t_{HD_STA}	V_{IN} = 3.6 V	0.6			µs
SDA data setup time	t_{SU_DAT}	V_{IN} = 3.6 V	100			ns
Setup time for start (repeated) condition	t_{SU_STA}	V_{IN} = 3.6 V	0.6			µs
SDA data hold time	t_{HD_DAT}	V_{IN} = 3.6 V	0		0.9	µs
Setup time for stop condition	t_{SU_STO}	V_{IN} = 3.6 V	0.6			µs
Bus free time between stop and start conditions	t_{BUF}	V_{IN} = 3.6 V	1.3			µs
Capacitive load for each bus line	C_B				400	pF

Note 1: Performance is guaranteed only under the conditions listed in this table.

Note 2: Min and Max limits are specified by design, test, or statistical analysis.

Safe Operating Area Characteristics

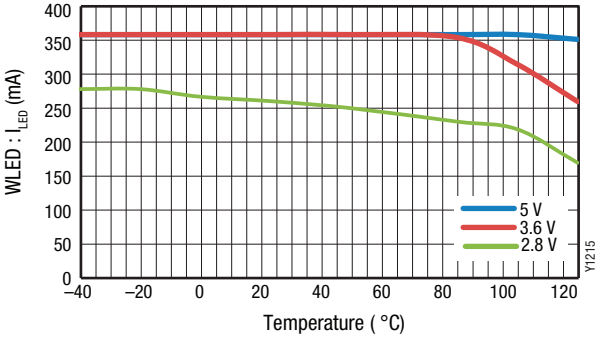


Figure 3. WLED: Maximum LED Current vs Temperature (6S3P)

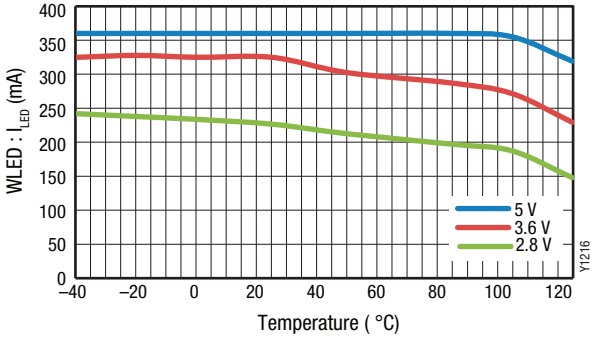


Figure 4. WLED: Maximum LED Current vs Temperature (7S3P)

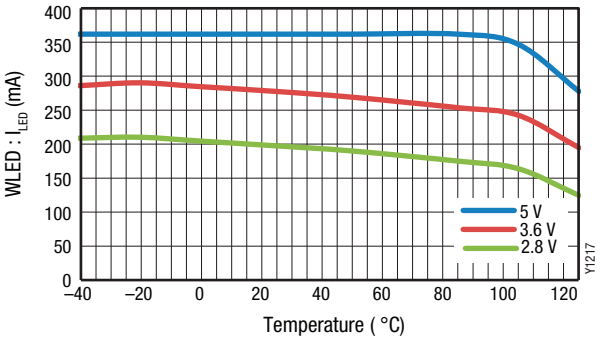


Figure 5. WLED: Maximum LED Current vs Temperature (8S3P)

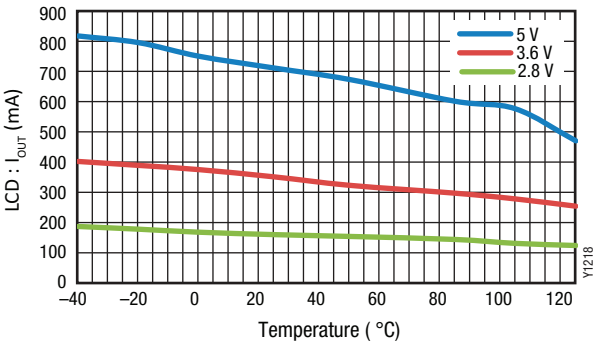


Figure 6. LCD: Maximum Load Current vs Temperature

Typical Performance Characteristics

(V_{IN} = 5 V, V_{DD} = 12 V, A_{VDD} = 13.2 V, L1 = 4.7 µH, L2 = 4.7 µH, C_{IN} = 10 µF, C_{WIN} = 4.7 µF, C_{WOUT} = 3 × 2.2 µF, C_{OUT} = 4 × 2.2 µF, T_A = –40 °C to +105 °C, Typical Values are T_A = +25 °C, Unless Otherwise Noted)

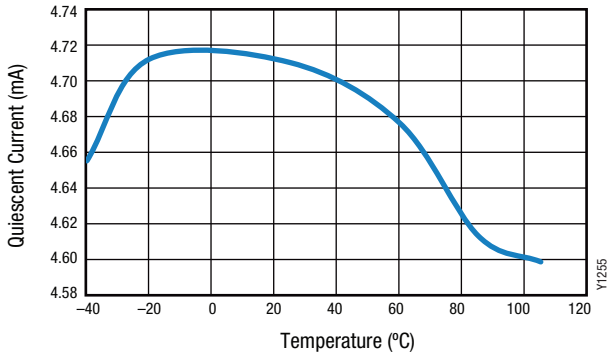


Figure 7. Quiescent Current vs Temperature

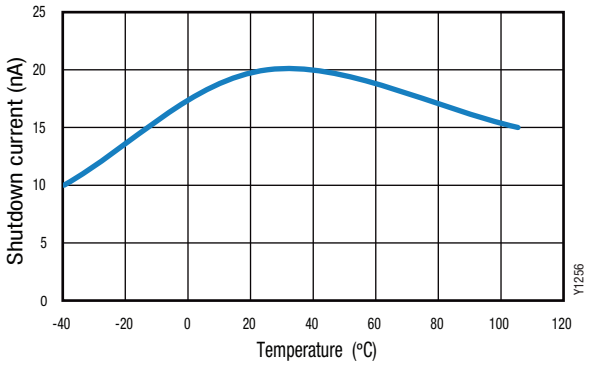


Figure 8. Shut Down Current vs Temperature

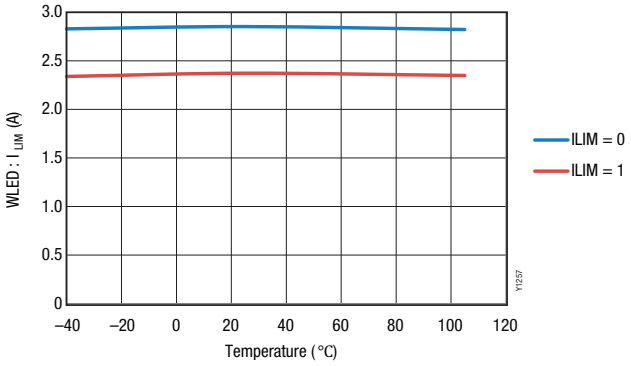


Figure 9. WLED: I_{LIM} vs Temperature

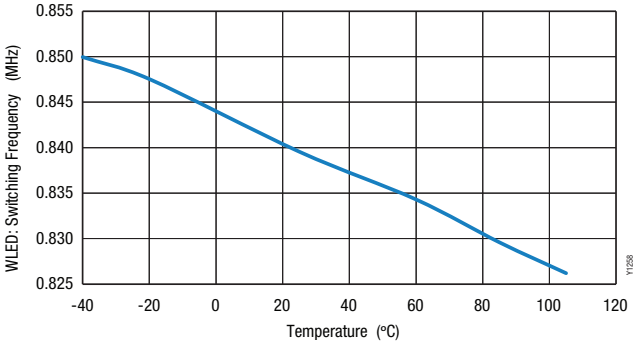


Figure 10. WLED: Switching Frequency vs Temperature (VIN = 5 V, RFOSC = 24.3 kΩ)

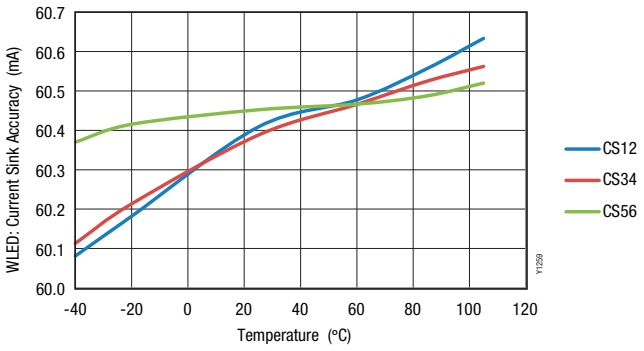


Figure 11. WLED: Current Sink Accuracy vs Temperature

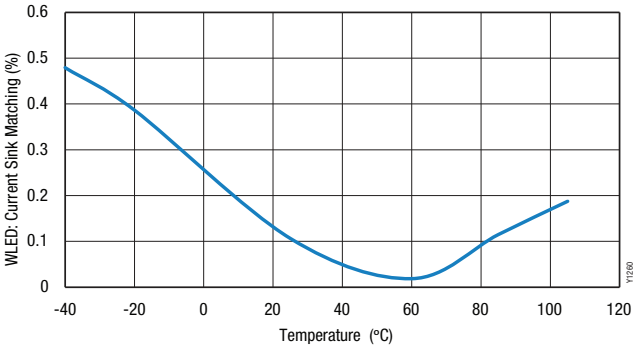


Figure 12. WLED: Current Sink Matching vs Temperature

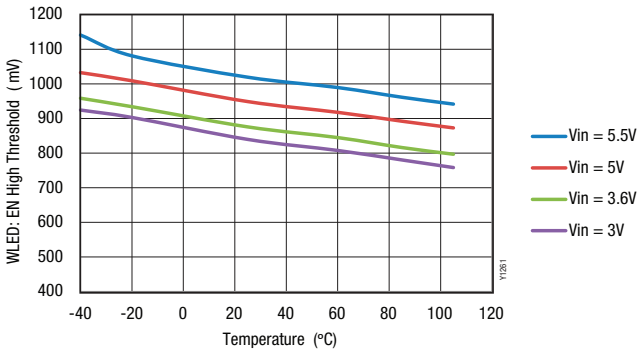


Figure 13. WLED: EN High Threshold vs Temperature

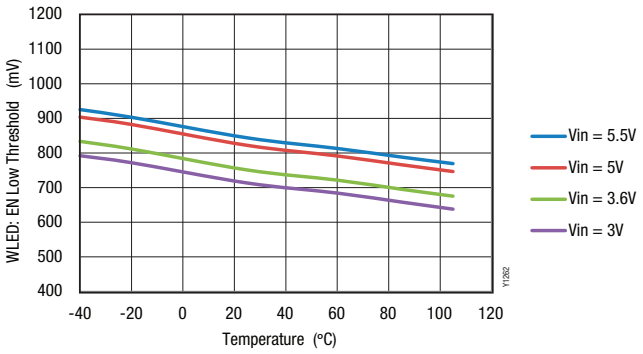


Figure 14. WLED: EN Low Threshold vs Temperature

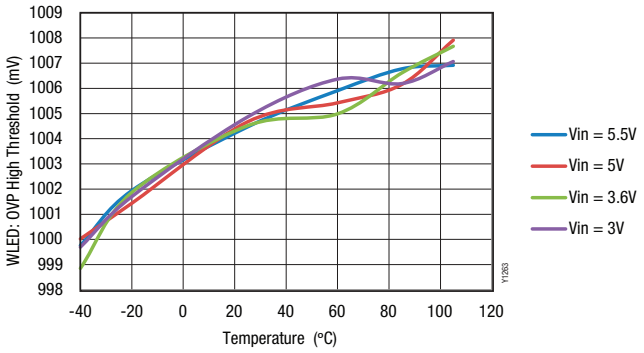


Figure 15. WLED: OVP High Threshold vs Temperature

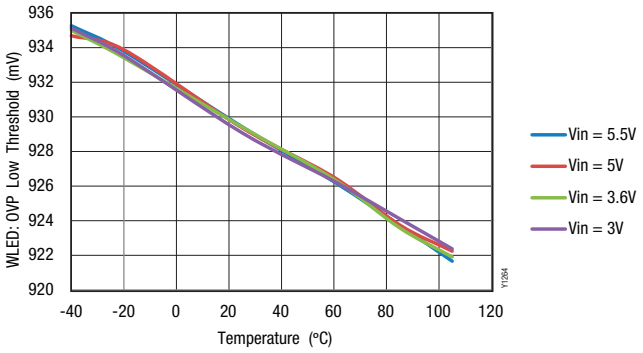


Figure 16. WLED: OVP Low Threshold vs Temperature

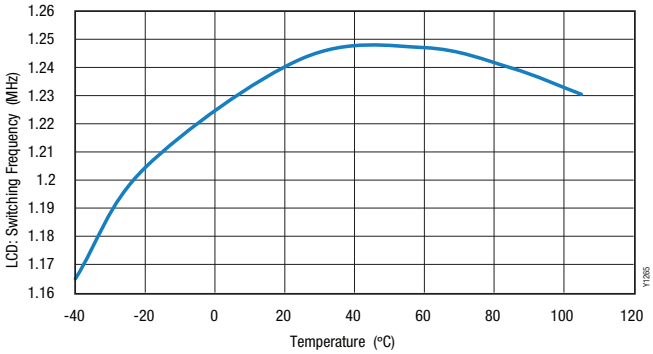


Figure 17. LCD: Switching Frequency vs. Temperature

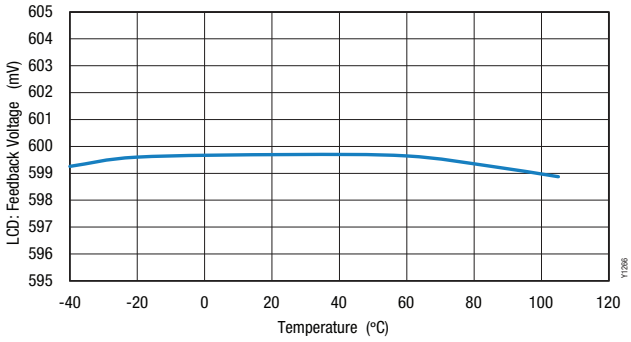


Figure 18. LCD: Feedback Voltage vs Temperature

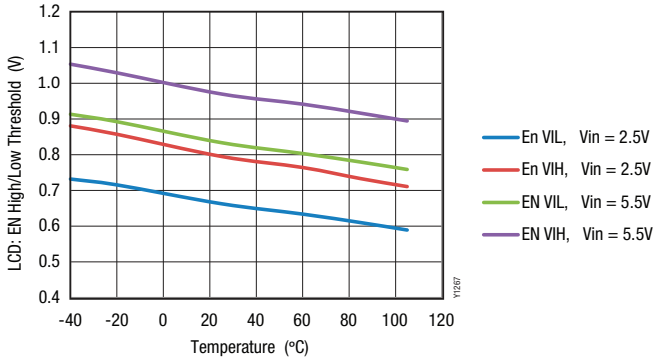


Figure 19. LCD: EN High/Low Threshold vs Temperature

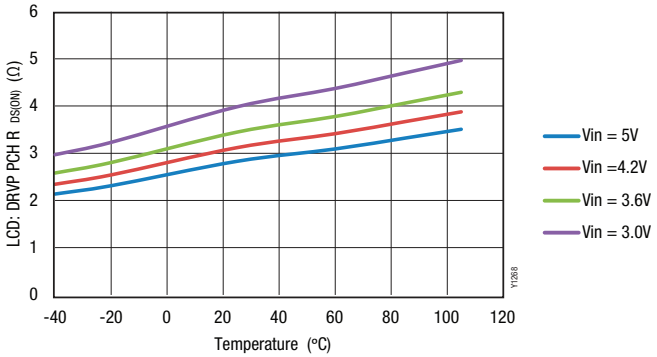


Figure 20. LCD: DRVP P Channel RDS(ON) vs Temperature

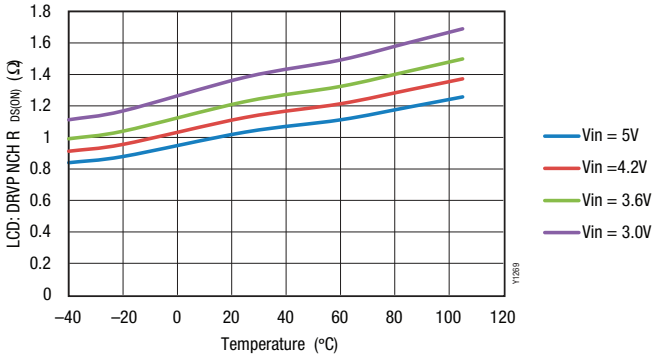


Figure 21. LCD: DRVP N Channel RDS(ON) vs Temperature

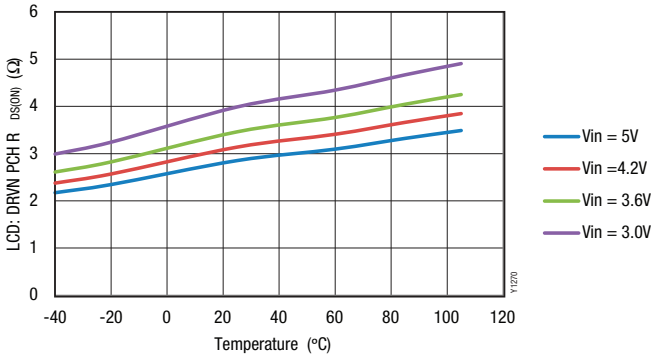


Figure 22. LCD: DRVN P Channel RDS(ON) vs Temperature

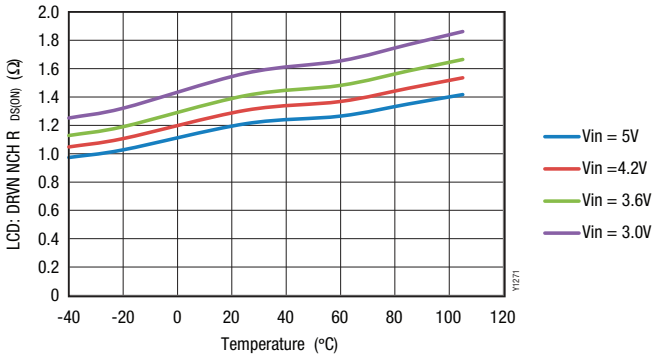


Figure 23. LCD: DRVN N Channel RDS(ON) vs Temperature

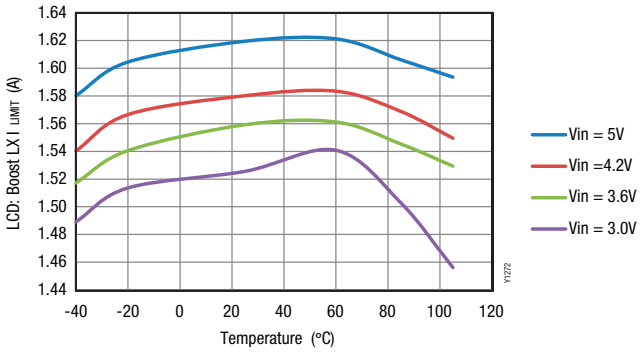


Figure 24. LCD: Boost LX ILIMIT vs Temperature

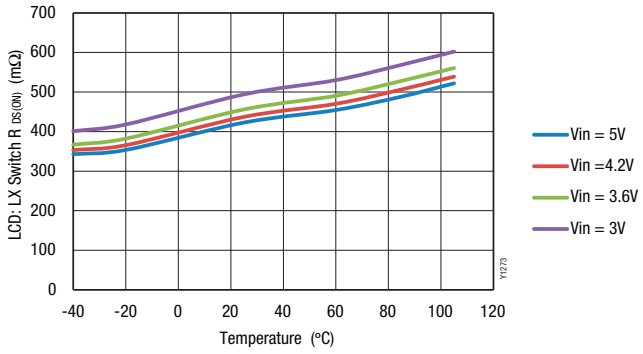


Figure 25. LCD: LX Switch RDS(ON) vs Temperature

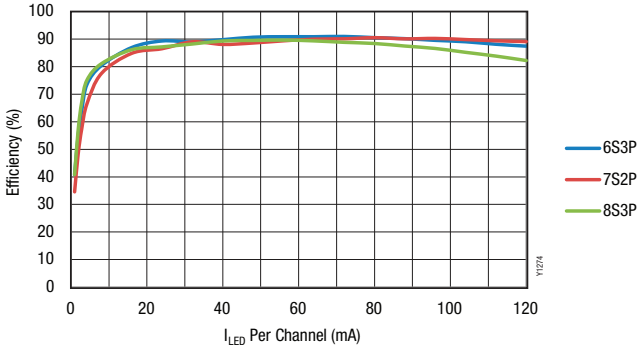


Figure 26. WLED: Boost Efficiency vs LED Configuration

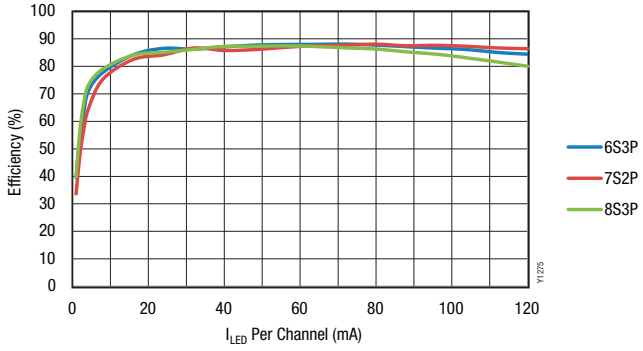


Figure 27. WLED: LED Efficiency vs LED Configuration

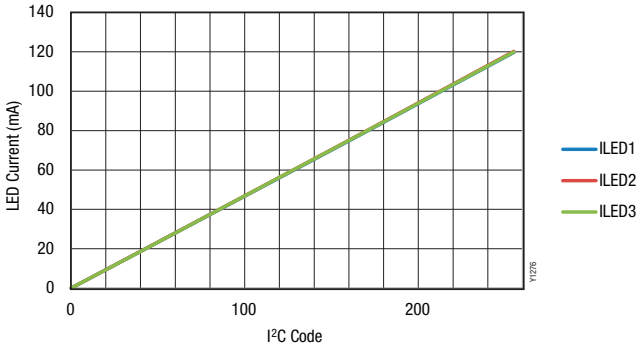


Figure 28. WLED: LED Current Accuracy (RSET = 23.2 kΩ)

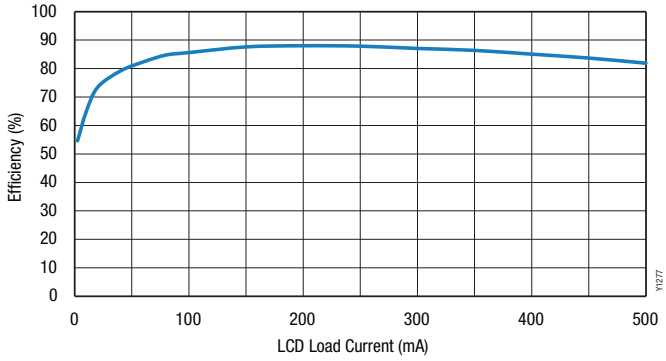


Figure 29. LCD: Efficiency

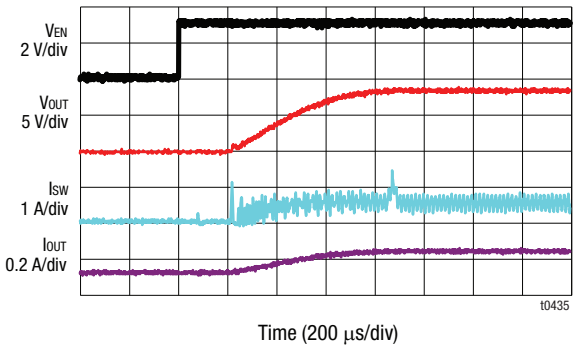


Figure 30. LCD: Enable Waveform (0.2 A Load)

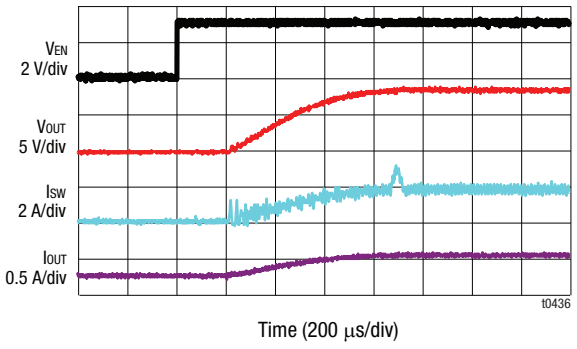


Figure 31. LCD: Enable Waveform (0.5 A Load)

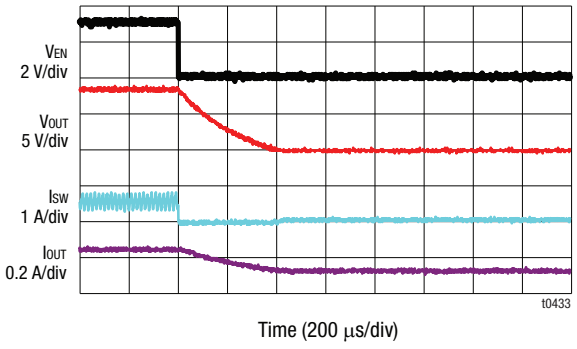


Figure 32. LCD: Disable Waveform (0.2 A Load)

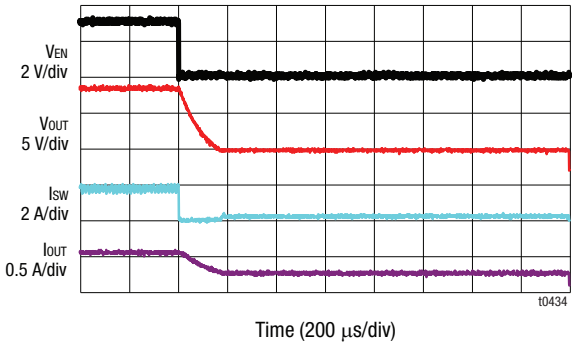


Figure 33. LCD: Disable Waveform (0.5 A Load)

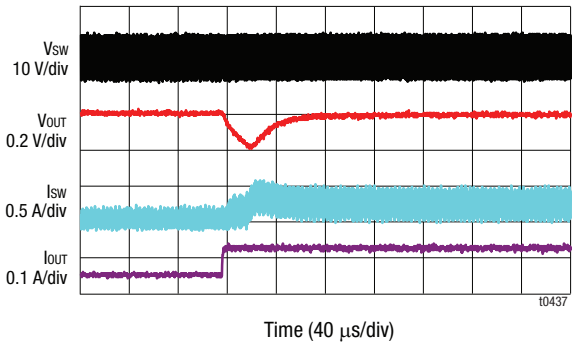


Figure 34. LCD: Load Transient (10 mA to 100 mA Load)

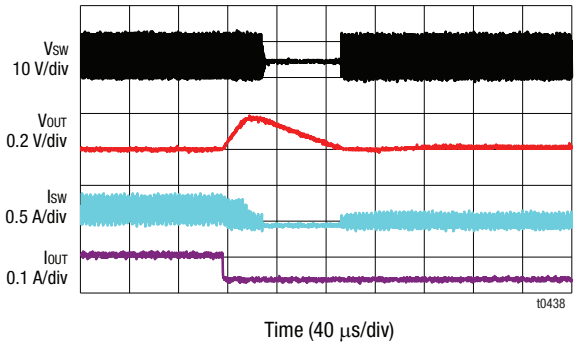


Figure 35. LCD: Load Transient (100 mA to 10 mA Load)

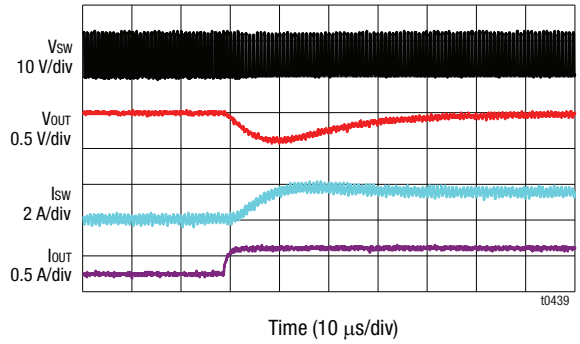


Figure 36. LCD: Load Transient (100 mA to 500 mA Load)

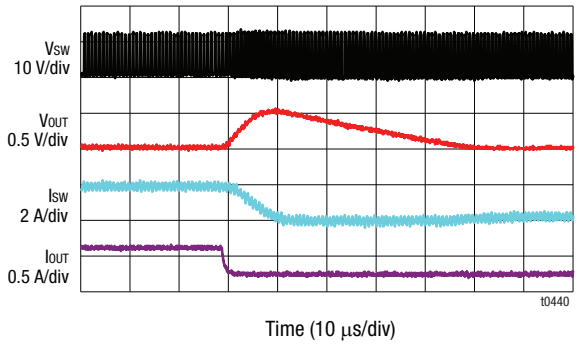


Figure 37. LCD: Load Transient (500 mA to 100 mA Load)

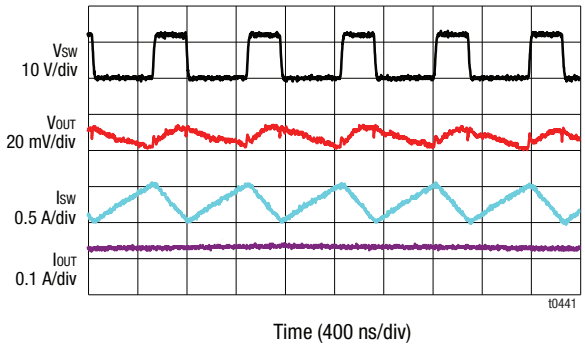


Figure 38. LCD: Work Waveform (0.1 A Load)

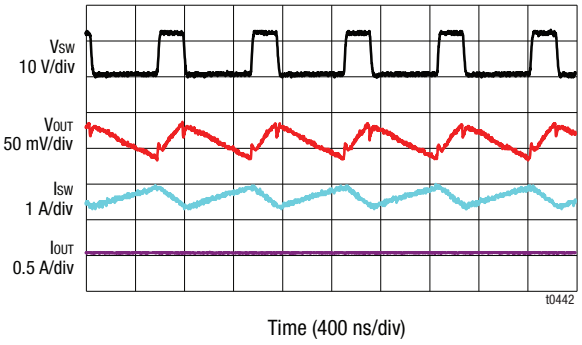


Figure 39. LCD: Work Waveform (0.5 A Load)

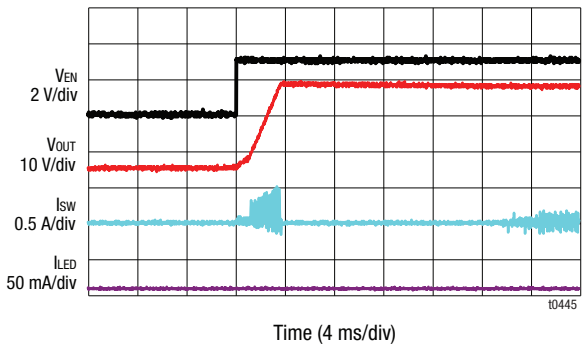


Figure 40. WLED: Enable via Enable Pin (60 mA Load)

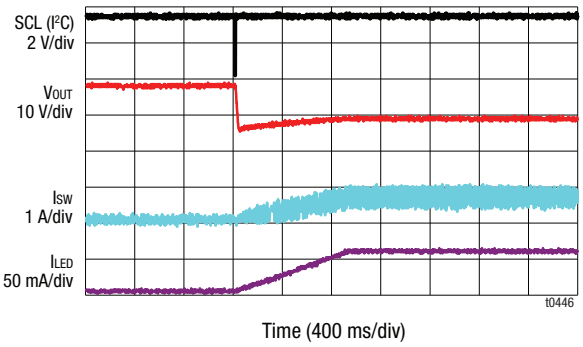


Figure 41. WLED: Enable via I²C interface (60 mA Load)

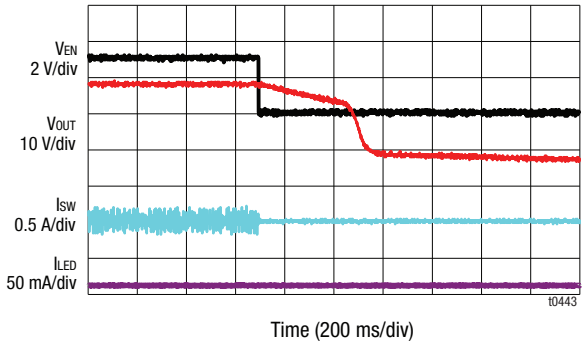


Figure 42. WLED: Disable via Enable Pin (60 mA Load)

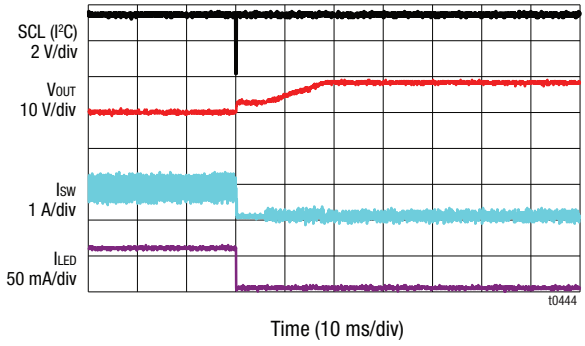


Figure 43. WLED: Disable via I²C interface (60 mA Load)

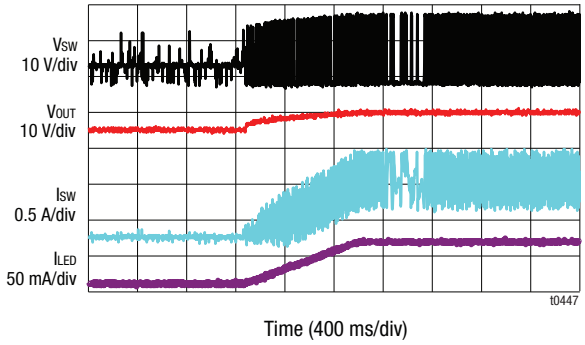


Figure 44. WLED: Load Transient (1 mA to 60 mA Load)

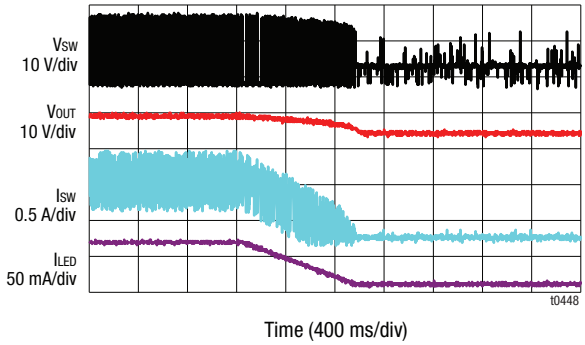


Figure 45. WLED: Load Transient (60 mA to 1 mA Load)

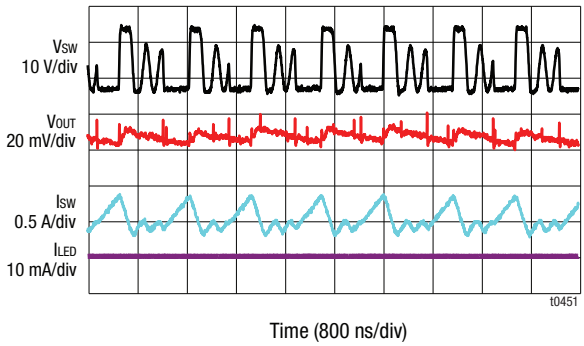


Figure 46. WLED: Work Waveform without PWM (10 mA Load)

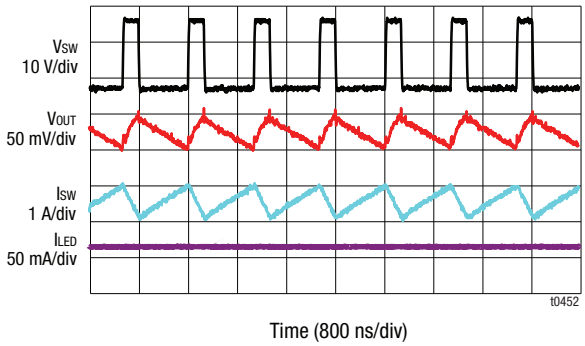


Figure 47. WLED: Work Waveform without PWM (60 mA Load)

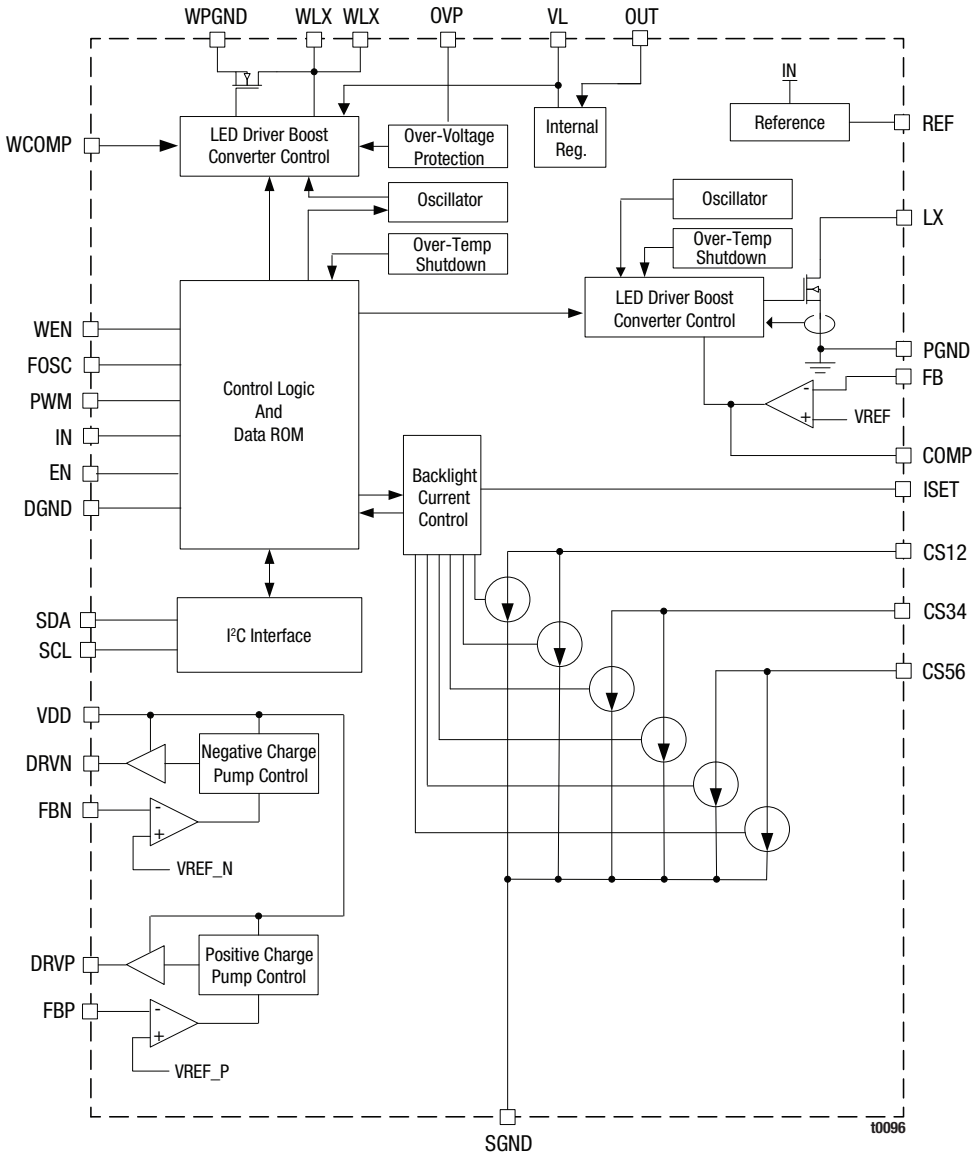


Figure 48. SKYA21004 Functional Block Diagram

Functional Description

A functional block diagram is provided in Figure 48.

Main Boost Converter

The main boost regulator contains a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads typical of TFT-LCD panel source drivers. The 1.3 MHz switching frequency allows the use of low-profile, low-value inductors and ceramic capacitors to minimize the thickness of LCD panel designs.

If the output of any of the regulators (AVDD or VGH or VGL) drops below the fault trip point for more than 200 msec, the AVDD boost turns off.

Setting the Output Voltage of Main Boost Converter

The resistive divider network of R20 and R22 (see Figure 56) programs the AVDD output to regulate at a feedback voltage of 0.6 V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R22 is 6.04 kΩ. The resistive divider can be calculated in the following equation:

$$R_{20} = R_{22} \times \left(\frac{V_{AVDD}}{V_{FB}} - 1 \right) = R_{22} \times \left(\frac{V_{AVDD}}{0.6\,V} - 1 \right)$$

Dual Charge-Pump Regulator

The SKYA21004 provides low-power regulated output voltages from two individual charge pumps to provide the VGH and VGL supplies. Using a single stage, the VGL charge pump inverts the supply voltage (VDD) and provides a regulated negative output voltage. The VGH charge pump doubles VDD and provides a regulated positive output voltage. These outputs use external Schottky diodes and capacitor multiplier stages (dependent upon the required output voltage) to regulate up to ±30 V. Integrated soft-start circuitry minimizes the start-up inrush current and eliminates output voltage overshoot across the full input voltage range and all load conditions. A constant switching frequency of 1.3 MHz minimizes output ripple and capacitor size.

Dual Charge-Pump Stages

The number of charge-pump stages required for a given output (VGH) varies with the input voltage applied (VAVDD) from the main boost. A lower input voltage requires more stages for a given output. If the number of stages increases, the maximum load current limitation of the charge pump decreases to maintain output voltage regulation.

The number of stages required can be estimated by:

For the positive output: $\eta_P = \frac{V_{GH} - V_{IN}}{V_{DD} - 2V_F}$

For the negative output: $\eta_N = \frac{V_{GL}}{2V_F - V_{DD}}$

Where:

VDD = VAVDD(MIN) – 2VF1 (V F1 = 0.7 V, the forward voltage of the 1N4148 diode [D2 and D3 in Figure 56] at 4 mA forward current).

VF = 0.31 V, the forward voltage of the BAT54 Schottky diode (D31, D32, D33, and D34 in Figure 56) at 4 mA forward current.

When solving for n_P and n_N, round up the calculated result to the next integer number to determine the number of stages required.

Negative Output Voltage (Vgl)

The negative output voltage is adjusted by a resistive divider from the output (VGL) to the FBN and REF pins. The maximum REF output current is 200 µA; therefore, the minimum allowable value for R42 in Figure 56 is 6.04 kΩ. It is best to select the smallest value possible for R42 to keep the value of R40 to a minimum. With R42 selected, R40 can be determined:

$$R_{40} = \frac{V_{GL}}{V_{REF}} \times R_{42} = \frac{V_{GL}}{1.2\ V} \times R_{42}$$

Positive Output Voltage (Vgh)

The positive output voltage is set by a resistive divider from the output (VGH) to the FBP and ground pins. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R32 is 6.04 kΩ.

Once R32 is determined, calculate the value for R30:

$$R_{30} = R_{32} \times \left(\frac{V_{GH}}{V_{FBP}} - 1 \right) = R_{32} \times \left(\frac{V_{GH}}{0.6\ V} - 1 \right)$$

LED Driver

The SKYA21004 drives up to three strings of backlight LEDs with a boost converter.

The integrated high voltage boost (step-up) converter is designed to drive multiple strings of series LEDs. The maximum number of LEDs that can be driven by this device depends on the current limit and the voltage rating of the boost. The SKYA21004 LED driver can drive up to 28 V (up to about 7 or 8 series LEDs). The boost switch current limit can be set to a minimum of either 2.75 A or 2.30 A to optimize the boost operation for a given application.

Three precision current sinks provide a constant current drive to each LED string. The full-scale LED current is set by a single external resistor and may be programmed from 30 mA to 120 mA per string. The full-scale LED current is programmed according to the following equation:

$$R_{SET} = \frac{600\ mV}{I_{CH\_MAX}\ (mA)} \times \frac{51\ k\Omega}{11}$$

The controller derives output feedback from the current sink channel with the lowest current sink voltage while maintaining the programmed current for each LED string. The LED string current sink with the lowest operation voltage represents the LED string with the greatest summed LED forward voltage (VF) for the given operation condition. This ensures that the system can operate with the lowest possible boost converter output voltage and highest efficiency for continuous operation with potentially mismatched LED strings.

The SKYA21004 LED driver block is designed for maximum flexibility to allow unused current sinks to be disabled by hardware configuration by connecting them to ground. The SKYA21004 can also disable the unused current sinks through software configuration. The maximum number of LEDs per channel is set by the LED VF and the maximum output voltage of the DC/DC switching boost converter.

The boost switching frequency can be adjusted from 600 kHz to 2 MHz using the FOSC signal for optimum efficiency and the smallest external components. The relationship between external set resistor (RFOSC) and switching frequency is shown in Figure 49 and Table 5.

Open/short LED protection circuitry protects the system from LED fault damage.

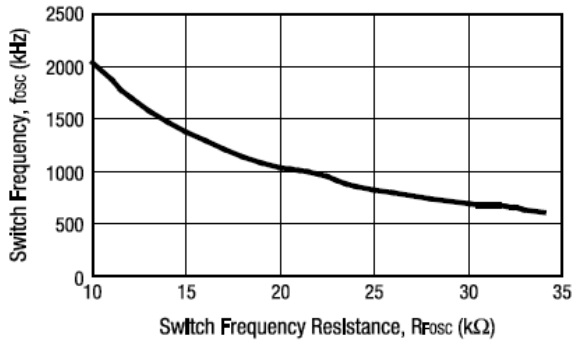


Figure 49. Relationship between External Set Resistor (RFOSC) and Switching Frequency

Table 5. Switching Frequency vs RFOSC

fosc (kHz)	RFOSC (kΩ)	fosc (kHz)	RFOSC (kΩ)
2034	10	856	24
1704	12	791	26
1466	14	737	28
1293	16	687	30
1136	18	664	32
1035	20	627	33
974	22	608	34

PWM Dimming

After the PWM signal is applied, the channels start to follow the PWM signal with the maximum LED current determined by the RSET resistor value. The maximum LED current can be programmed from 30 mA to 120 mA by changing the RSET resistance. The PWM input signal frequency range is 100 Hz to 25 kHz. In the direct PWM (DPWM-bit[4], PWMMD, in the Control Register, REG2, is set as 1), dimming mode, the LED current is set by using data in the Current Sink Dimming Register, REG0, and the RSET resistance. The DPWM frequency and duty follows the PWM signal. In the analog dimming mode (APWM-bit[4], PWMMD, in the Control Register, REG2, is set as 0), the LED current is set by multiplying the PWM duty, REG0 data, and the RSET resistance. For example, if the PWM duty is 50 percent and REG0 data is set to 50 percent (0x80), the output current is 25 percent of the maximum LED current, which is set by the RSET resistance. When the PWM signal is not used, it should be pulled high. To ignore the PWM signal for the dimming control, set IGPW (bit[5] in the Control Register, REG2). A change to the PWM duty is applied to the output on the next rising edge of the PWM. In the phase-delay mode, the other channels follow the preceding channel with a delay. The PWM signal has hysteresis (typically 0.5 percent) on the duty information that allows the signal not to respond to input jitter. This signal also has a 40-ns deglitch filter.

Fault Protection of LED Driver

The SKYA21004 LED driver is protected from system faults caused by open or shorted LED strings, over-temperature operation, boost converter over-current limit or boost converter output over-voltage conditions. The integrated thermal shutdown, over-voltage protection, and over-current limit protection are designed to prevent catastrophic damage to the system. An open LED condition is detected by the internal system control circuit at startup by monitoring a low voltage on each LED current sink and disabling the open current sink while LED strings operating normally continue to operate. A disabled LED string remains disabled until the WEN signal or power is cycled. A shorted LED string condition results in a higher voltage appearing on the current sink of the affected channel. That current sink dissipates additional power since the voltage increases. To prevent thermal shutdown, the shorted LED string is disabled while normal operating strings continue to function. The shorted LED string remains disabled until a power-on or an LED driver enable (WEN) is cycled

The SKYA21004 LED driver has a programmable boost current limit to optimize the inductor for the given applications. The default value is 2.75 A (minimum) and the boost current limit can be switched to 2.30 A on an I²C interface.

The over-voltage protection of the SKYA21004 LED driver can prevent the LED driver output from rising over the preprogrammed OVP threshold level, and the OVP threshold level can be set through external OVP set-up resistors.

The OVP threshold level is set according to the following equation:

$$V_{OVP} = \frac{1V \times (R1 + R2)}{R2}$$

Register Programming

The SKYA21004 LED driver is programmed using an I²C interface. There are five programming registers to program the LED driver block. Programming functions are described in Table 6. Each register is 8 bits, as defined in Tables 7 through 11.

I2C Interface Protocol

The I²C protocol uses two open-drain inputs: serial data line (SDA) and serial clock line (SCL). The I²C protocol is bidirectional.

Devices on the I²C bus can either be a master or a slave. Both master and slave devices can send and receive data over the bus, but the master device controls all communication on the bus.

Bus communications begin by the master initiating a "start" condition. Next, the master transmits the 7-bit slave address and a read/write bit (R/W). Each slave device on the bus has a unique address. The 7-bit slave address of the SKYA21004 is 0x2C (0101100b).

An I²C interface timing diagram is shown in Figure 50. A Start and Stop timing diagram is shown in Figure 51.

Figures 52 and 53 illustrate the bit transfer of device addresses and data.

Start and Stop Conditions

"Start" and "stop" conditions are always generated by the master. Before initiating a "start," both the SDA and SCL pins are inactive and are pulled high through external pull-up resistors.

As shown in Figure 51, a "start" condition occurs when the master pulls the SDA line low. After the "start" condition hold time (t_{HD_STA}), the master strobes the SCL line low. A "start" condition acts as a signal to devices on the bus that the device producing the "start" condition is active and will be communicating on the bus.

A "stop" condition, as shown in Figure 51, occurs when the SCL signal changes from low to high after the "stop" condition setup time (t_{SU_STO}), by an SDA low-to-high transition. The master does not issue an Acknowledge (ACK) signal but does release SCL and SDA.

Transferring Device Address and Data

Addresses and data are sent with the Most Significant Bit (MSB) transmitted first and the Least Significant Bit (LSB) transmitted last. After each address or data transmission, the target device transmits an ACK signal to indicate that it has received the transmission. The ACK signal is generated by the target after the master releases the SDA data line by driving SDA low.

Write to Slave Device

When the read/write bit is cleared and the address transmitted by the master matches the address of the slave device, the slave device transmits an ACK signal to indicate that it is ready to receive data.

Next, the master transmits the 8-bit register address, and the slave device transmits an ACK signal to indicate that it received the register address. The master transmits the 8-bit data word, and, again, the slave device transmits an ACK signal indicating that it received the data. This process continues until the master finishes writing to the slave device, at which time the master generates a "stop" condition.

A write timing diagram is presented in Figure 54.

Read from Slave Device

When the read/write bit is set and the address transmitted by the master matches the address of the slave device, the slave device transmits an ACK signal to indicate that it is ready to receive data.

Next, the slave device transmits the 8-bit data word, and the master reads the data byte and transmits an ACK signal to indicate that it received the byte. Finally, the master generates a "stop" condition.

A read timing diagram is presented in Figure 55.

Table 6. Register Programming Functions

Register										
Name	*Location (HEX)*	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
REG0	00	Current sink dimming	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]
REG1	01	Channel enable	X	X	EN1[1]	EN1[0]	EN2[1]	EN2[0]	EN3[1]	EN3[0]
REG2	02	Control	X	X	IGPW	PWMMD	PHASE	ILIM	SHRT[1]	SHRT[0]
REG3	03	Reserved	X	X	X	X	X	X	X	X
REG4	04	Fault	OCP	OTMP	SHRT1	SHRT1	SHRT2	SHRT2	SHRT3	SHRT3
REG5	05	Fault	X	X	OPEN1	OPEN1	OPEN2	OPEN2	OPEN3	OPEN3

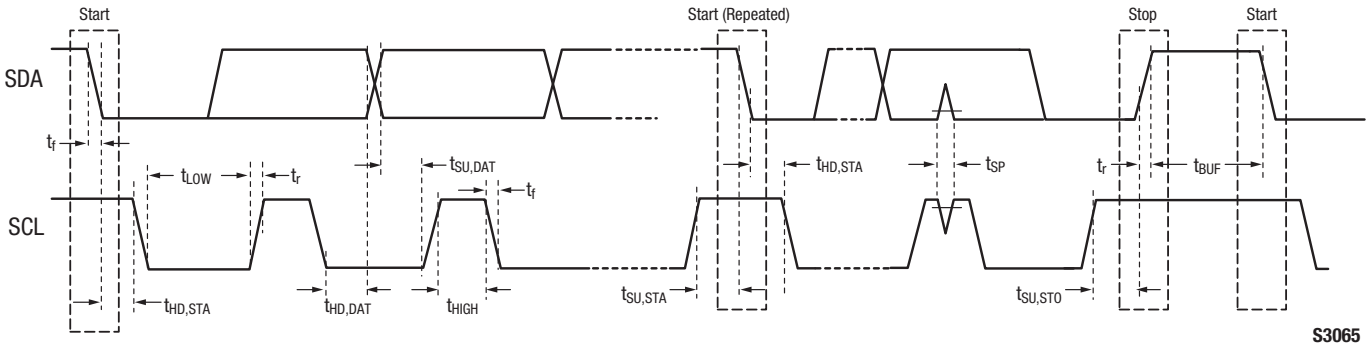


Figure 50. I²C Interface Timing Diagram

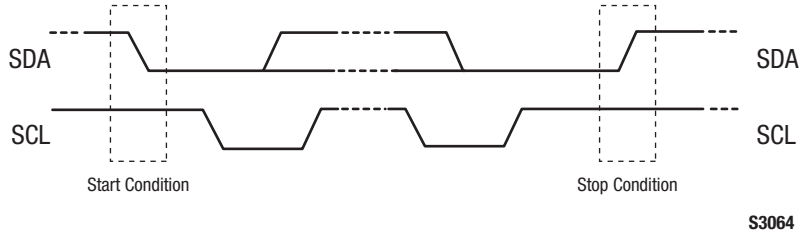


Figure 51. I²C Interface Start and Stop Timing Diagram

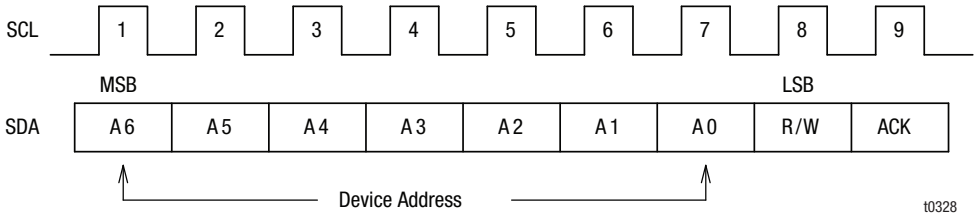


Figure 52. I²C Device Address Transmission

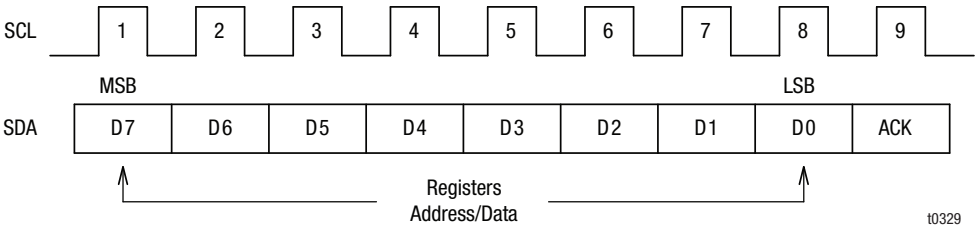


Figure 53. I²C Device Data Transmission

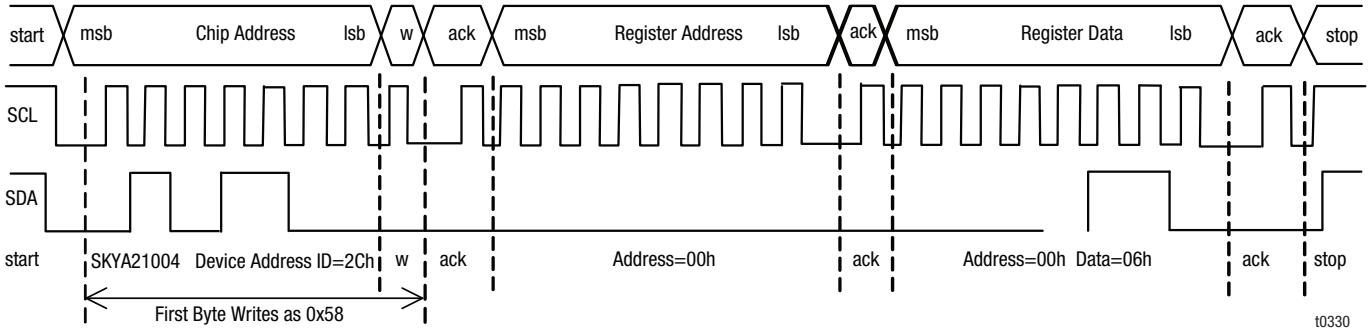


Figure 54. I²C Write Timing Diagram

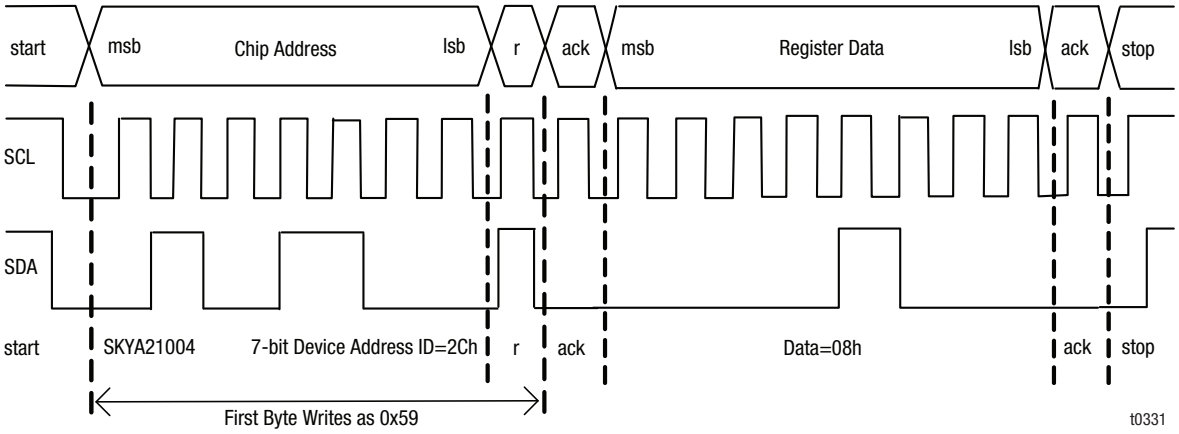


Figure 55. I²C Read Timing Diagram

Table 7. Current Sink Dimming Register, REG0

Parameter	Function	State Description	Default
CS	Current Sink Dimming	Bits[7:0]; 00000000 = 0% of maximum LED current ••• 11111111 = 100% of maximum LED current	11111111

Table 8. Channel Enable Register, REG1

Parameter	Function	State Description	Default
RSVD	Reserved	Bits[7,6]	00
EN1[1:0]	Channel 1 enable	Bits[5:4]; 00: fully turn off 01, 10: half turn on 11: fully turn on	00
EN2[1:0]	Channel 2 enable	Bits[3:2]; 00: fully turn off 01, 10: half turn on 11: fully turn on	00
EN3[1:0]	Channel 3 enable	Bits[1:0]; 00: fully turn off 01, 10: half turn on 11: fully turn on	00

Table 9. Control Register, REG2

Parameter	Function	State Description	Default
RSVD	Reserved	Bits[7,6]	00
IGPW	Ignore PWM input	Bit[5]; 0: receive PWM input 1: ignore PWM input	0
PWMMD	PWM dimming mode	Bit[4] 0: APWM 1: DPWM	0
PHASE	Phase shift enable	Bit[3]; 0: phase shift enable 1: phase shift disable	0
ILIM	LED driver boost current limit	Bit[2]; 0: 2.75A(min) 1: 2.3A(min)	0
SHRT[1:0]	LED short detection voltage	Bit[1,0]; 00 = 7 V 01 = 6 V 10 = 5 V 11 = 4 V	00

Table 10. Fault Register 1, REG4

Parameter	Function	State Description	Default
OCP	LED driver boost over current	Bit[7]	0
OTMP	LED driver over-temperature	Bit[6]	0
SHRT1	CH1 LED short detect	Bits[5:4]; 00: CH1 no short 11: CH1 short detect	00
SHRT2	CH2 LED short detect	Bits[3:2]; 00: CH2 no short 11: CH2 short detect	00
SHRT3	CH3 LED short detect	Bits[1:0]; 00: CH3 no short 11: CH3 short detect	00

Table 11. Fault Register 2, REG5

Parameter	Function	State Description	Default
RSVD	Reserved	Bit[7:6]	00
OPEN1	CH1 LED open detect	Bits[5:4]; 00: CH1 no open 11: CH1 open detect	00
OPEN2	CH2 LED open detect	Bits[3:2]; 00: CH2 no open 11: CH2 open detect	00
OPEN3	CH3 LED open detect	Bits[1:0]; 00: CH3 no open 11: CH3 open detect	00

Evaluation Board Description

The SKYA21004 Evaluation Board is used to test the performance of the SKYA21004. An Evaluation Board schematic diagram is provided in Figure 56. Layer details for the Evaluation Board are shown in Figures 57.

Package Dimensions

Typical part markings are shown in Figure 58. Package dimensions for the 36-pin QFN package are shown in Figure 59. Tape and reel dimensions are shown in Figure 60.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKYA21004 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

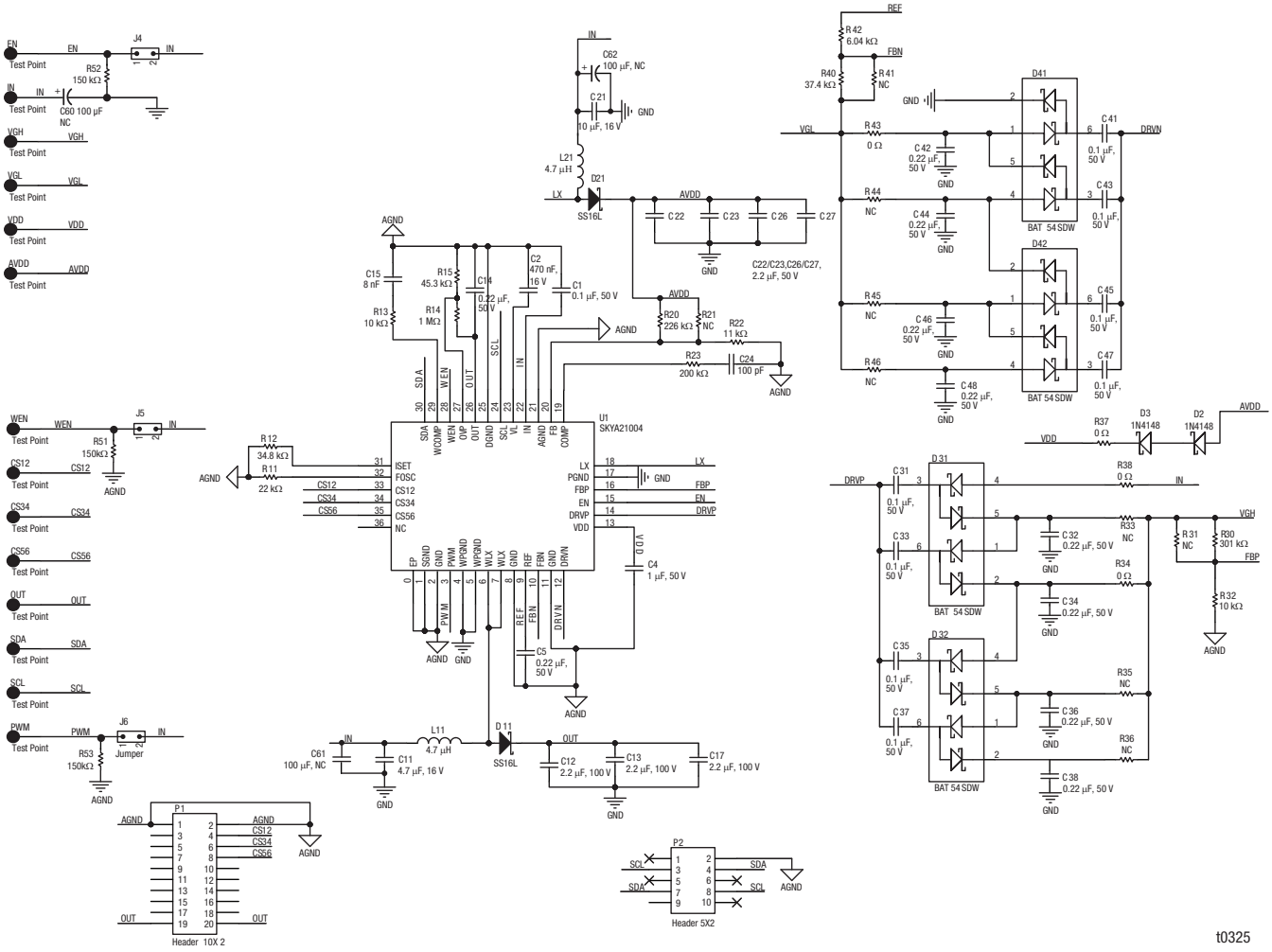


Figure 56. SKYA21004 Evaluation Board Schematic

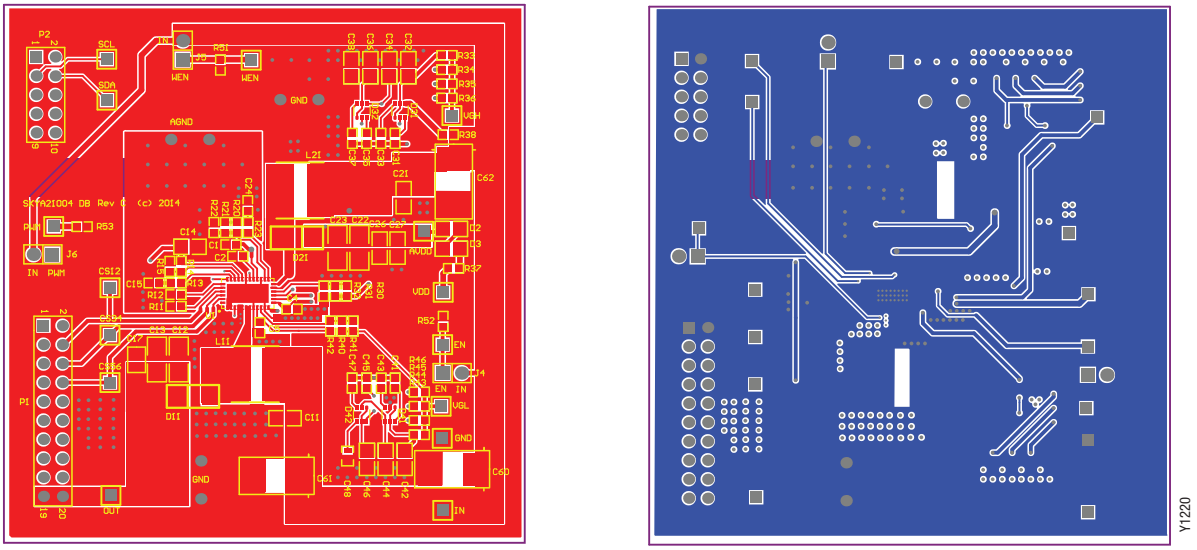


Figure 57. SKYA21004 Evaluation Board Layer Details

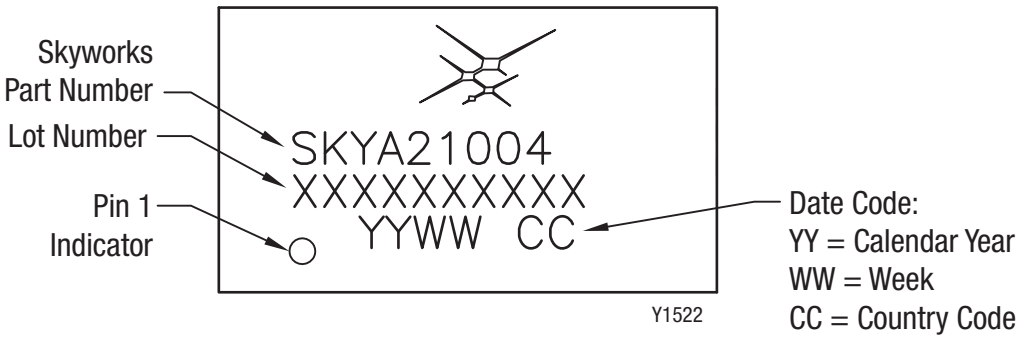
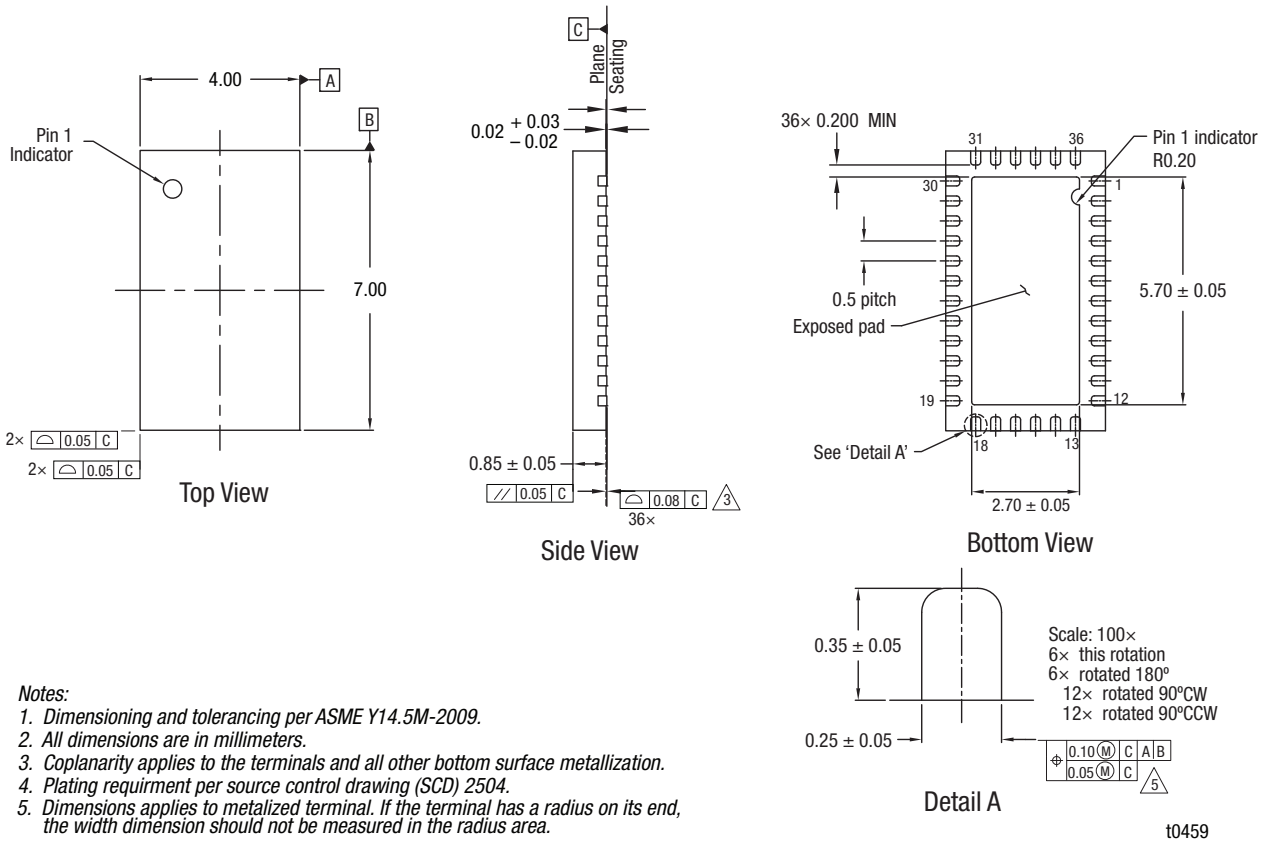
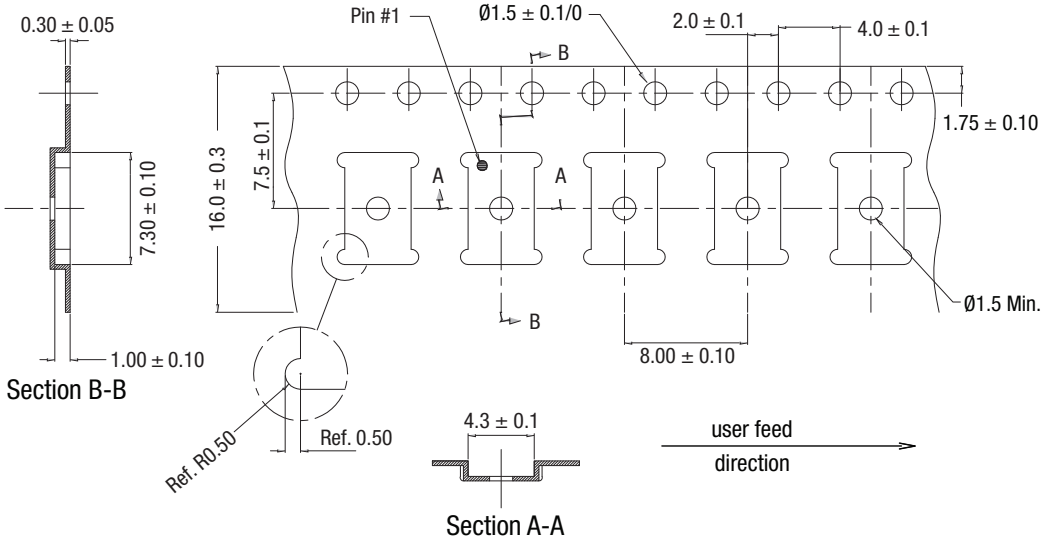


Figure 58. Typical Part Markings (Top View)



Notes:
1. *Dimensioning and tolerancing per ASME Y14.5M-2009.*
2. *All dimensions are in millimeters.*
3. *Coplanarity applies to the terminals and all other bottom surface metallization.*
4. *Plating requirment per source control drawing (SCD) 2504.*
5. *Dimensions applies to metalized terminal. If the terminal has a radius on its end, the width dimension should not be measured in the radius area.*

Figure 59. SKYA21004 36-Pin QFN Package Dimensions



Notes:
1. *Carrier tape must meet all requirements of Skyworks GP01-D232 procurement spec for tape and reel shipping.*
2. *Carrier tape shall be black conductive polystyrene.*
3. *ESD-surface resistimity shall be <1x10[10] ohms/square per EIA JEDEC TNR specification.*
4. *Cumulative tolerance of 10 sprocket holes pitch is ±0.20 mm.*
5. *All measurements are in millimeters.*

t0327

Figure 60. SKYA21004 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKYA21004: Three-Channel LCD Bias Power Management IC with Three-Channel High Efficiency White LED Driver	SKYA21004	SKYA21004-EVB