3 A Current Mode Constant On-Time Synchronous Buck Regulator

DESCRIPTION

The SiP12117 is a high frequency current-mode constant on-time (CM-COT) synchronous buck regulator with integrated high-side and low-side power MOSFETs. Its power stage is capable of supplying up to 3 A continuous current at 600 kHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 4.5 V to 15 V input rail to accommodate a variety of applications, including consumer electronics, computing, telecom, and industrial.

SiP12117's CM-COT architecture delivers ultrafast transient response and low ripple over the full load range with minimum output capacitance and no ESR requirements. The device features a built in soft start of 2.9 ms and integrated compensation.

The device also includes cycle-by-cycle current limit, over temperature protection (OTP) and input under-voltage lockout (UVLO).

The SiP12117 is available in lead (Pb)-free 3 mm x 3 mm DFN 10 lead package with thermal pad.

FEATURES

- 4.5 V to 15 V input voltage
- Adjustable output voltage down to 0.6 V
- 3 A continuous output current
- Integrated compensation
- 600 kHz switching frequency
- Ultrafast transient response
- < 5 µA typical shutdown current
- Cycle by cycle current limit
- Power good function
- Fixed soft start: 2.9 ms, typ.
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Graphics cards
- Set-top-box
- LCD TV
- Notebook computers
- HDD / SSD

TYPICAL APPLICATION CIRCIUT AND PACKAGE OPTIONS

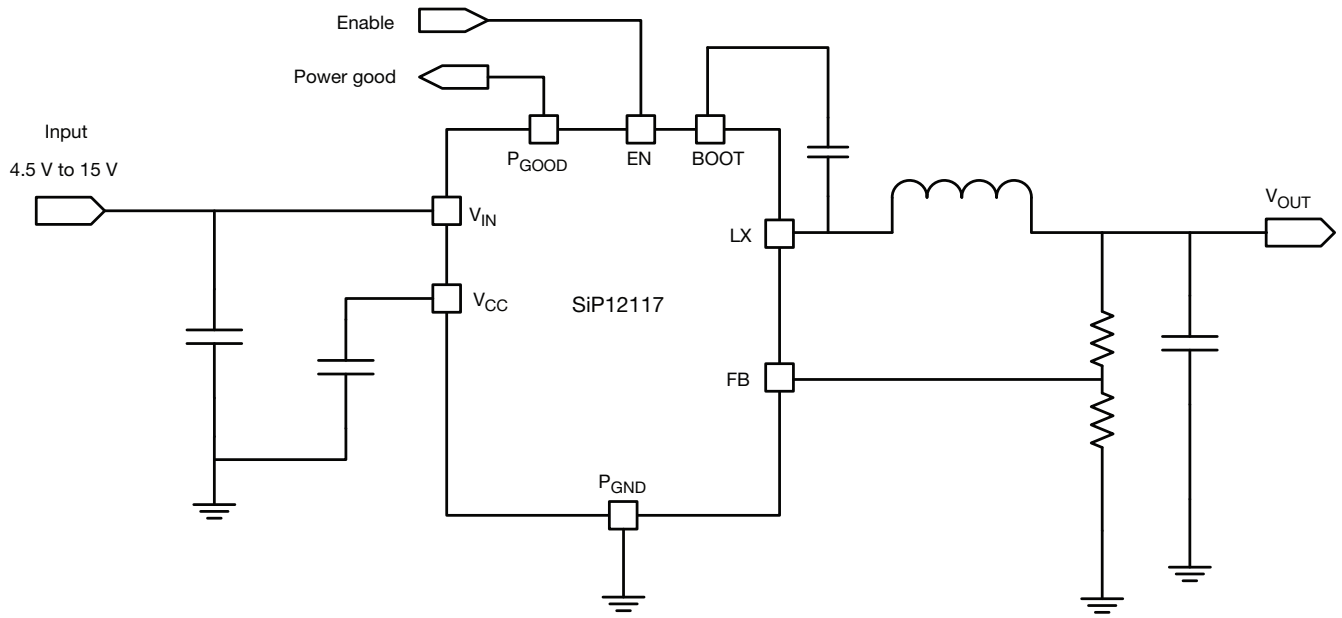


Fig. 1 - Typical Application Circuit for SiP12117

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PIN CONFIGURATION

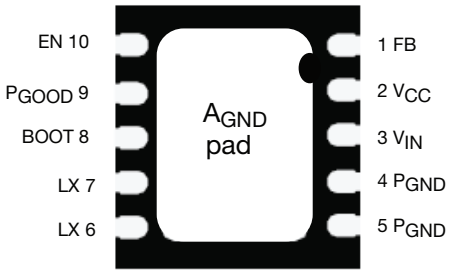
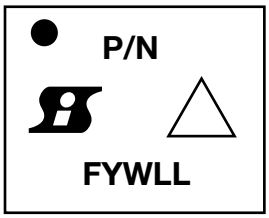


Fig. 2 - SiP12117 Pin Configuration (Bottom View)

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1	FB	Feedback voltage 0.6 V (typ.) input. Use a resistor divider between V_{OUT} and thermal pad to set the output voltage
2	V_{CC}	Internal regulator output
3	V_{IN}	Input supply voltage for power MOS and regulator. V_{IN} = 4.5 V to 15 V
4, 5	P_{GND}	Power ground
6, 7	LX	Switching node, inductor connection point
8	BOOT	Bootstrap pin - connect a capacitor of at least 100 nF from BOOT to LX to develop the floating supply for the high-side gate driver
9	P_{GOOD}	Power good output. Open drain
10	EN	Enable input. Pull enable above 1.5 V to enable and below 0.4 V to disable the part. Do not float this pin
Pad	A_{GND}	Analog ground. The pad also improves thermal performance

ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING (LINE 1: P/N)**
SiP12117DMP-T1-GE4	DFN10 3 x 3	2117
SiP12117DB	Reference board	

MARKING



Format:

Line 1: Dot
Line 2: P/N
Line 3: Siliconix logo + ESD dymbol
Line 4: Factory code + year code + work week code + LOT code

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ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMIT**	**UNIT**
V_{IN}	Reference to P_{GND}	-0.3 to +16	V
V_{CC}	Reference to A_{GND}	-0.3 to +6	
LX	Reference to P_{GND}	-1 to +16	
LX (AC)	100 ns	-2 to +17	
	10 ns	-6 to +17	
BOOT	Reference to P_{GND}	-0.3 to V_{IN} + V_{CC}	
All Logic Input and Output (EN, FB, P_{GOOD})	Reference to A_{GND}	-0.3 to V_{CC} + 0.3	
TEMPERATURE			
Junction Temperature		-40 to +150	°C
Storage Temperature		-65 to +150	
POWER DISSIPATION			
Junction to Ambient Thermal Impedance (R_{thJA})		36.3	°C/W
ESD PROTECTION			
Electronic Discharge Protection	HBM	2	kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (all voltages referenced to GND = 0 V)				
ELECTRICAL PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**UNIT**
V_{IN}	4.5	-	15	V
V_{OUT}	0.6	-	5.5	
TEMPERATURE				
Recommended Ambient Temperature	-40 to +85			°C
Operating Junction Temperature	-40 to +125			

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ELECTRICAL SPECIFICATIONS (test condition unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITION** V_{IN} = 12 V, T_A = -40 °C to +85 °C	**LIMITS**			**UNIT**
			MIN.	**TYP.**	**MAX.**	
POWER SUPPLY						
Input Voltage	V_{IN}		4.5	-	15	V
V_{CC} Voltage	V_{CC}		-	5	-	
Input Current	IV_{IN_NOLOAD}	T_A = 25 °C, non-switching, no load	-	1.5	-	mA
Shutdown Current	IV_{IN_SHDN}	EN = 0 V	-	5	10	µA
V_{IN} U_{VLO} Threshold	V_{IN_UVLO}	Rising edge	-	2.8	-	V
V_{IN} U_{VLO} Hysteresis	$V_{IN_UVLO_HYS}$		-	550	-	mV
CONTROLLER AND TIMING						
Feedback Voltage	V_{FB}	T_A = 25 °C	588	600	612	mV
		T_A = -40 °C to +85 °C	585	600	615	
V_{FB} Input Bias Current	I_{FB}		-	-	100	nA
On-Time (600 kHz)	t_{ON}	V_{IN} = 12 V, (V_{OUT} = 1 V)	-	138	-	ns
Soft Start Timing (1)			-	2.9	5	ms
POWER MOSFETs						
High-Side On Resistance	R_{ON_HS}	V_{GS} = 5 V	-	85	140	mΩ
Low-Side On Resistance	R_{ON_LS}		-	55	105	
FAULT PROTECTIONS						
Over Current Limit	I_{OCP}	Inductor valley current, T_A = 25 °C	3.6	4.25	5.1	A
Over Temperature Protection (1)		Rising temperature	-	145	-	°C
		Hysteresis	-	35	-	
POWER GOOD						
Power Good Output Threshold	$V_{FB_RISING_VTH_OV}$	Rising (% V_{OUT})	-	95	-	%
	$V_{FB_FALLING_VTH_UV}$	Falling (% V_{OUT})	-	-10	-	
Power Good Pull Low Resistance	R_{ON_PGOOD}		-	28	50	Ω
Power Good Delay Time	t_{DLY_PGOOD}		-	8	-	µs
ENABLE THRESHOLD						
Logic High Level	V_{EN_H}		1.5	-	-	V
Logic Low Level	V_{EN_L}		-	-	0.4	

Note

(1) Not tested, guaranteed by design.

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FUNCTIONAL BLOCK DIAGRAM

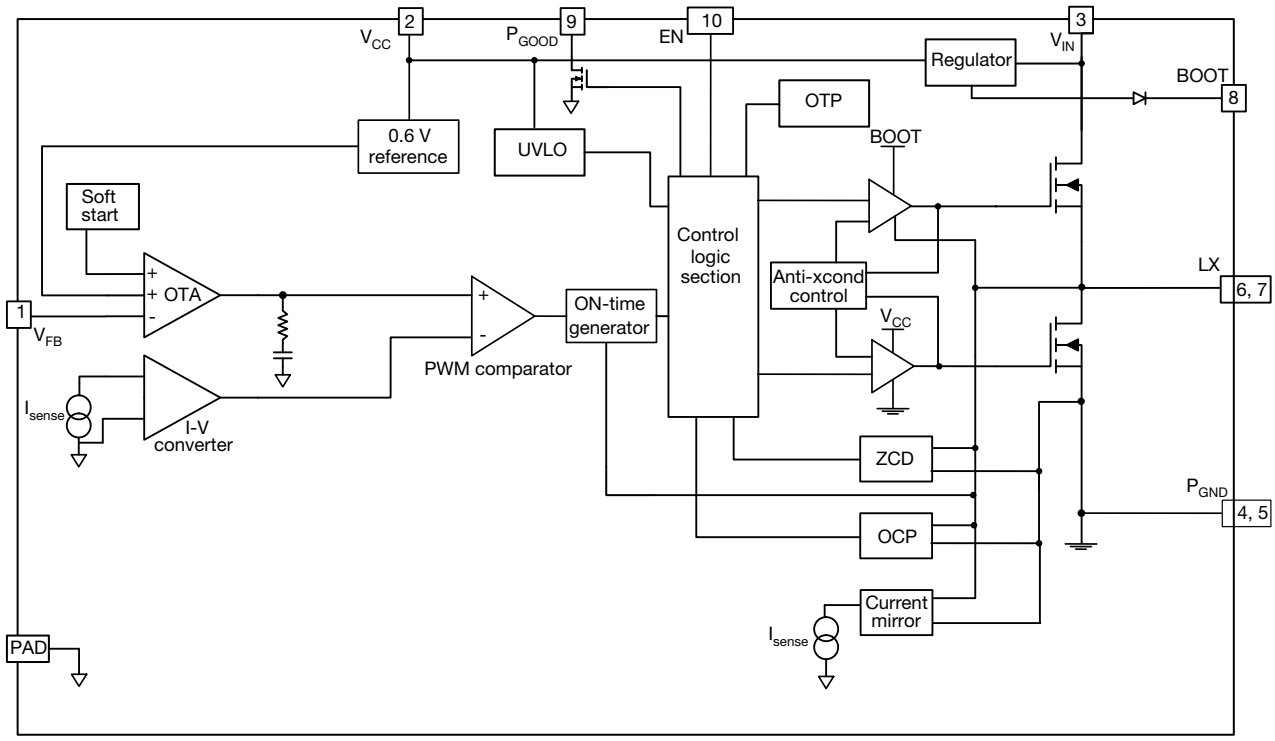


Fig. 3 - SiP12117 Functional Block Diagram

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ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1 V, L = 1.5 µH, C = 3 x 22 µF (ceramic), unless noted otherwise)

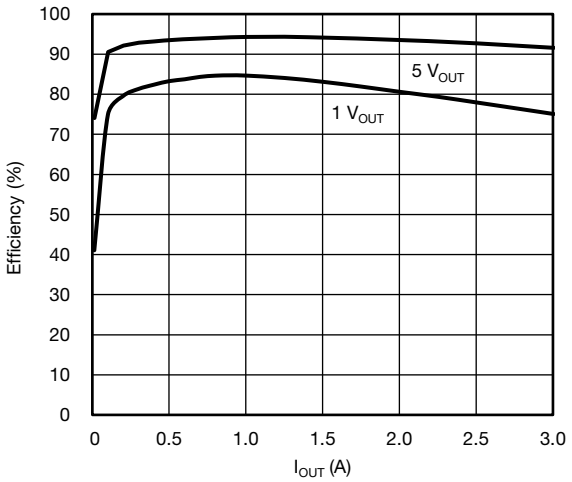


Fig. 4 - Efficiency vs. I_{OUT}

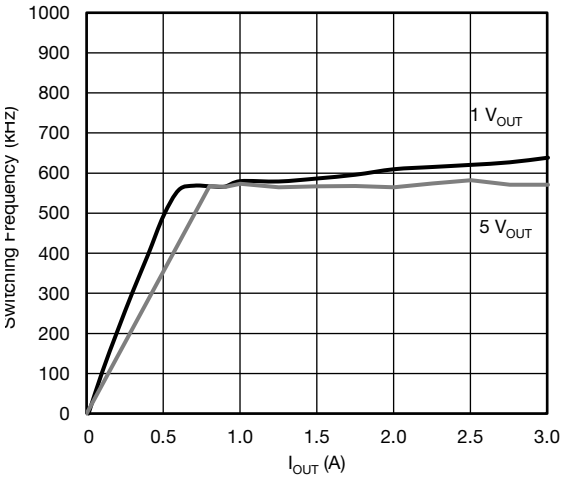


Fig. 5 - Frequency Variation vs. I_{OUT}

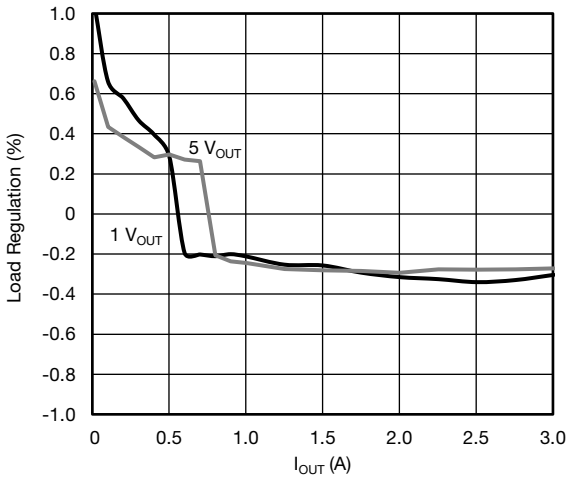


Fig. 6 - Load Regulation vs. I_{OUT}

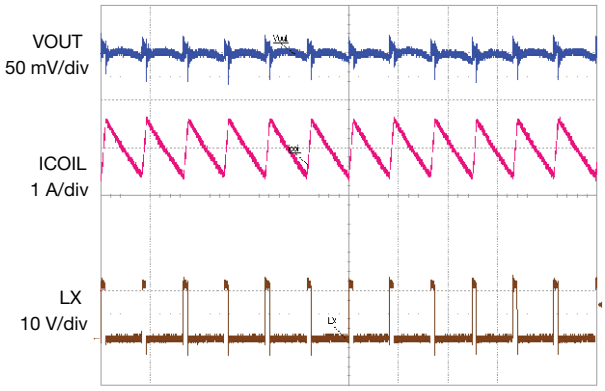


Fig. 7 - Steady-State, I_{OUT} = 3 A
Time = 2 µs/div

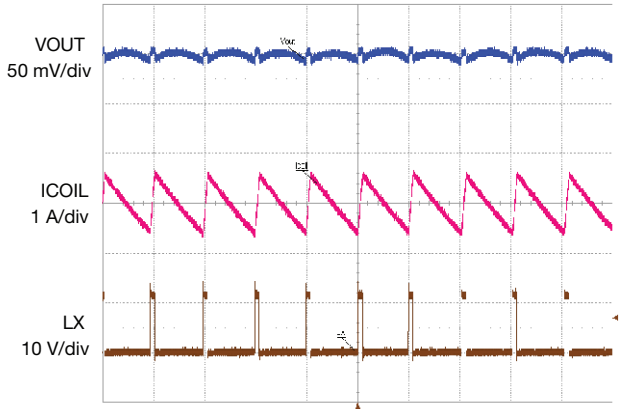


Fig. 8 - Steady-State, I_{OUT} = 0 A
Time = 2 µs/div

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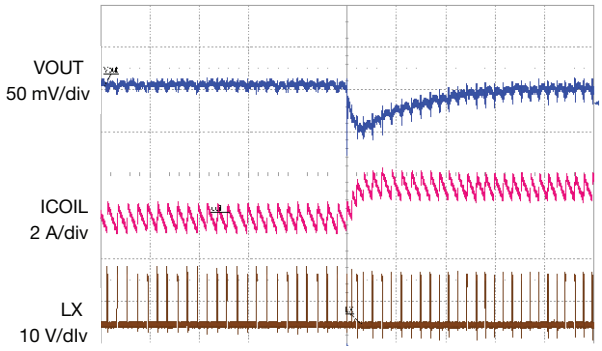


Fig. 9 - Load Step Undershoot Response, I_{OUT} = 0 A to 1.5 A
Time = 10 µs/div

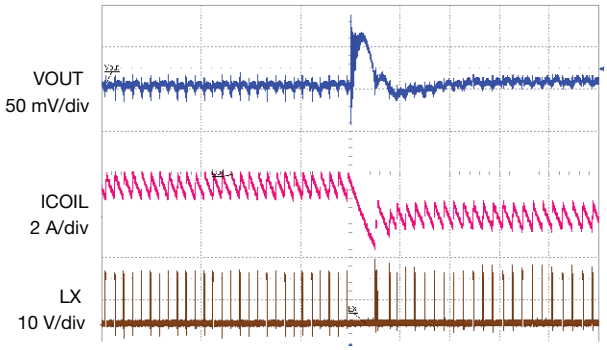


Fig. 12 - Load Step Overshoot Response, I_{OUT} = 1.5 A to 0 A
Time = 10 µs/div

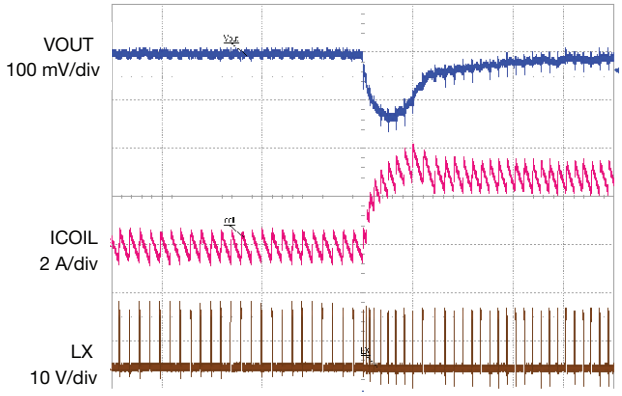


Fig. 10 - Load Step Undershoot Response, I_{OUT} = 0 A to 3 A
Time = 10 µs/div

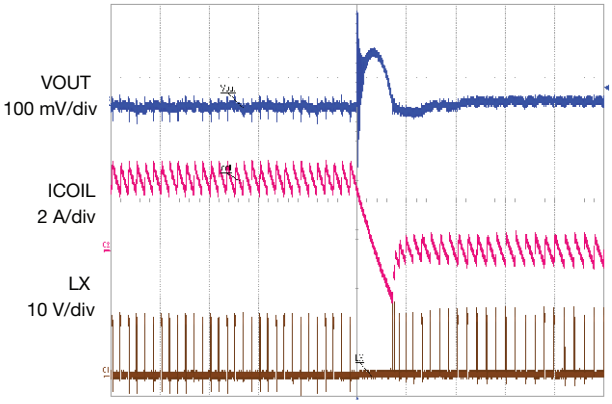


Fig. 13 - Load Step Overshoot Response, I_{OUT} = 3 A to 0 A
Time = 10 µs/div

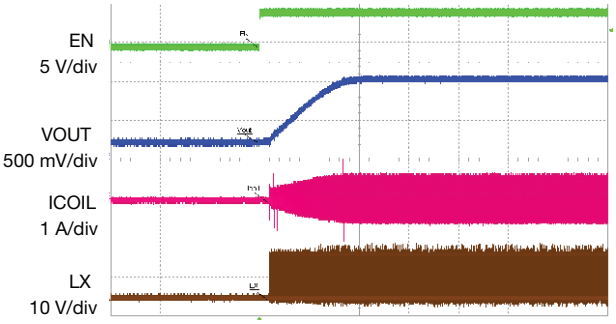


Fig. 11 - Start-Up, I_{OUT} = 0 A
Time = 1 µs/div

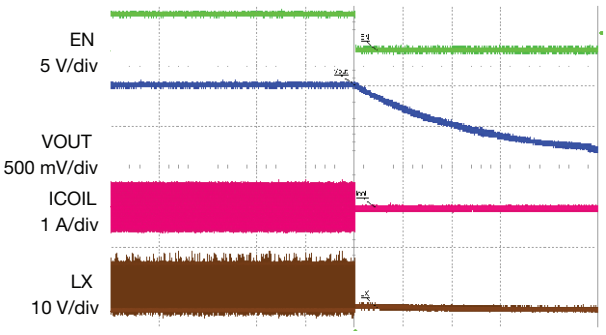


Fig. 14 - Shut-Down, I_{OUT} = 0 A
Time = 200 ms/div

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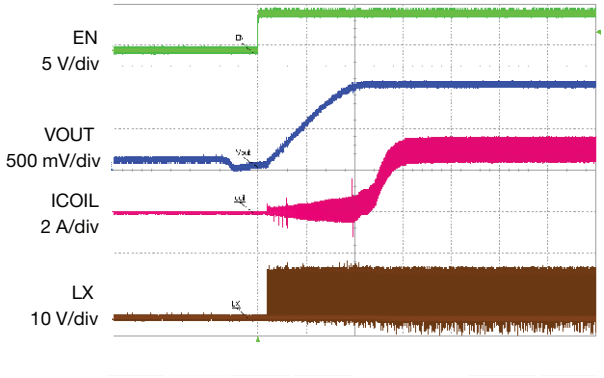


Fig. 15 - Load Step Undershoot Response I_{OUT} = 0 A to 3 A
Time = 1 ms/div

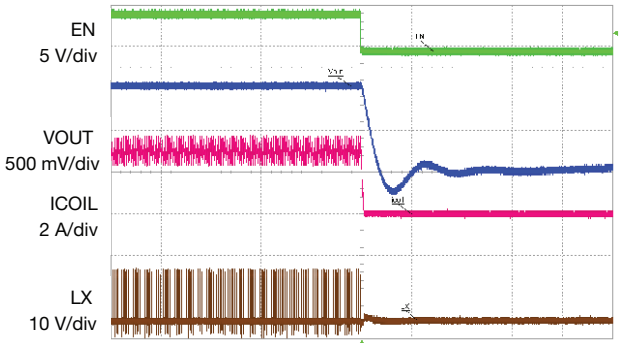


Fig. 17 - Shut-Down, I_{OUT} = 3 A
Time = 50 µs/div

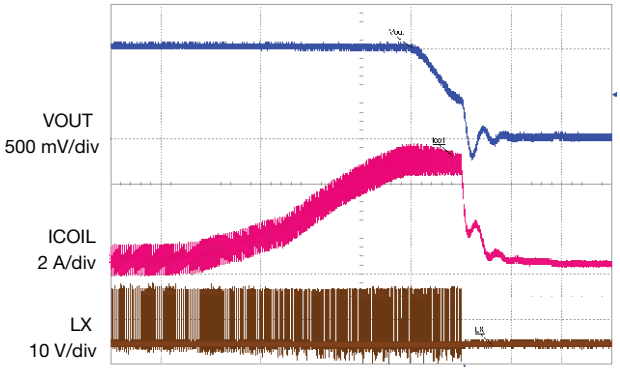


Fig. 16 - Over Current Protection, I_{VALLEY} = 4 A
Time = 100 µs/div

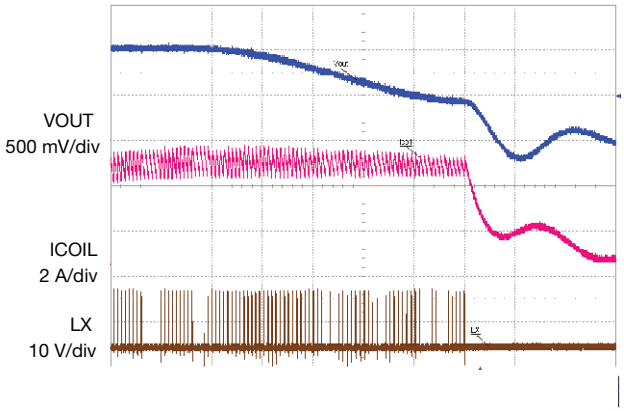


Fig. 18 - Over Current Protection, I_{VALLEY} = 4 A
Time = 20 µs/div

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OPERATIONAL DESCRIPTION

Device Overview

SiP12117 is a high-efficiency monolithic synchronous buck regulator capable of delivering up to 3 A continuous current. The device has fixed switching frequency of 600 kHz. The control scheme is based on current - mode constant-on-time architecture, which delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high-ESR output bulk or virtual ESR network is required for the loop stability.

SiP12117 has a full set of protection features:

- Cycle by cycle over current protection
- Over temperature protection with hysteresis

The device also features a dedicated enable pin for easy power sequencing and an open drain power good output.

The device is available in 3 x 3 DFN10 package with an exposed power pad to deliver high power density with ease of use.

Power Stage

SiP12117 integrates a high-performance power stage with an 85 mΩ n-channel high side MOSFET and a 55 mΩ n-channel low side MOSFET. The MOSFETs are optimized to achieve up to 95 % efficiency at 600 kHz switching frequency.

The power input voltage (V_{IN}) can go up to 15 V and down as low as 4.5 V for power conversion.

PWM Control Mechanism

SiP12117 employs a state-of-the-art current - mode COT (CM-COT) control mechanism. During steady-state operation, output voltage is compared with internal reference (0.6 V typ.) and the amplified error signal (V_{comp}) is generated. In the meantime, inductor valley current is sensed, and its slope (I_{sense}) is converted into a voltage signal ($V_{current}$) to be compared with V_{comp}. Once $V_{current}$ is lower than V_{comp}, a single shot on-time is generated for a fixed time set by an internal R_{ON}.

Light Load Operation

To further improve efficiency at light-load condition, SiP12117 provides a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal Zero Crossing Detector (ZCD) monitors LX node voltage to determine when inductor current starts to flow negatively. In light load operation as soon as inductor valley current crosses zero, the device first deploys diode emulation mode by turning off LS FET. If load further decreases, switching frequency is further reduced proportional to load condition to save switching losses while keeping output ripple within tolerance. The switching frequency is set by the control loop to maintain regulation. At zero load this frequency can go as low as hundreds of Hz.

Fig. 19 illustrates the basic block diagram for CM-COT architecture and fig. 20 demonstrates the basic operational principle:

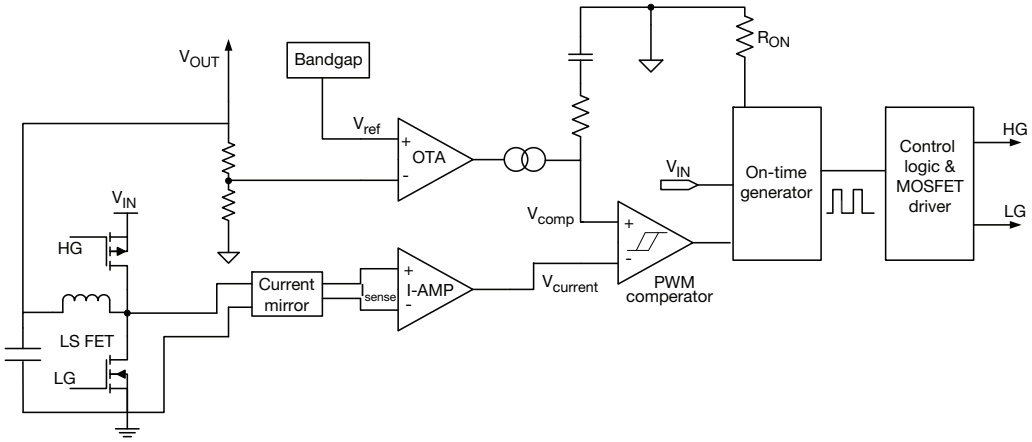


Fig. 19 - CM-COT Block Diagram

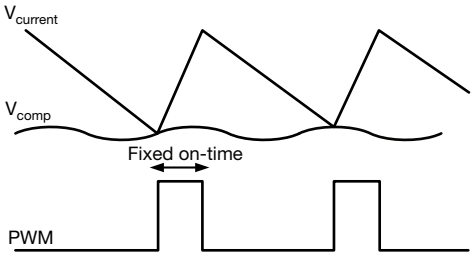


Fig. 20 - CM-COT Operational Principle

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OUTPUT MONITORING AND PROTECTION FEATURES

Output Over-Current Protection (OCP)

SiP12117 has cycle by cycle over-current limit control. The inductor valley current is monitored during LS FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined blanking time, the valley current is compared with internal threshold (4.25 A typ.) to determine the threshold for OCP. If the monitored current is higher than the internal threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

OCP is enabled immediately after V_{IN} passes UVLO level and enable is high.

In the figure below we see the ripple current riding on the DC load current. The valley current is calculated by taking one half the ripple current minus the DC load current.

For example if I_{OUT} = 3 A and ripple current = 1.2 A, I_{VALLEY} = 3 A - 0.6 A = 2.4 A. The typical DC full load current would be 4.85 A which is calculated by 4.25 A (OCP typ.) + 0.6 A. Here we see changing the ripple current (inductor value) can change the maximum DC load current value.

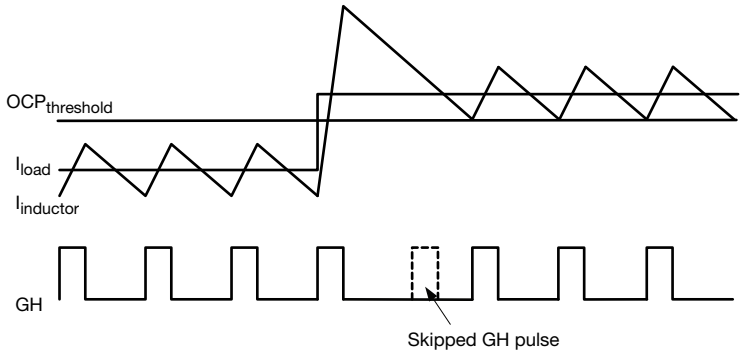


Fig. 21 - Over-Current Protection Illustration

Negative Current Protection

Similar to the output over-current protection, the negative current protection is realized by monitoring the current across the LS FET.
When the valley point of the inductor current reaches -2.5 A for first cycles, both HS and LS FETs are off.

Over-Temperature Protection (OTP)

SiP12117 has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 145 °C (typ.). A hysteresis of 35 °C is implemented, so when junction temperature drops below 110 °C, the device restarts by initiating soft-start sequence again.

Soft Start

SiP12117 has a built in soft-start function of ~2.9 ms. Once V_{IN} is above UVLO level (2.8 V typ.), V_{OUT} will ramp up slowly, rising monotonically to the programmed output voltage.

Pre-bias Startup

In case of pre-bias startup, the output is monitored through the FB pin. If the sensed voltage on FB is higher than the internal reference ramp value, control logic prevents HS and LS FET from switching to avoid a negative output voltage spike due to LS FET turn on.

Design Procedure

The design process of the SiP12117 is quite straight forward. Only few passive components such as output capacitors and Inductor need to be selected.

The following paragraph describes the selection procedure for these peripheral components for a given operating conditions.

In the next example the following definitions apply:

V_{IN} max.: the highest specified input voltage

V_{IN} min.: The minimum effective input voltage subject to voltage drops due to connectors, fuses, switches, and PCB traces.

There are two values of load current to evaluate - continuous load current and peak load current.

Continuous load current relates to thermal stress considerations which drive the selection of the inductor and input capacitors.

Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following specifications are used in this design:

- V_{IN} = 12 V ± 10 %
- V_{OUT} = 1.2 V ± 1 %

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Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Cost, PCB size, output ripple, and efficiency are all used in the selection process. Low inductor values result in smaller size and allow faster transient performance but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current, and transient response. Efficiency especially at higher load currents will also be compromised due to the higher DCR (within a given case size).

The ripple current also sets the boundary for power-save operation. The switching regulator will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 1 A then power-save operation will typically start at loads approaching 0.5 A. Alternatively, if ripple current is set at 40 % of maximum load current, then power-save will start for loads less than ~20 % of maximum current.

Setting the ripple current 20 % to 50 % of the maximum load current provides an optimal trade-off of the areas mentioned above.

This table provides a simple easy guide for setting up the board. If excessive jitter is noticed then reducing the inductor to the next standard value may be needed.

SiP12117 CONFIGURATION LOOK UP TABLE

V_{IN} (V)	V_{OUT} (V)	INDUCTOR (µH)	R_{FB_TOP} (Ω)	R_{FB_BOTTOM} (Ω)
12	1	1.5	4.53k	6.81k
12	3.3	3.3	4.53k	1k
12	5	3.3	4.53k	619R
5	1	1.5	4.53k	6.81k
5	3.3	1.5	4.53k	1k

The equation for determining inductance is shown next.

Example

In this example, the inductor ripple current is set equal to 30 % of the maximum load current. Thus ripple current will be 30 % x 3 A or 0.9 A. To find the minimum inductance needed, use the V_{IN} and t_{ON} values that correspond to $V_{IN\ max.}$.

$$L = (V_{IN} - V_{OUT}) \times \frac{t_{ON}}{\Delta i}$$

Plugging numbers into the above equation we get

$$L = (13.2\ V - 1.2\ V) \times \frac{151 \times 10^{-9}\ s}{0.9\ A} = 2\ \mu H$$

A smaller value of 1.5 µH is selected which is a standard value. This will increase the maximum ripple current by 25 %.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current. The actual ripple current using the chosen 1 µH inductor comes out to be.

$$\Delta i = (13.2\ V - 1.2\ V) \times \frac{151\ ns}{1.5\ \mu H} = 1.2\ A$$

Output Capacitance Calculation

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < $1/f_{sw}$ µs), the output capacitor must absorb all the inductor's stored energy. This will approximately cause a peak voltage on the capacitor according to the following equation.

$$C_{OUT\ min.} = \frac{L \times (I_{OUT} + \frac{1}{2} \times I_{RIPPLE\ max.})^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.3 V (100 mV rise upon load release), and a 3 A load release, the required capacitance is shown by the next equation.

$$C_{OUT\ min.} = \frac{1.5\ \mu H \times (3\ A + 0.5 \times (1.2\ A)^2}{(1.3\ V)^2 - (1.2\ V)^2} = 77.8\ \mu F$$

If the load release is relatively slow, the output capacitance can be reduced.

Using MLCC ceramic capacitors we will use 3 x 22 µF or 66 µF as the total output capacitance.

Switching Frequency Variations

The switching frequency variation in COT can be mainly attributed to the increase in conduction losses as the load increases. Since the on time is constant the controller must account for losses and maintain output regulation by reducing the off time. Hence the f_{sw} tends to increase with load.

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LAYOUT CONSIDERATIONS

The SiP12117 offers the designer a small part count, 3 A buck regulator solution. If the below layout recommendations are followed, the same layout can be used to cover a wide range of output currents and voltages without any changes to the board design and only minor changes to the component values in the schematic.

The reference design has a majority of the components placed on the top layer. This allows for easy assembly and straightforward layout.

Fig. 22 outlines the pointers for the layout considerations and the explanations follow.

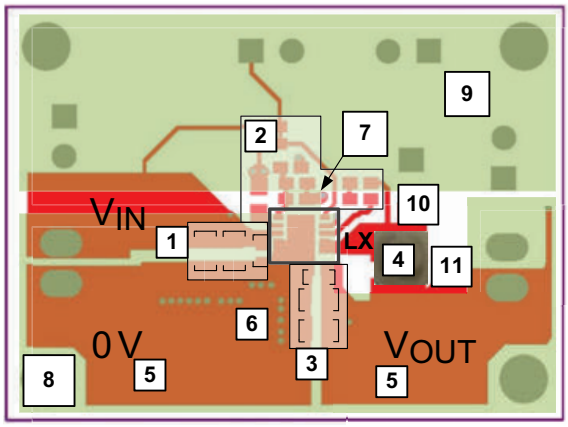


Fig. 22 - Reference Design Pointers

1. Place input ceramic capacitors close to the voltage input pins with a small 10 nF / 100 nF placed as close as the design rules will allow. This will help reduce the size of the input high frequency current loop and consequently reduce the high frequency ripple noise seen at the input and the LX node.
2. Place the setup and control passive devices logically around the IC with the intention of placing a quiet ground plane beneath them on a secondary layer.
3. It is advisable to use ceramic capacitors at the output to reduce impedance. Place these as close to the IC P_{GND} and output voltage node as design will allow. Place a small 10 nF / 100 nF ceramic capacitor closest to the IC and inductor loop.
4. The loop between LX, V_{OUT} and the IC P_{GND} should be as compact as possible. This will lower series resistance and also make the current loop smaller enabling the high frequency response of the output capacitors to take effect.
5. The output impedance should be small when high current is required; use high current traces, multiple layers can be used with many vias if the design allows.
6. Use many vias when multiple layers are involved. This will have the effect of lowering the resistance between layers and reducing the via inductance of the PCB nets.
7. The quiet A_{GND} should be connected to the P_{GND} plane near to the input GND at one connection only of at least 1 mm width.
8. P_{GND} can be used on internal layers if the resistance of the PCB is to be small; this will also help remove heat. Use extra vias if needed but be mindful to allow a path between the vias.
9. A quiet plane should be employed for the A_{GND}, this is placed under the small signal passives. This can be placed on multiple layers if needed for heat removal.
10. The LX copper can also be used on a single or multiple layers, use a number of vias to stitch the layers.
11. The copper area beneath the inductor has been removed (on all layers) in this design to reduce the inductive coupling that occurs between the inductor and the GND trace. No other voltage planes should be placed under this area.

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PCB LAYOUT

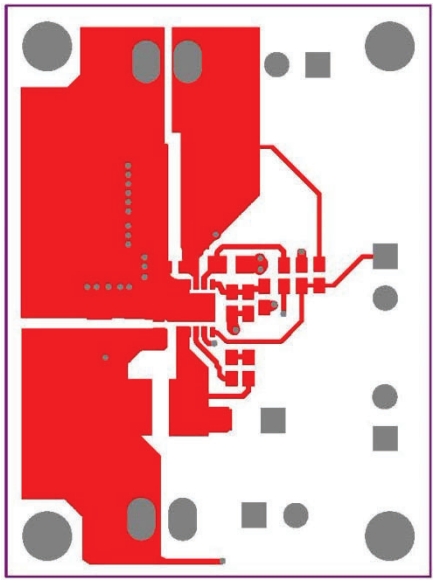


Fig. 23 - Top Layer

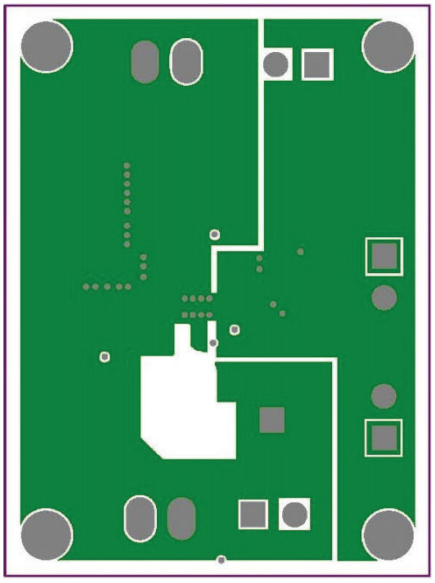


Fig. 25 - Inner Layer 1

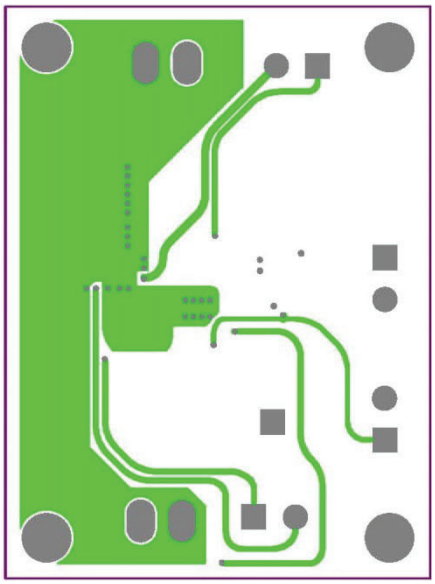


Fig. 24 - Inner Layer 2

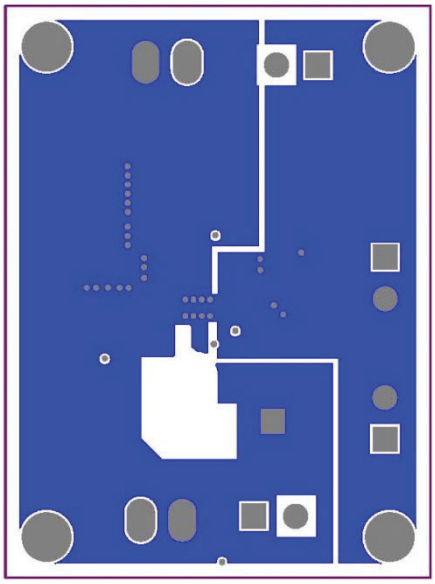
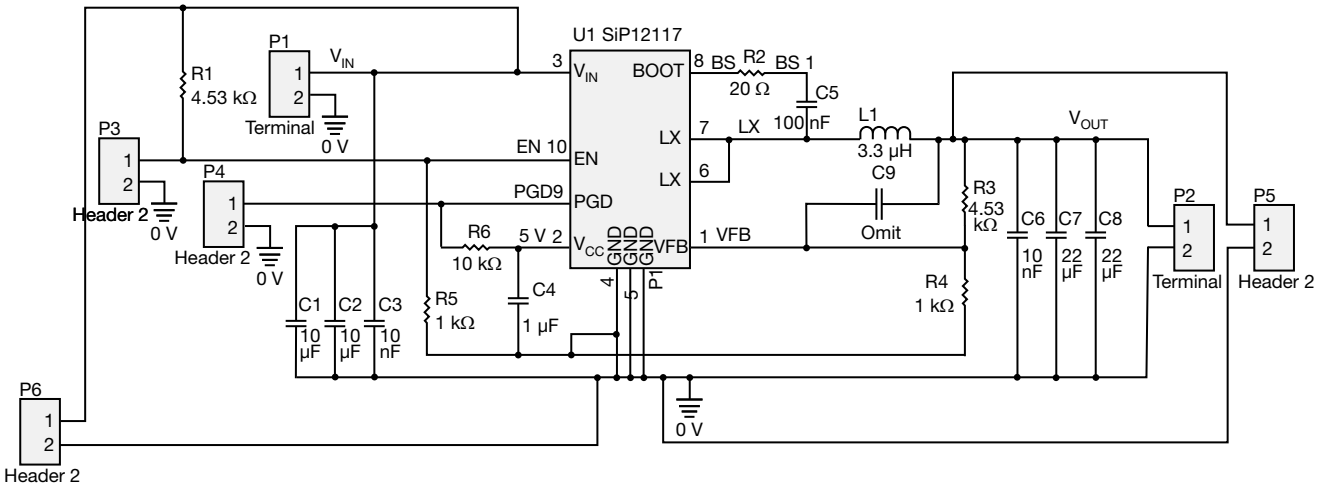


Fig. 26 - Bottom Layer

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SCHEMATIC

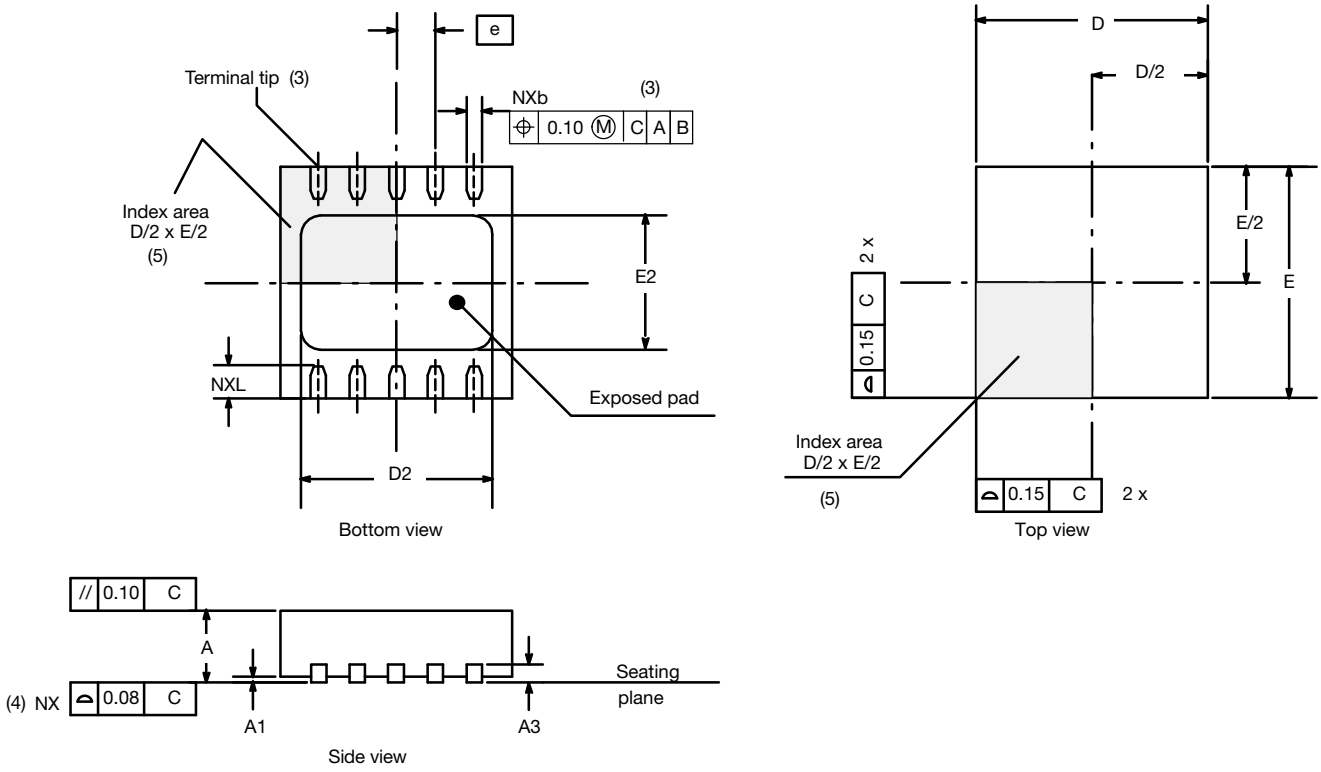


BILL OF MATERIAL (V_{IN} = 12 V, V_{OUT} = 3.3 V, F_{SW} = 600 kHz)

ITEM	QTY	REFERENCE	PCB FOOTPRINT	VALUE	VOLTAGE	PART NUMBER	MANUFACTURER
1	2	C1, C2	1210	10 µF	35 V	C1210C106M6PACTU	Kemet
2	2	C3, C6	0402	10 nF	50 V	GRM155R71H103KA88D	Murata
3	1	C4	0603	1 µF	10 V	C0402C105M8PACTU	Kemet
4	1	C5	0402	100 nF	35 V	CGA2B3X7R1V104K050BB	Vishay
5	2	C7, C8	0805	22 µF	10 V	CL21A226MPQNNNE	Samsung
6	1	R2	0402	20R	-	CRCW040220R0FKED	Vishay
7	1	R3	0402	4K53	-	CRCW04024K53FKED	Vishay
8	1	R4	0402	1K	-	CRCW0402249KFKED	Vishay
9	1	L1	IHLP2525	3µ3	-	IHLP2020BZER3R3M01	Vishay
10	1	U1	DFN10-3x3	-	-	SiP12117	Vishay
11	1	R1	0402	4K53	-	CRCW04024K53FKED	Vishay
12	1	R5	0402	1K	-	CRCW0402249KFKED	Vishay
13	1	R6	0402	10K	-	CRCW040210K0FKED	Vishay
14	4	P3, P4, P5, P6	HDR1x2	-	-	90120-0126	Vishay
15	2	P1, P2	TERM2	-	-	282834-2	TE Connectivity

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CASE OUTLINE



DIMENSION	MILLIMETERS [1]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20 BSC			0.008 BSC	
b	0.18	0.23	0.30	0.007	0.009	0.012
D		3.00 BSC			0.118 BSC	
D2	2.20	2.38	2.48	0.087	0.094	0.098
e		0.50 BSC			0.020 BSC	
E		3.00 BSC			0.118 BSC	
E2	1.49	1.64	1.74	0.059	0.065	0.069
L	0.30	0.40	0.50	0.012	0.016	0.020

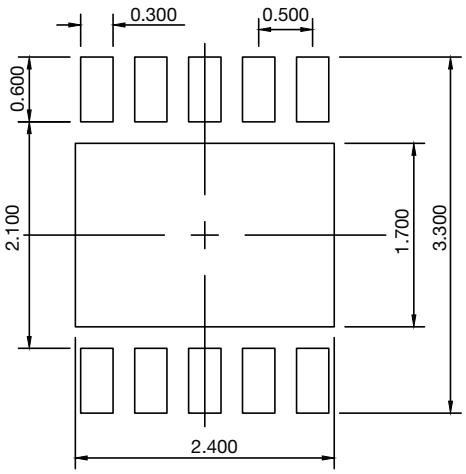
Notes

(2) Use millimeters as the primary measurement.
(3) N is the number of terminals.
(4) Dimensions b applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) Coplanarity applies to the exposed heat sink slug as well as the terminal.
(6) The pin #1 identifier may be either a mold or marked feature, it must be located within the zone indicated.

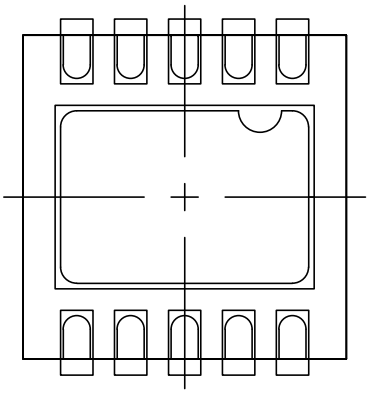
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RECOMMENDED LAND PATTERN

Recommended Land Pattern



Recommended Land Pattern vs. Case Outline

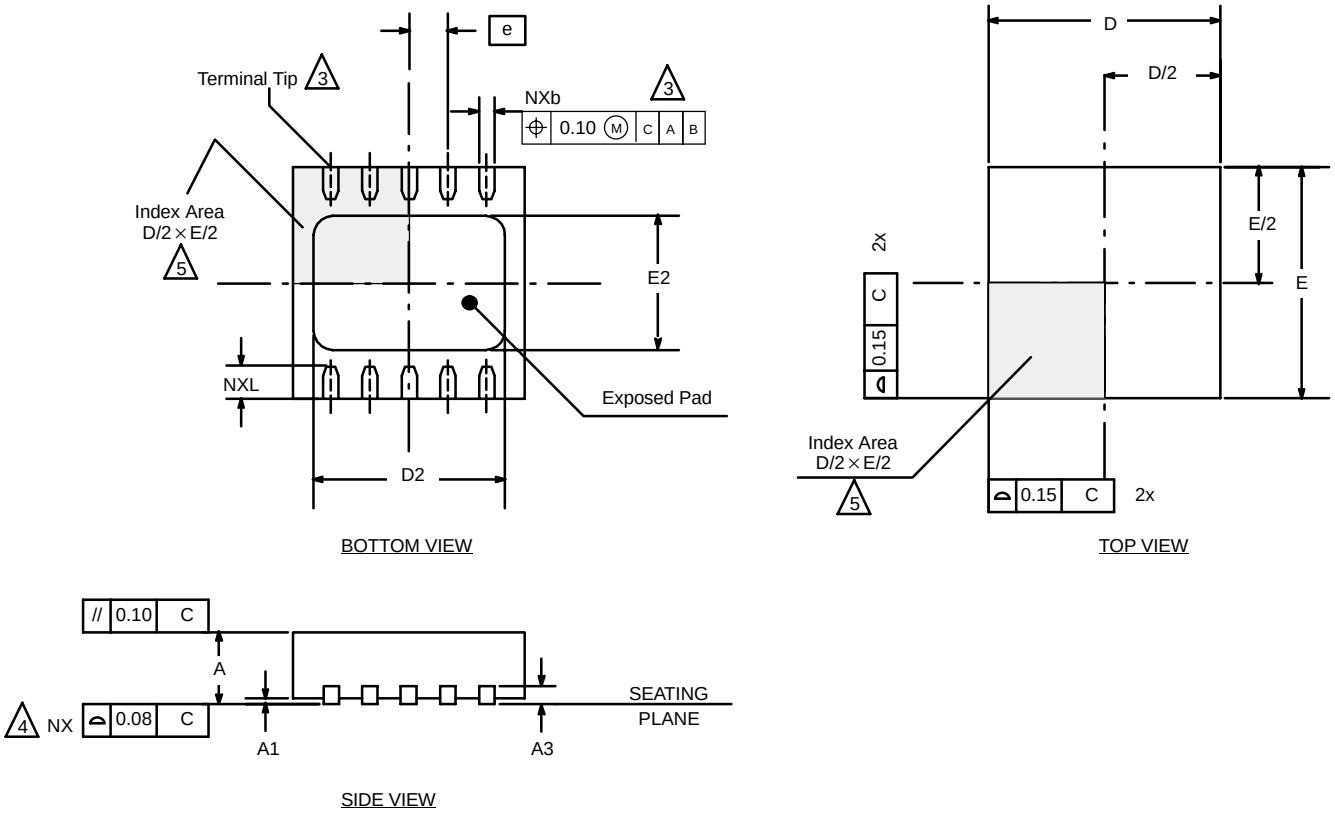


Dimensions are in millimeters

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DFN-10 LEAD (3 X 3)



NOTES:

1. All dimensions are in millimeters and inches.
2. N is the total number of terminals.
3. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30 mm from terminal tip.
4. Coplanarity applies to the exposed heat sink slug as well as the terminal.
5. The pin #1 identifier may be either a mold or marked feature, it must be located within the zone iindicated.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 BSC			0.008 BSC	
b	0.18	0.23	0.30	0.007	0.009	0.012
D		3.00 BSC			0.118 BSC	
D2	2.20	2.38	2.48	0.087	0.094	0.098
E		3.00 BSC			0.118 BSC	
E2	1.49	1.64	1.74	0.059	0.065	0.069
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

*Use millimeters as the primary measurement.

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DWG: 5943

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