6 A, 4.5 V to 15 V Input Synchronous Buck Regulator

DESCRIPTION

The SiP12110 is a high frequency current-mode constant on-time (CM-COT) synchronous buck regulator with integrated high-side and low-side power MOSFETs. Its power stage is capable of supplying 6 A continuous current at 1.0 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 4.5 V to 15 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiP12110's CM-COT architecture delivers ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The part is stable with any capacitor type and no ESR network is required for loop stability. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The regulator integrates a full protection feature set, including output overvoltage protection (OVP), output under voltage protection (UVP) and thermal shutdown (OTP). It also has UVLO for input rail and internal soft-start ramp.

The SiP12110 is available in lead (Pb)-free power enhanced 3 mm x 3 mm QFN-16 package.

FEATURES

- 4.5 V to 15 V input voltage
- Adjustable output voltage down to 0.6 V
- 6 A continuous output current
- Selectable switching frequency from 400 kHz to 1.0 MHz with an external resistor
- 95 % peak efficiency
- Stable with any capacitor. No external ESR network required
- Ultrafast transient response
- Power saving scheme for increased light load efficiency
- ± 1 % accuracy of V_{OUT} setting
- Cycle-by-cycle current limit
- Fully protected with OTP, SCP, UVP, OVP
- P_{GOOD} indicator
- -40 °C to +125 °C operating junction temperature
- Output voltage tracking
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Low voltage, distributed power architectures with 5 V or 12 V rails
- Computing, broadband, networking, LAN / WAN, optical, test and measurement
- A/V, high density cards, storage, DSL, STB, DVR, DTV, Industrial PC

TYPICAL APPLICATION CIRCUIT

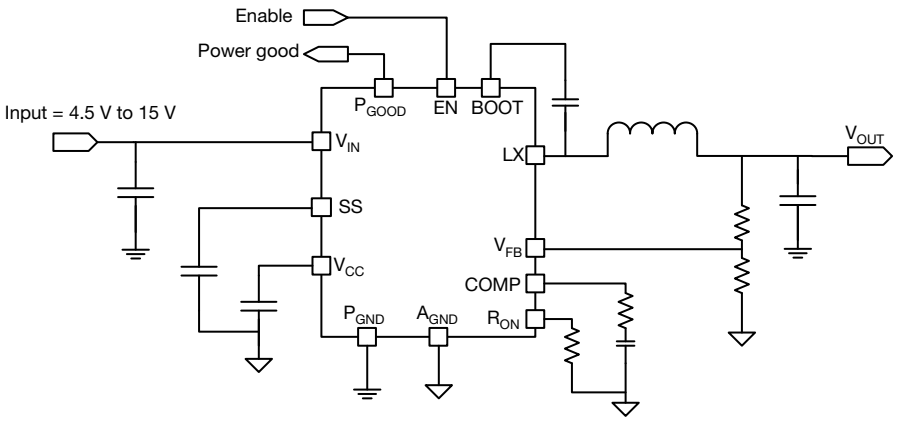

Fig. 1 - Typical Application Circuit for SiP12110

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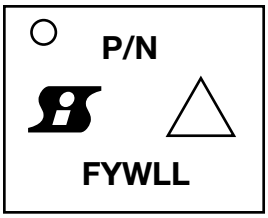
ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING (LINE 2: P/N)**
SiP12110DMP-T1-GE4	QFN16 3x3	2110
SiP12110DB	Reference board	

MARKING



Format:

Line 1: Dot
Line 2: P/N
Line 3: Siliconix logo + ESD symbol
Line 4: Factory code + year code + work week code + LOT code

ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMIT**	**UNIT**
V_{IN}	Reference to P_{GND}	-0.3 to +16	V
V_{CC}	Reference to A_{GND}	-0.3 to +6	
LX	Reference to P_{GND}	-1 to +16	
LX (AC voltage)	100 ns; reference to P_{GND}	-2 to +17	
	10 ns; reference to P_{GND}	-6 to +17	
BOOT		-0.3 to V_{IN} + V_{CC}	
A_{GND} to P_{GND}		-0.3 to +0.3	
All Logic Inputs and Outputs (R_{ON}, COMP, V_{FB}, SS, EN, P_{GOOD})	Reference to A_{GND}	-0.3 to V_{CC} +0.3	
TEMPERATURE			
Max. Operating Junction Temperature		-40 to +150	°C
Storage Temperature		-65 to +150	
POWER DISSIPATION			
Junction to Ambient Thermal Impedance (R_{thJA})		36.3	°C/W
Maximum Power Dissipation	Ambient temperature = 25 °C	3.4	W
	Ambient temperature = 100 °C	1.3	
ESD PROTECTION			
Electrostatic Discharge Protection	Human body model, JESD22-A114	2	kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING RANGE (all voltages referenced to GND = 0 V)				
ELECTRICAL PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**UNIT**
V_{IN}	4.5	-	15	V
V_{CC}	4.5	-	5.5	
V_{OUT}	0.6	-	5.5	
TEMPERATURE				
Recommended Ambient Temperature	-40 to 85			°C
Operating Junction Temperature	-40 to 125			

ELECTRICAL SPECIFICATIONS (test condition unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITION** V_{IN} = 12 V, T_A = -40 °C to 85 °C	**LIMITS**			**UNIT**
			MIN.	**TYP.**	**MAX.**	
POWER SUPPLY						
Power Input Voltage Range	V_{IN}	Note 1	4.5	-	15	V
V_{CC} Regulator Voltage	V_{CC}		4.5	5	5.5	
Input Current	IV_{IN_NOLOAD}	T_A = 25 °C, R_{on} = 75 kΩ, Non-switching, I_O = 0 A	-	1.2	-	mA
Shutdown Current	IV_{IN_SHDN}	EN = 0 V	-	5	8	µA
V_{CC} UVLO Threshold	V_{CC_UVLO}	V_{CC} rising	2.3	2.55	2.8	V
V_{CC} UVLO Hysteresis	$V_{CC_UVLO_HYS}$		-	300	-	mV
CONTROLLER AND TIMING						
Feedback Reference	V_{FB}	T_A = 25 °C	0.596	0.600	0.604	V
		T_A = -40 °C to +85 °C	0.594	0.600	0.606	
V_{FB} Input Bias Current	I_{FB}		-	2	200	nA
Transconductance	g_m		-	1	-	mS
COMP Source Current	I_{COMP_SOURCE}		-	50	-	µA
COMP Sink Current	I_{COMP_SINK}		-	50	-	
On-Time	t_{ON}	R_{on} = 75 kΩ	100	135	170	ns
Minimum Off-Time	$t_{OFF_MIN.}$		145	200	255	
Soft Start Current	I_{SS}		3	5	7	µA
POWER MOSFETS						
High-Side On Resistance	R_{ON_HS}	V_{GS} = 5 V	-	45	67	mΩ
Low-Side On Resistance	R_{ON_LS}		-	27	41	
FAULT PROTECTIONS						
Over Current Limit	I_{OCP}	Inductor valley current	-	7.5	-	A
Output OVP Threshold	V_{FB_OVP}	V_{FB} with respect to 0.6 V reference	-	21	-	%
Output UVP Threshold	V_{FB_UVP}		-	-65	-	
Over Temperature Protection		Rising temperature	-	160	-	°C
		Hysteresis	-	35	-	
POWER GOOD						
Power Good Output Threshold	$V_{FB_RISING_VTH_OV}$	V_{FB} rising above 0.6 V reference	-	21	-	%
	$V_{FB_FALLING_VTH_UV}$	V_{FB} falling below 0.6 V reference	-	-12.5	-	
Power Good On Resistance	R_{ON_PGOOD}		-	30	60	Ω
Power Good Delay Time	t_{DLY_PGOOD}		-	5	-	µs
ENABLE THRESHOLD						
Logic High Level	V_{EN_H}		1.5	-	-	V
Logic Low Level	V_{EN_L}		-	-	0.4	

Note

(1) Tie V_{CC} to V_{IN} when V_{IN} < 5.5 V.

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FUNCTIONAL BLOCK DIAGRAM

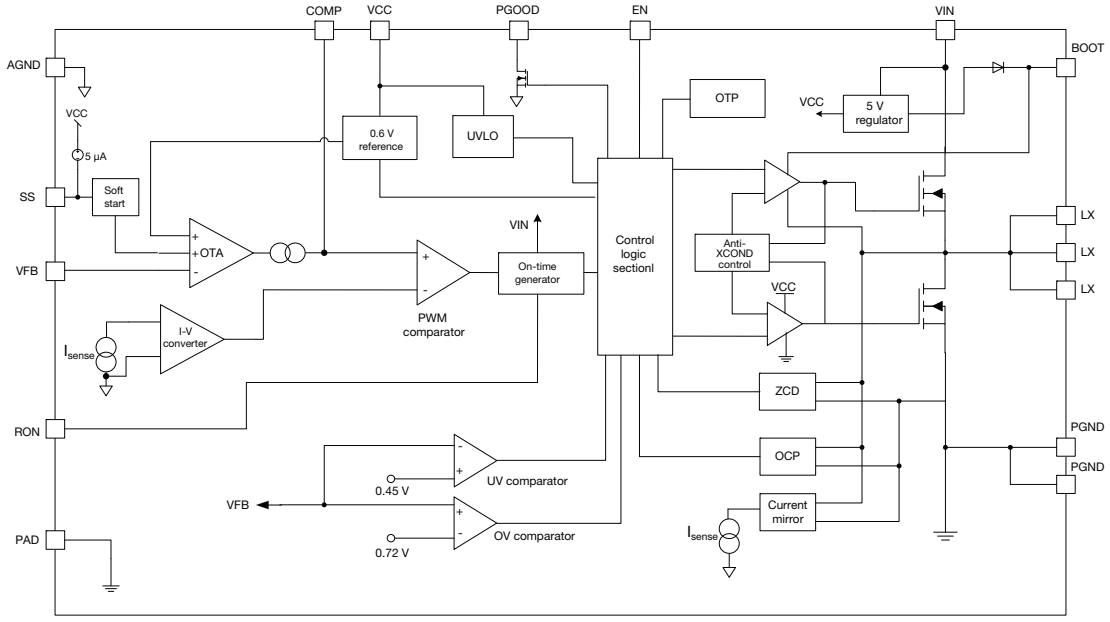

Fig. 2 - SiP12110 Functional Block Diagram

PIN CONFIGURATION

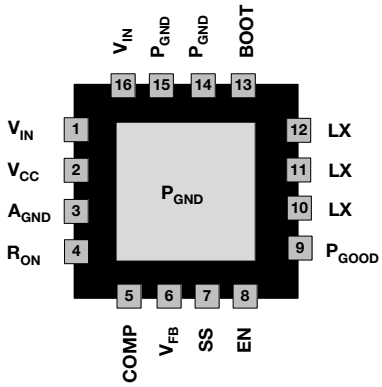

Fig. 3 - SiP12110 Pin Configuration (Top View)

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1, 16	V_{IN}	Input supply voltage for power MOS. V_{IN} = 4.5 V to 15 V
2	V_{CC}	Internal regulator output, tie V_{CC} to V_{IN} when V_{IN} < 5.5 V
3	A_{GND}	Analog ground
4	R_{ON}	An external resistor between R_{ON} and A_{GND} sets the switching on time.
5	COMP	Connect to an external RC network for loop compensation and droop function.
6	V_{FB}	Feedback voltage. 0.6 V (typ.). Use a resistor divider between V_{OUT} and A_{GND} to set the output voltage.
7	SS	An external capacitor between SS and A_{GND} sets the soft start time.
8	EN	Enable pin. Pull enable above 1.5 V to enable and below 0.4 V to disable the part. Do not float this pin.
9	P_{GOOD}	Power good output. Open drain.
10, 11, 12	LX	Switching node, inductor connection point
13	BOOT	Bootstrap pin - connect a capacitor of at least 100 nF from BOOT to LX to develop the floating supply for the high-side gate drive.
14, 15, PAD	P_{GND}	Power ground

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ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 1.5 µH, C = 3 x 22 µF, unless otherwise noted)

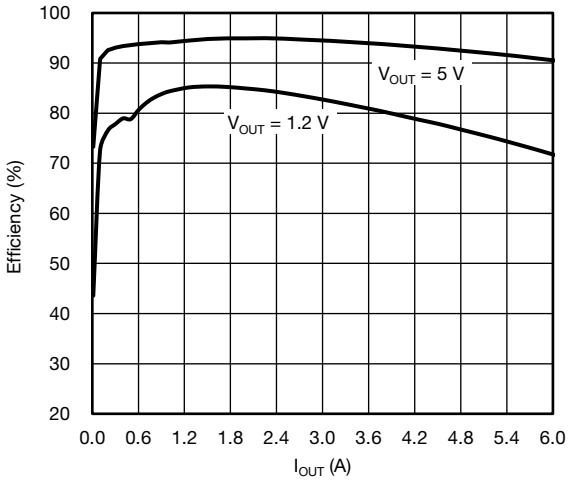

Fig. 4 - Efficiency vs. I_{OUT}

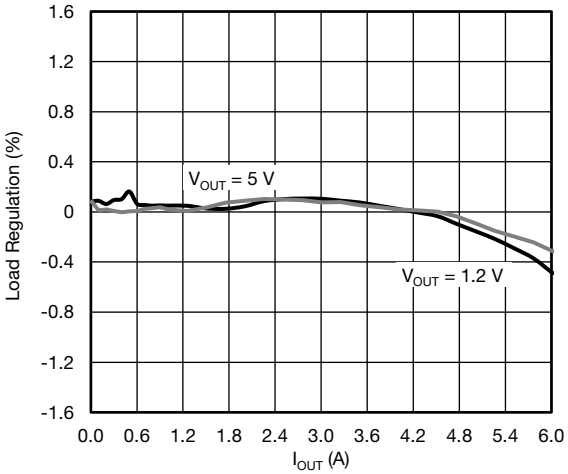

Fig. 7 - Load Regulation vs. I_{OUT}

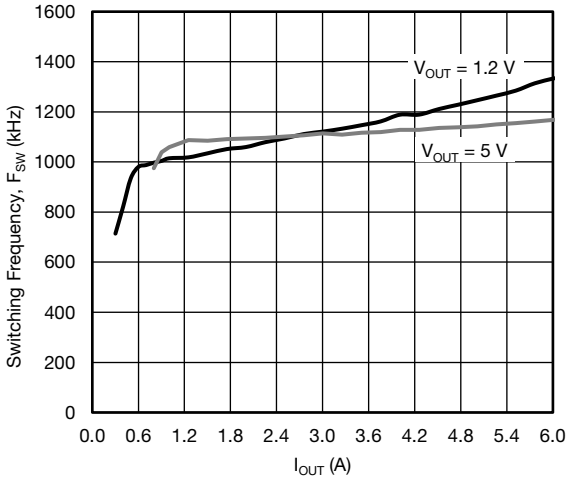

Fig. 5 - Frequency Variation vs. I_{OUT}

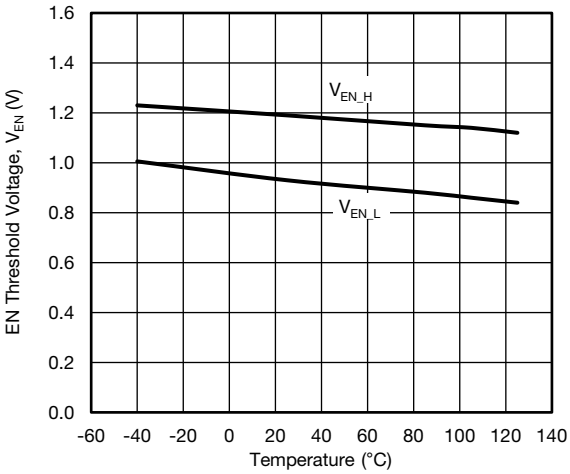

Fig. 8 - EN Threshold vs. Temperature

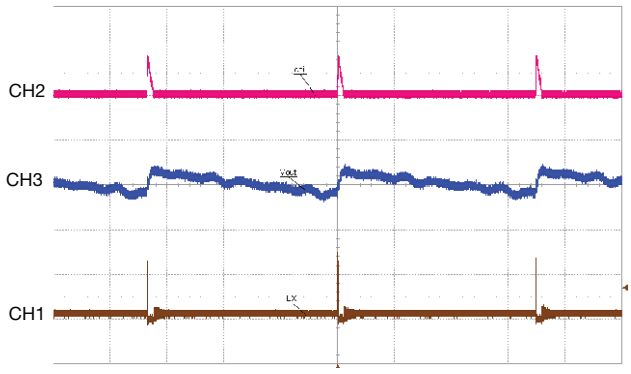

Fig. 6 - Steady-State, I_{OUT} = 0 A
CH1 (BRN) = LX (10 V/div), CH3 (BLU) = V_{OUT} (20 mV/div), CH2 (RED) = I_{COIL} (1 A/div), Time = 10 µs/div

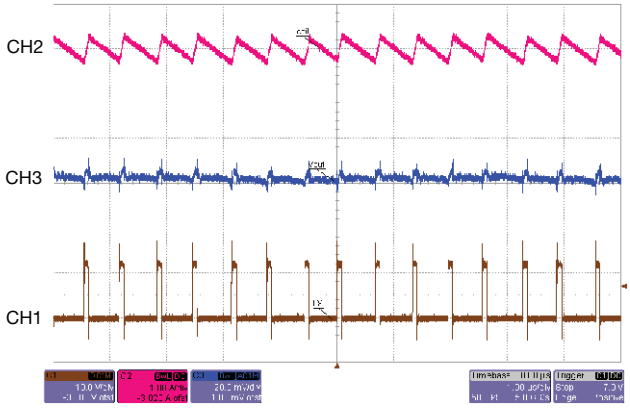

Fig. 9 - Steady-State, I_{OUT} = 6 A
CH1 (BRN) = LX (10 V/div), CH3 (BLU) = V_{OUT} (20 mV/div), CH2 (RED) = I_{COIL} (1 A/div), Time = 1 µs/div

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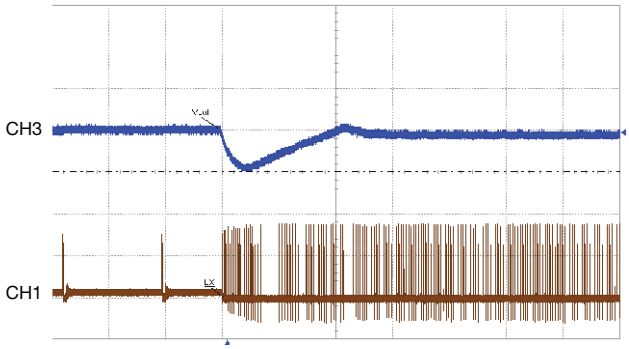

Fig. 10 - Load Step Undershoot Response, I_{OUT} = 0 A to 6 A
CH3 (BLU) = V_{OUT} (500 mV/div),
CH1 (BRN) = LX (10 V/div), Time = 20 µs/div

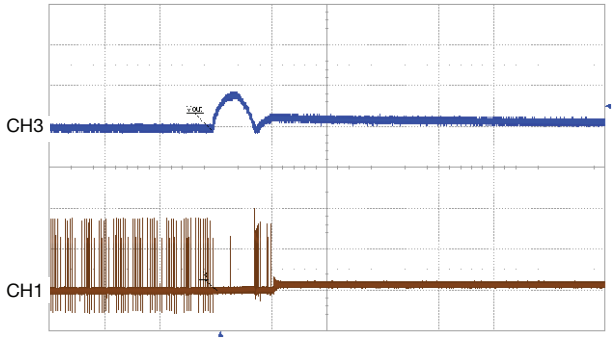

Fig. 13 - Load Step Overshoot Response, I_{OUT} = 6 A to 0 A
CH3 (BLU) = V_{OUT} (500 mV/div),
CH1 (BRN) = LX (10 V/div), Time = 20 µs/div

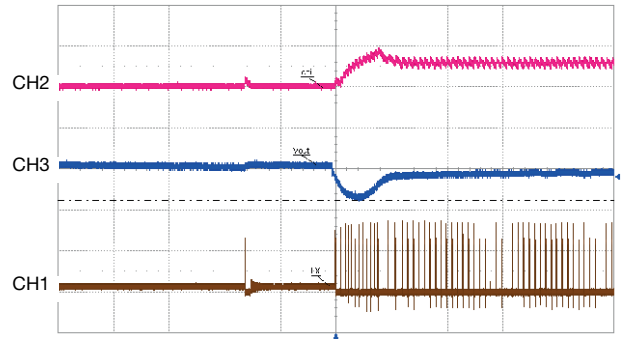

Fig. 11 - Load Step Undershoot Response, I_{OUT} = 0 A to 3 A
CH2 (RED) = I_{COIL} (5 A/div), CH3 (BLU) = V_{OUT} (200 mV/div),
CH1 (BRN) = LX (10 V/div), Time = 10 µs/div

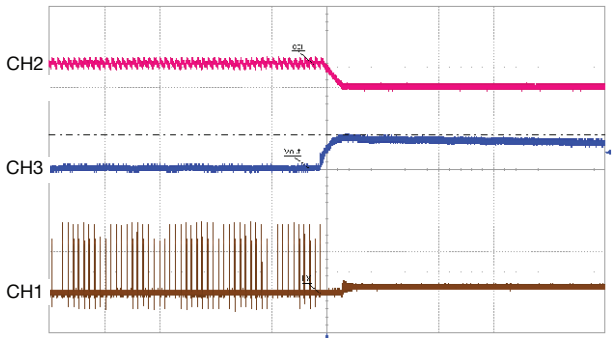

Fig. 14 - Load Step Overshoot Response, I_{OUT} = 3 A to 0 A
CH2 (RED) = I_{COIL} (5 A/div), CH3 (BLU) = V_{OUT} (200 mV/div),
CH1 (BRN) = LX (10 V/div), Time = 10 µs/div

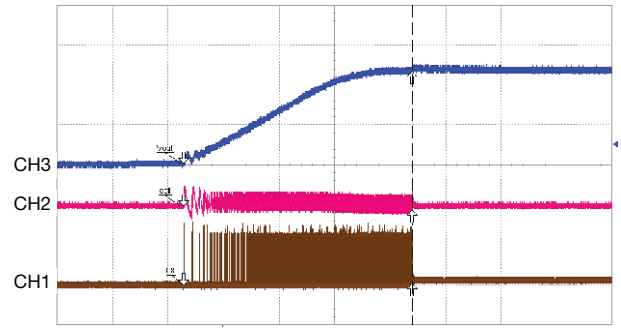

Fig. 12 - Start-Up, I_{OUT} = 0 A
CH1 (BRN) = LX (10 V/div), CH3 (BLU) = V_{OUT} (0.5 V/div),
CH2 (RED) = I_{COIL} (2 A/div), Time = 200 µs/div

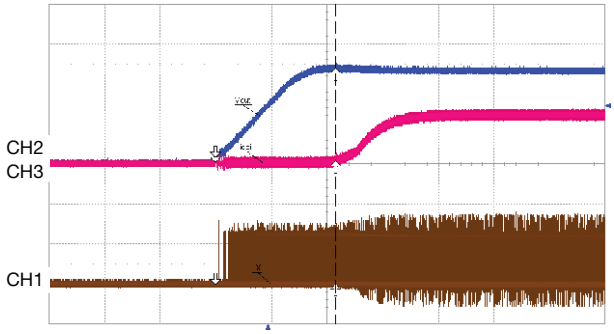

Fig. 15 - Start-Up, I_{OUT} = 6 A
CH1 (BRN) = LX (10 V/div), CH3 (BLU) = V_{OUT} (0.5 V/div),
CH2 (RED) = I_{COIL} (5 A/div), Time = 500 µs/div

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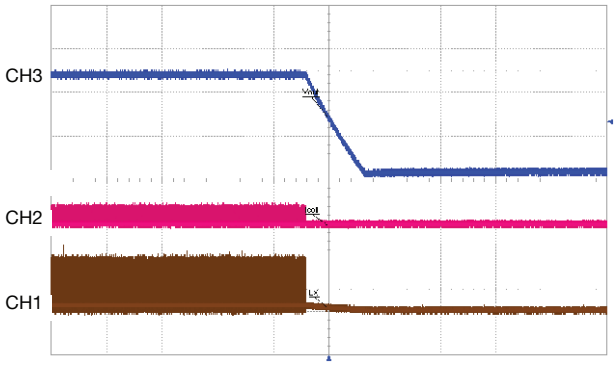

Fig. 16 - Shut-Down, I_{OUT} = 0 A
CH1 (BRN) = LX (10 V/div), CH3 (BLU) = V_{OUT} (0.5 V/div),
CH2 (RED) = I_{COIL} (2 V/div), Time = 5 ms/div

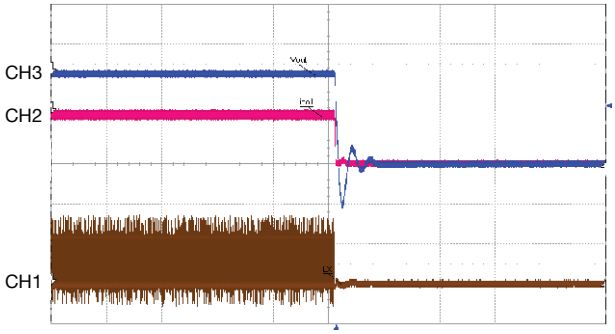

Fig. 18 - Shut-Down, I_{OUT} = 6 A
CH1 (BRN) = LX (10 V/div), CH3 (BLU) = V_{OUT} (0.5 V/div),
CH2 (RED) = I_{COIL} (5 A/div), Time = 200 µs/div

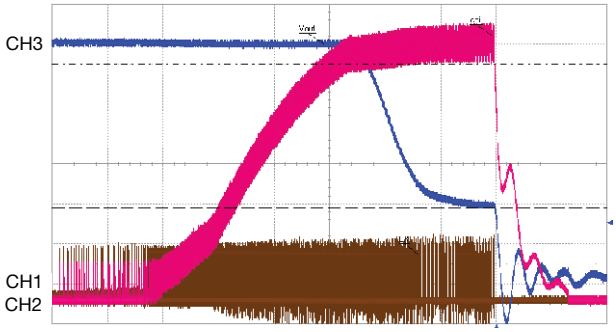

Fig. 17 - Over Current Protection, I_{VALLEY} = 6 A
CH2 (RED) = I_{COIL} (1 A/div), CH3 (BLU) = V_{OUT} (200 mV/div),
CH1 (BRN) = LX (10 V/div), Time = 100 µs/div

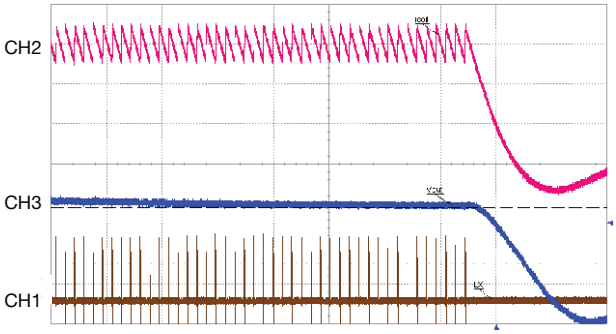

Fig. 19 - Over Current Protection, I_{VALLEY} = 6 A
CH2 (RED) = I_{COIL} (1 A/div), CH3 (BLU) = V_{OUT} (200 mV/div),
CH1 (BRN) = LX (10 V/div), Time = 10 µs/div

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OPERATIONAL DESCRIPTION

Device Overview

SiP12110 is a high-efficiency monolithic synchronous buck regulator capable of delivering up to 6 A continuous current. The device has programmable switching frequency up to 1 MHz. The control scheme is based on current-mode constant-on-time architecture, which delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high-ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature by enabling diode emulation mode and frequency foldback as load decreases.

SiP12110 has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output

This device is available in QFN16 3 x 3 package to deliver high power density and minimize PCB area.

Power Stage

SiP12110 integrates a high-performance power stage with a ~ 45 mΩ high side n-channel MOSFET and a ~ 27 mΩ low side n-channel MOSFET. The MOSFETs are optimized to achieve 95 % efficiency at up to 1 MHz switching frequency.

The power input voltage (V_{IN}) can go up to 15 V and down as low as 4.5 V for the power conversion. The logic bias voltage (V_{CC}) ranges from 4.5 V to 5.5 V.

PWM Control Mechanism

SiP12110 employs a state-of-the-art current-mode COT control mechanism. During steady-state operation, output voltage is compared with internal reference (0.6 V typ.) and the amplified error signal (V_{COMP}) is generated on the COMP pin. In the meantime, inductor valley current is sensed, and its slope (I_{sense}) is converted into a voltage signal ($V_{current}$) to be compared with V_{COMP}. Once $V_{current}$ is lower than V_{COMP}, a single shot on-time is generated for a fixed time programmed by the external R_{ON}. Figure 20 illustrates the basic block diagram for CM-COT architecture and figure 21 demonstrates the basic operational principle:

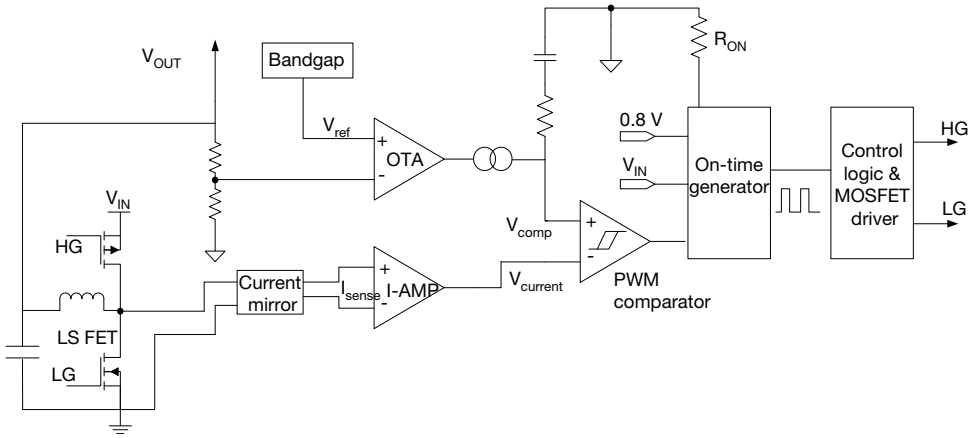

Fig. 20 - CM-COT Block Diagram

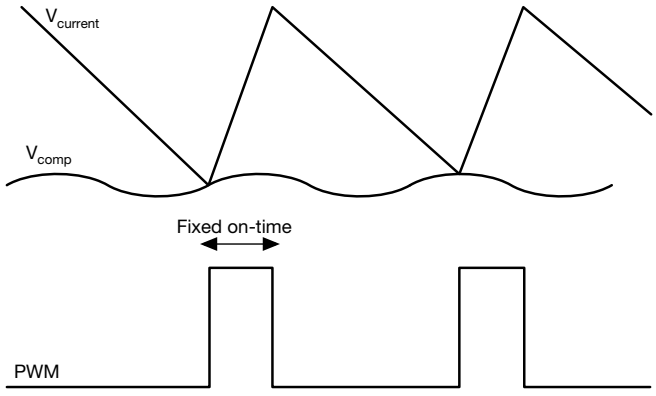

Fig. 21 - CM-COT Operational Principle

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The following equation illustrates the relationship between on-time, V_{IN}, V_{OUT} and R_{ON} value:

$$T_{ON} = R_{ON} \times K \times \frac{1}{V_{IN}}$$, where K = 17.5 x 10^{-12} is a constant set internally

Once on-time is set, the pseudo constant frequency is then determined by the following equation:

$$f_{sw} = \frac{D}{t_{on}} = \frac{\frac{V_{OUT}}{V_{IN}}}{\frac{1}{V_{IN}} \times R_{ON} \times K} = \frac{V_{OUT}}{R_{ON} \times K}$$

Loop Stability and Compensator Design

Due to the nature of current mode control, a simple RC network (type II compensator) is required between COMP and A_{GND} for loop stability and transient response purpose. The general concept of this loop design is to introduce a single zero through the compensator to determine the crossover frequency of overall close loop system.

The overall loop can be broken down into following segments.

Output feedback divider transfer function $H_{fb}Z$:

$$H_{fb} = \frac{R_{fb2}}{R_{fb1} \times R_{fb2}}$$

Voltage compensator transfer function G_{COMP} (s):

$$G_{COMP}(s) = \frac{R_O \times (1 + sC_{COMP}R_{COMP})}{(1 + sR_OC_{COMP})} gm$$

Modulator transfer function H_{mod} (s):

$$H_{mod}(s) = \frac{1}{AV_1 \times R_{DS(on)}} \times \frac{R_{load} \times (1 + sC_OR_{ESR})}{(1 + sC_OR_{load})}$$

The complete loop transfer function is given by:

$$H_{mod}(s) = \frac{R_{fb2}}{R_{fb1} \times R_{fb2}} \times \frac{R_O \times (1 + sC_{COMP}R_{COMP})}{(1 + sR_OC_{COMP})} gm \times \frac{1}{AV_1 \times R_{DS(on)}} \times \frac{R_{load} \times (1 + sC_OR_{ESR})}{(1 + sC_OR_{load})}$$

When:

C_{COMP} = compensation capacitor
R_{COMP} = compensation resistor
gm = error amplifier transconductance
R_{load} = load resistance
C_O = output capacitor
$R_{DS(on)}$ = LS switch resistance
R_{fb1} = feedback resistor connect to LX
R_{fb2} = feedback resistor connect to ground
R_O = output impedance of error amplifier = 20 MΩ
AV_1 = voltage to current gain = 3

Light Load Operation

To further improve efficiency at light-load condition, SiP12110 provides a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal zero crossing detector (ZCD) monitors LX node voltage to determine when inductor current starts to flow negatively. In light load operation as soon as inductor valley current crosses zero, the device first deploys diode emulation mode by turning off LS FET. If load further decreases, switching frequency is further reduced proportional to load condition to save switching losses while keeping output ripple within tolerance. The switching frequency is set by the controller to maintain regulation. At zero load this frequency can go as low as hundreds of Hz.

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over-Current Protection (OCP)

SiP12110 has pulse-by-pulse over-current limit control. The inductor valley current is monitored during LS FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined time, the valley current is compared with internal threshold (7.5 A typ.) to determine the threshold for OCP. If monitored current is higher than threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

In the severe over-current condition, pulse-by-pulse current limit eventually triggers output under-voltage protection (UVP), which latches the device off to prevent catastrophic thermal-related failure. UVP is described in the next section.

OCP is enabled immediately after V_{CC} passes UVLO level.

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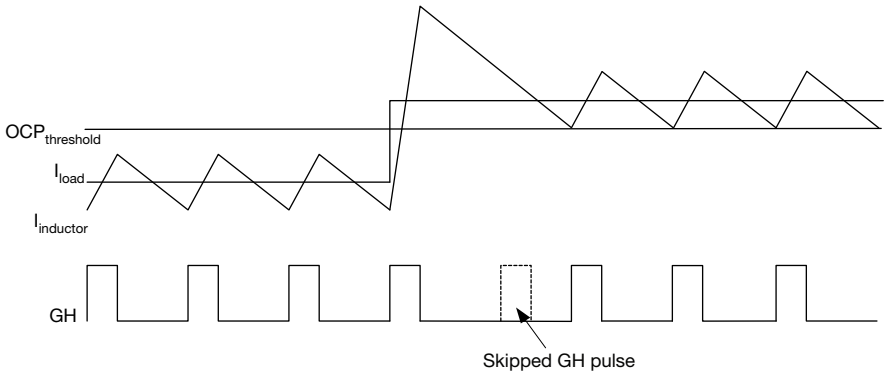

Fig. 22 - Over-Current Protection Illustration

Output Under-Voltage Protection (UVP)

UVP is implemented by monitoring output through V_{FB} pin. Once the voltage level at V_{FB} is below 0.2 V for more than 20 µs, then UVP event is recognized and both HS and LS MOSFETs are turned off. UVP latches the device off until either V_{CC} or EN is recycled.

UVP is only active after the completion of soft-start sequence.

Output Over-Voltage Protection (OVP)

For OVP implementation, output is monitored through V_{FB} pin. After soft-start, if the voltage level at V_{FB} is above 21 % (typ.), OVP is triggered with HS FET turning off and LS FET turning on immediately to discharge the output. Normal operation is resumed once V_{FB} drops back to 0.675 V.

OVP is active immediately after V_{CC} passes UVLO level.

Over-Temperature Protection (OTP)

SiP12110 has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 160 °C (typ.). A hysteresis of 30 °C is implemented, so when junction temperature drops below 130 °C, the device restarts by initiating the soft-start sequence again.

Soft Start up

SiP12110 soft-start time is adjustable by selecting a capacitor value from the following equation. Once V_{CC} is above UVLO level (2.55 V typ.), V_{OUT} will ramp up slowly, rising monotonically to the programmed output voltage. There is an internal 5 µA current source tied to the soft start pin which charges the external soft start cap

$$\text{SS time} = \frac{\text{Cext} \times 0.8\ \text{V}}{5\ \mu\text{A}}$$

During soft-start period, OCP is activated. OVP and short-circuit protection are not active until soft-start is complete.

Pre-bias Startup

In case of pre-bias startup, output is monitored through V_{FB} pin. If the sensed voltage on V_{FB} is higher than the internal reference ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.

Power Good (P_{GOOD})

SiP12110's power good is an open-drain output. Pull P_{GOOD} pin high up to 5 V through a 10K resistor to use this signal. power good window is shown in the below diagram. If voltage level on V_{FB} pin is out of this window, P_{GOOD} signal is de-asserted by pulling down to GND.

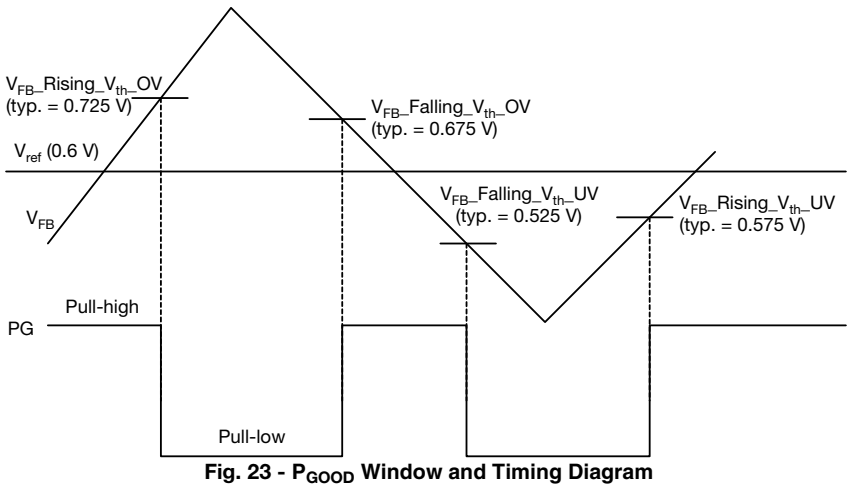

Fig. 23 - P_{GOOD} Window and Timing Diagram

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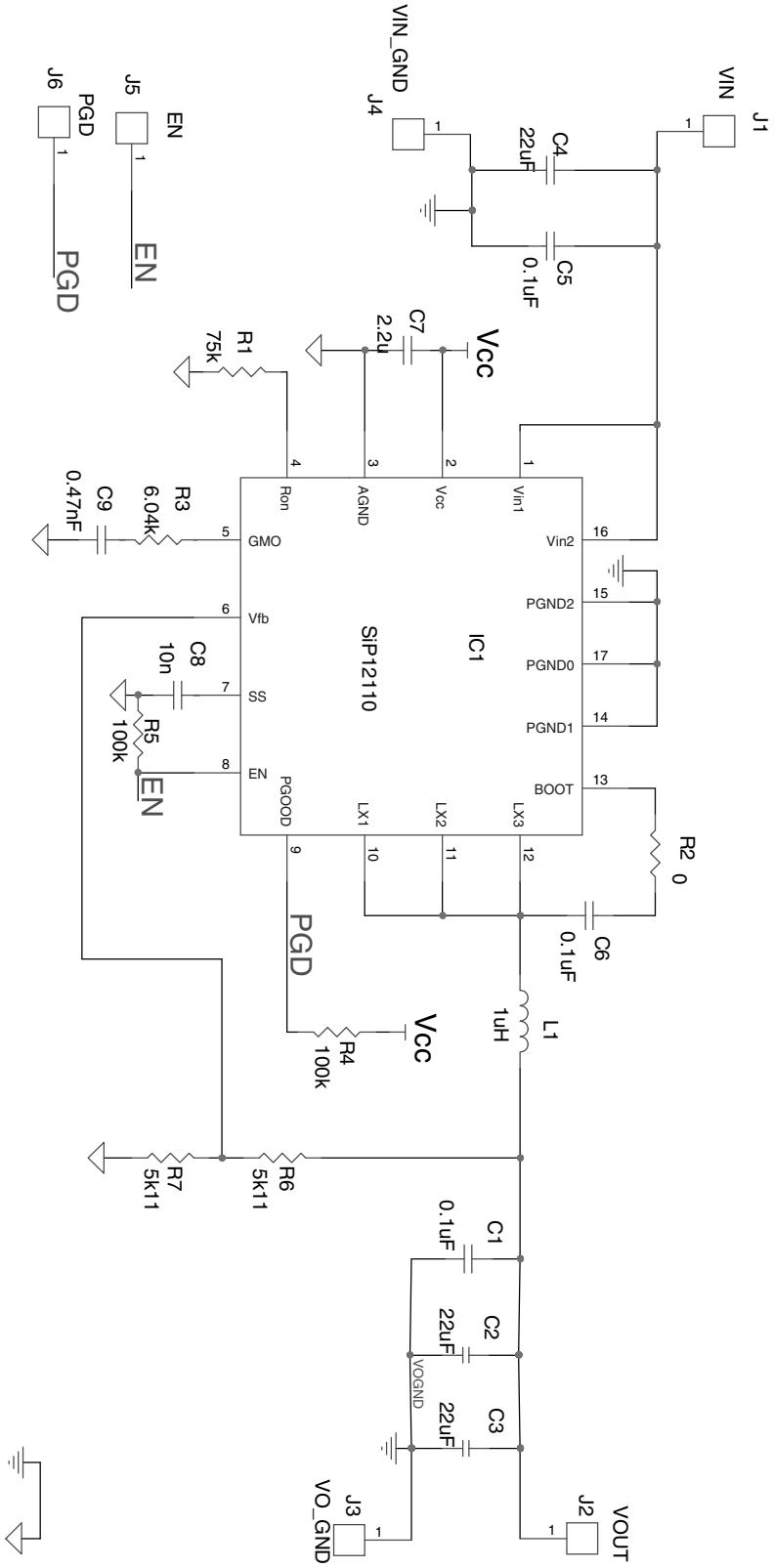

Fig. 24 - Reference Board Schematic

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BILL OF MATERIAL							
ITEM	QTY	REFERENCE	VALUE	VOLTAGE	FOOTPRINT	PART NUMBER	MANUFACTURER
1	3	C1, C5, C6	0.1 µF	35 V	C0402-TDK	GMK105BJ104KV-F	Taiyo Yuden
2	2	C2, C3	22 µF	10 V	C0805-TDK	LMK212BJ226MG-T	Taiyo Yuden
3	1	C4	22 µF	35 V	C0805-TDK	C2012X5R1V226M125AC	TDK
4	1	C7	2.2 µF	16 V	C0603-TDK	C0603C225K4PACTU	Kemet
5	1	C8	10 nF	16 V	C0402-TDK	CC0402KRX7R7BB103	Yageo
6	1	C9	0.47 nF	50 V	C0402-TDK	C1005C0G1H471J050BA	TDK
7	1	IC1	SiP12110	-	QFN16 3 x 3	SiP12110DMP-T1-GE4	Vishay
8	6	J1, J2, J3, J4, J5, J6	V_{IN}, V_{OUT}, V_{O_GND}, V_{IN_GND}, EN, PGD	-	TP30	2108-2-00-44-00-00-07	Mill-Max
9	1	L1	1 µH	-	IHLP1616	IHLP1616BZER1R0M11	Vishay
10	1	R1	75 kΩ	-	R0402-Vishay	CRCW040275K0FKEDHP	Vishay
11	1	R2	0	-	R0402-Vishay	RCG04020000Z0ED	Vishay
12	1	R3	6.04 kΩ	-	R0402-Vishay	CRCW04026K04FKED	Vishay
13	2	R4, R5	100 kΩ	-	R0402-Vishay	CRCW0402100KFKED	Vishay
14	2	R6, R7	5.11kΩ	-	R0402-Vishay	CRCW04025K11FKED	Vishay

PCB LAYOUT OF REFERENCE BOARD

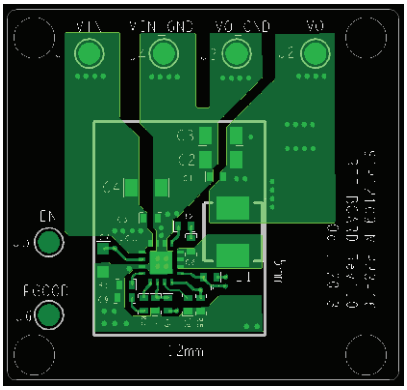

Fig. 25 - Top Layer

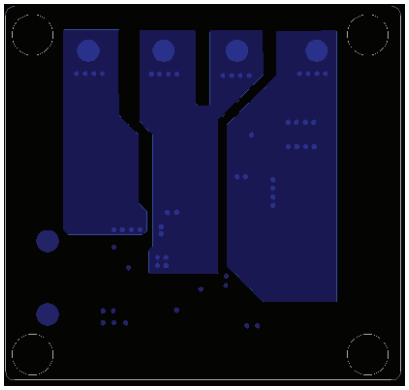

Fig. 27 - Bottom Layer

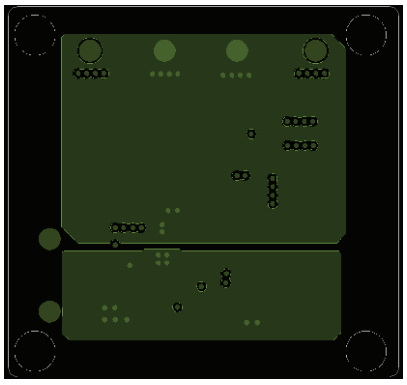

Fig. 26 - Inner Layer1

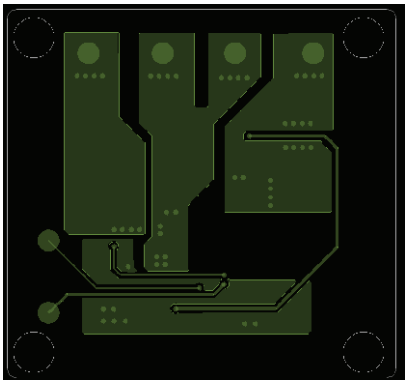

Fig. 28 - Inner Layer2

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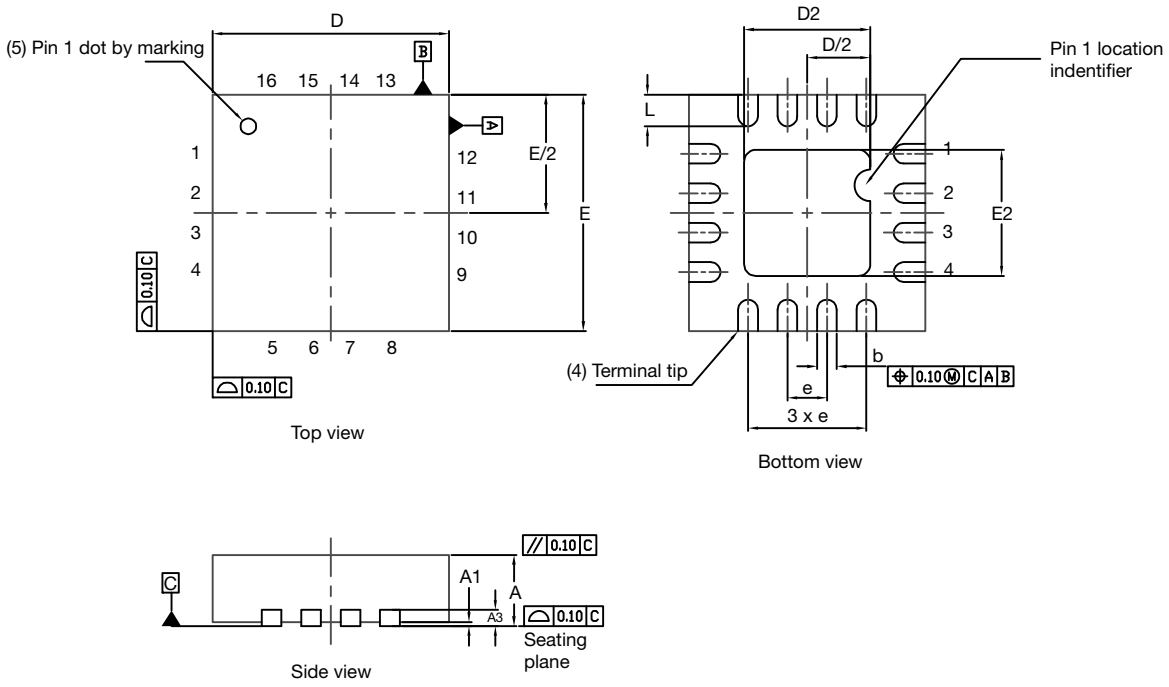
CASE OUTLINE



DIMENSION	MILLIMETERS [1]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002
A3		0.20 ref.			0.001 ref.	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		3.00 BSC			0.118 BSC	
D2	1.5	1.6	1.7	0.059	0.063	0.067
e		0.50 BSC			0.020 BSC	
E		3.00 BSC			0.118 BSC	
E2	1.5	1.6	1.7	0.059	0.063	0.067
L	0.3	0.4	0.5	0.012	0.016	0.020
N [3]		16			16	
Nd [3]		4			4	
Ne [3]		4			4	

Notes

(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

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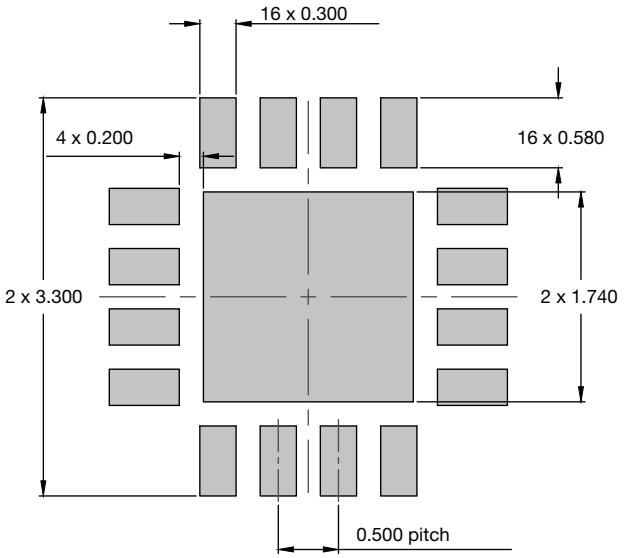
RECOMMENDED LAND PATTERN FOR QFN16 3 mm x 3 mm



Dimensions are in millimeters

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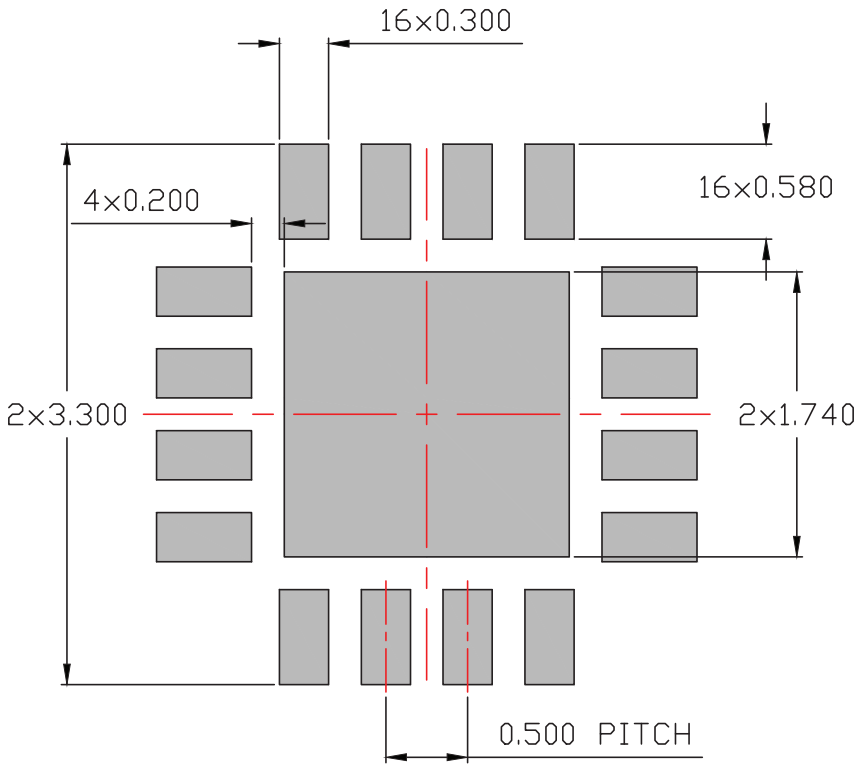
Recommended Land Pattern QFN16 3x3



All dimensions are in millimeters

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