SiP11203 Demonstration Board

DEMONSTRATION BOARD TEST SETUP

This demonstration board test setup information details the test procedure for using the SiP11203 demonstration board and its associated host board. The demonstration board is plugged vertically into the host board. Only one orientation is possible for correct plug-in. The input and output power leads and an optional enable lead are wired into the host board connectors as shown in Figure 1. A mechanical toggle switch is also available on the host board for manual enabling and disabling of the demonstration board. The host board is configured by default for manual switch toggling of enable/disable. If an electrical control signal is preferred, this can be wired into the enable connector J2. However, in this case the zero ohm link connected in the R4 position must be removed and reconnected in the R1 position, which is vacant by default. A 5 V input to the enable pin disables the demonstration board and a 0 V or open circuit input signal causes the demonstration board to be enabled. Test pins are available on the host board, at the input, output, and enable pins, for the easy connection of scope probes. These wiring connections are depicted in Figure 1. The input connections should be wired as closely as possible to the power supply, using cable rated at 2 A or more. However, lead lengths of up to a meter or two are probably acceptable. If the leads are significantly longer, a second input decoupling capacitor should be connected in position C1, which is left blank by default. At the load side, four 8 A rated wires should be connected from both +Vout and -Vout terminals to the load.

The Vsense terminals can be connected remotely to the load terminals for good regulation at the load, but this is not essential, as the Vsense terminals are connected to the output terminals through 4.7 Ω resistors on the demonstration board. A small fan should be placed adjacent to the host board, blowing cooling air over both vertical faces of the demonstration board. There is over temperature protection within the demonstration board, so the system will function without fan cooling, but the demonstration board will disable operation if the PCB temperature exceeds 85 ºC, and will re-enable once the temperature drops to 75 ºC.

The rated input voltage range is 36 V - 75 V, and the converter can operate at input voltage levels up to 100 V for 100 ms. The maximum rated load is 50 W. The output voltage is regulated to 3.3 V with an output load current range of 0 A - 15 A.

FEATURES

- High efficiency, > 87 % at full rated load current
- Delivers up to 15 amps of output current with minimal de-rating - no heat sink required
- Wide input voltage range: 35 V - 75 V, with 100 V 100 ms input voltage transient capability
- No minimum load requirement means no preload resistors required
- Remote sense for the output voltage compensates for output distribution drops
- On/Off control referenced to input side
- Input under-voltage lockout disables converter at low input voltage conditions
- Output short circuit protection protects converter and load from permanent damage and consequent hazardous conditions
- Output over-voltage protection protects load from damaging voltages
- Thermal shutdown protects converter from abnormal environmental conditions

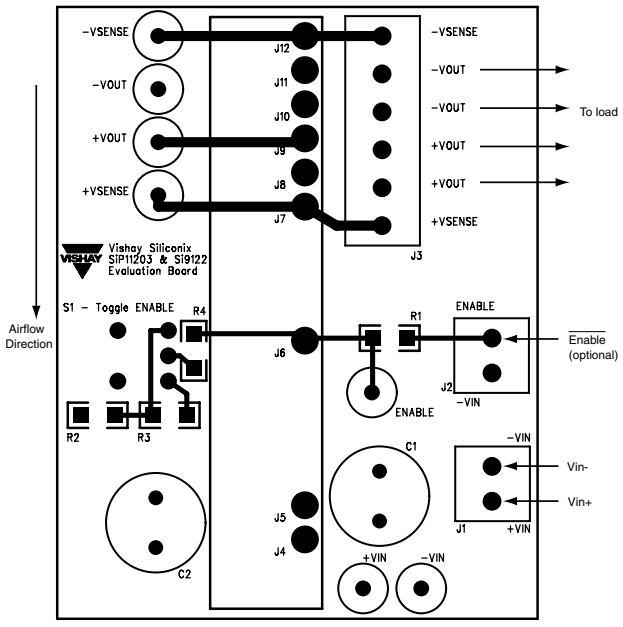


Figure 1. SiP11203 Test Board Layout

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DEMONSTRATION BOARD INFORMATION

The demonstration board is an 8-layer board in the eighth-brick form factor, manufactured in 2 oz copper. The circuit schematics for the SiP11203 demonstration board are illustrated in Figure 2 and Figure 3.

Power Conversion Circuit

The primary power circuit is a half-bridge configuration with a 4:1 turns ratio transformer, T_2, connected between the switching pole of the half-bridge and the center tap of the capacitive input filter. The half-bridge capacitors C_{10} to C_{17} are configured as two series-connected banks of four parallel-connected 1 µF ceramic capacitors. Resistors R_{20} and R_{21} provide voltage balancing and discharge paths for the capacitor banks. The primary side half-bridge circuit is driven using the Si9122 controller IC. This generates both the primary MOSFET drive signals as well as the timing signals for the secondary side synchronous MOSFETs. These timing signals, SRL and SRH, are coupled to the secondary through the pulse transformer T_1. The SiP11203 uses the timing information to drive the secondary synchronous MOSFETs Q_3 to Q_6. The secondary side synchronous MOSFETs rectify the center-tapped transformer secondary voltage, the output of which is filtered by the LC-filter L_1-C_{28}-C_{31}. L_1 is a 900 nH inductor, C_{28} is a 22 µF tantalum capacitor and C_{31} is a 100 µF ceramic capacitor.

RCD snubbers are placed across the synchronous rectifier MOSFETs in order to clamp the secondary leakage inductance voltage spike and reduce switching losses. Some of the main switching circuit waveforms are plotted in Figure 4. The converter efficiency over the line and load range is depicted in Figure 5. Note that these efficiency readings do not take account of the voltage drops across the plug-in pins of the demonstration board.

Bias Supply

The primary bias supply, V_{CC}, is a 10.4 V supply that is generated from an auxiliary winding, $L_{1\text{-}B}$ of the output filter inductor. The auxiliary winding turns ratio is 3.333:1, resulting in an auxiliary winding voltage of approximately 11 V during the inductor current ramp-down period. This voltage is rectified and filtered by diode D_4 and capacitors C_{23} and C_{26}. During startup and other conditions such as short-circuited output, the primary bias voltage is supplied by means of a 9.1 V linear pre-regulator on the Si9122 controller. An external PNP pre-regulator transistor Q_8 is provided to divert the main power dissipation away from the Si9122 during the period when the 9.1 V bias is being utilised. The rise of V_{CC} and V_O during startup is depicted in Figure 6 (a). It is clear that converter operation commences when V_{CC} reaches 9.1 V and, the change to the auxiliary bias level can also be seen.

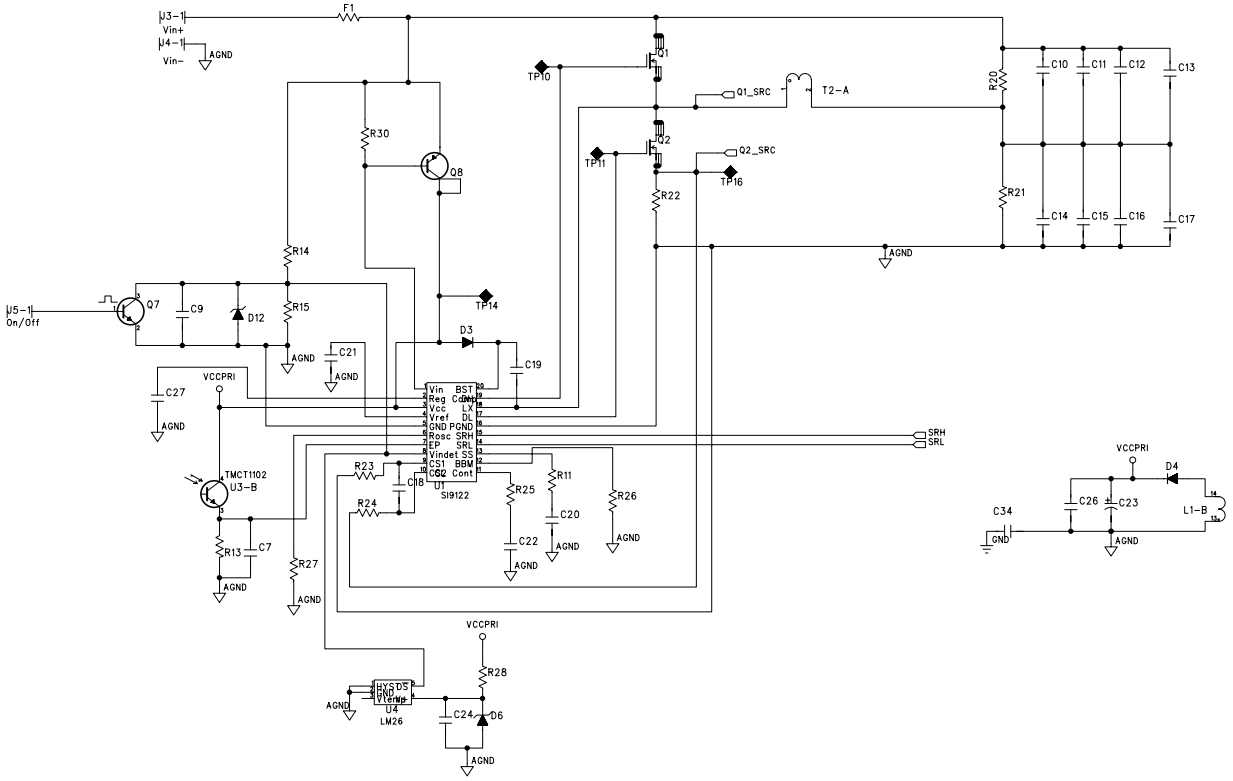


Figure 2. SiP11203 Demonstration Board Primary Side Schematic

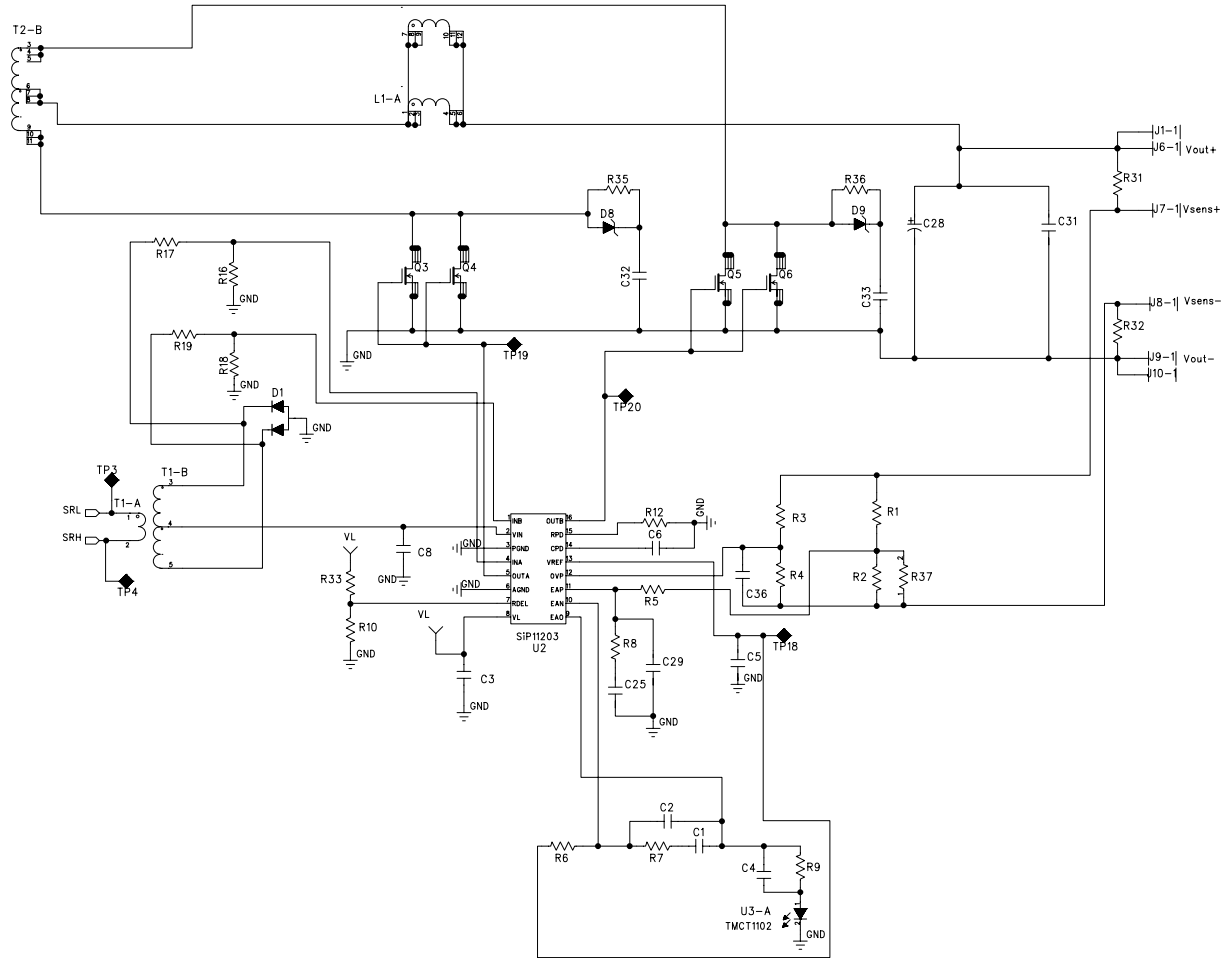


Figure 3. SiP11203 Demonstration Board Secondary Side Schematic

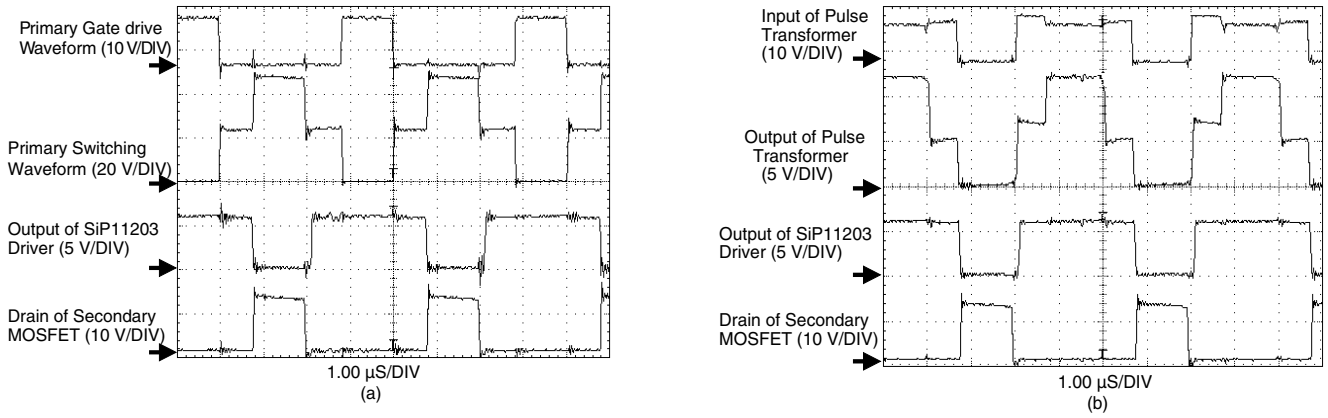


Figure 4. (a) Primary switching waveforms and the secondary switching waveforms. (b) The gate driving waveform and the secondary switching waveform.

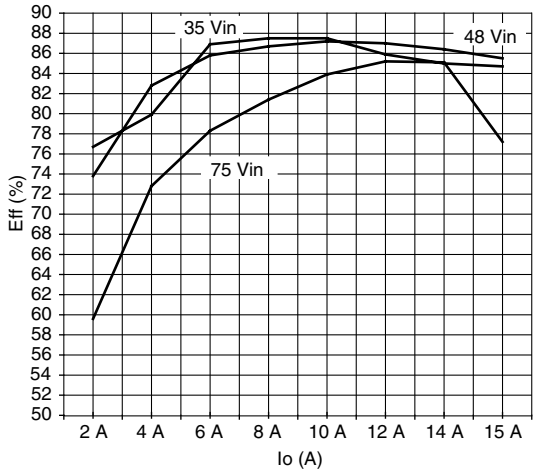


Figure 5. Converter efficiency over line voltage and load range

The secondary bias supply (V_{IN} on the SiP11203) is provided from V_{CC} via the timing signals SRH and SRL generated by the Si9122. These timing signals drive the positive and negative terminals of the primary winding of pulse transformer T_1. This transformer has a step-down ratio of 4:3 for each secondary winding. The secondary windings are center tapped, with a capacitive filter placed at the center tap point, and rectifier diodes anode-connected to ground, connected to each end of the secondary windings. This arrangement means that the timing information is coupled to the SiP11203, while a bias voltage is also available at the center-tap to power the SiP11203. This bias voltage V_{IN} is used to power the output drivers OUTA and OUTB. It is also internally regulated to a 5 V bias, V_L, which powers the other internal circuitry on the SiP11203. The voltage on one of the pulse transformer secondary windings wrt ground is shown in Figure 6 (b). It can be seen from this that the center-tap voltage, which provides the V_{IN} supply to the SiP11203, is equal to the average value of the secondary voltage.

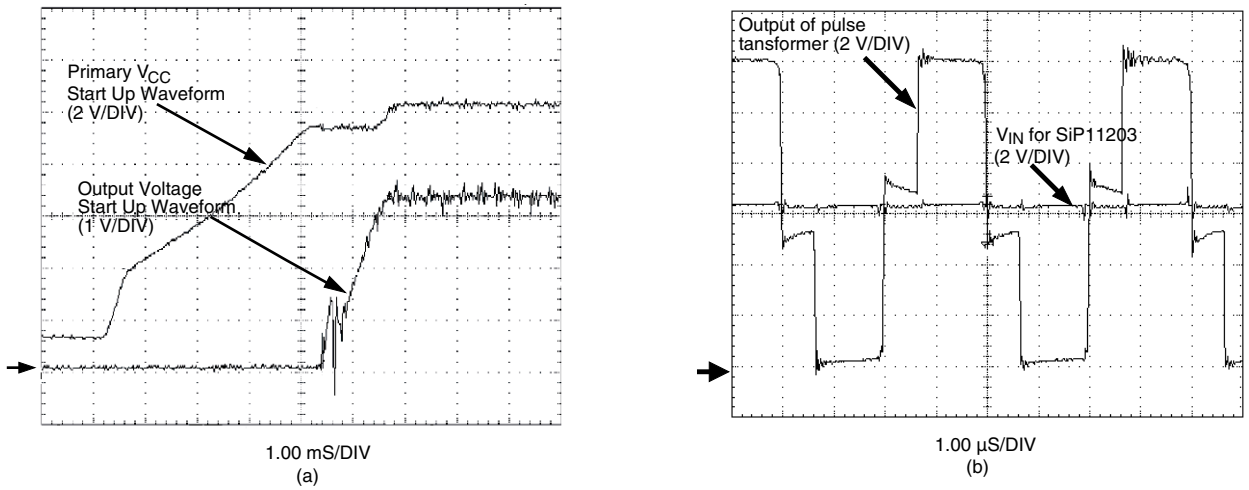


Figure 6. (a)V_{CC}, V_O, during startup (b)Pulse Transformer Secondary Voltage, Pulse Transformer Center-Tap Voltage, V_{IN}.

Magnetic Component

The main power transformer structure is illustrated in Figure 7. The multilayer PCB layout is described in Table 1. The primary magnetizing inductance is between 11 µH and 15 µH, and the turns ratio is 4:1:1. The core is a combination of an E14/3.5/5 core and its associated I-plate in 3F3 material. The output filter inductor structure is illustrated in Figure 8 and the multilayer PCB layout is described in Table 2. The inductor has 2 sections of 3 turns connected in parallel, with a custom ground center gap to yield an inductance value between 850 nH and 900 nH. The auxiliary winding is constructed of 10 turns, divided between 2 layers, resulting in a 10:3 turns ratio between the auxiliary and main windings. The core is a combination of an E14/3.5/5 core and its associated I-plate in 3F3 material.

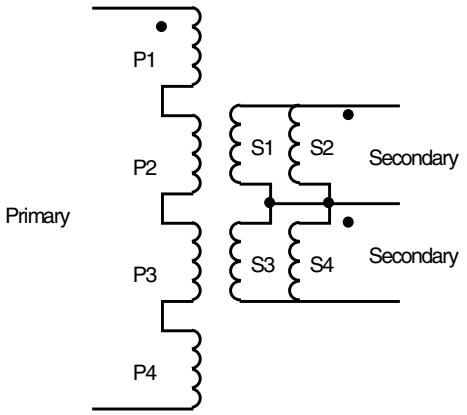


Figure 7. Power Transformer Structure

MULTILAYER PCB DESIGN FOR POWER TRANSFORMER		
Layer	**Winding**	**No. of Turns**
1	P1	1
2	S1	1
3	P2	1
4	S2	1
5	P3	1
6	S3	1
7	P4	1
8	S4	1

Table 1.

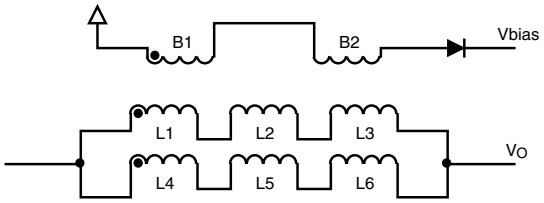


Figure 8. Power Inductor Structure

MULTILAYER PCB DESIGN FOR POWER INDUCTOR		
Layer	**Winding**	**No. of Turns**
1	L1	1
2	L2	1
3	L3	1
4	B1	5
5	B2	5
6	L4	1
7	L5	1
8	L6	1

Table 2.

The pulse transformer structure is illustrated in Figure 9. The multilayer PCB layout is described in Table 3. The primary magnetizing inductance is between 90 µH and 130 µH, and the turn ratio is 8:6:6. The core is a combination of two E8.8 cores in high permeability T38 material from EPCOS. These cores must be aligned very carefully, and glued together while clamped, with no glue being placed between the core legs, in order to ensure the required magnetizing inductance. If the magnetizing inductance is too low, the Si9122 will be overloaded, and the circuit will not function.

MULTILAYER PCB DESIGN FOR PULSE TRANSFORMER		
Layer	**Winding**	**No. of Turns**
1	Pa	3
2	Sa	3
3	Sb	2
4	Pb	3
5	Sc	3
6	Sd	3
7	Pc	3
8	-	-

Table 3.

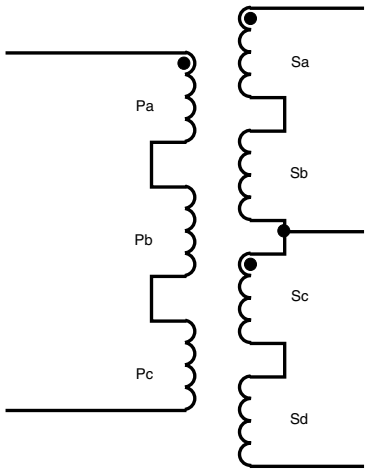


Figure 9. Pulse Transformer Structure

Controller

The SiP11203 possesses a voltage reference and Op Amp, which can be used to control the output voltage. The reference voltage V_{REF} is compared with the scaled output voltage, and the compensated error voltage drives the opto-coupler diode $U_{3\text{-}A}$. The current in the opto-coupler transistor $U_{3\text{-}B}$ is converted to a voltage signal by R_{13} and this signal is applied to the EP pin of the Si9122, where it is converted to a PWM output.

The compensation structure is depicted in Figure 10.

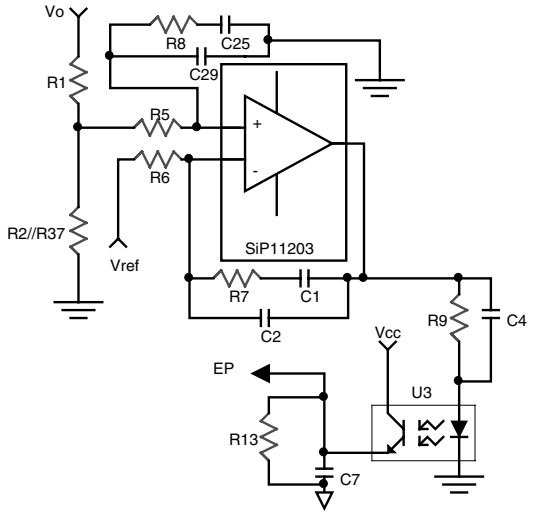


Figure 10. Controller Compensation Structure

The equation describing the compensation circuitry is:

$$\frac{R_{13}CTR}{R_9}\ \frac{(1+SR_7C_1)(1+SR_9C_4)}{SR_6(C_1+C_2)(1+SR_{13}C_7)\left(1+SR_2\frac{C_1C_2}{C_1+C_2}\right)}$$

Where CTR is the current transfer ratio of the opto-coupler, and where $R_5 = R_6$, $R_8 = R_7$, $C_{25} = C_1$ and $C_{29} = C_2$.

An origin pole, two zeroes and two poles can be potentially synthesized. Hence, either Type 2 or Type 3 compensation can be implemented. In the demonstration board, Type 2 compensation is implemented, resulting in a bandwidth in the region of 10 kHz. The transient response of the output voltage to 5 A load steps is depicted in Figure 11.

Startup and Shutdown

The startup sequence is described as follows:

1. The primary side duty cycle ramps up from its minimum value at rate determined by the charging of the soft-start capacitor C_{20}. At this point, the converter is operating open loop.
2. Simultaneously, the bias voltage V_{IN} for the SiP11203 increases as decoupling capacitor C_8 is charged from SRH and SRL through the pulse transformer. Regulated voltage V_L also increases as C_8 is charged.
3. Once the voltage on the V_L pin of the SiP11203 has reached 3.5 V, the internal circuitry on the IC (apart from output drivers) becomes functional, and the converter begins to regulate. However, the reference voltage is still at zero.
4. When V_L reaches 4.5 V, the reference voltage ramps towards 1.225 V, at rate determined by the charging of C_5. The output voltage should then track the reference voltage increase.

The various time constants described above must be designed and synchronized to ensure a smooth startup sequence for the converter. The SiP11203 also incorporates a functionality whereby the on-time of the synchronous MOSFETs is increased gradually at startup, in order to minimize oscillation and steps in the output voltage. This is the phase-in function of SiP11203. This is accomplished by variation of R_{10}. This functionality is disabled if the RDEL pin of the SiP11203 is tied to V_L, by connecting a zero ohm link in the R_{33} position. In Figure 12(a), the two distinct stages of startup can be seen, where the output initially rises open loop, and subsequently follows the reference voltage.

The SiP11203 incorporates a controlled shutdown feature, whereby the gates of the synchronous MOSFETs are pulled to ground gradually once it is ascertained that a shutdown event has indeed occurred. This prevents destructive under-voltage transients due to LC-filter oscillation that normally occurs on shutdown when both gate voltages remain high. Variation of the shutdown detection time and gate discharge time is accomplished by variation of R_{12} and C_6. The controlled shutdown and minimal under-voltage swing are depicted in Figure 12(b). The maximum under-voltage seen is 0.7 V.

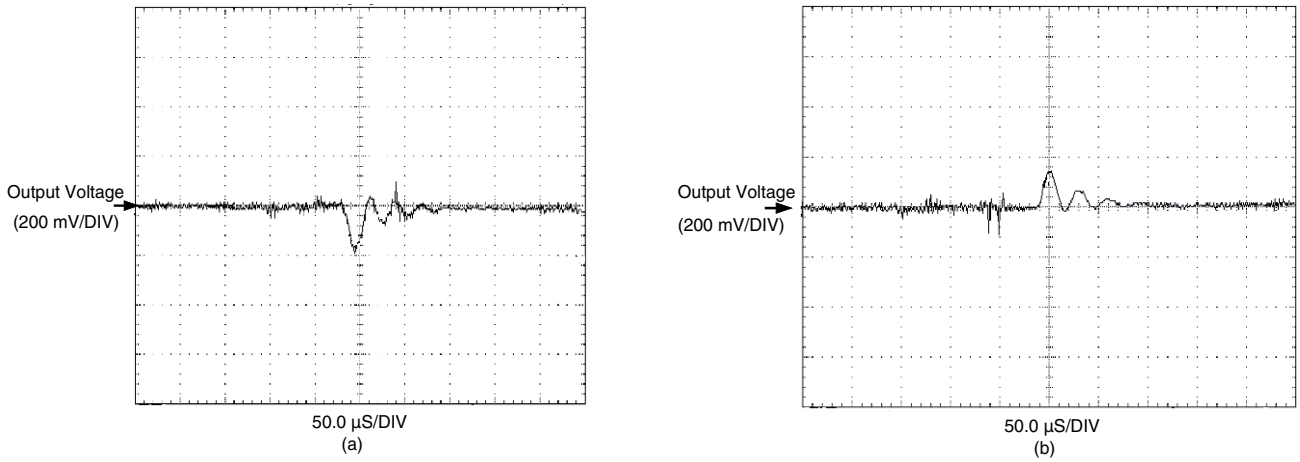


Figure 11. (a) Output voltage response to 5 A step load increase (b) Output voltage response to 5 A step load decrease (both ac coupling; 200 mV/div- 12.5 A ↔ 7.5 A, 48 V input, 200 mA/µS slew rate)

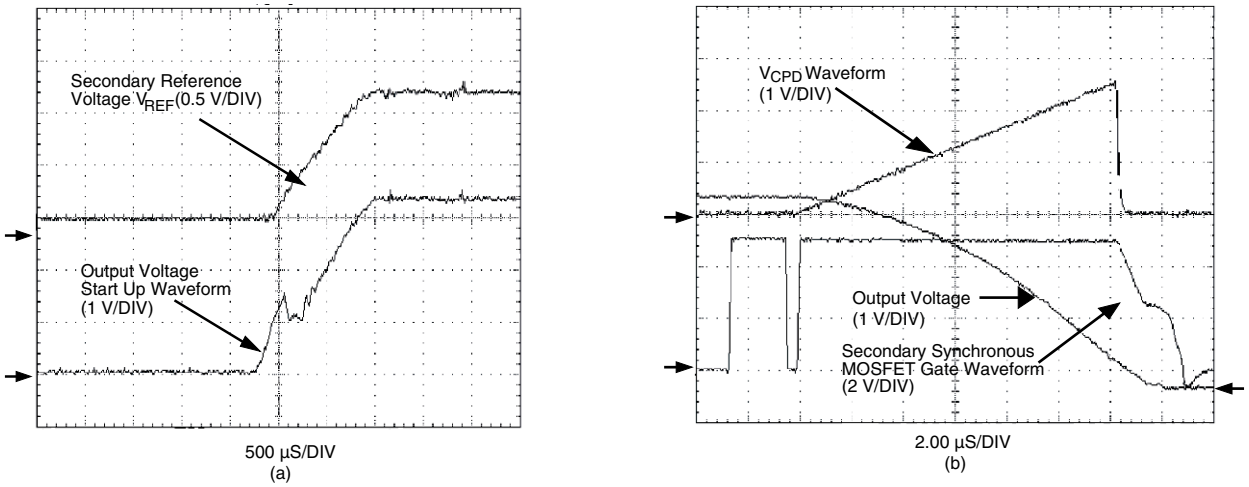


Figure 12. (a) Rise of V_{REF} and V_O during startup (b) V_{Cpd}, OUTA and V_O during shutdown (both at 48 V input and 15 A load)

Protection

Over-current detection and protection is performed within the Si9122 in conjunction with the current sense resistor R_{22}. Over-voltage protection is incorporated in the SiP11203 and can be set using the potential divider R_3-R_4. Startup into an over-voltage is illustrated in Figure 13, where the over-voltage is discharged, and the switching and reference voltage are then disabled. Thermal protection is implemented in IC U4, an LM26 temperature sensing IC, which will disable operation if the PCB temperature exceeds 85 ºC, and will re-enable once the temperature drops to 85 ºC.

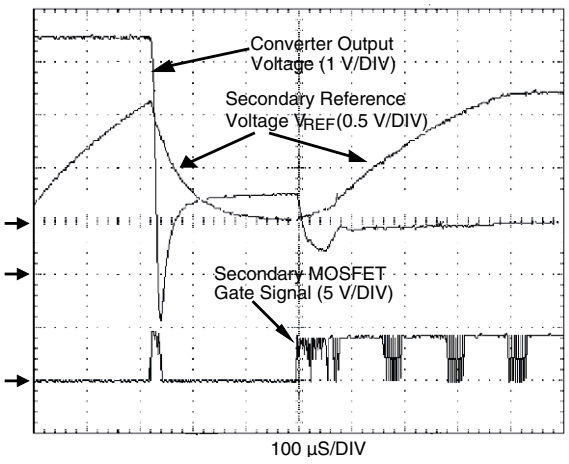


Figure 13. Vo, Vref and OUTA on startup into an over-voltage.

Test Points

Several test points are provided on the topside of the demonstration board for ease of probing. These are the primary side MOSFET gate signals (TP10 and TP11), the primary current sense signal (TP16), primary V_{CC} (TP14), pulse transformer primary signals SRL and SRH (TP3 and TP4), secondary side synchronous MOSFET gate signals (TP19 and TP20) and SiP11203 reference voltage (TP18). The locations for these test points are shown in Figure 14. The bottom side component locations are also shown.

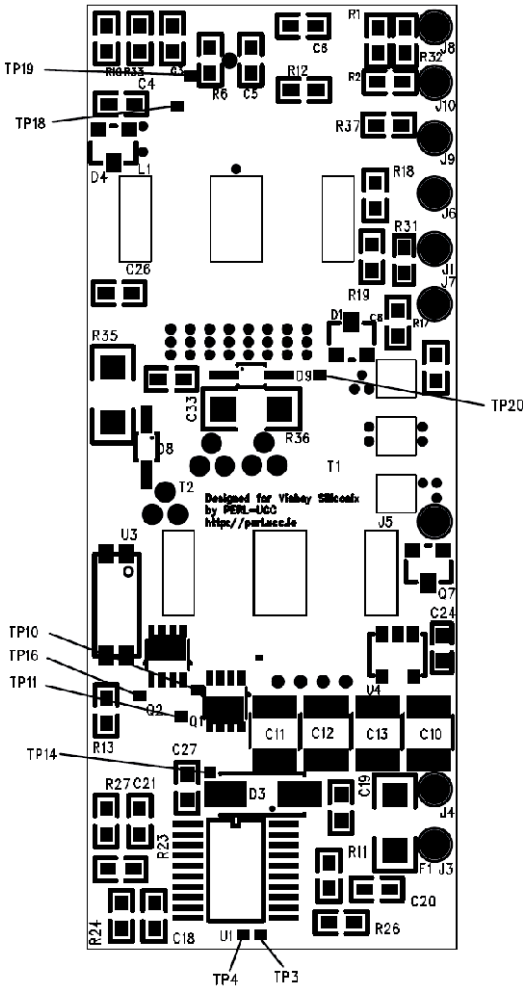
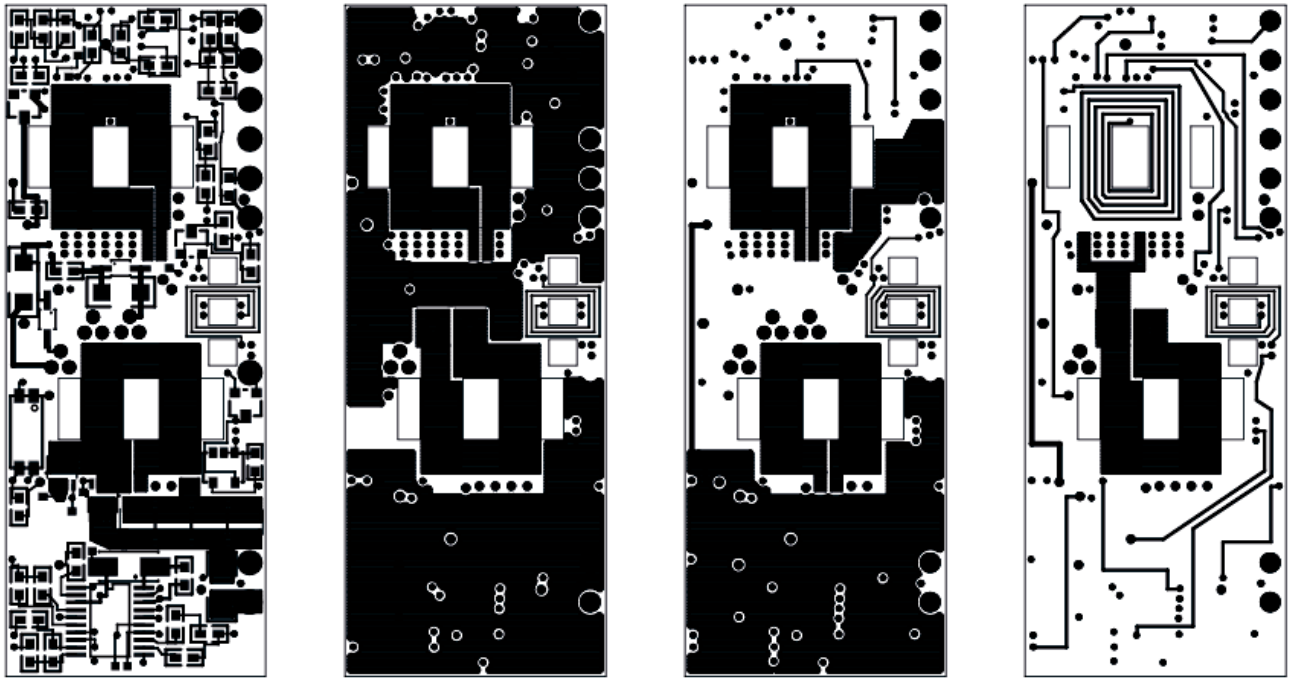


Figure 14. SiP11203 Demonstration Board Component Layout

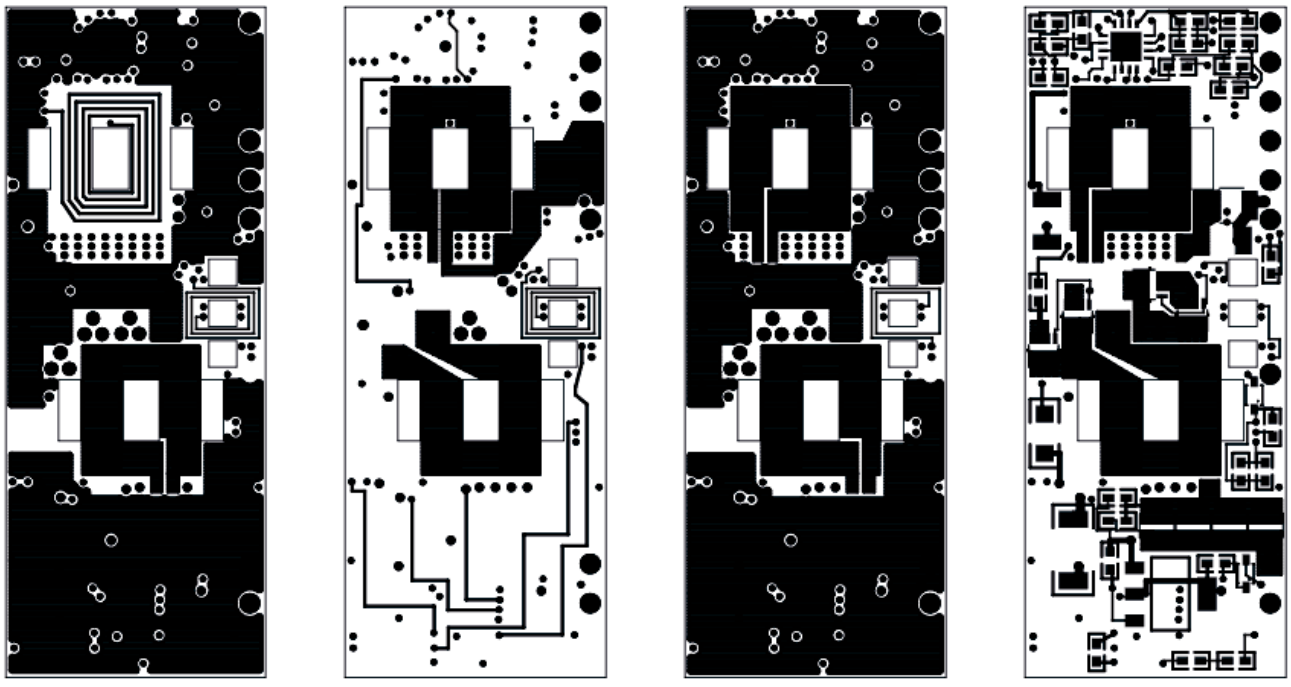
PCB Layout and Bill of Materials

The other PCB layers are shown in Figure 15 and Figure 16. The component listing is given in Table 4.



Layer 1 Layer 2 Layer 3 Layer 4

Figure 15. SiP11203 Demonstration Board PCB layers 1-4



Layer 1 Layer 2 Layer 3 Layer 4

Figure 16. SiP11203 Demonstration Board PCB Layers 5-8

PARTS LIST

Line Number	Reference Designator	Value/Type	Manufacturer	Vishay/Farnell/Digikey Part No.
1	C01	6.8 nF, 50 V, X7R, 0603	Vishay	VJ0603Y682KXACW1BC
2	C02	470 pF, 50 V, X7R, 0603	Vishay	VJ0603A471JXACW1BC
3	C03	220 nF, 10 V, X5R, 0603	Vishay	VJ0603V224ZXJCW1BC
4	C04	NC		
5	C05	470 nF, 50 V, Y5V, 0603	Vishay	VJ0603V474MXJCW1BC
6	C06	10 pF, 50 V, X7R, 0603	Vishay	VJ0603A100JXACW1BC
7	C07	47 pF, 50 V, NP0, 0603	Vishay	VJ0603A470JXACW1BC
8	C08	1 uF, 50 V, X5R, 0603	Vishay	VJ0603G105KXQCW1BC
9	C09	1 nF, 50 V, X7R, 0603	Vishay	VJ0603Y102KXACW1BC
10	C10	1 uF, 50 V, X7R, 1210		490-1863-2-ND
11	C11	1 uF, 50 V, X7R, 1210		490-1863-2-ND
12	C12	1 uF, 50 V, X7R, 1210		490-1863-2-ND
13	C13	1 uF, 50 V, X7R, 1210		490-1863-2-ND
14	C14	1 uF, 50 V, X7R, 1210		490-1863-2-ND
15	C15	1 uF, 50 V, X7R, 1210		490-1863-2-ND
16	C16	1 uF, 50 V, X7R, 1210		490-1863-2-ND
17	C17	1 uF, 50 V, X7R, 1210		490-1863-2-ND
18	C18	220 pF, 50 V, NP0, 0603	Vishay	VJ0603A221JXACW1BC
19	C19	100 nF, 50 V, Y5V, 0603	Vishay	VJ0603V104MXACW1BC
20	C20	10 nF, 50 V, X7R, 0603	Vishay	VJ0603Y103KXACW1BC
21	C21	1 uF, 10 V, X5R, 0603	Vishay	VJ0603G105KXQCW1BC
22	C22	4.7 nF, 50 V, X7R, 0603	Vishay	VJ0603Y472KXACW1BC
23	C23	22 uF, 16 V, Tantalum, Case B	Vishay	293D226X9016B2TE3
24	C24	100 nF, 50 V, Y5V, 0603	Vishay	VJ0603V104MXACW1BC
25	C25	6.8 nF, 50 V, X7R, 0603	Vishay	VJ0603Y682KXACW1BC
26	C26	100 nF, 50 V, Y5V, 0603	Vishay	VJ0603V104MXACW1BC
27	C27	3.3 nF, 50 V, X7R, 0603	Vishay	VJ0603Y332KXACW1BC
28	C28	22 uF, 16 V, Tantalum, Case B	Vishay	293D226X9016B2TE3
29	C29	470 pF, 50 V, X7R, 0603	Vishay	VJ0603A471JXACW1BC
30	C31	100 uF, 6.3 V, X5R, 1210		587-1388-1-ND
31	C32	2.2 nF, 50 V, X7R, 0603	Vishay	VJ0603Y222KXACW1BC
32	C33	2.2 nF, 50 V, X7R, 0603	Vishay	VJ0603Y222KXACW1BC
33	C34	1 nF, 2 kV, X7R, 1206		7569289
34	C36	220 pF, 50 V, NP0, 0603	Vishay	VJ0603A221JXACW1BC
35	D01	25 V 200 mA Dual Schottky Diode SOT-23	Vishay	BAS40-06-GS08
36	D03	1 A, 100 V Ultrafast Rectifier	Vishay	ES1B-E3
37	D04	0.2 A 200 V Switching Diode SOT23	Vishay	BAS20-V-GS08
38	D06	4.3 V 300 mW Zener Diode SOD-323	Vishay	BZX384C4V3-V-GS08
39	D08	400 mA, 40 V Schottky SOD-323		ZHCS400CT-ND
40	D09	400 mA, 40 V Schottky SOD-323		ZHCS400CT-ND
41	D12	6V8 300 mW Zener Diode SOD-323	Vishay	BZX384C6V8-V-GS08
42	F01	3A Quick Blow 1206, 3216CP-3A		968912
43	J01	PC PIN .040 DIA 3301 SERIES, 3301-2-14-21-00-00-08-0		ED5058-ND
44	J03	PC PIN .040 DIA 3301 SERIES, 3301-2-14-21-00-00-08-0		ED5058-ND
45	J04	PC PIN .040 DIA 3301 SERIES, 3301-2-14-21-00-00-08-0		ED5058-ND
46	J05	PC PIN .040 DIA 3301 SERIES, 3301-2-14-21-00-00-08-0		ED5058-ND
47	J06	PC PIN .040 DIA 3301 SERIES, 3301-2-14-21-00-00-08-0		ED5058-ND
48	J07	PC PIN .040 DIA 3301 SERIES, 3301-2-14-21-00-00-08-0		ED5058-ND
49	J08	PC PIN .040 DIA 3301 SERIES, 3301-2-14-21-00-00-08-0		ED5058-ND
50	J09	PC PIN .040 DIA 3301 SERIES, 3301-2-14-21-00-00-08-0		ED5058-ND

PARTS LIST				
Line Number	**Reference Designator**	**Value/Type**	**Manufacturer**	**Vishay/Farnell/Digikey Part No.**
51	J10	PC PIN .040 DIA 3301 SERIES, 3301-2-14-21-00-00-08-0		ED5058-ND
52	L01	E14/3.5/5, 3F3, 900nH, AL = 100 nH/T^2		
53	Q01	100 V PowerPak 1212 MOSFET	Vishay	Si7810DN-T1-E3
54	Q02	100 V PowerPak 1212 MOSFET	Vishay	Si7810DN-T1-E3
55	Q03	20 V, PowerPak 1212 MOSFET	Vishay	Si7108DN-T1-E3
56	Q04	20 V, PowerPak 1212 MOSFET	Vishay	Si7108DN-T1-E3
57	Q05	20 V, PowerPak 1212 MOSFET	Vishay	Si7108DN-T1-E3
58	Q06	20 V, PowerPak 1212 MOSFET	Vishay	Si7108DN-T1-E3
59	Q07	50 V, 100 mA digital NPN transistor, SOT23	Vishay	MMUN2213LT1OSCT-ND
60	Q08	100 V, 5 A SOT223 PNP transistor		ZX5T953GCT-ND
61	R01	1k 0603 1 %	Vishay	CRCW06031K00FKEA
62	R02	604R 0603 1 %	Vishay	CRCW0603604RFKEA
63	R03	12k 0603 1 %	Vishay	CRCW060312K0FKEA
64	R04	6k8 0603 1 %	Vishay	CRCW06036K80FKEA
65	R05	5k1 0603 1 %	Vishay	CRCW06035K10FKEA
66	R06	5k1 0603 1 %	Vishay	CRCW06035K10FKEA
67	R07	560R 0603 1 %	Vishay	CRCW0603560RFKEA
68	R08	560R 0603 1 %	Vishay	CRCW0603560RFKEA
69	R09	5k1 0603 1 %	Vishay	CRCW06035K10FKEA
70	R10	NC		
71	R11	10k 0603 1 %	Vishay	CRCW060310K0FKEA
72	R12	100k 0603 1 %	Vishay	CRCW0603100KFKEA
73	R13	15k 0603 1 %	Vishay	CRCW060315K0FKEA
74	R14	91k 0603 1 %	Vishay	CRCW060391K0FKEA
75	R15	10k 0603 1 %	Vishay	CRCW060310K0FKEA
76	R16	NC		
77	R17	100R0 0603 1 %	Vishay	CRCW0603100RFKEA
78	R18	NC		
79	R19	100R0 0603 1 %	Vishay	CRCW0603100RFKEA
80	R20	100k 0603 1 %	Vishay	CRCW0603100KFKEA
81	R21	100k 0603 1 %	Vishay	CRCW0603100KFKEA
82	R22	0R015 2010 1 %	Vishay	WSL2010R0150FEA
83	R23	100R0 0603 1 %	Vishay	CRCW0603100RFKEA
84	R24	100R0 0603 1 %	Vishay	CRCW0603100RFKEA
85	R25	4k7 0603 1 %	Vishay	CRCW06034K70FKEA
86	R26	56k 0603 1 %	Vishay	CRCW060356K0FKEA
87	R27	30k 0603 1 %	Vishay	CRCW060330K0FKEA
88	R28	56k 0603 1 %	Vishay	CRCW060356K0FKEA
89	R30	1MEG 0603 1 %	Vishay	CRCW06031M00FKEA
90	R31	4R7 0603 1 %	Vishay	CRCW06034R70FKEA
91	R32	4R7 0603 1 %	Vishay	CRCW06034R70FKEA
92	R33	0R0 0603 1 %	Vishay	CRCW06030000Z0EA
93	R35	47R 1206 1 %	Vishay	CRCW120647R0FKEA
94	R36	47R 1206 1 %	Vishay	CRCW120647R0FKEA
95	R37	12k 0603 1 %	Vishay	CRCW060312K0FKEA
96	T01	E8.8-T38		
97	T02	E14/3.5/5, 3F3, 4:1:1		926462 / 926474
98	U01	Si9122 Half Bridge Controller	Vishay	Si9122
99	U02	'Mulligan' Secondary Side Controller	Vishay	SiP11203
100	U03	TMCT1102 Opto-coupler	Vishay	TCMT1102
101	U04	Digital thermostat with preset trip, LM26CIM5-TPA, SOT23		4125125
102	PCB	SiP9122/SiP11203 demo board PCB		

Table 4.

Host Board Fixture Schematic, Layout and Bill of Materials

The schematic and PCB layers are shown in Figure 17 and Figure 18. The component listing is given in Table 5.

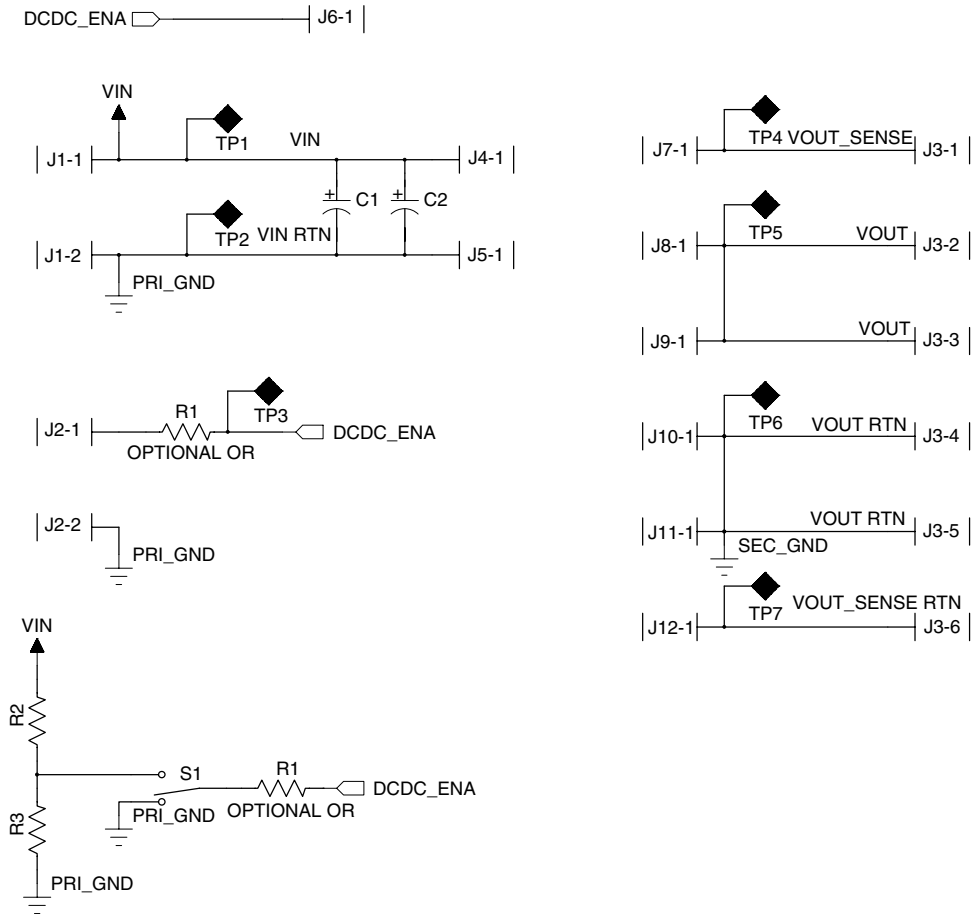


Figure 17. Host Board Fixture Schematic

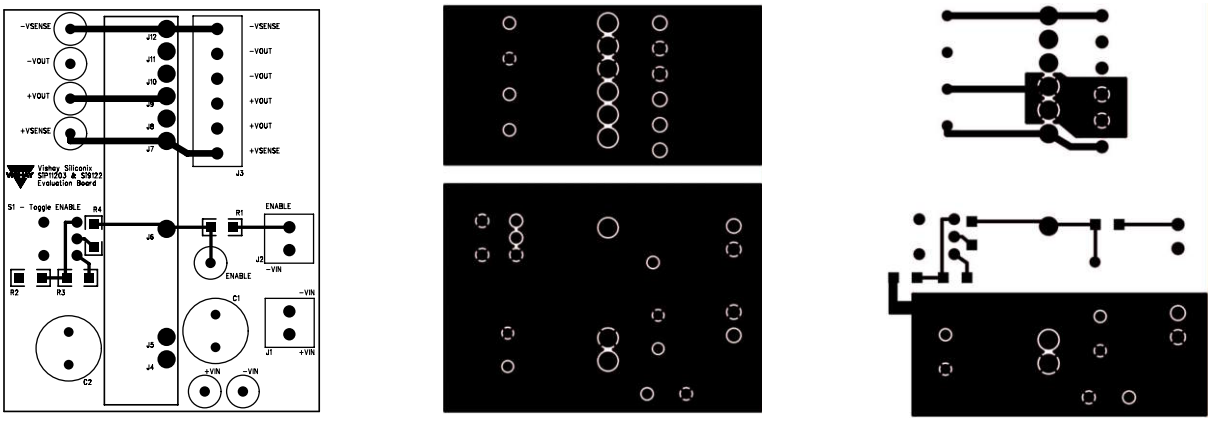


Figure 18. Host Board Fixture PCB Layers

PARTS LIST				
Per Board	**Reference Designator**	**Value/Type**	**Manufacturer**	**Vishay/Farnell/Digikey Part No.**
2	C1, C2	47 uF, 160 V EEUED2C470	Vishay	EKV00FE247M00K
2	R1, R4	0R0 link 1206	Vishay	CRCW12060000Z0EA
1	R2	16k, 1206	Vishay	CRCW120616K0FKEA
1	R3	1k1 1206	Vishay	CRCW12061K10FKEA
1	S1	Switch PCB, SPDT		9574590
2	J1, J2	Terminal Block, 3.81 mm, 2 way, 10 A		3704579
1	J3	Terminal Block, 3.81 mm, 6 way, 10 A		3704610
9	J4-J12	Socket 1.0 mm PCB hole 1.93 mm H3161-01		149318
4	TP1, TP3, TP4, TP5	Red PCB Terminal		8731144
3	TP2, TP6, TP7	Black PCB Terminal		8731128
1	PCB	SiP9122/SiP11203 demo board test fixture PCB		

Table 5.

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