Si8751/52 Data Sheet

Isolated FET Driver with Pin Control or Diode Emulator Inputs

The Si875x enables new pathways to creating custom solid state relay (SSR) configurations. Supporting customer-selected external FETs, the Si875x combines robust isolation technology with an SSR FET driver to form a complete, isolated switch. Versatile inputs provide digital CMOS pin control (Si8751) or diode emulation (Si8752) to best suit the application, plus flexible outputs to support driving ac or dc load configurations. A floating secondary side dc voltage source is unnecessary as the product generates its own self-contained gate drive output voltage, reducing cost, size, and complexity.

The Si875x eliminates the need for bulky mechanical relays which can be difficult to assemble onto PCBs and add switching noise to the system. Further, with the customer selecting their own flexible FET switch, the design can be completely optimized for the application's power, cost, and performance requirements. Traditional SSRs also integrate optocoupler-style LED inputs, which limit the operating temperature range of the solution, but the Si875x, with its input diode emulator or digital input control, experiences no such limitation and can support full industrial and automotive temperature ranges with increased stability and longer life.

The Si875x drives FET gates with a nominal 10 V using as little as 1 mA input current. Increasing the input current to 10 mA enables turn-on times as fast as 94 µs. Input side voltages on the Si8751 are flexible from 2.25 V to 5.5 V supporting seamless connection to low-power controllers. The Si875x devices provide a clamping device to prevent unintended turn-on of the external FET when a high dV/dt is present on the FET's drain.

The Si875x is qualified to the AEC-Q100 standard, making it suitable for automotive applications. Further, its 2.5 kVrms isolation rating forms the basis for full certification to UL, CSA, VDE, and CQC (pending).

Applications include mechanical relay , photo switch, or SSR replacement in motor control, valve control, HVAC relay, automotive, charging, battery monitoring, ac mains line switching, and more.

The Si8751 and Si8752 come in ROHS-compliant SOIC-8 packaging, providing a compact, industry-standard footprint and generous margin to creepage and clearance requirements.

KEY FEATURES

- Digital CMOS input option
- Diode emulation input option
- 10 V output with 1 mA input current
- As fast as 94 µs turn-on time
- Internally-generated secondary side power supply
- Miller clamp cap support for reducing inductive chatter
- DC or AC load switching support
- Drives user-selected external FETs
- 2.5 kVrms isolation rating
- UL, CSA, VDE, and CQC certifications (pending)
- AEC-Q100 qualified
- Industrial –40 to 105 °C or Automotive –40 to 125 °C temperature ranges
- ROHS-compliant SOIC-8 Package

APPLICATIONS

- Motor Controls
- Valve Controls
- HVAC Relays
- HEV/EV Automotive Charging
- Battery Monitoring
- AC Mains Line Switching

This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

1. Ordering Guide

Table 1.1. Si8751/2 Ordering Guide

Ordering Part Number[1, 2]	Input Support	Package	Temperature Range (Ambient)	Isolation Rating (kVrms)
Si8751AB-IS	Digital CMOS	SOIC-8	–40 to 105 °C Industrial	2.5 kV
Si8751AB-AS[3]	Digital CMOS	SOIC-8	–40 to 125 °C Automotive	2.5 kV
Si8752AB-IS	Diode Emulation	SOIC-8	–40 to 105 °C Industrial	2.5 kV
Si8752AB-AS[3]	Diode Emulation	SOIC-8	–40 to 125 °C Automotive	2.5 kV

Note:

1. "Si" and "SI" are used interchangeably.
2. Add an “R” at the end of the device to denote tape and reel option; 2500 quantity per reel.
3. Si875xAB-AS automotive qualification expected Q1 2017.

2. System Overview

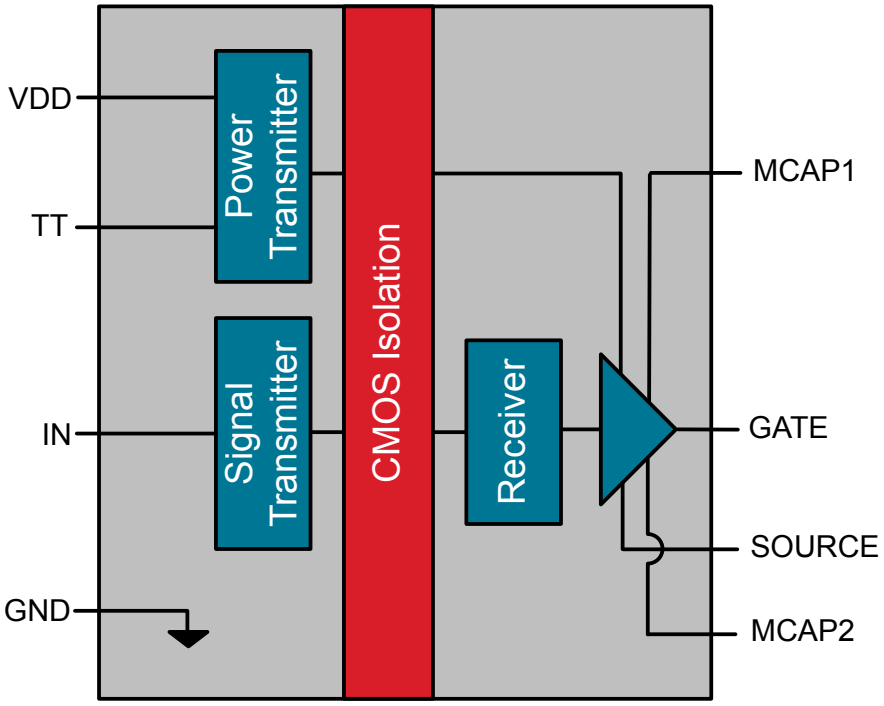

Figure 2.1. Si8751 Block Diagram

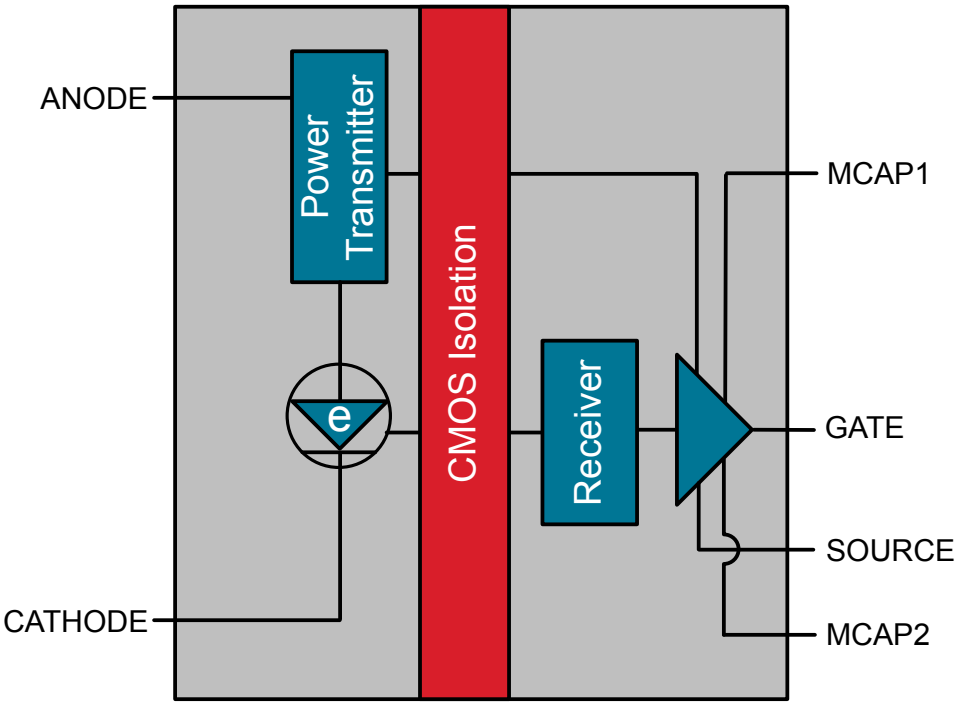

Figure 2.2. Si8752 Block Diagram

The operation of an Si875x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si875x channel is shown in the figure below.

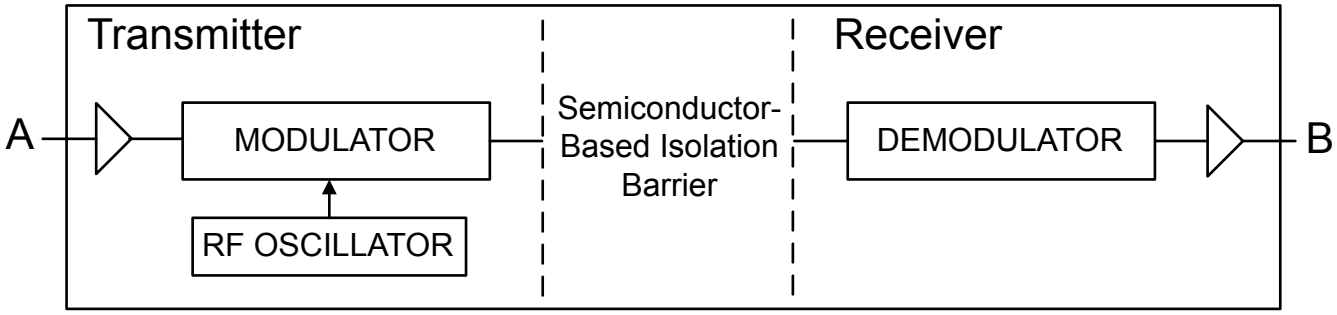

Figure 2.3. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 2.4 Modulation Scheme on page 3 for more details.

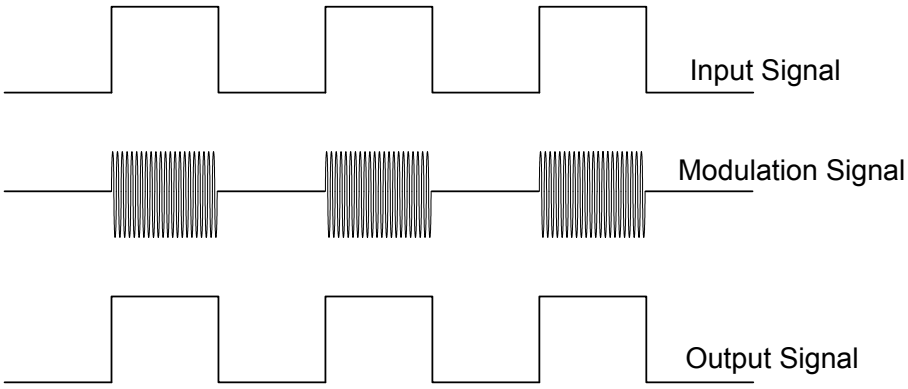

Figure 2.4. Modulation Scheme

2.1 Device Behavior

The following are truth tables for the Si875x family.

Table 2.1. Si8751 Truth Table

VDD	IN	Gate
Powered	H	H
Powered	L	L
Unpowered	X	L

Table 2.2. Si8752 Truth Table

Input Current	Gate
> $I_{f(TH)}$	H
< $I_{f(TH)}$	L

2.2 Power Supply Connections (Si8751 Only)

The Si8751 requires a 0.1 µF bypass capacitor between VDD and GND. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include a 1 µf capacitor for bulk decoupling as well as a resistor (50–300 Ω) in series with the input if the system is excessively noisy.

2.3 TT Pin Description (Si8751 Only)

The Si8751 provides a pin to control how much current is consumed by the supply when the input pin is logic high. The more current consumed by the input supply, the faster the output can turn on the external FET. This allows the application designer to optimize the tradeoff between power consumption and switching time.

Typically, this pin is connected to the supply ground through a resistor. The greater the value of the resistor, the less current is consumed by the input supply. Values can range from 0 Ω (shorted to ground) to open (TT not connected).

In addition to a resistor, a capacitor, typically 0.1 µf, can be placed in parallel to the resistor. This allows the device to draw more current to switch the external FET on quickly yet draw less supply current in the steady state. Total power over time is reduced while maintaining fast switching of the FET.

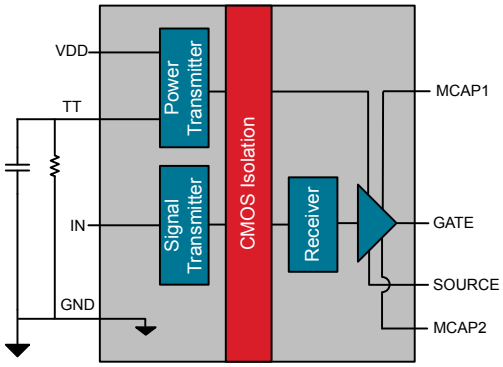

Figure 2.5. Si8751 TT Example

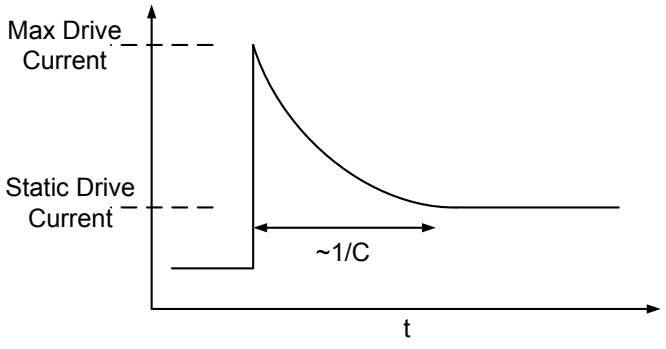

Figure 2.6. Drive Current vs. Time Using TT with Capacitor

2.4 LED Emulator Input (Si8752 Only)

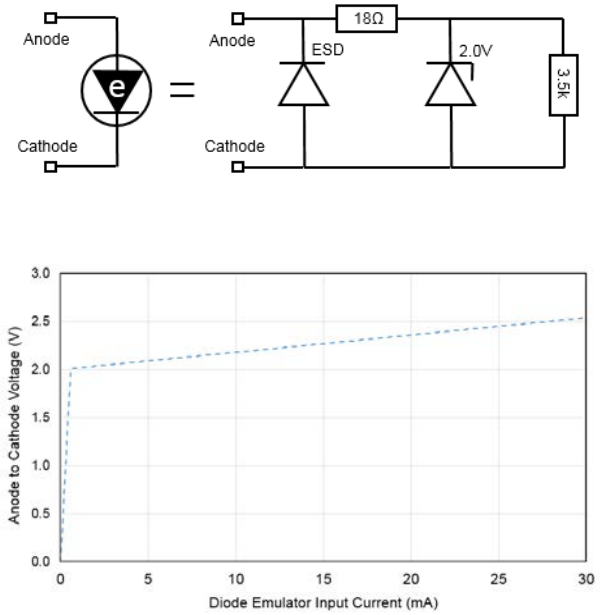

Figure 2.8. Diode Emulator Model and I-V Curve

The Si8752 uses input current to achieve the development of power across the isolation barrier. Therefore, the more current provided to the input, the more power is developed on the isolated side of the device. This translates into a faster turn on time of the external FET. This benefit is limited to an input current of about 15 mA. Beyond that, increasing the input current has little effect on the switching time of the external FET.

2.5 Output Description

The output of the Si875x device develops a positive voltage on the GATE pin with respect to the SOURCE pin. This voltage is used to turn on a typical field effect transistor (FET). Because power is transmitted across the isolation barrier, no isolated supply is required.

This can be used to drive a FET configured as a switch for a dc load. It can also be used to drive a pair of FETs configured as a switch for an ac load. See 3. Applications.

2.6 Miller Clamp

2.6.1 Miller Clamp Description

The Si875x devices provide a clamping device to prevent unintended turn on of the external FET when a high dV/dt is present on the FET's drain. To use this feature, a capacitor is connected between the drain(s) of the FET(s) and one of the MCAPx inputs. A sudden, positive slope on this pin will cause the clamp device within the Si875x to activate and provide a low impedance path between the gate and source pins. This will prevent the FET from being unintentionally turned on.

The Si875x device provides two miller clamp input pins. This allows for both FET's to be protected from unintended turn on when the device is used in an AC switch configuration. In this case each drain is connected to an MCAPx input through a capacitor.

Connection to a MCAPx pin, and use of the Miller Clamp feature, is optional. The device will function as expected if these pins are left unconnected.

2.6.2 Sizing Miller Clamp Capacitors

The recommended value of the capacitor used to connect the drain of the external FET to the Si875x device is typically 10 pf. If the application has a very large dV/dt and the clamp is not adequately keeping the external FET off, then this capacitor value can be increased up to 100 pf. The voltage rating of the capacitor should be greater than or equal to the peak voltage expected at the drain of the FET.

3. Applications

The following examples illustrate typical circuit configurations using the Si8751/52.

3.1 DC SSR Example

The Si875x device can be used to control a dc load as shown in the following figure:

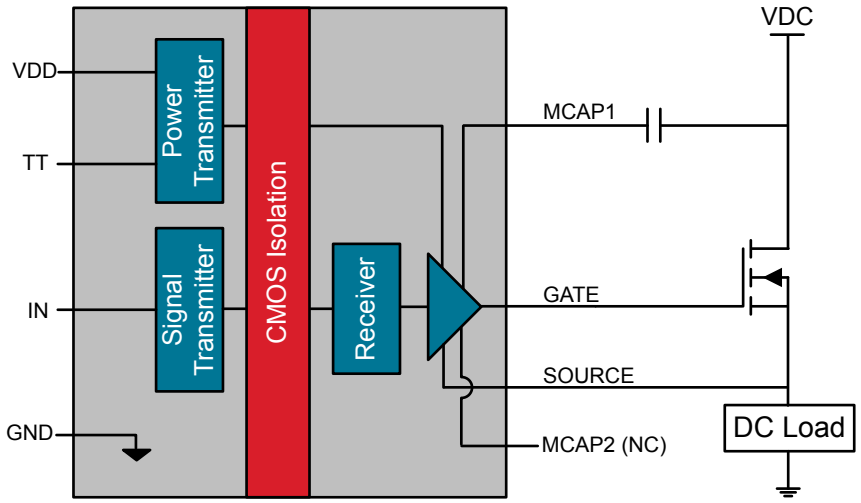

Figure 3.1. Driving an FET for DC Load Including Miller Clamp Capacitor

In this configuration, the Si8751 charges the gate of the external FET; turning it on. This switches on power, supplied by VDC, to the load. The output side circuitry is identical if using the Si8752.

3.2 AC SSR Example

The Si875x can be used to control power to an ac load using the following circuit:

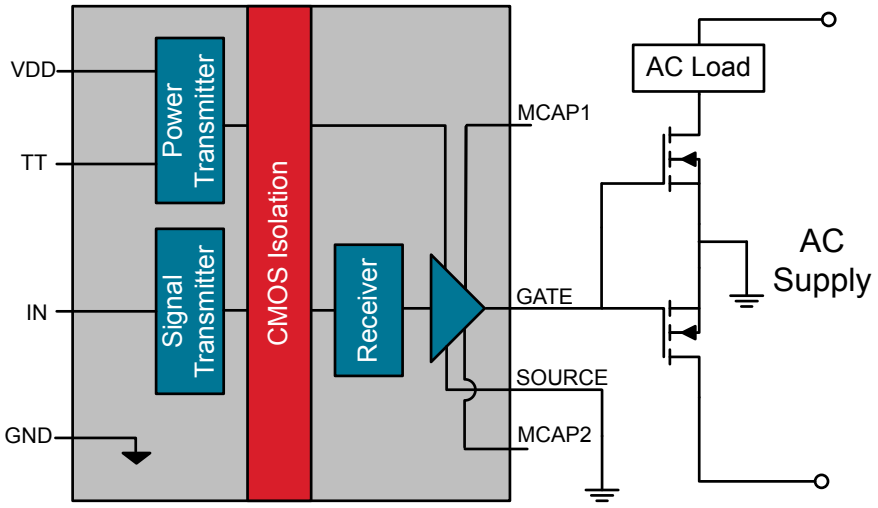

Figure 3.2. Driving FETs for AC Load Switching

In this configuration, both FET's are turned on by the charge delivered by the Si8751. This allows ac current to flow to the load. When the Si875x is turned off, charge is drained form the gates of both FET's and the ac current is turned off. The output side circuitry is identical if using the Si8752.

4. Electrical Specifications

Table 4.1. Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8751 Only						
Input Side						
Supply Voltage	VDD		2.25	3.3	5.5	V
Supply Current	IDD	IN = 0V	—	140	—	nA
		IN = VDD, TT = GND	—	13.8	17	mA
		IN = VDD, TT = 10 kΩ	—	7.8	9.5	mA
		IN = VDD, TT unconnected	—	1.5	1.8	mA
High Level Input Voltage	V_{IH}		50% of VDD	—	—	V
Low Level Input Voltage	V_{IL}		—	—	25% of VDD	V
Input Hystersis	V_{HYS}		—	180	—	mV
Driver Side						
GATE Off Voltage	$V_{G(OFF)}$	IN = 0 V	—	0	—	mV
GATE On Voltage	$V_{G(ON)}$	IN = VDD, TT = GND	7.5	10	13	V
		IN = VDD, TT = 10 kΩ	9	10.8	13	V
		IN = VDD, TT unconnected	9	10.8	13	V
GATE On Impedance	R_G	IN = VDD, TT = GND	—	162	330	kΩ
		IN = VDD, TT = 10 kΩ	—	265	370	kΩ
		IN = VDD, TT unconnected	—	1.5	1.85	MΩ
Turn-off Time	$T_{G(OFF)}$	IN = 0 V	—	15	35	µs
Turn-on Time (50% of $V_{G(ON)}$)	$T_{G(ON)}$	TT = GND	—	42	120	µs
		TT = 10 kΩ	—	58	170	µs
		TT unconnected	—	286	650	µs
Turn-on Time (90% of $V_{G(ON)}$)	$T_{G(ON)}$	TT = GND	—	85.3	190	µs
		TT = 10 kΩ	—	130	260	µs
		TT unconnected	—	0.7	1.2	ms
Si8752 Only						
Input Side						
Input Current	$I_{F(ON)}$		1.0	—	30.0	mA
Guaranteed Off Current	$I_{F(OFF)}$		—	—	10	µA
Forward Voltage (OFF)	$V_{F(OFF)}$	Measured ANODE with respect to Cathode	—	0	—	V
Forward Voltage (ON)	$V_{F(ON)}$	Measured ANODE with respect to Cathode (IF = 1 to 10 mA)	1.8	—	2.35	V
		Measured ANODE with respect to Cathode (IF >10 mA and <30 mA)	2.03	—	2.7	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Driver Side						
GATE Off Voltage	$V_{G(OFF)}$	I_F = 0 mA	—	0	—	mV
GATE On Voltage	$V_{G(ON)}$	I_F = 1 mA	8	10.3	13	V
		I_F = 10 mA	8	10.3	13	V
		I_F = 30 mA	8	10.9	13	V
GATE On Impedance	R_G	I_F = 1 mA	—	2.7	3.5	MΩ
		I_F = 10 mA	—	194	300	kΩ
		I_F = 30 mA	—	168	290	kΩ
Turn-off Time	$T_{G(OFF)}$	I_F = 0 mA	—	15	35	µs
Turn-on Time (50% of $V_{G(ON)}$)	$T_{G(ON)}$	I_F = 1 mA	—	463	720	µs
		I_F = 10 mA	—	41	125	µs
		I_F = 30 mA	—	36	90	µs
Turn-on Time (90% of $V_{G(ON)}$)	$T_{G(ON)}$	I_F = 1 mA	—	1.1	1.49	ms
		I_F = 10 mA	—	94	190	µs
		I_F = 30 mA	—	82	180	µs
Si8751 and Si8752						
Miller Clamp Current	I_{MC}		—	—	6	mA
Miller Clamp Pull-Down Current	I_G	I_C = 50 µA; V_G = 1 V	5	12.8	—	mA
Gate OFF Impedance		I_{anode} = 0 mA; IN = 0	—	21.5	—	MΩ
Common Mode Transient Immunity		VCM = 1500 V	20	—	—	kV/µs

Note:
1. All measurements use 100 pF gate capacitance load unless specified.

4.1 Test Circuits

The following figure depicts a common-mode transient immunity test circuit

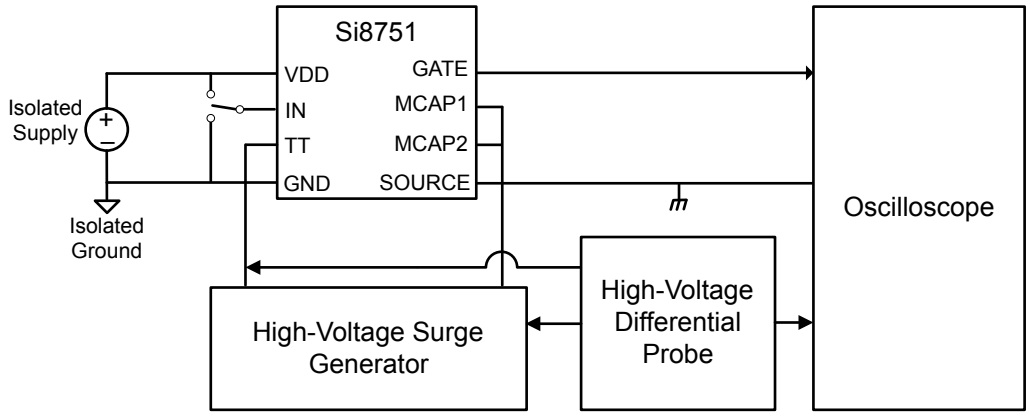

Figure 4.1. Common-Mode Transient Immunity Test Circuit

4.2 Regulatory Information

Table 4.2. Regulatory Information[1,2]

CSA
The Si875x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
60950-1: Up to 125 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
VDE
The Si875x is certified according to VDE 0884-10. For more details, see File 5006301-4880-0001.
VDE 0884-10: Up to 630 V_{peak} for basic insulation working voltage.
UL
The Si875x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V_{RMS} isolation voltage for basic protection.
CQC
The Si875x is certified under GB4943.1-2011.
Rated up to 125 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. 2. For more information, see 1. Ordering Guide.

Table 4.3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	SOIC-8 Value	Unit
Nominal Air Gap (Clearance)	L(1O1)		4.7	mm
Nominal External Tracking (Creepage)	L(1O2)		3.9	mm
Minimum Internal Gap (Internal Clearance)			0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	V
Erosion Depth	ED		0.04	mm
Resistance (Input-Output)[1]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	0.5	pF
Input Capacitance[2]	C_I		3.0	pF

Notes:

1. To determine resistance and capacitance, the Si875x is converted into a 2-terminal device. All pins on side 1 are shorted to create terminal 1, and all pins on side 2 are shorted to create terminal 2. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 4.4. IEC 60664-1 Ratings

Parameter	Test Condition	SOIC-8 Specification
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I-IV
	Rated Mains Voltages < 300 V_{RMS}	I-III
	Rated Mains Voltages < 400 V_{RMS}	I-II
	Rated Mains Voltages < 600 V_{RMS}	I-II

Table 4.5. VDE 0884 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		630	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1181	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

Note:
1. Maintenance of the safety data is ensured by protective circuits. The Si875x provides a climate classification of 40/125/21.

Table 4.6. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	SOIC-8	Unit
Safety Temperature	T_S		150	°C
Safety Input Current (Si8751)	I_S	θ_{JA} = 110 °C/W VDD = 5.5 V, T_J = 150 °C, T_A = 25 °C	206	mA
		θ_{JA} = 110 °C/W VDD = 3.63 V, T_J = 150 °C, T_A = 25 °C	313	mA
		θ_{JA} = 110 °C/W VDD = 2.75 V, T_J = 150 °C, T_A = 25 °C	413	mA
Safety Input Current (Si8752)	I_S	θ_{JA} = 110 °C/W VF = 2.5 V, T_J = 150 °C, T_A = 25 °C	454	mA

Parameter	Symbol	Test Condition	SOIC-8	Unit
Safety Input Power (Si8752)	P_S	θ_{JA} = 110 °C/W VF = 2.5 V, T_J = 150 °C, T_A = 25 °C	1136	mW
Device Power Dissipation	P_D		1	W

Note:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curves below.

Table 4.7. Thermal Characteristics

Parameter	Symbol	SOIC-8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	110	°C/W

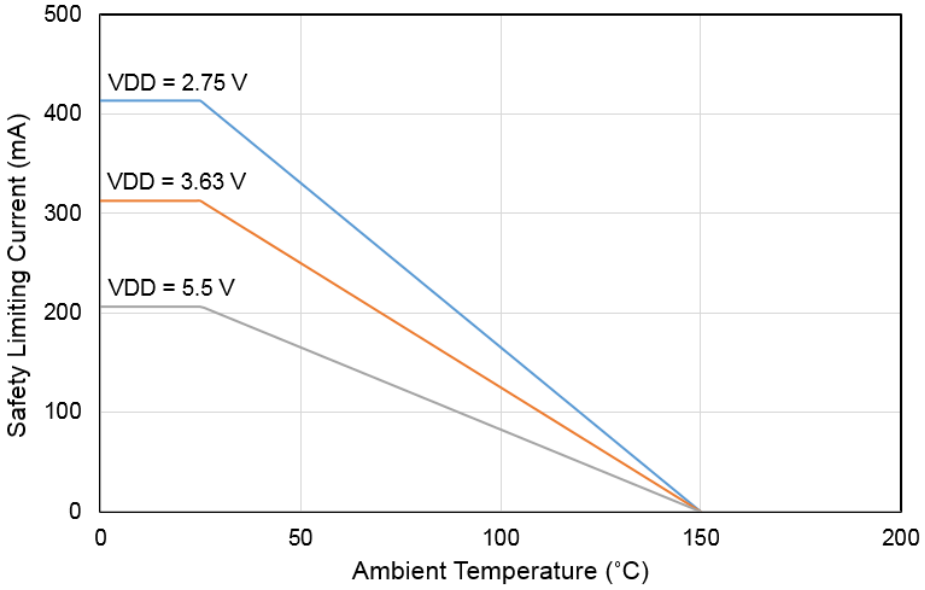

Figure 4.2. Thermal Derating Curve for Safety Limiting Current (Si8751)

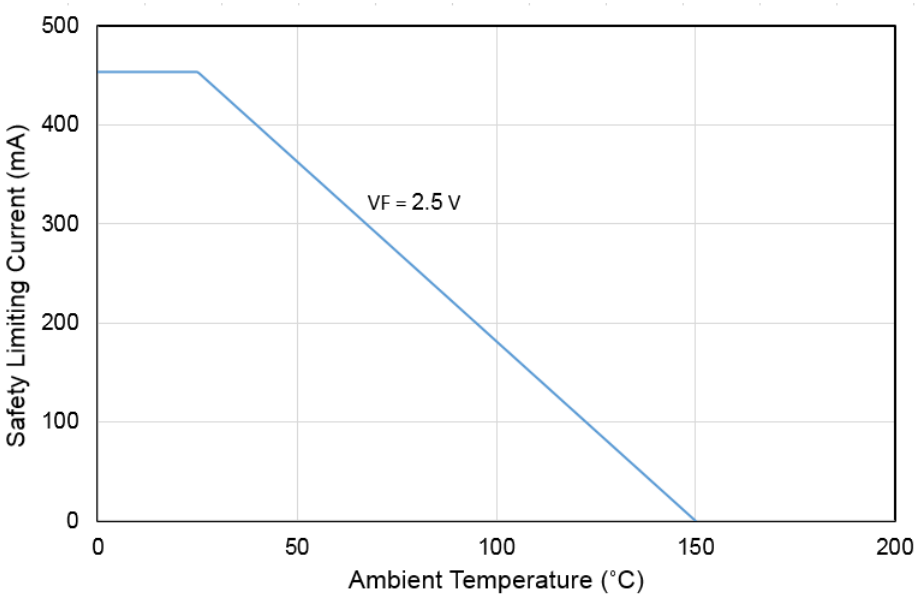

Figure 4.3. Thermal Derating Curve for Safety Limiting Current (Si8752)

Table 4.8. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_{STG}	–65	+150	°C
Operating Temperature	T_A	–40	+125	°C
Junction Temperature	T_J	—	+150	°C
Input-side supply voltage (Si8751)	VDD	–0.6	6.0	V
Voltage on any pin with respect to ground (Si8751)	V_{IO}	–0.5	VDD + 0.5	V
Average Forward Anode Current (Si8752)	$I_{F(AVG)}$	—	30	mA
Reverse Anode Voltage (Si8752)	V_R	—	0.3	V
Lead Solder Temperature (10 s)		—	260	°C
HBM Rating ESD		—	3.5	kV
CDM		—	2000	V
Maximum Isolation Voltage (Input to Output) (1 sec) SOIC-8		—	3000	V_{RMS}
Latch-up Immunity		—	400	kV/µs

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.

4.3 Typical Operating Characteristics

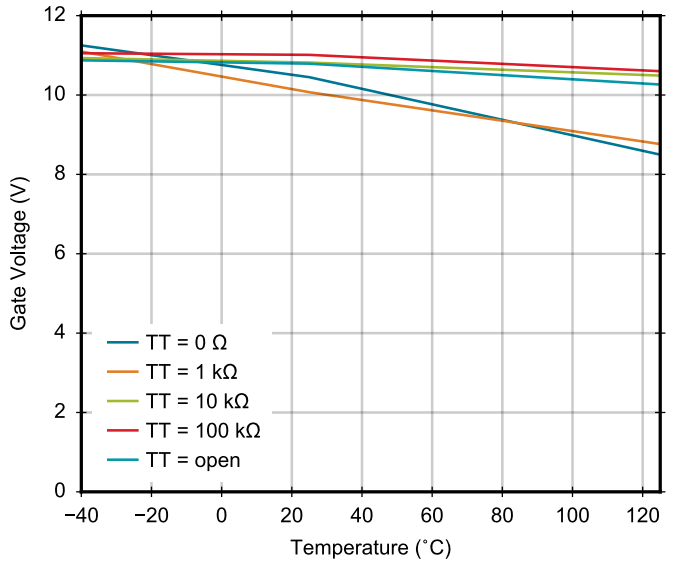

Figure 4.4. Si8751 Typical Gate Voltage vs. Temperature and TT

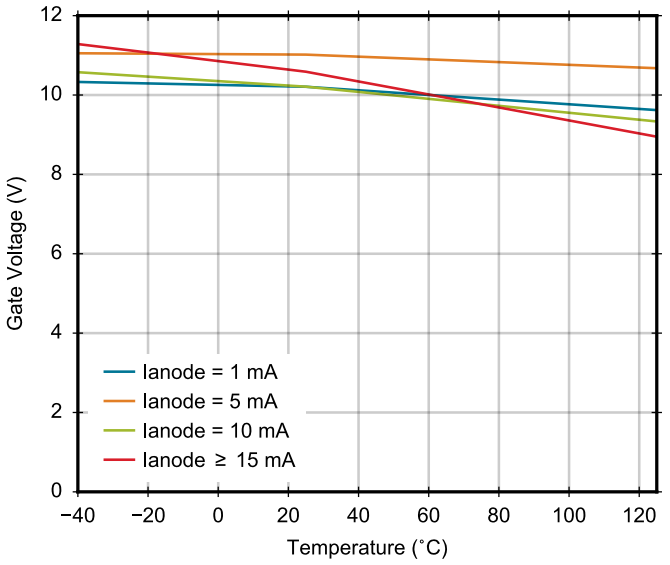

Figure 4.5. Si8752 Typical Gate Voltage vs. Temperature and Anode Current

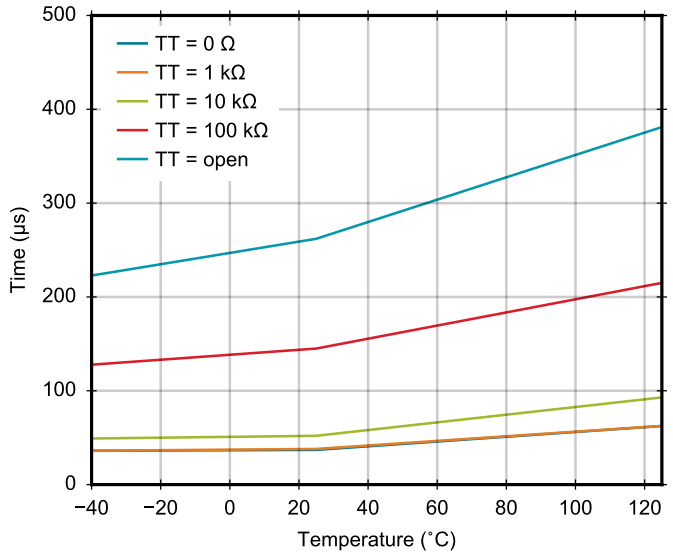

Figure 4.6. Si8751 Typical Turn-On Time vs. Temperature and TT with 100 pF Load (50% of Output)

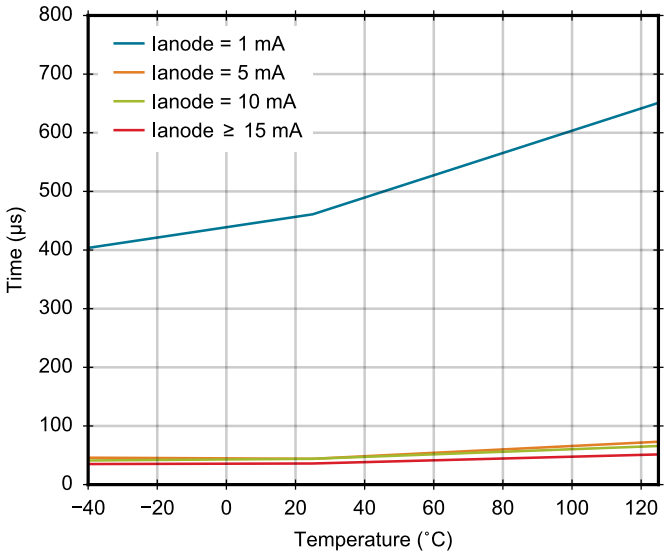

Figure 4.7. Si8752 Typical Turn-On Time vs. Temperature and Anode Current with 100 pF Load (50% of Output)

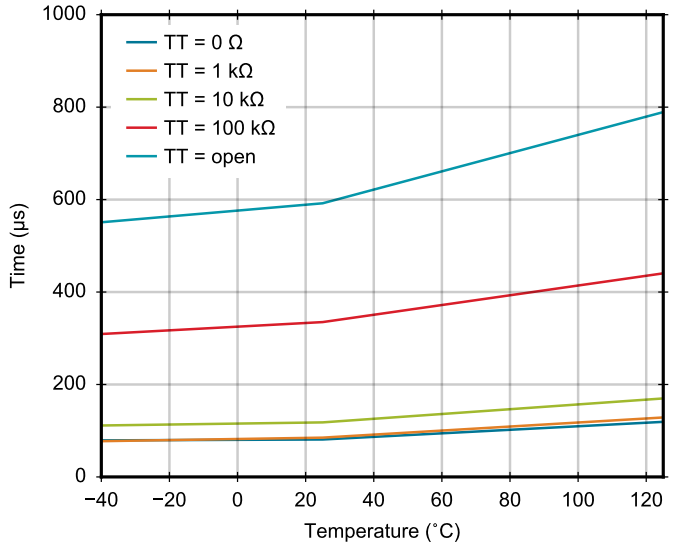

Figure 4.8. Si8751 Typical Turn-On Time vs. Temperature and TT with 100 pF Load (90% of Output)

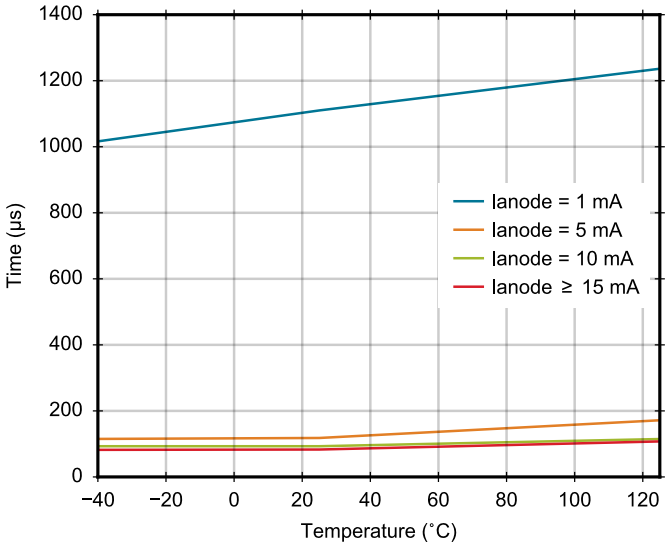

Figure 4.9. Si8752 Typical Turn-On Time vs. Temperature and Anode Current with 100 pF Load (90% of Output)

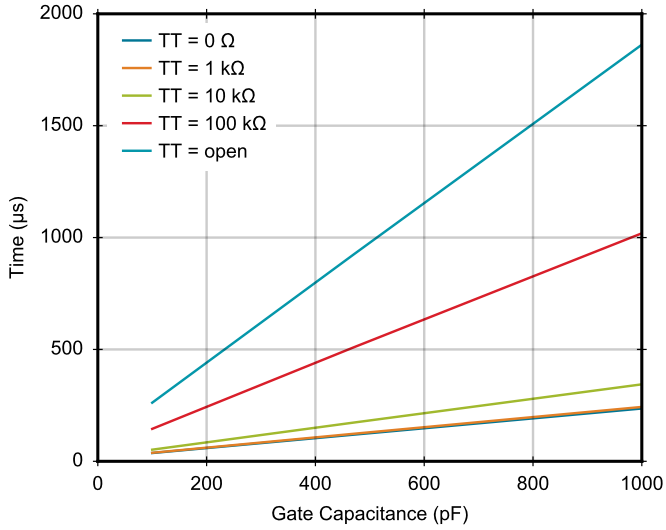

Figure 4.10. Si8751 Typical Turn-On Time vs. Capacitance and TT (50% of Output)

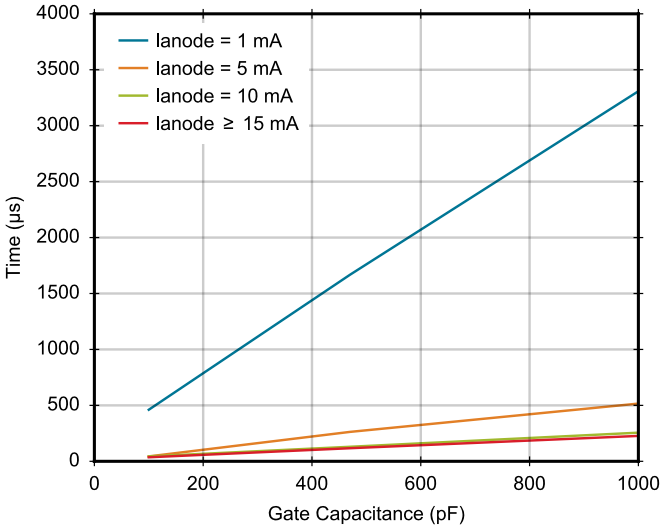

Figure 4.11. Si8752 Typical Turn-On Time vs. Capacitance and Anode Current (50% of Output)

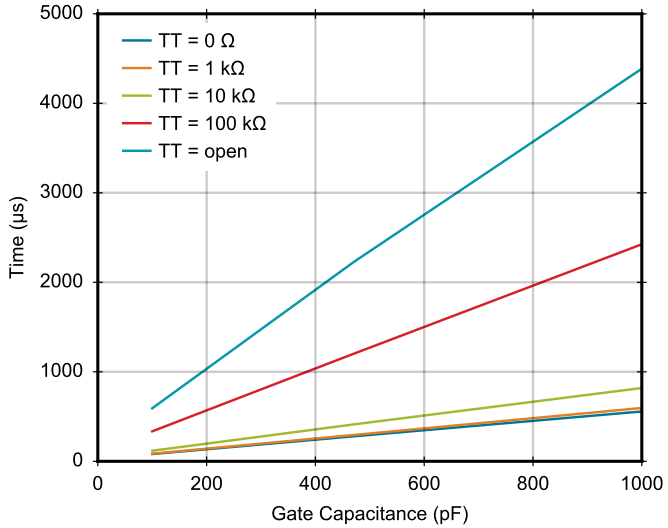

Figure 4.12. Si8751 Typical Turn-On Time vs. Capacitance and TT (90% of Output)

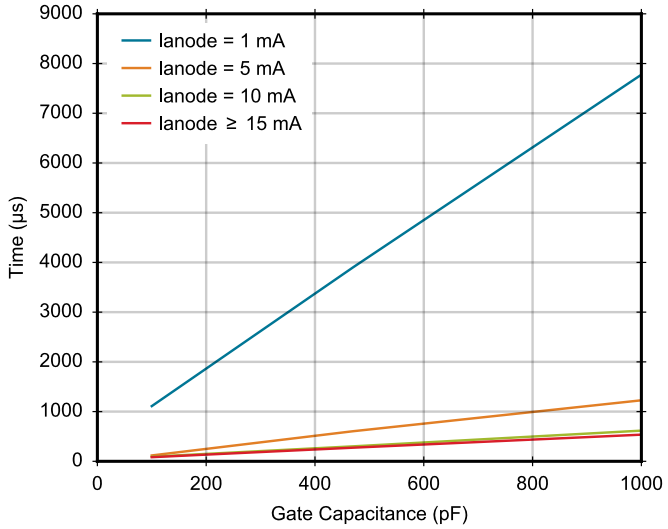

Figure 4.13. Si8752 Typical Turn-On Time vs. Capacitance and Anode Current (90% of Output)

5. Pin Descriptions

5.1 Si8751 Pin Descriptions

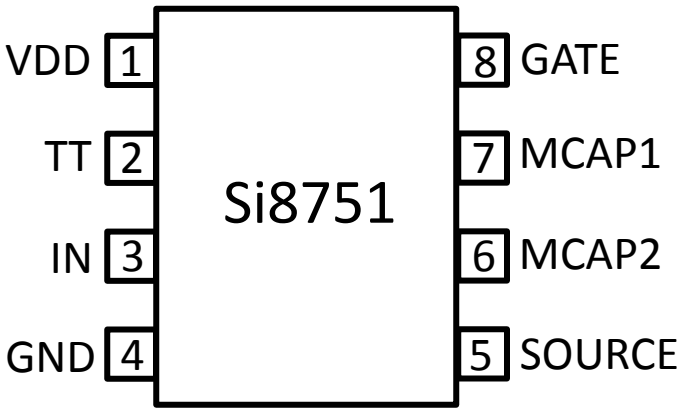

Figure 5.1. Pin Assignments Si8751

Table 5.1. Si8751 Pin Descriptions

Pin	Name	Description
1	VDD	Input side power supply
2	TT	Turn-on time control (optional)
3	IN	Digital control input
4	GND	Input side ground
5	SOURCE	Connection to switch FET Source
6	MCAP2	Miller capacitance control 2 (optional)
7	MCAP1	Miller capacitance control 1 (optional)
8	GATE	Connection to switch FET Gate

5.2 Si8752 Pin Descriptions

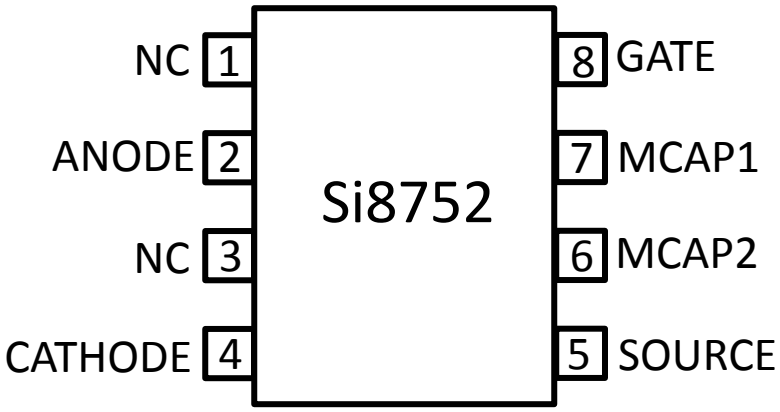

Figure 5.2. Pin Assignments Si8752

Table 5.2. Si8752 Pin Descriptions

Pin	Name	Description
1	NC	No Connect
2	ANODE	Anode of LED emulator
3	NC	No Connect
4	CATHODE	Cathode of LED emulator
5	SOURCE	Connection to switch FET Source
6	MCAP2	Miller capacitance control 2 (optional)
7	MCAP1	Miller capacitance control 1 (optional)
8	GATE	Connection to switch FET Gate

6. Package Outlines

6.1 Package Outline: 8-Pin Narrow Body SOIC

The figure below illustrates the package details for the Si875x in an 8-pin narrow-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

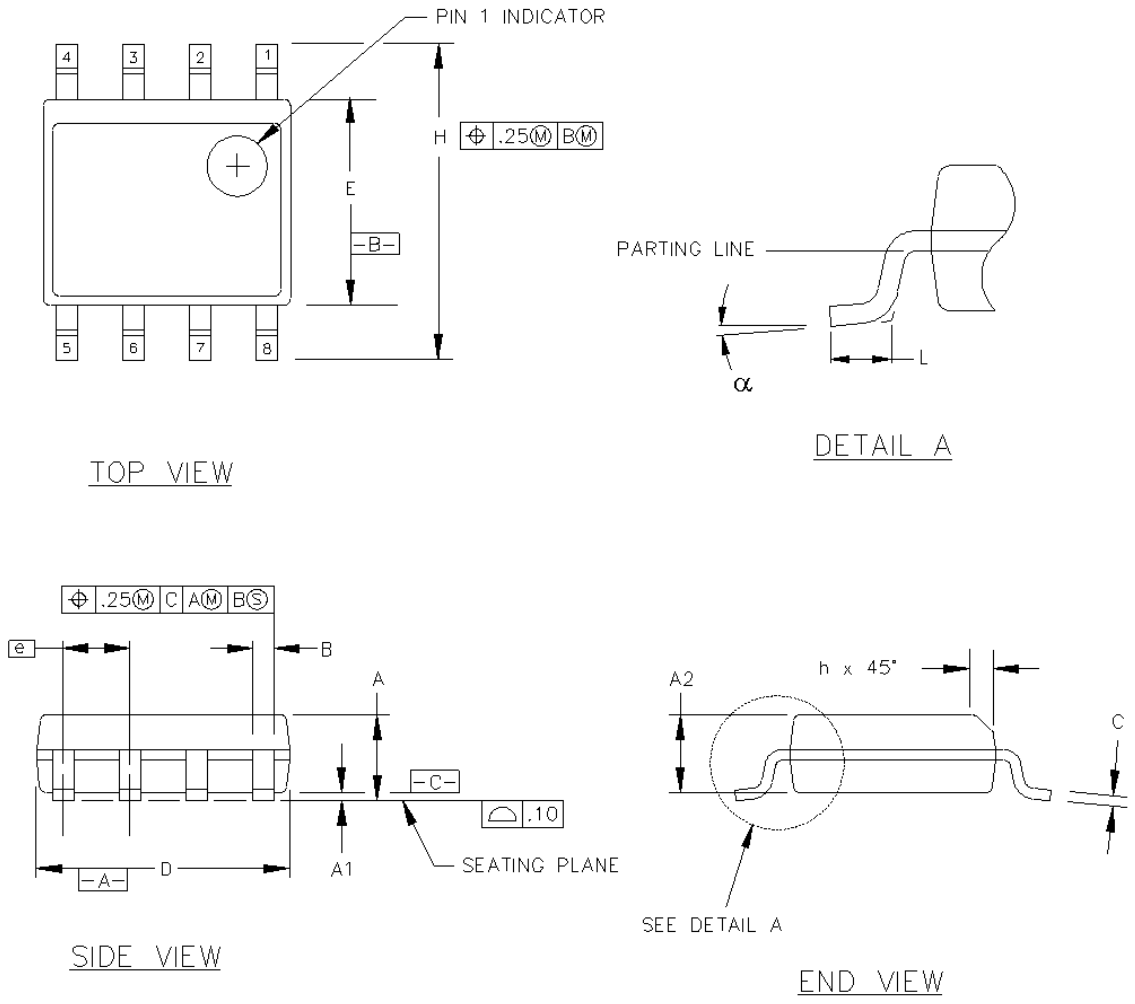

Figure 6.1. 8-Pin Narrow Body SOIC Package

Table 6.1. 8-Pin Narrow Body SOIC Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
	0°	8°

7. Land Patterns

7.1 Land Pattern: 8-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the Si875x in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

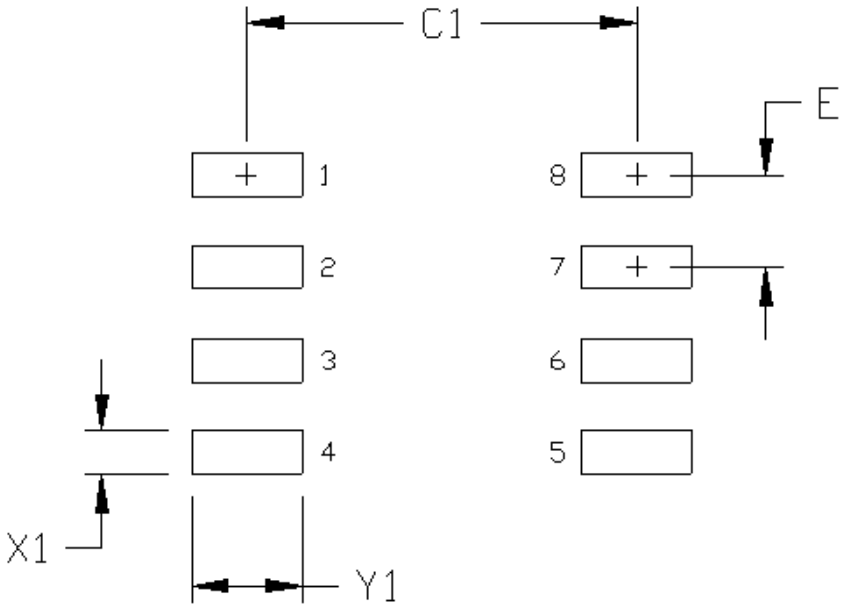

Figure 7.1. 8-Pin Narrow Body SOIC Land Pattern

Table 7.1. 8-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Top Markings

8.1 8-Pin Narrow Body SOIC

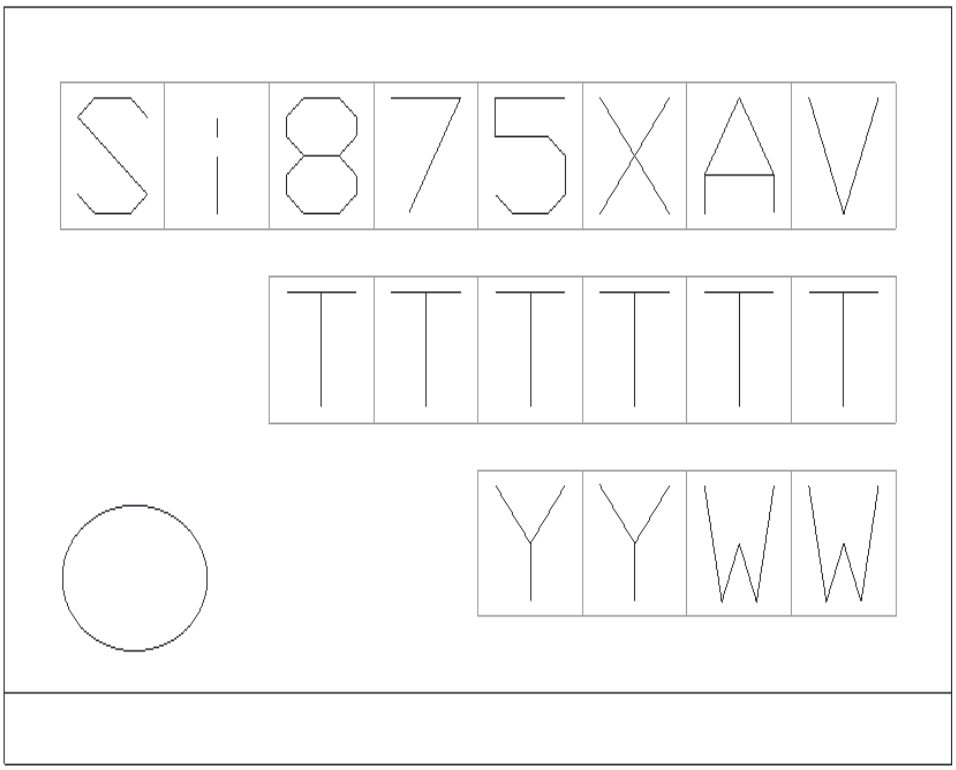

Table 8.1. Top Marking Explanation

Line 1 Marking:	Customer Part Number	Si875 = ISOdriver product series X: 1 = Digital input, 2 = LED emulator input A: Reserved V: B = 2.5 kV isolation rating
Line 2 Marking:	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	YY = Year WW = Work week	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.

9. Revision History

Revision 0.5, September 2016

- Significant edits with production electrical specifications.

Revision 0.1, May 2016

- Initial revision.

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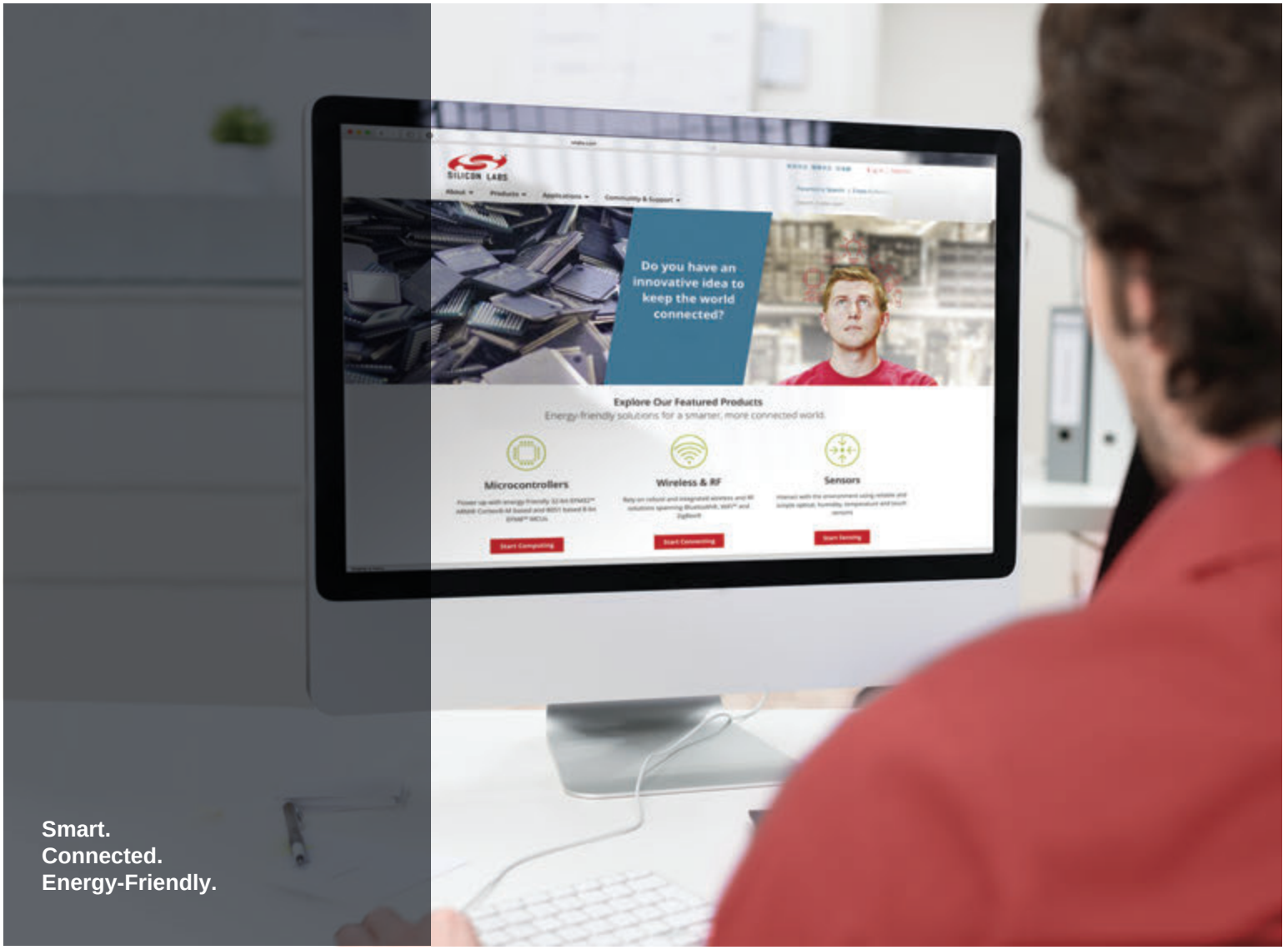

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