N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.0075 @ V_{GS} = 10 V	20
	0.0088 @ V_{GS} = 4.5 V	18.5

FEATURES

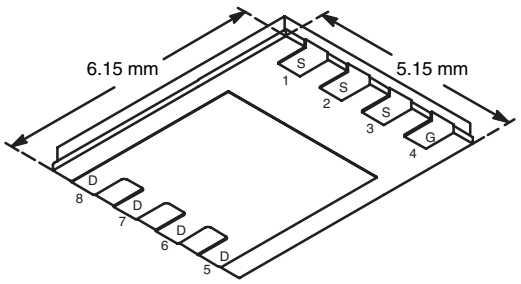
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100 % R_g Tested

Pb-free
RoHS COMPLIANT

APPLICATIONS

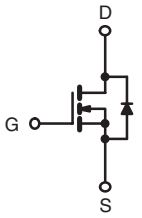
- Automotive Such As:
  - High-Side Switch
  - Motor Drives
  - 12-V Boardnet

PowerPAK SO-8



Bottom View

Ordering Information: Si7478DP-T1—E3 (Lead (Pb)-Free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	60		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	20	15	A
	T_A = 70°C		16	12	
Pulsed Drain Current		I_{DM}	60		
Continuous Source Current (Diode Conduction)[a]		I_S	4.5	1.6	
Avalanche Current		I_{AS}	35		
Avalanche Energy		E_{AS}	61		mJ
Maximum Power Dissipation[a]	T_A = 25°C	P_D	5.4	1.9	W
	T_A = 70°C		3.4	1.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C
Soldering Recommendations (Peak Temperature)[b, c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	18	23	°C/W
	Steady State		52	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.3	

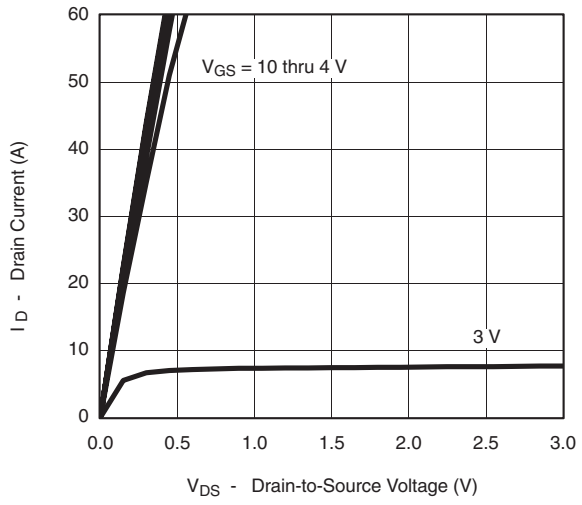
Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (*http://www.vishay.com/ppg?73257*). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 55°C			5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.006	0.0075	Ω
		V_{GS} = 4.5 V, I_D = 18.5 A		0.007	0.0088	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A		63		S
Diode Forward Voltage[a]	V_{SD}	I_S = 4.5 A, V_{GS} = 0 V		0.76	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 20 A		105	160	nC
Gate-Source Charge	Q_{gs}			22		
Gate-Drain Charge	Q_{gd}			19		
Gate Resistance	R_g		0.5	1.0	1.5	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		25	40	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			115	175	
Fall Time	t_f			45	70	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 4.5 A, di/dt = 100 A/µs		41	70	

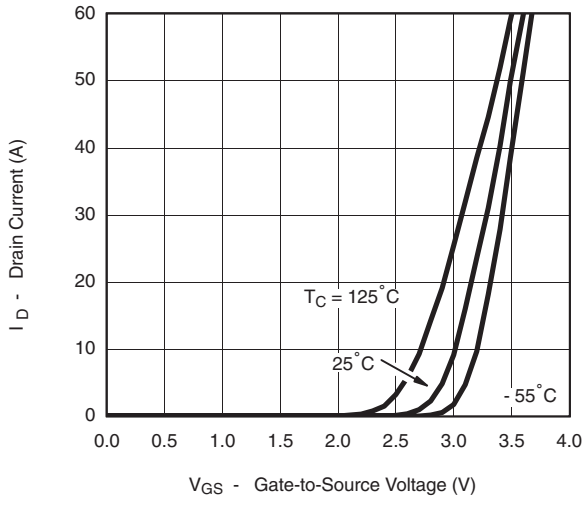
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless noted



Output Characteristics



Transfer Characteristics

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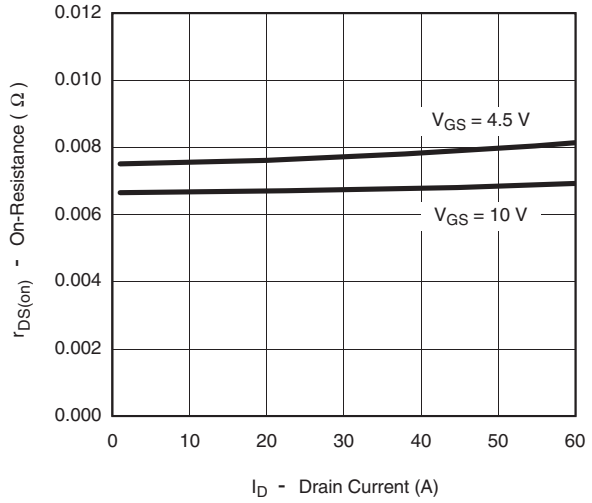
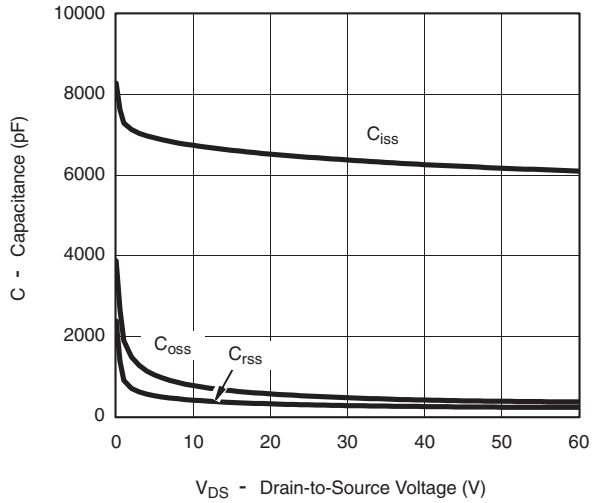
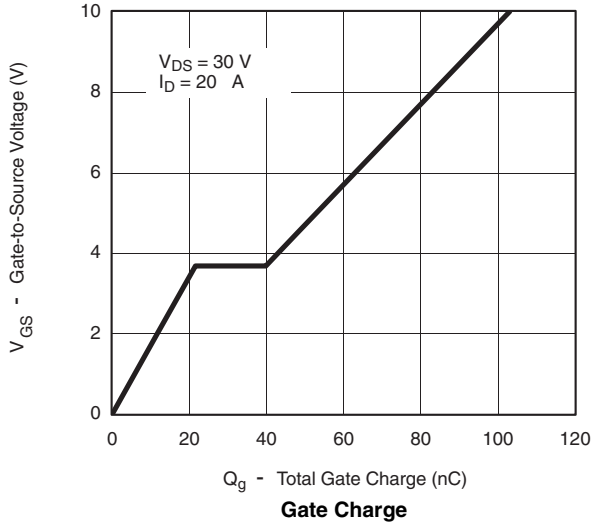


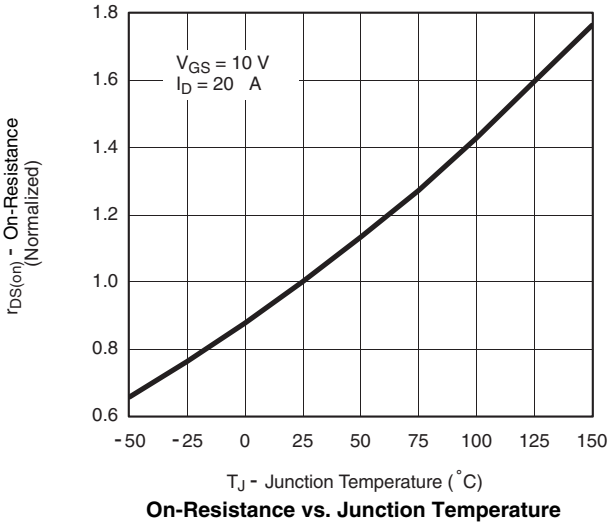
On-Resistance vs. Drain Current



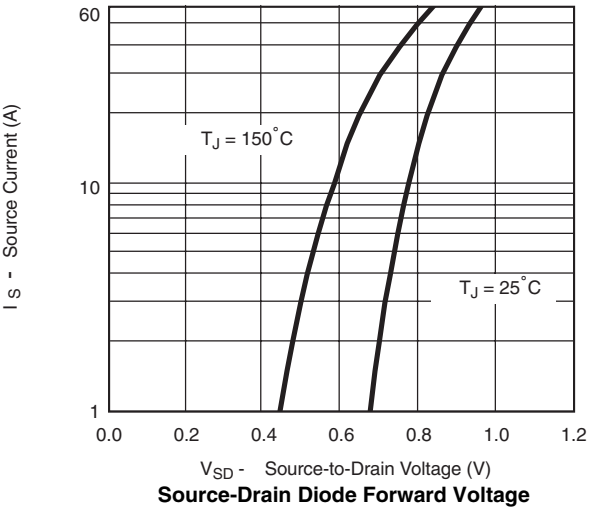
Capacitance



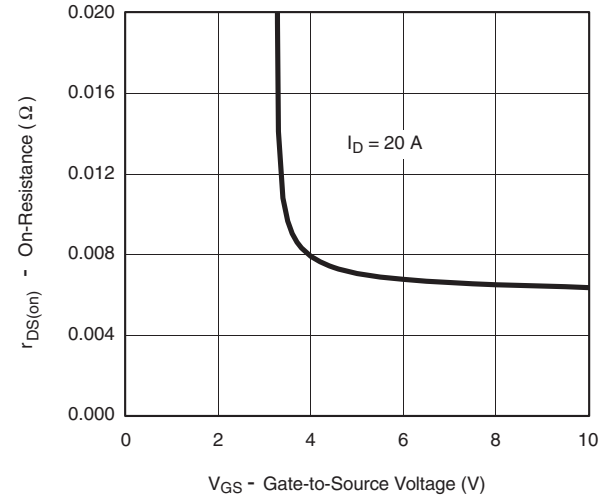
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

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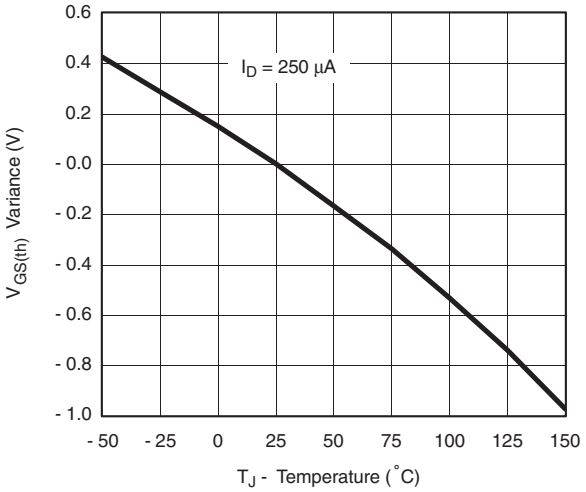
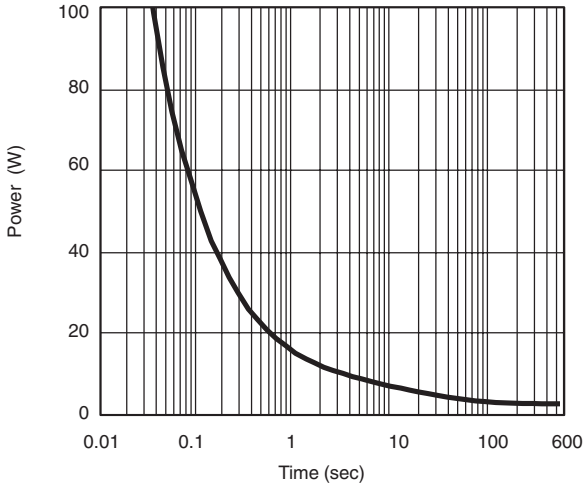
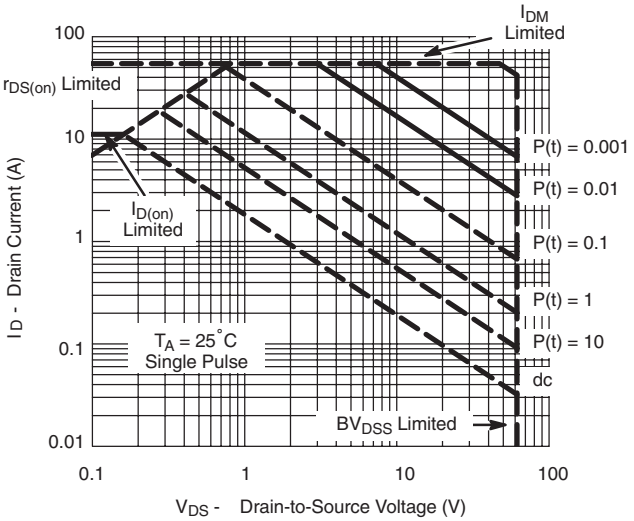


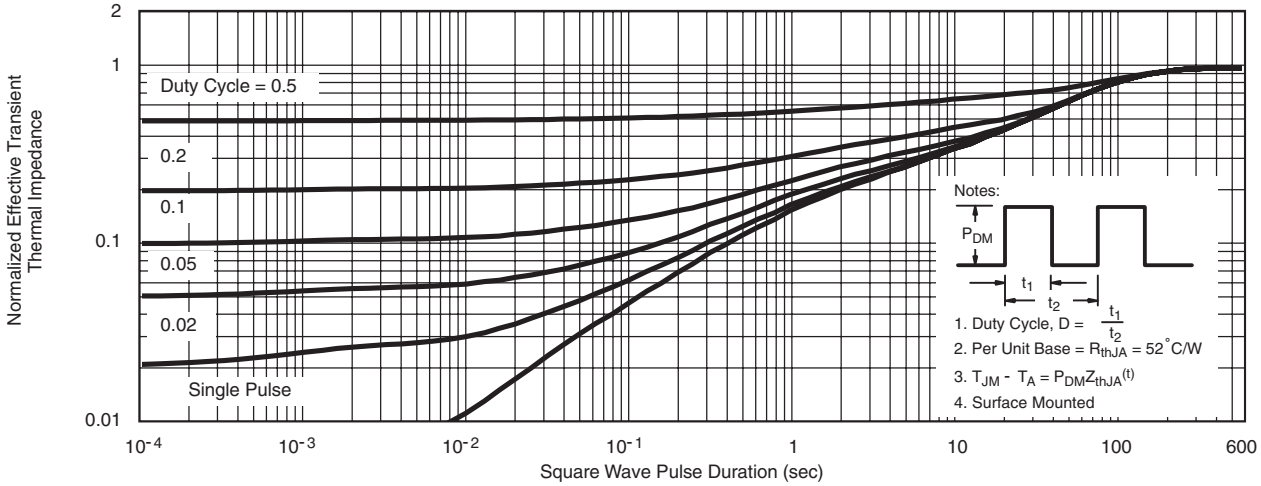
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

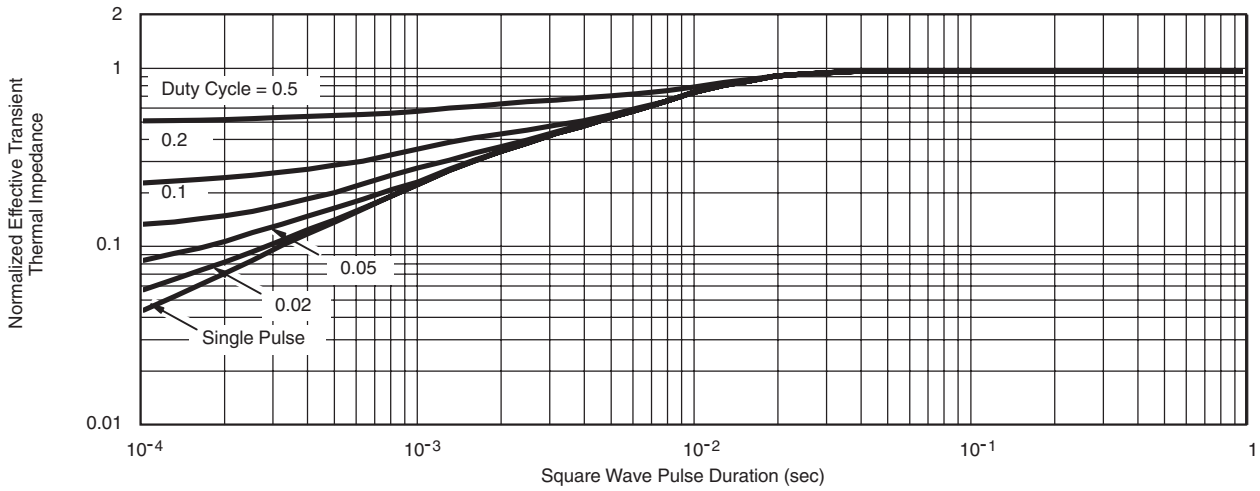


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72913.