Si4311

315/433.92 MHz FSK Receiver

Features

- Single chip receiver with only six external components
- Selectable 315/433.92 MHz carrier frequency
- Supports FSK modulation
- High sensitivity (–104 dBm @ 5 kbps)
- Excellent interference rejection
- Selectable IF bandwidths
- Automatic Frequency Centering (AFC)
- Data rates up to 10 kbps
- Direct battery operation with on-chip low drop out (LDO) voltage regulator
- 16 MHz crystal oscillator support
- 3x3x0.85 mm 20L QFN package (RoHS compliant)
- –40 to +85 °C temperature range

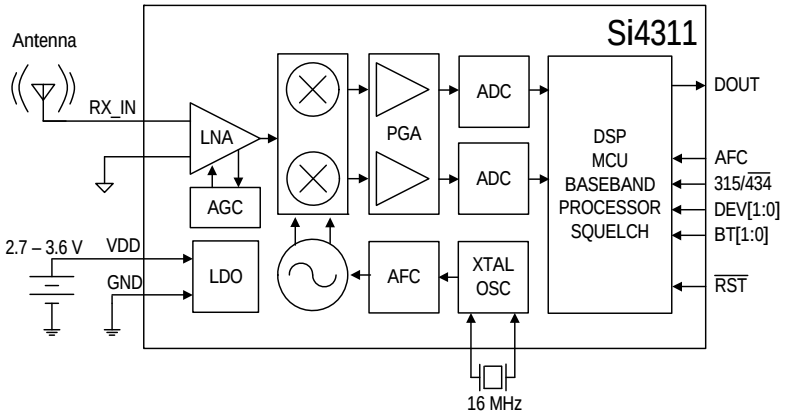
Applications

- Satellite set-top box receivers
- Remote controls, IR replacement/extension
- Garage and gate door openers
- Home automation and security
- Remote keyless entry
- After market alarms
- Telemetry
- Wireless point of sale
- Toys

Description

The Si4311 is a fully-integrated FSK CMOS RF receiver that operates in the unlicensed 315 and 433.92 MHz ultra high frequency (UHF) bands. It is designed for high-volume, cost-sensitive RF receiver applications, such as set-top box RF receivers, remote controls, garage door openers, home automation, security, remote keyless entry systems, wireless POS, and telemetry. The Si4311 offers industry-leading RF performance, high integration, flexibility, low BOM, small board area, and ease of design. No production alignment is necessary as all RF functions are integrated into the device.

Functional Block Diagram



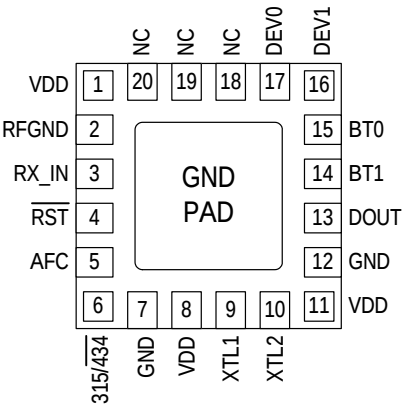


Ordering Information:

See page 14.

Pin Assignments

Si4311
(Top View)



Patents pending

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This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	3.3	3.6	V
Supply Voltage Powerup Rise Time	$V_{DD\text{-}RISE}$		10	—	—	µs
Ambient Temperature	T_A		–40	25	85	°C

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Operating Temperature	T_{OP}	–45 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{PK}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4311 device is a high-performance RF integrated circuit with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of this device should only be done at ESD-protected workstations.
3. For input pins 315/434, AFC, BT[1:0], and DEV[1:0].
4. At RF input pin RX_IN.

Table 3. DC Characteristics

(T_A = 25 °C, V_{DD} = 3.3 V, R_s = 50 Ω, F_{RF} = 433.92 MHz unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{VDD}		—	20	—	mA
Reset Supply Current	I_{RST}	Reset asserted	—	2	TBD	µA
High Level Input Voltage[1]	V_{IH}		0.7 x V_{DD}	—	V_{DD} + 0.3	V
Low Level Input Voltage[1]	V_{IL}		–0.3	—	0.3 x V_{DD}	V
High Level Input Current[1]	I_{IH}	V_{IN} = V_{DD} = 3.6 V	–10	—	10	µA
Low Level Input Current[1]	I_{IL}	V_{IN} = 0 V, V_{DD} = 3.6 V	–10	—	10	µA
High Level Output Voltage[2]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{DD}	—	—	V
Low Level Output Voltage[2]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{DD}	V

Notes:
1. For input pins 315/$\overline{434}$, AFC, BT[1:0], and DEV[1:0].
2. For output pin DOUT.

Table 4. Reset Timing Characteristics

(V_{DD} = 3.3 V, T_A = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width	t_{SRST}	100	—	—	µs

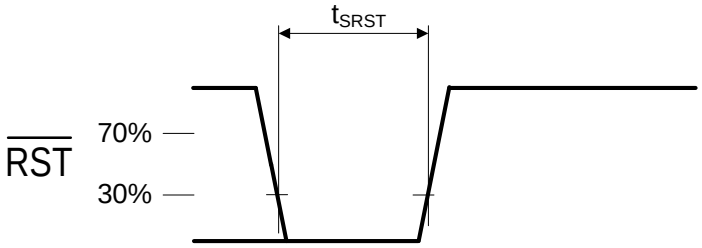


Figure 1. Reset Timing

Table 5. Si4311 Receiver Characteristics

(T_A = 25 °C, V_{DD} = 3.3 V, R_s = 50 Ω, F_{RF} = 433.92 MHz unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity @ BER = 10^{-3} (Note 1)		1.0 kbps, Δf = 50 kHz, xtal = ±20 ppm, 315 MHz (Note 2)	—	–104	—	dBm
		10 kbps, Δf = 50 kHz, xtal = ±20 ppm, 315 MHz (Note 2)	—	–101	—	dBm
		1.0 kbps, Δf = 50 kHz, xtal = ±20 ppm, 433.92 MHz (Note 2)	—	–102	—	dBm
		10 kbps, Δf = 50 kHz, xtal = ±20 ppm, 433.92 MHz	TBD	–100	—	dBm
Data Rate[3]			—	—	10	kbps
Adjacent Channel Rejection ±200 kHz[1]		Desired signal is 3 dB above sensitivity (BER = 10^{-3}), unmodulated interferer is at ±200 kHz, rejection measured as difference between desired signal and interferer level in dB when BER = 10^{-3}	TBD	35	—	dB
Alternate Channel Rejection ±400 kHz[1,2]		Desired signal is 3 dB above sensitivity (BER = 10^{-3}), unmodulated interferer is at ±400 kHz, rejection measured as difference between desired signal and interferer level in dB when BER = 10^{-3}	—	55	—	dB
Image Rejection, IF = 128 kHz[1,2]			—	35	—	dB
Blocking[1,2]		±2 MHz, 2.4 kbps, desired signal is 3 dB above sensitivity, CW interferer level is increased until BER = 10^{-3}	—	65	—	dB
		±10 MHz, 2.4 kbps, desired signal is 3 dB above sensitivity, CW interferer level is increased until BER = 10^{-3}	—	70	—	dB
Maximum RF Input Power [1,2]			—	8	—	dBm
Input IP3[3]		$\lvert f_2 - f_1 \rvert$ = 5 MHz, high gain mode, desired signal is 3 dB above sensitivity, CW interference levels are increased until BER = 10^{-3}	—	–10	—	dBm
FSK Deviation Input Range[3]			10	—	90	kHz
LNA Input Capacitance[3]			—	7	—	pF
RX Boot Time[3]		From reset	—	320	—	ms

Notes:

1. 1.0 kbps, Δf = 50 kHz, xtal = ±20 ppm, AFC = 0, BT[1:0] = 00, DEV[1:0] = 01.
2. Guaranteed by characterization.
3. Guaranteed by design.

Table 6. Crystal Characteristics
(V_{DD} = 3.3 V, T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Oscillator Frequency			—	16	—	MHz
Crystal ESR			—	—	100	Ω
XTL1, XTL2 Input Capacitance			—	11	—	pF

2. Typical Application Schematic

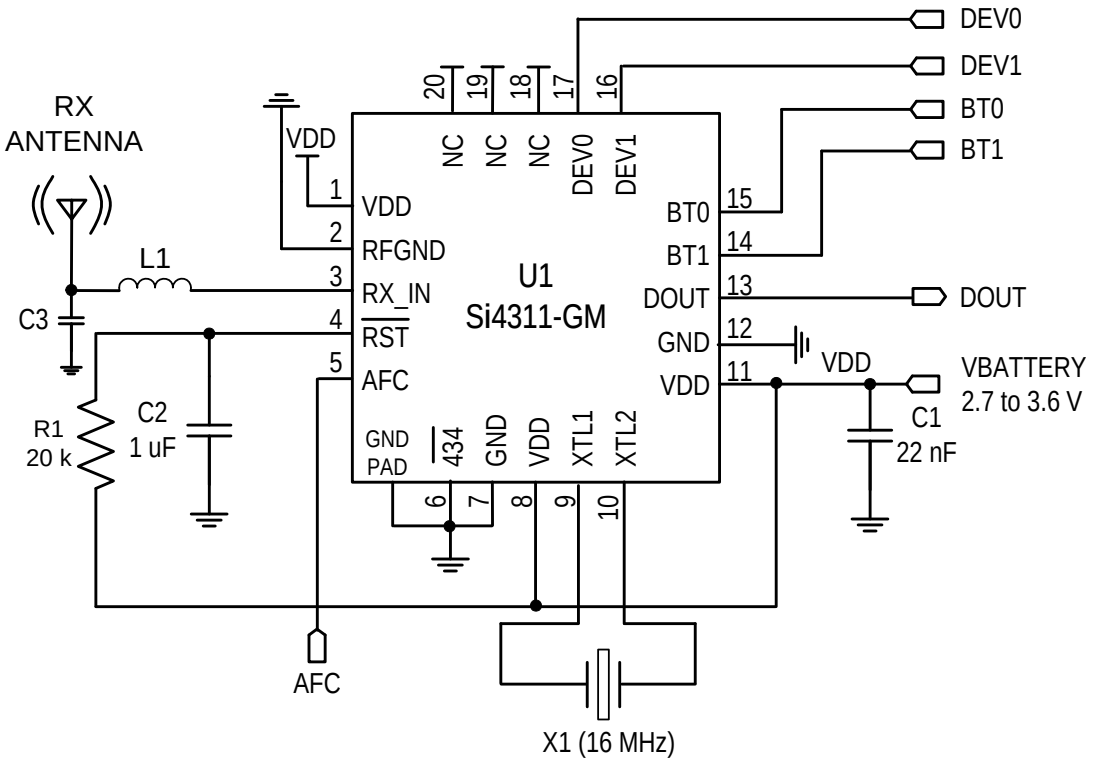


Figure 2. Si4311 FSK 433.92 MHz Application Schematic

2.1. Typical Application Bill of Materials

Table 7. Si4311 Typical Application Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2	Time constant capacitor, 1 µF	Murata
C3	Antenna matching capacitor, 15 pF	Murata
L1	Antenna matching inductor, 33 nH for 433.92 MHz and 62 nH for 315 MHz	Murata
R1	Time constant resistor, 20 kΩ	Murata
X1	16 MHz crystal	Hosonic
U1	Si4311 315/433.92 MHz FSK receiver	Silicon Laboratories

3. Functional Description

3.1. Overview

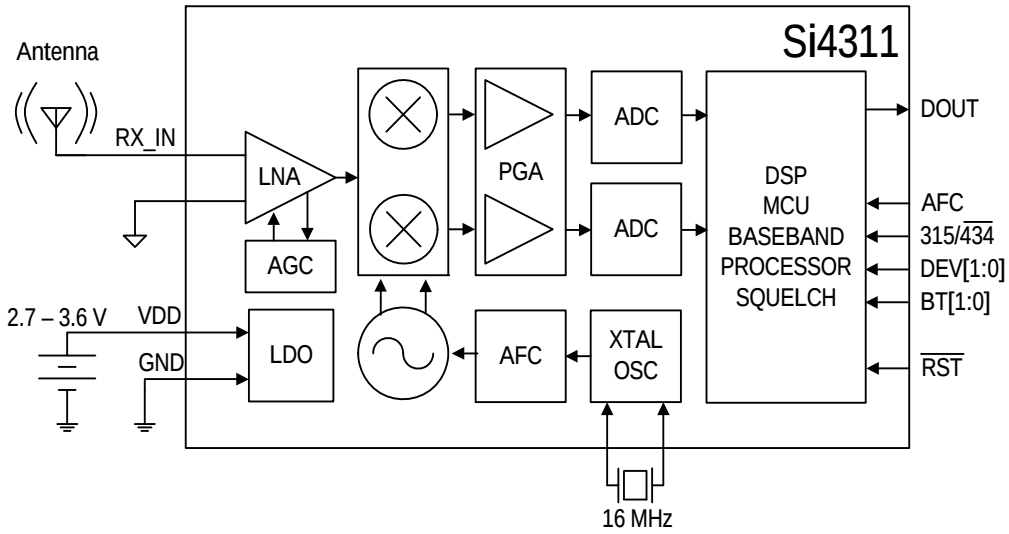


Figure 3. Functional Block Diagram

The Si4311 is a fully-integrated FSK CMOS RF receiver that operates in the unlicensed 315 and 433.92 MHz ultra high frequency (UHF) bands. It is designed for high-volume, cost-sensitive RF receiver applications. The chip operates at a carrier frequency of 315 or 433.92 MHz and supports FSK digital modulation with data rates of up to 10 kbps.

The device leverages Silicon Labs' patented and proven digital low-IF architecture and offers superior sensitivity and interference rejection. The Si4311 can achieve superior sensitivity in the presence of large interference due to its high dynamic range ADCs and digital filters. The digital low-IF architecture also enables superior blocking ability and low intermodulation distortion for robust reception in the presence of wide-band interference.

Digital integration reduces the number of required external components compared to traditional offerings, resulting in a solution that only requires a 16 MHz crystal and passive components allowing a small and compact printed circuit board (PCB) implementation area. The high integration of the Si4311 improves the system manufacturing reliability, improves quality, eases design-in, and minimizes costs.

3.2. Receiver Description

The RF input signal is amplified by a low-noise amplifier (LNA) and down-converts to a low intermediate frequency with a quadrature image-reject mixer. The mixer output is amplified by a programmable gain amplifier (PGA), filtered, and digitized with a high-resolution analog-to-digital converter (ADC). All RF functions are integrated into the device eliminating any production alignment issues associated with external components, such as SAW and ceramic IF filters.

Silicon Labs' advanced digital low-IF architecture achieves superior performance by using the DSP to perform channel filtering, demodulation, automatic gain control (AGC), automatic frequency control (AFC), and other baseband processing. DSP implementation of the channel filters provides better repeatability and control of the bandwidth and frequency response of the filter compared to analog implementations. No off-chip ceramic filters are needed with the Si4311 since all IF channel filtering is performed in the digital domain.

3.3. Carrier Frequency Selection

The Si4311 can be tuned to either 315 or 433.92 MHz by driving Pin 6 (315/$\overline{434}$) to VDD or GND. The 315 MHz operation is chosen by driving Pin 6 (315/$\overline{434}$) to VDD, and 433.92 MHz operation is chosen by driving Pin 6 (315/$\overline{434}$) to GND.

Table 8. Carrier Frequency Selection

Pin 6 (315/$\overline{434}$)	Frequency [MHz]
0	433.92
1	315

3.4. Bit Time BT[1:0] Selection

The Si4311 can operate with data rates of up to 10 kbps non-return to zero (NRZ) data or 5 kbps Manchester encoded data. However, FSK modulation uses other encoding schemes, such as pulse width modulation (PWM) and pulse position modulation (PPM) in which a bit can be encoded into a pulse with a certain duty cycle or pulse width (see Figure 4).

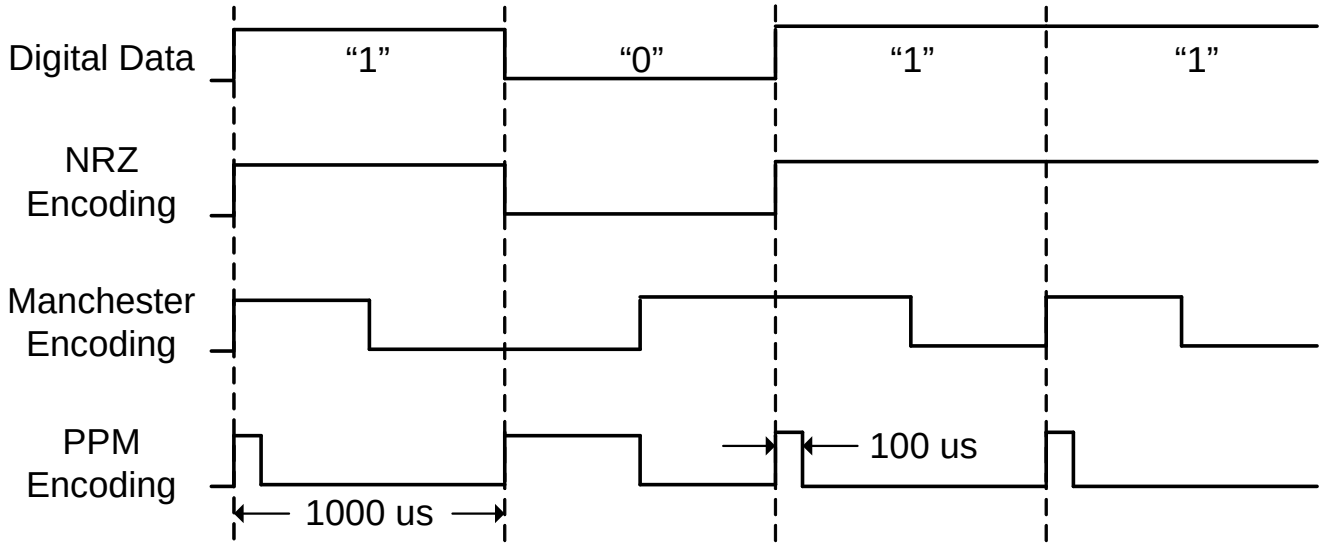


Figure 4. Example Data Waveforms

In order to set the data filter bandwidth correctly, the shortest pulse width of the transmitted encoded data should be chosen as the bit time. In the PPM example shown in Figure 4, the shortest pulse width is 100 µs, so the bit time is chosen as BT = 100 µs even though the actual data rate is 1 kbps (1000 µs). After finding BT, Table 9 can be used to find the bit settings for pins 14 and 15, BT[1:0]. In this PPM example, BT[1:0] is set as logic BT1 = 1 and BT0 = 1 or BT[1:0] = (1,1) since BT = 100 µs.

Table 9. How to Choose BT[1:0] Based on the Bit Time

Bit Time [us]	BT1 (pin 14)	BT0 (pin 15)
BT ≥ 1000	0	0
1000< BT ≤ 500	0	1
500 < BT ≤ 200	1	0
200 < BT ≤ 100	1	1

3.5. Frequency Deviation Selection

In order to accommodate wide frequency deviation ranges, the Si4311 FSK receiver uses two input pins, pins 16 and 17, to select a range of frequency deviations as shown in Table 10. For example, if the FSK signal has a frequency deviation (ΔF) of 50 kHz, then the DEV[1:0] = (0,1) or pin 16 = 0 and pin 17 = 1.

Table 10. Frequency Deviation Range Settings

DEV1 (pin 16)	DEV0 (pin 17)	Frequency Deviation [kHz]
0	0	1 < ΔF ≤ 30
0	1	30 < ΔF ≤ 50
1	0	50 < ΔF ≤ 70
1	1	70 < ΔF ≤ 90

3.6. Automatic Frequency Centering (AFC)

The channel bandwidth directly affects the sensitivity of any wireless receiver. Typical analog FSK receivers use an external ceramic filter with a large bandwidth to accommodate the data rate, frequency deviation, crystal tolerances, and transmit carrier frequency offsets, which leads to unnecessary amounts of noise and lower sensitivity levels. The Si4311 uses a narrow channel bandwidth of 200 kHz and automatic frequency centering (AFC) to obtain excellent sensitivity levels (–104 dBm at data rate of 5 kbps at 315 MHz) while still accommodating up to ±200 kHz of frequency tracking from its center frequency.

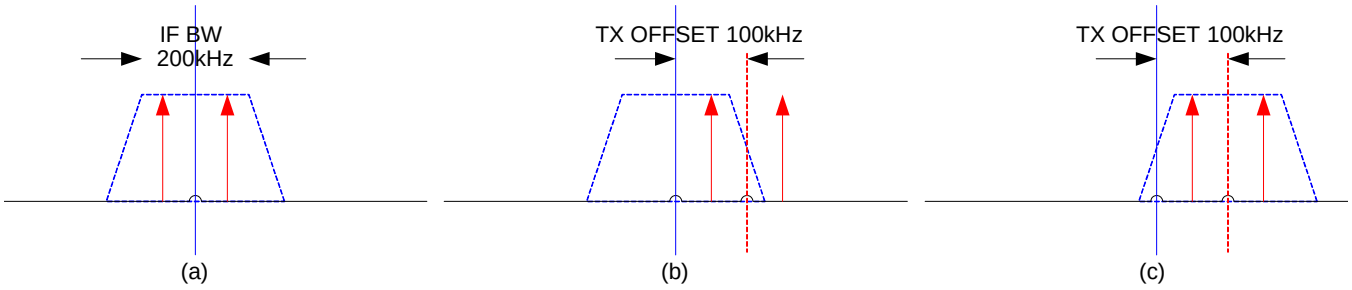


Figure 5. (a) Ideal case (b) Scenario with Tx Offset (c) Si4311 AFC Re-Centers IF BW

In the ideal case of no transmit carrier frequency errors or receiver frequency errors, both FSK tones for a logic "1" and "0" from the transmitter appear in the receiver IF channel bandwidth as shown in Figure 5 (a). However, if the transmitter has a large carrier offset such as shown in Figure 5 (b), then only one of the FSK tones falls in the receiver channel bandwidth and thus the receiver produces errors. The standard approach to resolving this problem is to use an IF channel filter that is large enough to accommodate the transmitter frequency error, but this leads to degraded sensitivity. The Si4311 uses AFC to re-center the channel bandwidth about the two FSK tones as shown in Figure 5 (c) to maintain excellent sensitivity with a small IF channel filter. The algorithm requires one FSK tone to be in-band and at most three alternating sequences of 0/1 data typically found in a preamble plus 700 µs of fixed delay time (approximately 230 µs per 0/1 data pair) to re-center the IF bandwidth. Worst case acquisition time is 1.3 ms for a data rate of 10 kbps.

The AFC algorithm includes a 200 ms hold time. The device holds the frequency found by the AFC algorithm for a time of 200 ms after no RF signal activity before restarting the frequency search. This allows a frequency found in the first packet of transmission to be held for any subsequent retransmissions of packets if the retransmissions occur before 200 ms. This hold frequency ensures all bits of the second and subsequent packets are recovered completely. The AFC frequency search resumes after 200 ms of no RF signal activity.

The AFC algorithm can be disabled by setting the logic level on pin 5 to a logic zero as shown in Table 11.

Table 11. AFC Selection Pin 5

Pin 5	AFC
0	Disable
1	Enable

3.7. Low Noise Amplifier Input Circuit

Figure 2 shows the typical application circuit with 50 Ω matching. Components C3 and L1 are used to transform the input impedance of the LNA. C3 is equal to 15 pF and L1 is equal to 33 nH at 433.92 MHz and 62 nH at 315 MHz for 50 Ω matching.

3.8. Crystal Oscillator

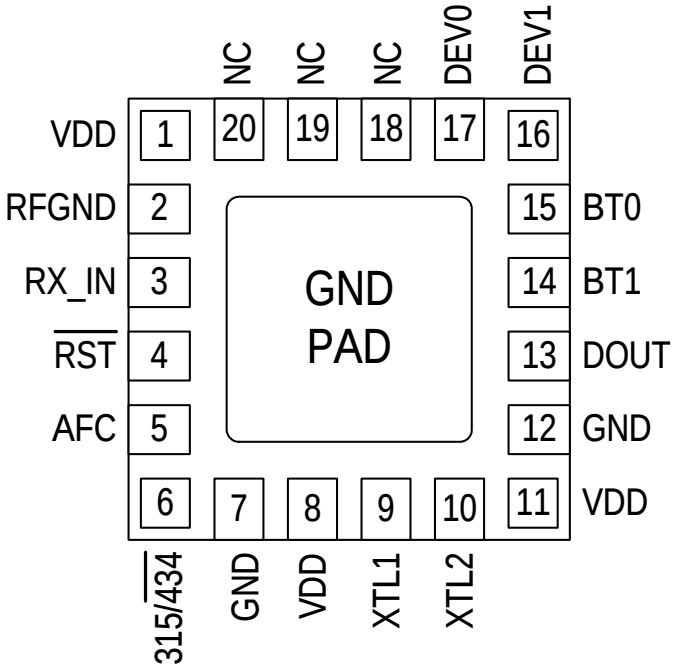
An on-board crystal oscillator is used to generate a 16 MHz reference clock for the Si4311. This reference frequency is required for proper operation of the Si4311 and is used for calibration of the on-chip VCO and other timing references. No external load capacitors are required to set the 16 MHz reference frequency if the recommended crystal load capacitor is around 14 pF, assuming the effective board capacitance between pins XTL1 and XTL2 is 3 pF and the chip input capacitance on pins XTL1 or XTL2 is 11 pF. Refer to Table 6, “Crystal Characteristics,” on page 7 for board capacitance and frequency tolerance information. The frequency tolerance of the crystal should be chosen such that the received signal is within the IF bandwidth of the Si4311 receiver.

Additionally, the Si4311 can be driven by an external 16 MHz reference clock. The clock signal can be applied to either the XTL1 or XTL2 inputs. When the 16 MHz reference clock is applied to one of the inputs, the other crystal input pin must be floating.

3.9. Reset Pin

Driving the $\overline{\text{RST}}$ pin (pin 4) low will disable the Si4311 and place the device into reset mode. All active blocks in the device are powered off in this mode, bringing the current consumption to <10 uA. The Si4311 is enabled by driving the $\overline{\text{RST}}$ pin (pin 4) to VDD. Refer to Table 4 "Reset Timing Characteristics" for the reset timing requirements. The chip requires about 320 ms to go from reset to active mode. The Si4311 can output invalid data during the 320 ms turn-on time.

4. Pin Descriptions: Si4311-B10-GM



Pin Number(s)	Name	Description
1, 8, 11	VDD	Supply voltage, may connect to external battery.
2	RFGND	RF ground. Connect to ground plane on PCB.
3	RX_IN	RF receiver input.
4	$\overline{\text{RST}}$	Device reset, active low input.
5	AFC	AFC selection input pin.
6	315/$\overline{434}$	Selectable logic input for 315 or 433.92 MHz operation.
7, 12, GND PAD	GND	Ground. Connect to ground plane on PCB.
9	XTL1	Crystal input.
10	XTL2	Crystal input.
13	DOUT	Data output.
14, 15	BT[1:0]	Bit time selection input pins.
16,17	DEV[1:0]	Frequency deviation input pins.
18,19,20	NC	No connect. Leave floating.

5. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4311-B10-GM	315/433.92 MHz FSK Receiver	QFN Pb-free	–40 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option.			

6. Package Markings (Top Marks)

6.1. Si4311 Top Mark

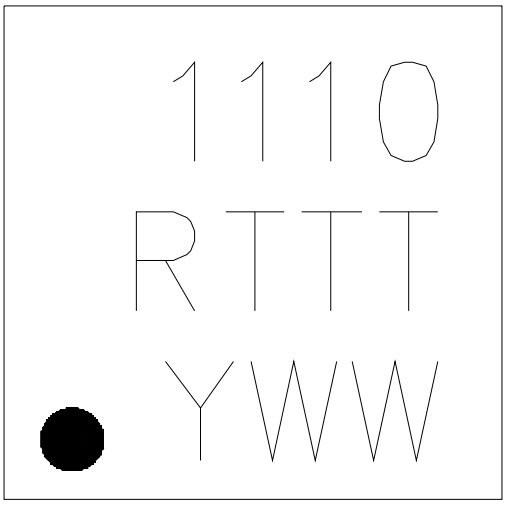


Figure 6. Si4311 Top Mark Example

6.2. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	11 = Si4311
	Firmware Revision	10 = Firmware Revision 1.0
Line 2 Marking:	Die Revision	B = Revision B Die
	TTT = Internal Code	Internal tracking code
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	YWW = Date Code	Assigned by the Assembly House. Corresponds to the last digit of the current year (Y) and the workweek (WW) of the mold date.

7. Package Outline: Si4311-B10-GM

Figure 7 illustrates the package details for the Si4311-B10-GM. Table 12 lists the values for the dimensions shown in the illustration.

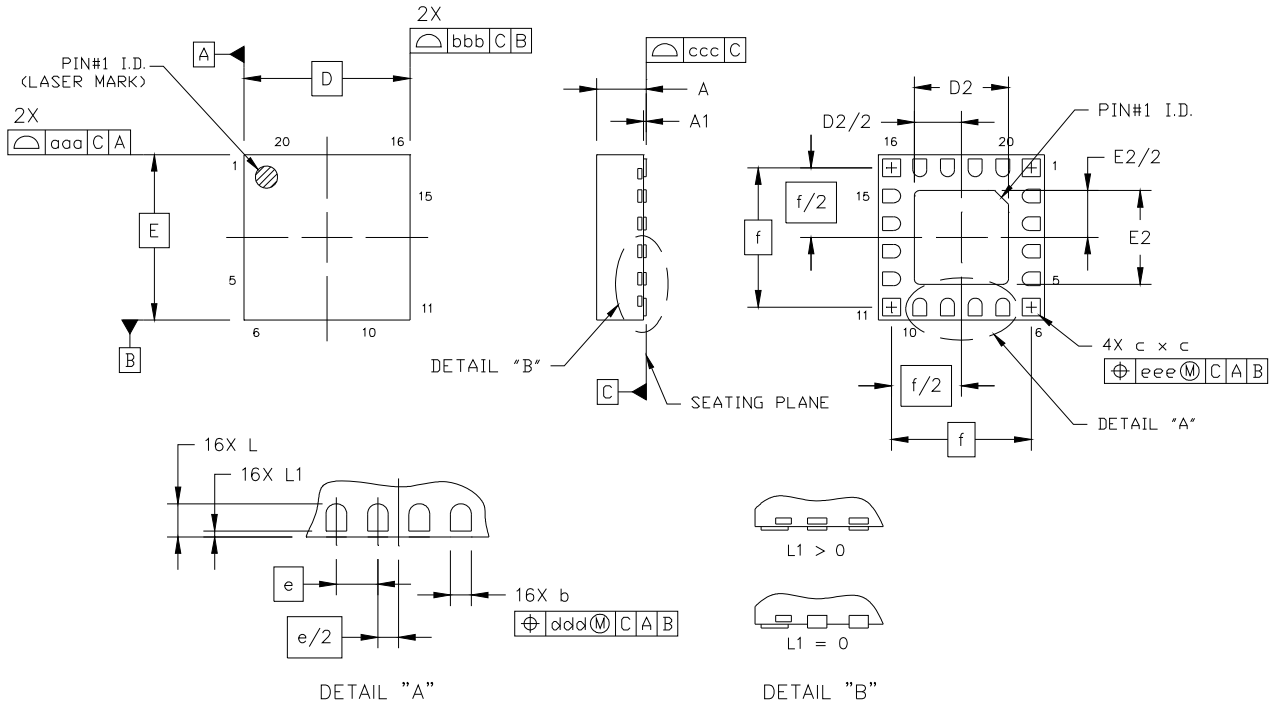


Figure 7. 20-Pin Quad Flat No-Lead (QFN)

Table 12. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D		3.00 BSC	
D2	1.65	1.70	1.75
e		0.50 BSC	
E		3.00 BSC	
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.30	0.35	0.40
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

8. PCB Land Pattern: Si4311-B10-GM

Figure 8 illustrates the PCB land pattern details for the Si4311-B10-GM. Table 13 lists the values for the dimensions shown in the illustration.

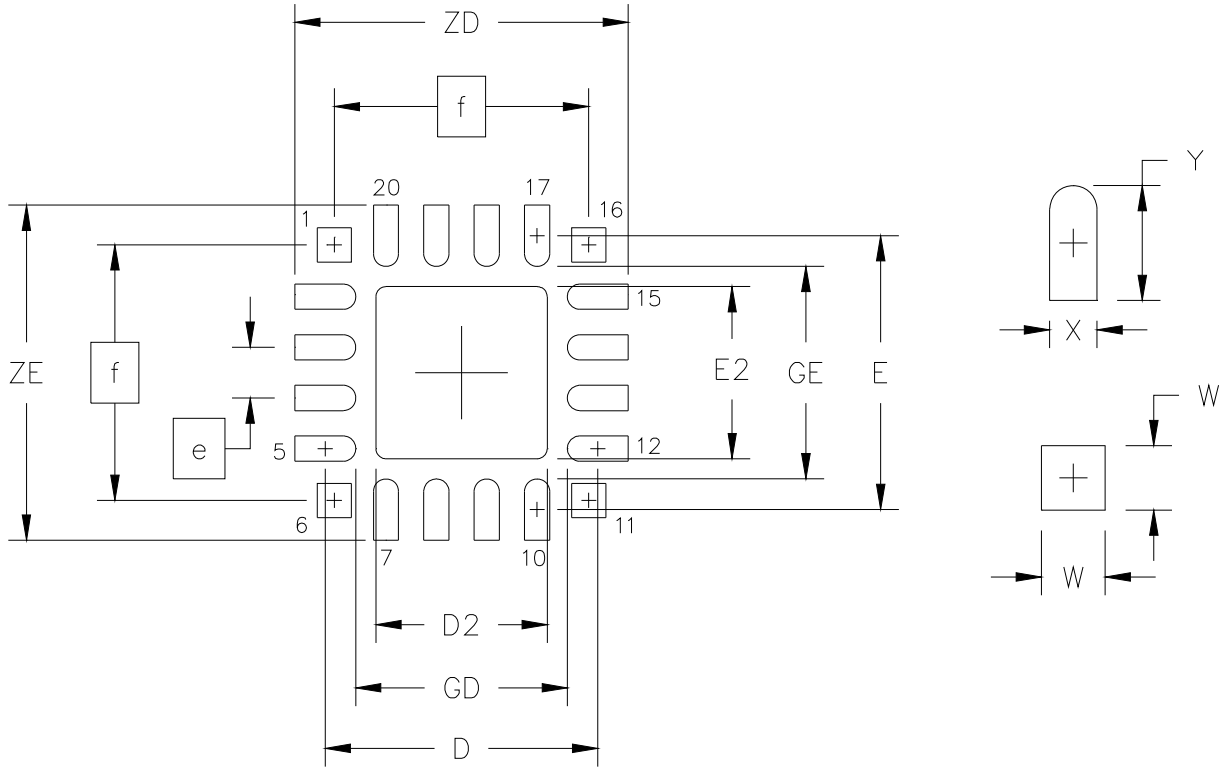


Figure 8. PCB Land Pattern

Table 13. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing is per the ANSI Y14.5M-1994 specification.
3. This land pattern design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder-mask-defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component standoff.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Maximum data rate changed from 10 to 4 kbps for FSK and from 5 to 2 kbps for OOK with Manchester encoding.
- Maximum RF input power changed from 5 to 10 dBm.
- Changed test conditions for sensitivity measurements and added the xtal frequency tolerance of 20 ppm.
- Updated text in section “3. Functional Description”.
- Added Ideal IF Bandwidth equation and description for choosing the IF bandwidth in Section “3.4. Bit Time BT[1:0] Selection”.
- Updated Table 11, “Typical Sensitivity @ 433 MHz, 2-FSK,” on page 11.
- Changed hysteresis level from 1 dB to 6 dB in Section “3.8. Crystal Oscillator”.
- Added text in section “3.8. Crystal Oscillator” regarding the crystal frequency tolerance and IF Bandwidth choice and sensitivity performance.

Revision 0.2 to Revision 0.3

- Updated features list
- Reduced font size in the test condition section of Table 5 "Si4311 Receiver Characteristics"
- Added crystal tolerance equation to Table 6 "Crystal Characteristics"
- Updated matching circuit and BOM to section “2. Test Circuit” and section “2. Typical Application Schematic”
- Modified text in Section “3. Functional Description”
- Changed bandwidth option in Table 11 "Bandwidth Selection Table Using BW[3:1] Pins" and test mode.
- Reset section updated to reflect active blocks are powered off in reset mode.

Revision 0.3 to Revision 0.4

- Removed crystal frequency tolerance range from Table 6 "Crystal Characteristics".
- Corrected data rates in Section “3.1. Overview”.
- Updated text in section “3.4. Bit Time BT[1:0] Selection” to show FSK receive IF bandwidth equations.
- Deleted voltage gain text in section “3.7. Low Noise Amplifier Input Circuit”.
- Removed squelch circuit description in section “3.8. Crystal Oscillator”.
- Included load capacitance requirement for crystal if no external capacitors are used in section “3.8. Crystal Oscillator”.
- Added reset to active time in section “3.9. Reset Pin”.
- Changed ordering guide part number in section “5. Ordering Guide”.
- Added FSK Automatic Frequency Calibration information
- Removed OOK feature.

Revision 0.4 to Revision 0.5

- Removed I_{VDD} current spec when input = –30 dBm from Table 3 "DC Characteristics"
- Updated sensitivity specs and test conditions in Table 5 "Si4311 Receiver Characteristics"
- Added AFC hold time description to section “3.6. Automatic Frequency Centering (AFC)”
- Added reference clock drive capability to section “3.8. Crystal Oscillator”

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