QUAD IEEE 802.3AT POE PSE CONTROLLER

Features

- Quad-Port Power Sourcing Equipment (PSE) controller
- IEEE 802.3at Type I and II compliant
- Port priority shutdown control
- Adds enhanced features for maximum design flexibility:
  - Per-port current and voltage monitoring
  - PoE Plus support with programmable current limits
  - Multi-point detection
  - Programmable power MOSFET gate drive control
  - Configurable watchdog timer enables failsafe operation
- Maskable interrupt pin
- Comprehensive fault protection circuitry includes:
  - Power undervoltage lockout
  - Output current limit and short-circuit protection
  - Thermal overload detection
- Supports pin-selectable AUTO mode
- Extended operating temp range: –40 to +85 °C
- 5x7 mm 38-pin QFN package (RoHS-compliant)
- On-chip dc-dc converter enables single-rail power operation



Ordering Information:

See page 49.

Applications

- IEEE Power Sourcing Equipment (PSE)
- Power over Ethernet (PoE) Switches
- IP Phone Systems
- Smartgrid Switches
- Ruggedized and Industrial Switches

Description

The Si3454 is a fully-programmable, four-port power management controller for IEEE 802.3 compliant Power Sourcing Equipment (PSE). Designed for use in PSE endpoint (switches), the Si3454 integrates four independent ports, each with IEEE-required powered device (PD) detection and classification functionality. In addition, the Si3454 features a fully-programmable architecture that enables powered device (PD) disconnect using a dc sense algorithm, a robust multipoint detection algorithm, software-configurable per-port current and voltage monitoring, and programmable current limits to support the IEEE 802.3at standard. Intelligent protection circuitry includes input undervoltage detection, output current limit, and short-circuit protection. The Si3454 operates by host processor control through a three-wire, I^2C-compatible serial interface. Independent serial data input and output pins enable high-voltage isolation through external isolators. An interrupt pin is used to alert the host processor of various status and fault conditions. The device also supports a pin-selectable AUTO mode for autonomous operation, without the need for a host processor. The Si3454 also features an on-chip dc-dc converter for creating the digital voltage rail from the PoE voltage, thus enabling single-rail power operation.

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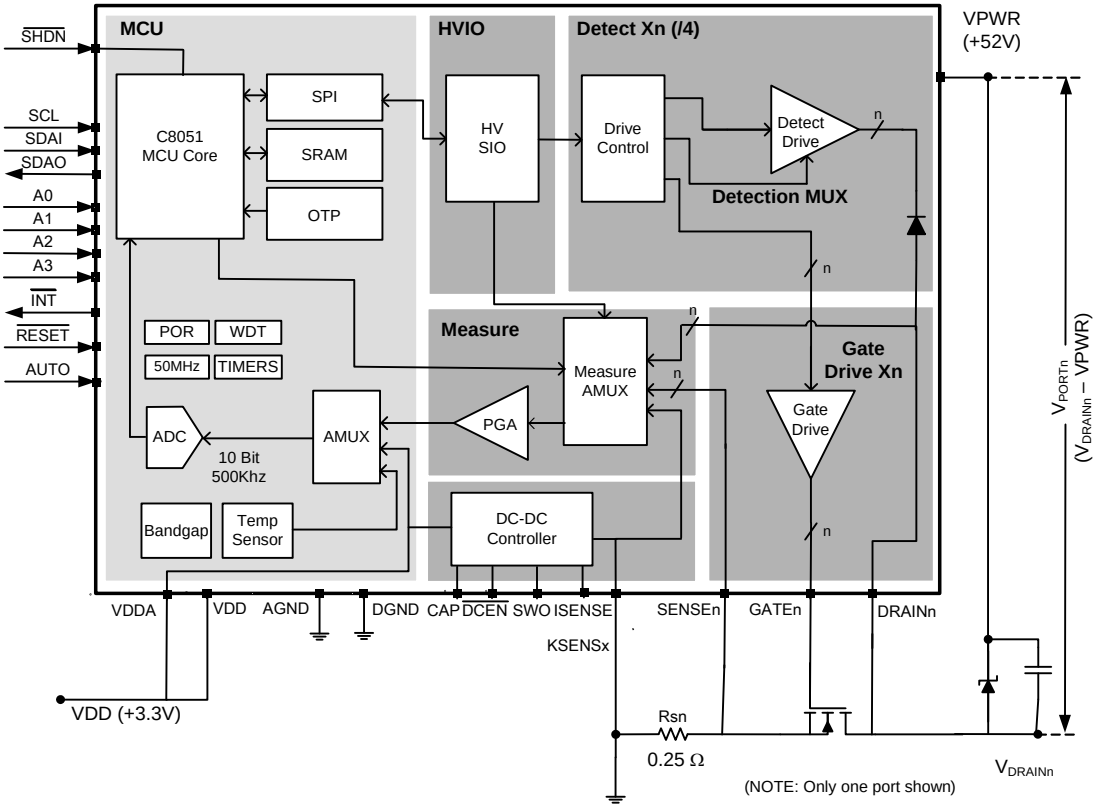
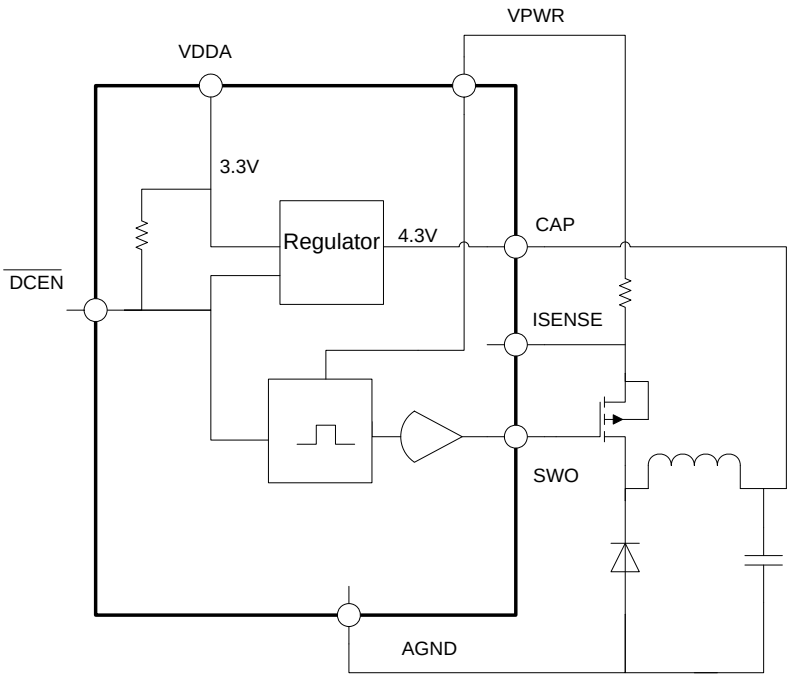
Functional Block Diagrams



DC-DC Converter Block Diagram



The case shown has both the DC-DC converter and series regulator enabled.
To enable ONLY the series regulator, tie SWO to VPWR. External components are unnecessary.

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1. Electrical Specifications

Table 1. PSE Port Interface Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Voltages						
VPWR Input Supply Voltage	V_{PWR}	When generating IEEE-compliant output voltage	44	48	57	V
VPWR UVLO Input Voltage (to turn on)[2]	V_{UVLO_ON}		—	32	—	V
VPWR UVLO Input Voltage (to turn off)[2]	V_{UVLO_OFF}		—	44	—	V
VDD Supply Voltage	V_{DD}		3.0	3.3	3.6	V
VDD UVLO Voltage[2]	V_{DD_UVLO}	VDD – AGND	—	2.8	—	V
Hardware Reset Voltage	V_{RESET}	VDD voltage causing an MCU reset	—	1.8	—	V

Notes:

1. Port voltages are referenced with respect to VPWR. All other voltages are referenced with respect to GND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 48 V.
2. For a description of the detailed behavior of VDD UVLO, see “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .
3. Positive values indicate currents flowing into the device; negative currents indicate current flowing out of the device.

Table 1. PSE Port Interface Recommended Operating Conditions[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Currents[3]						
VPWR Supply Current	I_{VPWR}	During normal operation	—	2	5	mA
VDD Supply Current	I_{DD}		—	18	25	mA
Detection Specification						
Detection Voltage when R_{DET} = 25.5kΩ	V_{PORTn}	Primary detection voltage	—	–4.0	–2.8	V
		Secondary detection voltage	–10	–8.0	—	V
Detection Current Limit	I_{DET}	Measured when V_{PORTn} = 0 V	—	3	4.9	mA
Minimum Signature Resistance @ PD	R_{DET_MIN}		15	—	19	kΩ
Maximum Signature Resistance @ PD	R_{DET_MAX}		26.5	—	33	kΩ
Shorted Port Threshold	R_{SHORT}		150	—	400	Ω
Open Port Threshold	R_{OPEN}		100	—	400	kΩ
Classification Specifications						
Classification Voltage	V_{CLASS}	0 mA < ICLASS < 45 mA	–20.5	—	–15.5	V
Classification Current	I_{CLASS}	Measured when V_{PORTn} = 0 V	55	—	95	mA
Classification Current Region	I_{CLASS_REGION}	Class 0	0	—	5	mA
		Class 1	8	—	13	mA
		Class 2	16	—	21	mA
		Class 3	25	—	31	mA
		Class 4	35	—	45	mA

Notes:

1. Port voltages are referenced with respect to VPWR. All other voltages are referenced with respect to GND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 48 V.
2. For a description of the detailed behavior of VDD UVLO, see “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .
3. Positive values indicate currents flowing into the device; negative currents indicate current flowing out of the device.

Table 1. PSE Port Interface Recommended Operating Conditions[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Classification Mark Specifications						
Mark Voltage	V_{MARK}	I_{PORT} = 0 mA	–10	—	—	V
		I_{PORT} = 5 mA	—	—	–7	V
Output Voltage Sense						
Threshold Voltage for Power Good Sense	V_{PGOOD}	Measured at V_{DRAINn} to AGND	1	—	3	V
Bias Current of DRAINn Pin	I_{DRAINn}	V_{DRAINn} = 0 V	—	–25	—	µA
Current Sense						
Sense resistor value	R_{SENSE}	1% tolerance	0.2475	0.25	0.2525	Ω
Sense Voltage at Current Limit	V_{ILIM}	V_{SENSEn}–$V_{KSENSEn}$ 1x Power Mode	100	106.25	112.5	mV
		V_{SENSEn}–$V_{KSENSEn}$ 2x Power Mode	200	212.5	225	mV
DC Disconnect Sense Voltage	V_{DC_MIN}	V_{SENSEn} – $V_{KSENSEn}$	1.25	1.875	2.5	mV
SENSEn Pin Bias Current	I_{SENSE}	V_{SENSEn} – AGND	—	–1	—	µA
MOSFET Gate Drive						
Drive Current from GATEn Pin (Active)		GATEn pin active V_{GATEn} = AGND 1x Power Mode	–60	–40	–20	µA
Drive Current from GATEn Pin (Off)		GATEn pin shut off V_{GATEn} = AGND + 5 V	—	50	—	mA
Voltage Difference Between any GATEn and AGND Pin		I_{GATEn} = –1 µA	10.5	12	13	V

Notes:

1. Port voltages are referenced with respect to VPWR. All other voltages are referenced with respect to GND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 48 V.
2. For a description of the detailed behavior of VDD UVLO, see “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .
3. Positive values indicate currents flowing into the device; negative currents indicate current flowing out of the device.

Table 1. PSE Port Interface Recommended Operating Conditions[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Measurement Accuracy						
Voltage Measurement	V_{PWR}	V_{PWR} = 50 V	47.5	—	52.5	V
Current Measurement	I (I_{PORT})	I_{PORT} = 7.5 mA	5	7.5	10	mA
		I_{PORT} = 350 mA	335	350	365	mA
		I_{PORT} = 700 mA	670	—	730	mA
Bad FET Measurement (Port Voltage at the Beginning of Detection that Causes a Bad FET Indication)	V_{PORTn}	Force port voltage	–20	–15	–10	V
	I_{PORTn}	Force current through sense resistor	0.5	2.0	4.0	mA

Notes:
1. Port voltages are referenced with respect to VPWR. All other voltages are referenced with respect to GND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 48 V.
2. For a description of the detailed behavior of VDD UVLO, see “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .
3. Positive values indicate currents flowing into the device; negative currents indicate current flowing out of the device.

Table 2. DC-DC Converter Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Regulator Input Voltage	V_{CAP}	—	3.6	4.3	4.6	V
DC-DC Switcher Output Current	I_{LOAD}	—	0.1	—	200	mA
Regulator Output Voltage	V_{DDA}	55 mA load	3.0	3.3	3.6	V
Regulator Output Current	I_{DDA}	—	0.1	—	55	mA

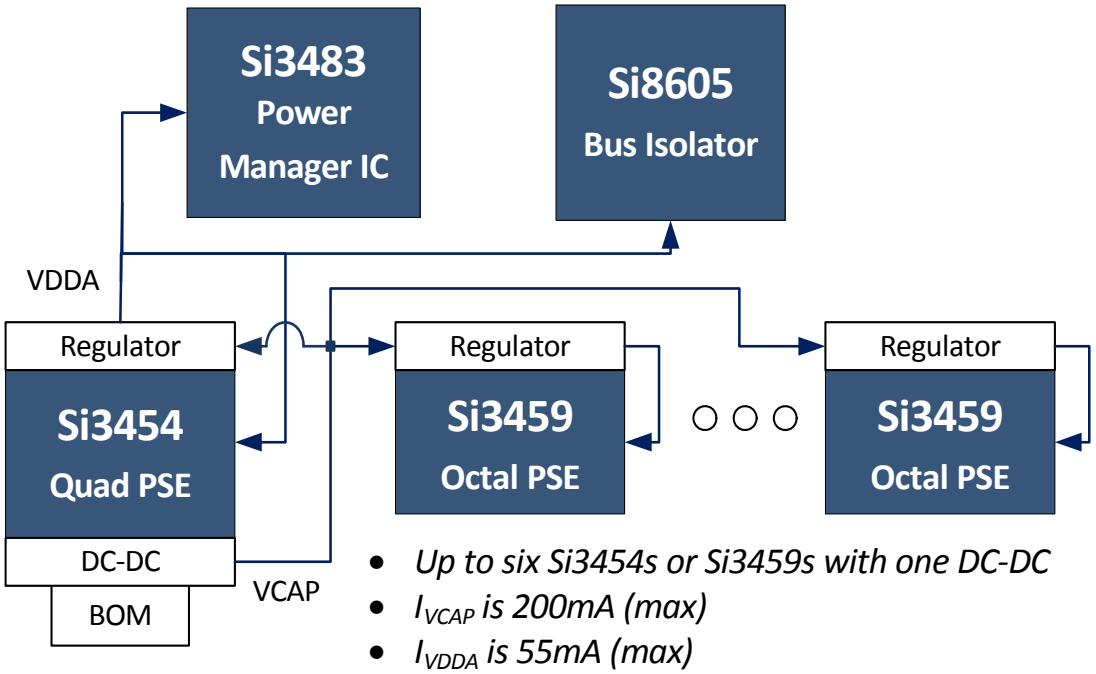


Figure 1. 55 mA and 200 mA Budget Loading Example

Table 3. Digital Pin Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Pins	Min	Typ	Max	Unit
Input low Voltage	V_{IL}		$\overline{\text{RESET}}$, SCL, SDAI, A4, A3, A2, A1	—	—	0.8	V
Input High Voltage	V_{IH}		$\overline{\text{RESET}}$, SCL, SDAI, A4, A3, A2, A1	2.0	—	—	V
Input Leakage	I_{IH}	V_{DD} = 4.2 V, Vpin = 4.2 V	$\overline{\text{RESET}}$, SCL, SDAI, A3, AIN, $\overline{\text{INT}}$, $\overline{\text{DCEN}}$	—	—	6	µA
			$\overline{\text{SHDN}}$	—	—	10	µA
	I_{IL}	V_{DD} = 4.2 V, Vpin = 0 V	$\overline{\text{SHDN}}$	—	85	—	µA
	I_{IL}	V_{DD} = 3.3 V, Vpin = 0 V	$\overline{\text{RESET}}$, SCL, SDAI, A4, A3, A2, A1, $\overline{\text{INT}}$, $\overline{\text{DCEN}}$	—	15	50	µA
Output Low Voltage[2]	V_{OL}	I_{SDAO} = 8 mA, $I_{\overline{INT}}$ = 8 mA I_{AOUT} = 8 mA		—	—	0.6	V

Notes:
1. All specification voltages are referenced with respect to DGND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise.
2. SDAO and $\overline{\text{INT}}$ are open drain outputs. Tie each pin to V_{DD} with a 1 kΩ resistor for normal operation.

Table 4. AC Timing Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Detection Delay Cycle	t_{DET_CYCLE}	Time from detect command or when PD is connected to port to when detection process is completed.* See Figure 6.	70	—	400	ms
Detection Time	t_{DETECT}	Time required to measure PD signature resistance.* See Figure 6.	—	70	—	ms
Classification Delay Cycle	t_{CLASS_CYCLE}	Time from successful detect in Semi-AUTO mode to classification complete.* See Figure 6.	10	—	30	ms
		Time from classify command in manual mode to class complete.* See Figure 6.	10	—	30	ms
Classification Time	t_{CLASS}	See Figure 6*	10	—	20	ms
Inrush Time	t_{INRUSH}		—	60	—	ms
Overload Time Limit	t_{CUT}		—	60	70	ms
Disconnect Delay	t_{CMPS}		—	360	—	ms
Timer Duration	t_{LIM}	1.71 ms times the value of TLIM12 (TLIM34) field rounded to nearest integer.	0	—	26	ms
DC Disconnect Minimum Pulse Width Sensitivity	t_{DC_SEN}	V_{DRAINn} = –48 V, V_{SENSEn} – AGND > 5 mV	—	—	3	ms
$\overline{\text{SHDN}}$ Pin Assertion Threshold (Time from $\overline{\text{SHDN}}$ falling edge to port turn off)	T_{SHDN}	Shutdown Priority Mode	1	—	50	µs

***Note:** This timing is determined by the MCU, and the clock reference is guaranteed to be 1 ms ±5%.

Table 5. I²C Bus Timing Specifications[1,2,3,4,5,6]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial Bus Clock Frequency	f_{SCL}	See Figure 5	0	—	800	kHz
SCL High Time	t_{SKH}	See Figure 5	300	—	—	ns
SCL Low Time	t_{SKL}	See Figure 5	650	—	—	ns
Bus Free Time	t_{BUF}	Between STOP and START conditions. See Figure 5	650	—	—	ns
Start Hold Time	t_{STH}	Between START and first low SCL. See Figure 5	300	—	—	ns
Start Setup Time	t_{STS}	Between SCL high and START condition. See Figure 5	300	—	—	ns
Stop Setup Time	t_{SPS}	Between SCL high and STOP condition. See Figure 5	300	—	—	ns
Data Hold Time	t_{DH}	See Figure 5[7]	75	—	—	ns
Data Setup Time	t_{DS}	See Figure 5	100	—	—	ns
Time from Hardware or Software Reset until Start of I²C Traffic	t_{RESET}	Reset to start condition	5	—	—	ms

Notes:

1. All specification voltages are referenced with respect to AGND and DGND at ground. Currents are defined as positive flowing into a pin and negative flowing out of a pin.
2. Not production tested (guaranteed by design).
3. All timing references measured at VIL and VIH.
4. SDAI must be low within ½ SCL clock cycle of SDAO going low for the following reasons:
   a.) During a read transaction, if the Si3454 is letting SDAO go high and another device is driving SDAO low, this should be recognized as bus contention, and the Si3454 should release the bus. If SDAO low is not present on SDAI within ½ clock cycle, the Si3454 will not recognize this as bus contention and will not release the bus.
   b.) During any I²C transaction, the Si3454 will ACK (SDAO low) when its address is sent. The Si3454 “expects” that SDAI will follow within ½ of the SCL clock cycle. If SDAI is not low, the Si3454 will release the bus.
5. SCL and SDA rise and fall times depend on bus pullup resistance and bus capacitance.
6. The time from a fault event to the INT pin being driven is software-defined. The Si3454 produces a new measurement result for the Port voltage or current every 3 msec and every 6 msec for the power supplies and temperature. After each port is monitored, the port status, port event registers, INT register, and INT pin are updated in sequence. For this reason, the INT pin can lag the contents of the event registers by approximately 5 ms.
7. 250 ns minimum and 350 ns maximum for the case where the Si3454 is transmitting data.

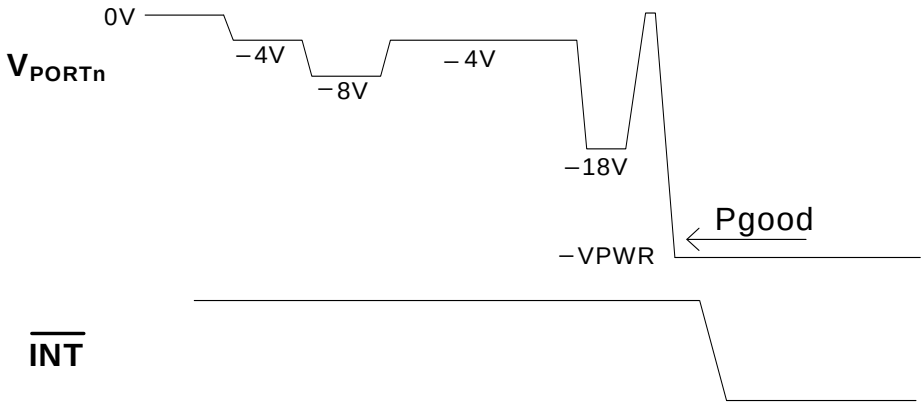


Figure 2. Semi-Auto Timing for Detect, Classification, and Power-Up Sequence

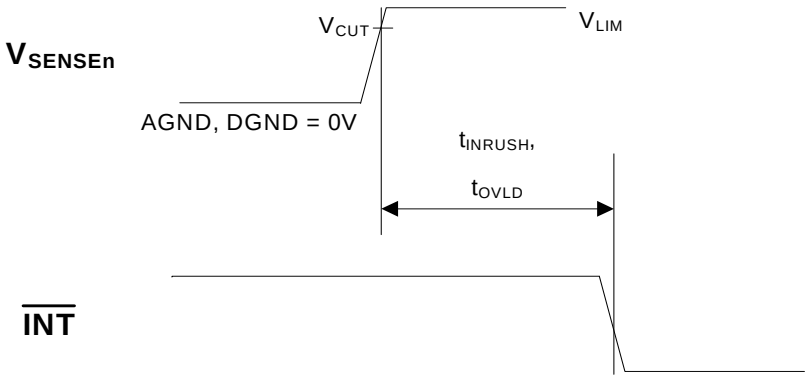


Figure 3. Current Limit Timing

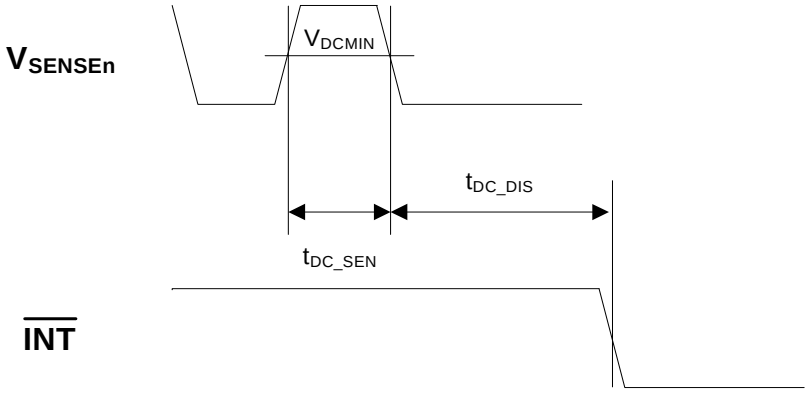


Figure 4. DC Disconnect Timing

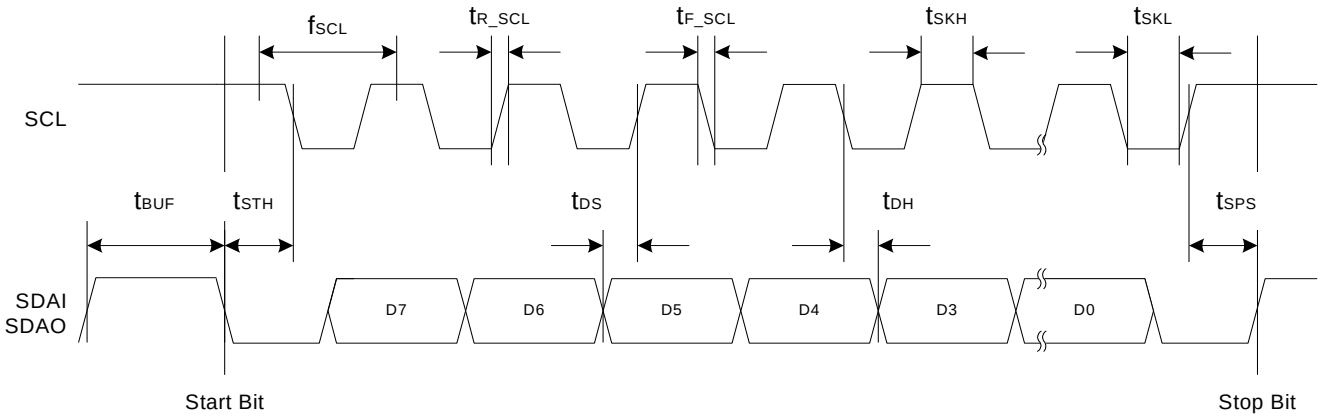


Figure 5. I²C Bus Interface Timing

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Temperature	T_A		–40	—	85	°C
Thermal Impedance	θ_{JA}	4-Layer PCB, no airflow	—	20	—	°C/W
Junction Temperature	T_J		–40	—	125	°C

Table 7. Absolute Maximum Ratings[1]

Type	Parameter	Rating	Unit
Supply Voltages	VPWR to AGND[2]	–0.3 to 70	V
	VDD to DGND[2]	–0.3 to 4.2	V
Voltage on Digital Pins	$\overline{\text{INT}}$, $\overline{\text{RESET}}$, A4, A3, A2, A1, SCL, SDAI, SDAO, $\overline{\text{SHDN}}$, AUTO	DGND–0.3 to DGND+5.8	V
Voltage on Analog Pins	SENSEn	AGND–0.6 to AGND+0.6	V
	GATEn[3,4]	AGND–0.3 to AGND+12	V
	DRAINn	–0.3 to VPWR	V
	KSENSA, KSENSB	AGND–0.6 to AGND+0.6	V
	ISENSE	VPWR–5 to VPWR	V
ESD HBM (Human Body Model[5]) Tolerance		–2 to +2	kV
Maximum Junction Temperature[6]		125	°C
Operating temperature range		–40 to +85	°C
Ambient Storage Temperature		–65 to 150	°C
Lead Temperature (Soldering, 10 Seconds Maximum)		260	°C

Notes:

1. Stresses beyond the absolute maximum ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Functional operation should be constrained to those conditions specified in Table 1, “PSE Port Interface Recommended Operating Conditions[1],” on page 4 and Table 3, “Digital Pin Recommended Operating Conditions[1],” on page 9.
2. AGND is shorted to DGND inside the package.
3. The GATE pins include an integrated clamp to limit the pins to a minimum of 12 V above AGND, GATE voltages in excess of AGND+12 V may cause permanent disconnect of the affected port.
4. The Si3454 includes protection circuitry to tolerate up to 80 mA of transient current for a maximum of 5 ms.
5. Charged Device Model (CDM), and Cable Discharge Event (CDE) electrical stress tolerance are typically 500 V and 3 kV.
6. Thermal overload protection shuts down the device when the silicon junction temperature exceeds 165 °C, including a temperature hysteresis of 20 °C.

2. Typical Performance Characteristics

This section shows various waveforms that describe typical behaviors and performance of the Si3454. The waveform in Figure 6 shows the part in semi-auto mode with Rgood and Cgood. The Si3454 uses a multi-point detection algorithm. Typically, a Cbad of >10 µF causes an Rlow indication. The Detection Signature is calculated for two measurements at the primary voltage and two measurements at the secondary voltage. For there to be an Rgood indication, the signature must be Rgood in all steps.

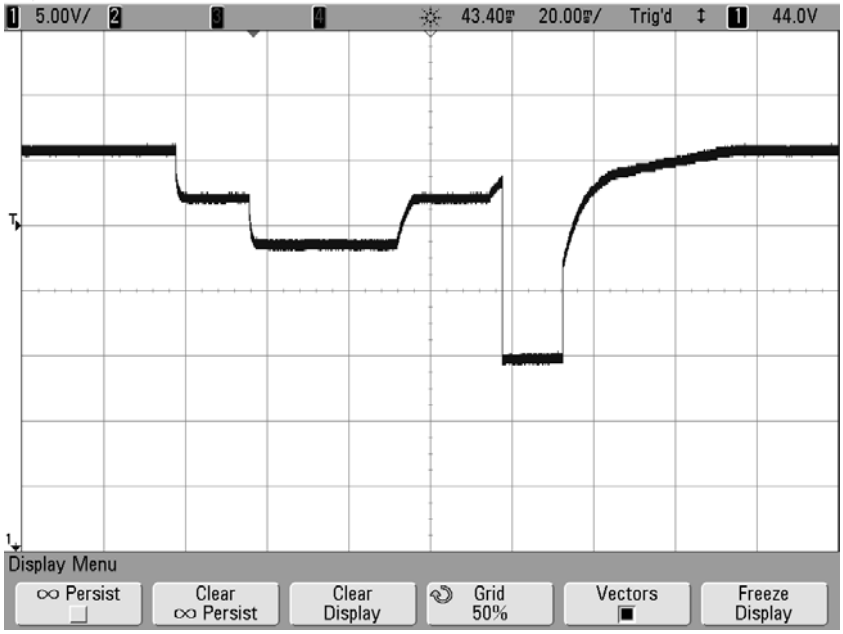


Figure 6. Typical Detect and Classify Sequence (Semi-Auto Mode)

Figure 7 shows the FET gate drive set to 50 µA for FET turn-on. The slew time is about 40 µs with this FET gate drive and is not strongly load-dependent.

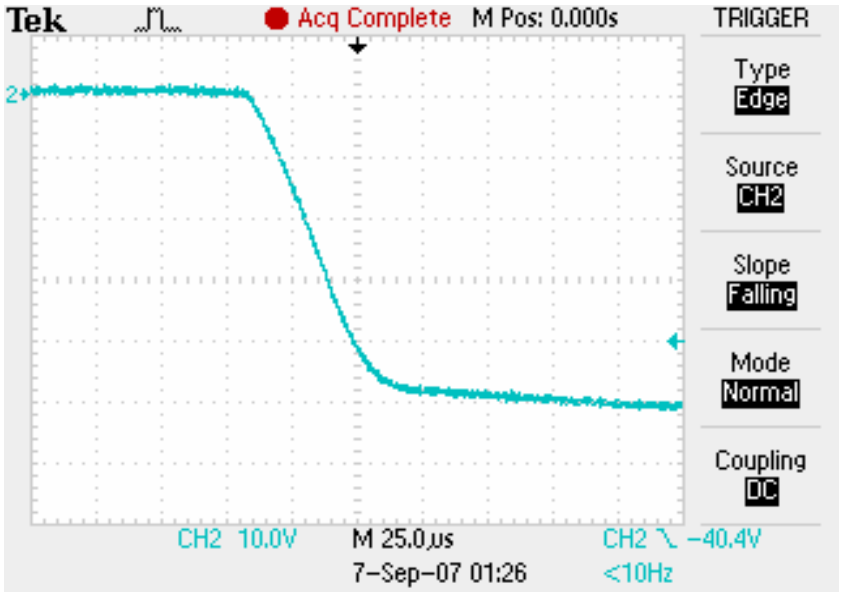


Figure 7. Typical Powerup (220 Ω Load)

The waveform in Figure 8 shows power down when the load is switched to 100 kΩ.

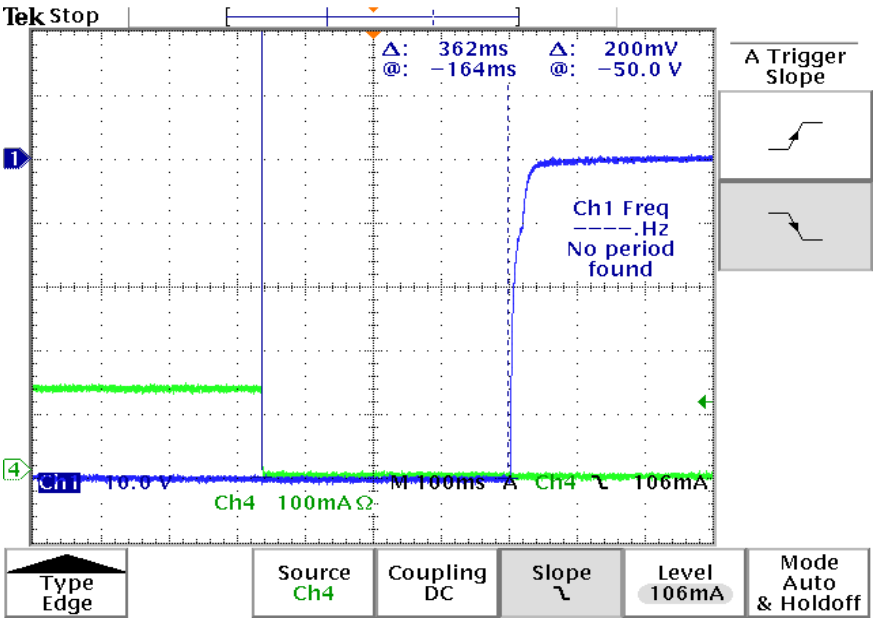


Figure 8. Typical DC Disconnect and Powerdown Sequence

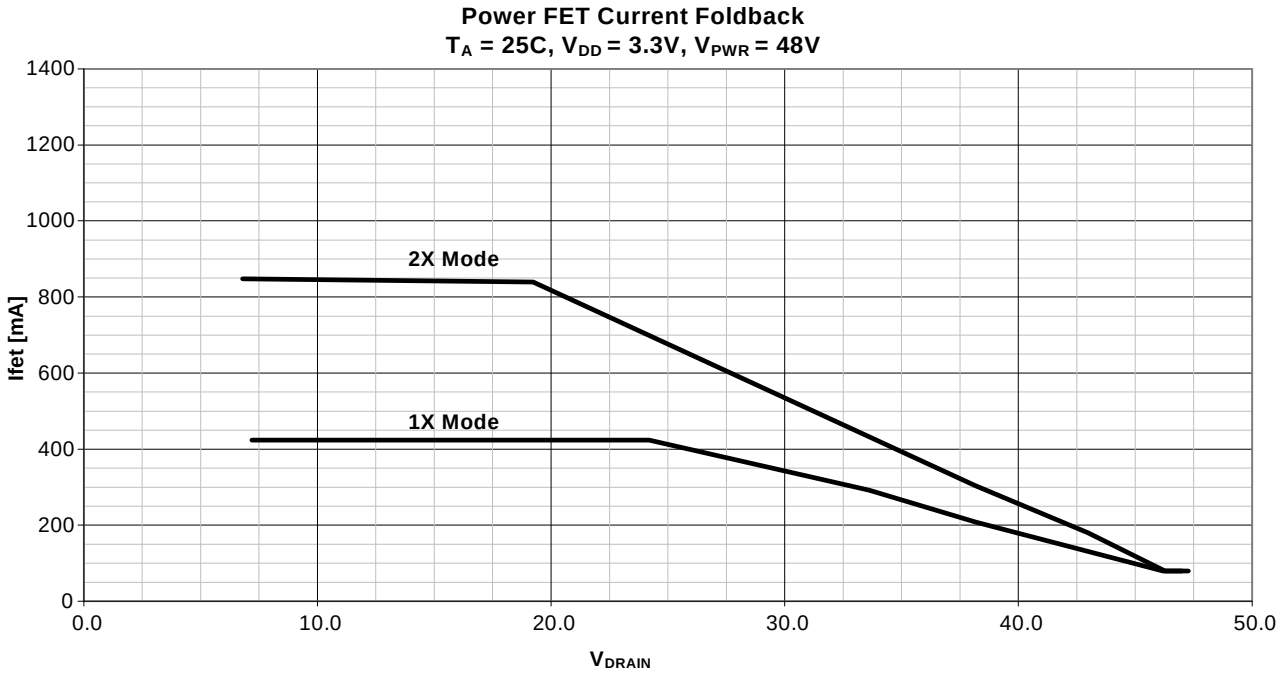


Figure 9. Fold Back Current in IEEE 802.3at (1X) and 2X Current Limit Modes

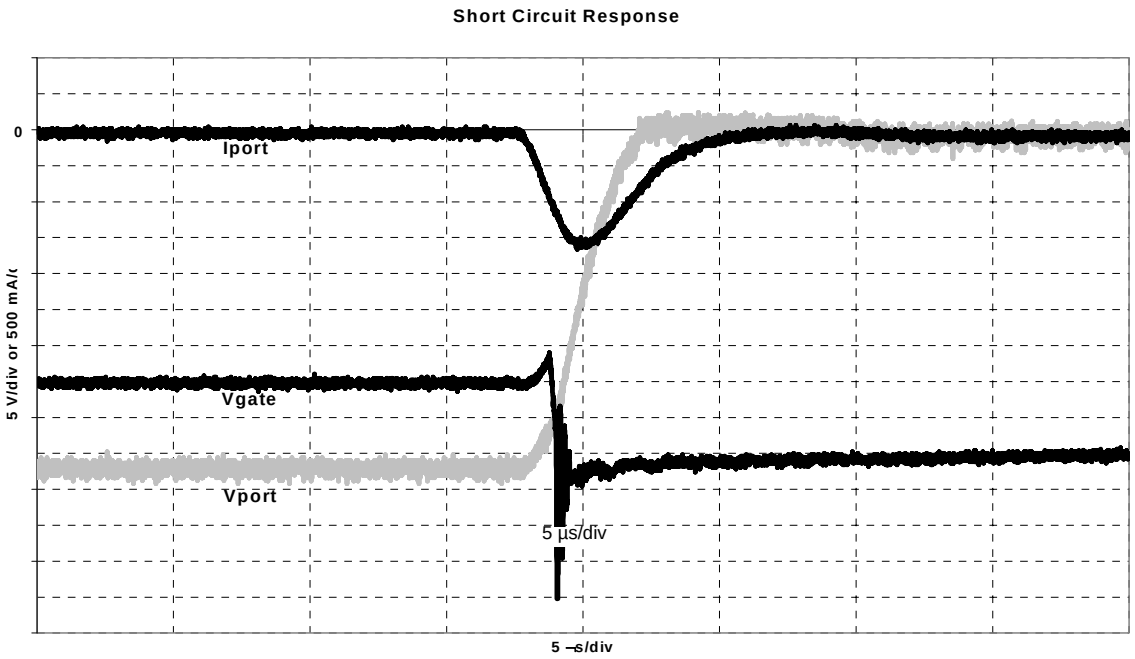


Figure 10. Short Circuit Response

3. Functional Description

Integrating a high-performance microcontroller with high-resolution A/D and D/A capabilities, along with four independent, high-voltage PSE port interfaces, the Si3454 enables an extremely flexible solution for virtually any PoE switch application. The Si3454 integrates all PSE controller functions needed for an quad-port PoE design.

The Si3454 includes many additional features that can be individually enabled or disabled by programming the extended register set appropriately.

- Per-port current / voltage monitoring and measurement
- Multipoint detection algorithms
- 802.3at support
- Programmable gate drive for external MOSFETs
- Watchdog timer (WDT)

3.1. Quad High-Voltage PSE Port Interfaces

In addition to the IEEE 802.3at detection and classification functionality, the high-voltage port interfaces provide accurate voltage and current control and measurement for each of the four output ports. The high-voltage port interface circuitry is controlled by the internal microcontroller and includes the following features beyond the 802.3at standard's base requirements.

3.1.1. Per-Port Measurement and Monitoring

The measurement function supports the following capabilities, which enable flexible per-port voltage and current monitoring.

- Detection and classification current measurement with on-chip sense resistors.
- FET current measurement through 0.25 Ω sense resistor with 1 A full-scale.
  - FET current scaling is changed dynamically so as to allow sensitive and accurate dc disconnect, even for a 2x current limit.
- Current measurement offset calibration circuitry.
- V_{PWR} and output voltage measurement.
  - Each channel and range is factory-calibrated.
  - Channel parameters can be read from each port's corresponding registers (output voltage, and current) and are sampled approximately every three milliseconds.
- Supply monitors on V_{DD} and V_{PWR}.

3.1.2. DC Disconnect

DC disconnect may be enabled on any port. If dc disconnect is not enabled when the load is disconnected, the port will not shut off except in response to other fault conditions.

3.1.3. Programmable MOSFET Gate Drivers

To provide maximum system-level design flexibility and optimal EMI performance when interfacing to external high-current MOSFET devices, the Si3454 provides four independent MOSFET gate drivers with the following features:

- Drive current is 50 µA nominal.
- A 100 mA pull-down that is automatically activated if a current transient of 25% over the programmed current limit is sensed.
- Current limit circuit that can be programmed to 425 or 850 mA typical.
  - Current limit is based on voltage sensed across 0.25 Ω sense resistor.
  - Each channel and range is internally trimmed to ±5% accuracy.
  - Linear fold-back behaves as shown in Figure 9 on page 16.

3.2. Operating Modes

The Si3454 normally operates in manual or semi-automatic mode when the AUTO pin is held low. If a valid set voltage level (described in Table 8) is applied to the AUTO pin, the Si3454 enters into fully autonomous operation, independent of a host. When setup voltages indicated as “Reserved” are applied to the AUTO pin, the Si3454 does not enter into fully autonomous mode but remains instead in Shutdown mode. The Si3454 also features dc disconnect detection algorithms to determine when a PD device is disconnected from any of the four independent ports.

The AUTO mode can be set via the AUTO pin or from the host via I^2C.

At power-up, the Si3454 reads the voltage on the AUTO pin (which can be set by a resistor divider from VDD to GND). If a valid setup voltage is applied, the Si3454 enters into AUTO mode (all ports operate fully autonomously). The AUTO pin voltage level configures the Si3454's behavior through the register default values as summarized in Table 8 below.

In Host-controlled mode, any port can be configured to AUTO mode through the confp_x register. In this case the Host should set the proper port configuration.

Table 8. Auto Pin Configurations

Voltage on the AUTO Pin	IEEE Class	Endpoint vs. Midspan	Restart	Detect+Classify Looping	Register Default Values		
					confp_x	tlimp_x	icutp_x
0 (AUTO pin pulled to GND)	Shutdown				0x00	0x00	0x54
0.22	Reserved						
0.44	Reserved						
0.66	3	Mid	Auto after 2 s	Automatic detect/ class loop	0x7f	0x00	0x54
0.88	Reserved						
1.10	Reserved						
1.32	Reserved						
1.54	3	End	Auto after 2 s	Automatic detect/ class loop	0x3f	0x00	0x54
1.76	Reserved						
1.98	Reserved						
2.20	Reserved						
2.42	4	Mid	Auto after 2 s	Automatic detect/ class loop	0x7f	0x20	0x54
2.64	Reserved						
2.86	Reserved						
3.08	Reserved						
3.30 (AUTO pin pulled to VDD)	4	End	Auto after 2 s	Automatic detect/ class loop	0x3f	0x20	0x54

3.2.1. Additional Operating Modes Notes

- By default the Icut limit is set to 375 mA (**icutp_x** = 0x54; Class 0 or Class 3 limits) initially for all operating modes

3.2.1.1. AUTO Mode-Specific Behaviors

- The “hpen” bit will be set automatically, but only if the 2-event classification was successful
- If there was a successful 2-event classification, then the Icut limit will be increased to 638 mA (Nominal) automatically (**icutp_x** = 0x62)
- The intmask register is set to 0xff in all pin configured AUTO modes

3.2.1.2. Manual and Semi-Auto Mode Behaviors

- To enable IEEE Type 2 Class 4 operation only the “pongen” bit need be set (**tlimp_x** = 0x20)
- It is the host role to set the “hpen” bit, but only if the 2-event classification was successful (the “pongpd” bit is set in the **pwrstatp_x** register)
- It is the host role to set the Icut limit properly

3.2.2. Port ON/OFF Control

The Si3454 offers various options for the Host to control the state of the ports. There is also logic in the part which controls the port state in response to an event.

3.2.2.1. HOST Controlled Port Turn ON

A port can be turned ON in the following ways:

1. In manual Mode, the port can be unconditionally turned on using the proper pushbutton register (set the “on_x” bit (Bit 0) in the **pb_p_x** register).
2. In Semi-Auto mode the port can be also turned on using the proper pushbutton register, but the port will not turn on until a valid PD signature is detected.
3. In Host controlled Auto mode (the AUTO pin is held low), the port will turn on automatically if detection and classification is enabled, a valid signature is detected, and the classification is successful. Otherwise the port can also be turned on using the proper pushbutton register, but in this Mode, the port will not turn on until a valid PD signature is detected. The following steps detail how a port can be turned on in the IEEE Std 802.3at-2012 Type 2 high-power manner:
   a. Enable detection and classification by setting the “detena_x” bit (Bit 2) “classena_x” bit (Bit 3) in the **confp**_x register
   b. Set the “hpen_x” bit (Bit 7) and the “pongen_x” bit (Bit 6) in the **tlimp**_x register to enable the 2-Event classification on the port, and
   c. Set the Icut limit in the **icutp**_x register according to the available power
4. In the Host independent Auto mode (positive voltage is applied to the AUTO pin), the detection and 2-event classification is enabled by default, so the port will turn on automatically if a valid signature is detected and the classification is successful. The current limits are set according to the classification result, so both Type 1 and Type 2 PDs are handled correctly.

3.2.2.2. Autonomous Port Turn ON

The only occurrence when the port could be turned ON automatically by the Si3454 is when the port is in Auto Mode and the detection and the classification were successful.

3.2.2.3. HOST Controlled Port Turn OFF

A port can be turned OFF at any time using one of the following methods:

1. By setting the “off_x” bit (Bit 1) in the **pb_p_x** registers (0x17, 0x27, 0x37, 0x47): The port is shut down, the event and status registers of the port are set to their default value, and the classification enable and detection enable bits are also cleared in the corresponding **confp**_x register (0x14, 0x24, 0x34, 0x44). The value of the other bits of the **confp**_x register are retained. The associated measurement data registers are also cleared.
2. By setting the “rst_x” bit (Bit 4) in the pb_p_x register: The port is shut down, and all associated events and configurations are cleared (all port registers are set to their default state)

3.2.2.4. Autonomous port turn OFF

In the following cases, a port is (or all ports are) turned OFF automatically by the Si3454:

1. In response to the over-temperature event all ports are turned OFF by using the “offall” bit in the **pb_global** register (0x0B). This is equivalent to the situation where the “off_x” of **pb_p**_x registers (0x17, 0x27, 0x37 and 0x47 for ports 1–4, respectively) were set.
2. In response to a UVLO event (either VDD or VPWR UVLO), all ports are reset by using the “rstall” bit in the **pb_global** register (0x0B). This is equivalent to the situation where the “rst_x” of the **pb_p**_x registers were set.
3. In response to the SHDN pin assertion the low priority ports are turned OFF by using the “off_x” bit (Bit 1) of **pb_p**_x register.
4. In response to an over-current event the port is shut down, i.e.: power is removed from the DRAINn pin, and the “pe_x” (Penable bit; Bit 0) and the “pg_x” (Pgood bit, Bit 1) for that port is set.
   The events are not cleared, and the full port configuration is retained.

3.3. V_{DD} Ramp Time

It is recommended that V_{DD} ramp into the operational range within 1 ms if reset is not held low. Slow ramp times are acceptable if reset is held low until V_{DD} is in the operational range. For additional detail on VDD and undervoltage lockout, refer to “4.2.2. Global Event Register and Global Event COR (0x02, 0x03)” .

3.4. I^2C Protocol

Controlling the features of the Si3454 is possible by programming a series of registers identified in the Register Map (see "4. Register Map" on page 26). Registers are accessible through a three-wire, I^2C-compatible serial interface.

3.4.1. Slave Address

The Si3454 slave base address is pin-assigned by logical ORing HW pins {A[3:0]} with value 0x20.

The complete base address is formed as “010[A3][A2][A1][A0]b”.

3.4.1.1. Available I²C Transfer Types

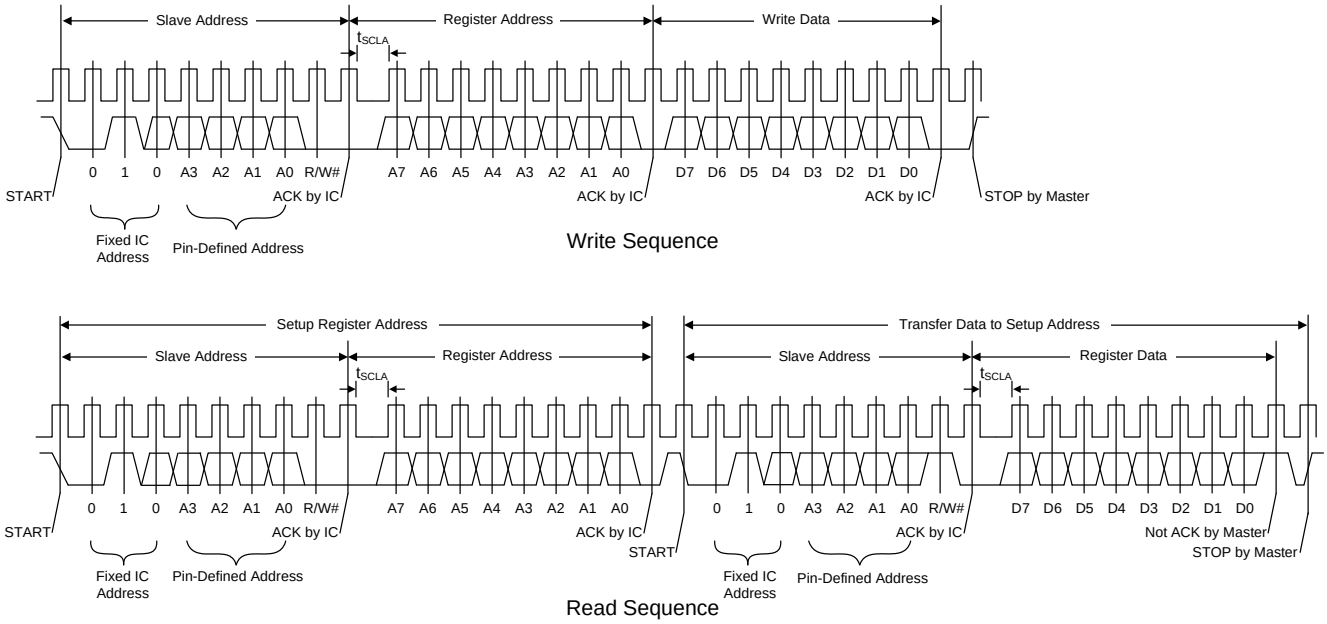


Figure 11. I²C Read and Write Sequences

8-Bit Read

All registers can be accessed this way, but it is not recommended for reading registers storing parametric measurement data (Iport and Vport, registers 0x19–0x1c, 0x29–0x2c, 0x39–0x3c, 0x49–0x4c).

Example Sequence

1. START condition, followed by the target slave's 7-bit address, and a write flag. The sequence is ACKed by the Si3454.
2. Then an 8-bit Si3454 register address is provided followed by an ACK. These steps set up a pointer register within the Si3454 that points to the address of an internal register to be read.
3. The transaction continues by sending a repeated START condition, followed by the target slave's 7-bit address, and a read flag. This sequence is ACKed by the Si3454.
4. Then the 8-bit IC register data is provided by the Si3454 (slave). This occurrence is followed by a master NACK (Not ACK).
5. Then the master frees the bus by sending a STOP condition.

See Figure 11, “I2C Read and Write Sequences,” on page 22 for more details.

8-Bit Write

All registers can be accessed this way (except the read only registers).

Example Sequence

1. START condition, followed by the Si3454 7-bit address, and a write flag. This is ACKed by the IC.
2. Then an 8-bit IC register address is provided followed by an ACK by the Si3454.
3. The transaction is completed by sending 8-bits of register data. This is ACKed by the Si3454.
4. Then the master frees the bus by sending a STOP condition.

See Figure 11, “I2C Read and Write Sequences,” on page 22 for more details.

16-Bit Read

This is the recommended access mode for reading registers storing parametric measurement data (Iport and Vport, registers 0x19–0x1c, 0x29–0x2c, 0x39–0x3c, 0x49–0x4c). Only these registers can be accessed this way in this mode.
The two byte (16-bit) read follows the same protocol described in the 8-bit read paragraph above, with the extra byte appended to the data field before the STOP condition. In this case, the Master should ACK the first byte, and NACK the second byte.

Example: Reading 2 Bytes from Offset 0x19 Gives the Current Measurement of Port 1

1. Start condition, followed by the target slave's 7-bit address, and a write flag. The sequence is ACKed by the Si3454.
2. Then an 8-bit Si3454 register address is provided followed by an ACK. These steps set up a pointer register within the Si3454 that points to the address of an internal register to be read.
3. The transaction continues by sending a repeated START condition, followed by the target slave's 7-bit address, and a read flag. This sequence is ACKed by the Si3454.
4. Then the LSB of PORT1 CURRENT MEASUREMENT (8-bit) data is provided by the Si3454 (slave). This occurrence is followed by a master ACK.
5. Then the MSB of PORT1 CURRENT MEASUREMENT (8-bit) data is provided by the Si3454 (slave). This occurrence is followed by a master NACK.
6. Then the master frees the bus by sending a STOP condition.

See Figure 11, “I2C Read and Write Sequences,” on page 22 for more details.

Quick Access to the Interrupt Register

Whenever a STOP is detected by the slave, its internal register address pointer is reset. Therefore, the next I^2C Read transaction will return the contents of the Interrupt register (0x00).

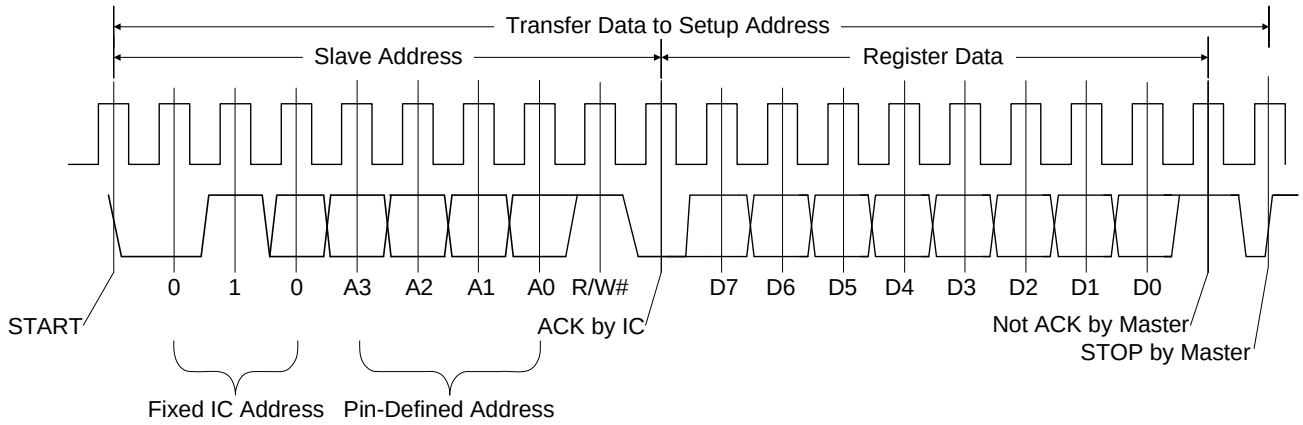


Figure 12. Quick Access Transaction

3.4.1.2. Global Address

Each device on the bus will respond to the global address (100 0000b) in exactly the same way it would to a read or write transaction using its specific slave address. The global address is primarily used to configure (write) all slaves the same after the PSE system is powered up. Global read transactions should be avoided.

3.4.1.3. Alert Response Address (ARA)

The ARA is used by the master as a quick way to determine which slaves are asserting (pulling low) the nINT line. The ARA address is 000 1100b

Each IC (“slave”) implements the following protocol:

- Only slaves that are asserting the nINT line respond when the master uses the ARA in a read cycle. All slaves that are not asserting nINT ignore read cycles that use the ARA.
- Each slave responding to the ARA transmits a byte consisting of its address in the upper 7 bits, and a 1 in the least significant bit.
- As each bit in the byte is transmitted, the slave determines whether to continue transmitting the remainder of the byte or terminate transmission. The slave terminates when it sees a 0 on SDA at a time when it’s attempting to send a 1; otherwise it continues transmitting bits until the entire byte has been sent.
- If a slave completes transmission of the entire byte without terminating, it releases (stops asserting) the nINT line. Any slave that terminated transmission continues to assert the nINT line.
  The result of this protocol is that the slave with the lowest address will complete the transmission and won’t respond to subsequent ARA read transactions until its event registers have been cleared. Other slaves, with higher addresses, terminate but will respond to the next ARA read cycle. Therefore, each time the master performs a read cycle using the ARA it receives the address of a different slave until all slaves have sent their addresses without terminating.

3.5. DC-to-DC Converter Description

The Si3454 includes a dc-dc converter for generation of an approximately 4.3 V intermediate power rail, which is further down-regulated to create the 3.3 V VDD power rail necessary for MCU operation and other support.

The dc-dc converter consists of a buck converter with accompanying external components to step down VPWR to approximately 4.3 V on the enabled “primary” converter. This voltage, called VCAP, can also be bussed to up to five adjacent “secondary” controllers. Each controller includes a series regulator for generation of 3.3 V for local use by that controller and an optional digital bus isolator.

The converter is enabled by asserting (tying low) $\overline{\text{DCEN}}$. In fact, $\overline{\text{DCEN}}$ should be asserted on the primary and all secondary controllers.

While the primary controller requires several external components to enable the dc-dc (see " DC-DC Converter Block Diagram" on page 2), the secondary controllers do not require those external components. On the secondary controllers, the SWO pin should be direct-tied to VPWR.

If $\overline{\text{DCEN}}$ is left floating the dc-dc converter is disabled, which eliminates excess current draw by the VPWR pin. To disable the dc-dc converter, the related pins (DCENb, CAP, and SWO) should be left floating.

The ISENSE pin implements a cycle-by-cycle current limit by comparing a sensed voltage to an internal reference. When the external power FET is conducting, if ISENSE drops more than 200 mV below VPWR, the FET will be shut off immediately to limit excessive currents. An appropriate external resistor should be selected to set the desired peak current level (i.e., Ipeak = 200 mV/Rsense). If ISENSE is left floating, an internal pull-up will effectively disable the current limit feature.

In the event of an extreme overcurrent event (e.g., short-circuit), the dc-dc output voltage, CAP, will drop below its target level of 3.6 V. If CAP falls below 90% of that level (i.e., 3.24 V) a dc-dc fault will be declared and the dc-dc and LDO will power down. The dc-dc will then attempt to restart in 4 ms intervals until the overcurrent fault is removed.

4. Register Map

4.1. Register Set

Table 9 lists the Si3454 registers.

Table 9. Si3454 Registers

Register		R/W	Port[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr[1]	Name											Auto Tied to DGND
Interrupt												
0x00	int	RO	Global	Overtemp	fetbad	uvlo3	uvlo48	p_4_ev	p_3_ev	p_2_ev	p_1_ev	0010 0000
0x01	intmask	R/W	Global	Status	ifault	startfault	dis	class	det	pwrgd	pwrena	1000 0000
Global Event Registers												
0x02	evn_global	RO	Global	Overtemp	fetbad	uvlo3	uvlo48	tsd	Reserved	Reserved	Reserved	0010 0000
0x03	evn_global_cor	COR	Global	Overtemp	fetbad	uvlo3	uvlo48	tsd	Reserved	Reserved	Reserved	0010 0000
Global Status Registers												
0x05	Status	RO	Global	tsd	slave_addr[4:0]					Reserved	Auto	0000 0000
0x06	Temperature	RO	Global	Die Temperature								0000 0000
0x07	VPWR_LSB	RO	Global	Vmain_LSB								0000 0000
0x08	VPWR_MSB	RO	Global	Vmain_MSB								0000 0000

Notes:

1. Register addresses not listed in the table are reserved and should not be written to.
2. The PORT column indicates which ports are associated with each register. For example, “2” means the register is associated with Port 2 only; “Global” refers to slave-level status and control registers.

Table 9. Si3454 Registers (Continued)

Register		R/W	Port[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr[1]	Name											Auto Tied to DGND
Global Configuration Registers												
0x0A	config	R/W	Global	intena	detchg	tsddisa	wddis[3:0]				wdstat	1001 0110
0x0B	pb_global	WO	Global	intclr	pinclr	lowpri	swrst	Reserved	Reserved	rstall	offall	0000 0000
0x0C	devid_sirev	RO	Global	Device_ID				Si_Revision				See "4.2.4.3. Device ID and Revision Registers (0x0C, 0x0D, 0x0E)"
0x0D	firmware	RO	Global	firmware_rev								
0x0E	manufid_dever	RO	Global	Manufacturer_ID				Device_Version				
Port 1 Registers												
0x10	evnp_1	RO	1	t_{LIM_1}	t_{CUT_1}	t_{START_1}	dis_1	cls_1	det_1	pwrgd_1	pwrena_1	0000 0000
0x11	evnp_1_cor	COR	1	t_{LIM_1}	t_{CUT_1}	t_{START_1}	dis_1	cls_1	det_1	pwrgd_1	pwrena_1	0000 0000
0x12	statp_1	RO	1	Reserved	class_1[2:0]			Reserved	detect_1[2:0]			0000 0000
0x13	pwrstatp_1	RO	1	Reserved	type2flt_1[2:0]			fetbad_1	pongpd_1	pg_1	pe_1	0000 0000
0x14	confp_1	R/W	1	legen_1	midsp_1	disena_1	priority_1	classena_1	detena_1	opmd_1[1:0]		0000 0000
0x15	tlimp_1	R/W	1	Reserved	hpen_1	pongen_1	Reserved	t_{LIM_1}[3:0]				0000 0000
0x16	icutp_1	R/W	1	Reserved	cutrng_1	I_{cut_1}[5:0]						0101 0100
0x17	pb_p_1	WO	1	Reserved	Reserved	Reserved	rst_1	cls_1	det_1	off_1	on_1	0000 0000
0x19	ip_1_lsb	RO	1	ip_1_lsb[7:0]								0000 0000
0x1A	ip_1_msb	RO	1	ip_1_msb[7:0]								0000 0000
0x1B	vp_1_lsb	RO	1	vp_1_lsb[7:0]								0000 0000
0x1C	vp_1_msb	RO	1	vp_1_msb[7:0]								0000 0000
0x1D	detresp_1	RO	1	p_1_detres[7:0]								0000 0000

Notes:

1. Register addresses not listed in the table are reserved and should not be written to.
2. The PORT column indicates which ports are associated with each register. For example, "2" means the register is associated with Port 2 only; "Global" refers to slave-level status and control registers.

Table 9. Si3454 Registers (Continued)

Register		R/W	Port[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr[1]	Name											Auto Tied to DGND
Port 2 Registers												
0x20	evnp_2	RO	2	t_{LIM_2}	t_{CUT_2}	t_{START_2}	dis_2	cls_2	det_2	pwrgd_2	pwrena_2	0000 0000
0x21	evnp_2_cor	COR	2	t_{LIM_2}	t_{CUT_2}	t_{START_2}	dis_2	cls_2	det_2	pwrgd_2	pwrena_2	0000 0000
0x22	statp_2	RO	2	Reserved	class_2[_2:0]			Reserved	detect_2[_2:0]			0000 0000
0x23	pwrstatp_2	RO	2	Reserved	Reserved	Reserved	Reserved	fetbad_2	pongpd_2	pg_2	pe_2	0000 0000
0x24	confp_2	R/W	2	legen_2	midsp_2	disena_2	priority_2	classena_2	detena_2	opmd_2[1:0]		0000 0000
0x25	tlimp_2	R/W	2	Reserved	hpen_2	pongen_2	Reserved	t_{LIM_2}[3:0]				0000 0000
0x26	icutp_2	R/W	2	Reserved	cutrng_2	I_{cut_2}[5:0]						0101 0100
0x27	pb_p_2	WO	2	Reserved	Reserved	Reserved	rst_2	cls_2	det_2	off_2	on_2	0000 0000
0x29	ip_2_lsb	RO	2	ip_2_lsb[7:0]								0000 0000
0x2A	ip_2_msb	RO	2	ip_2_msb[7:0]								0000 0000
0x2B	vp_2_lsb	RO	2	vp_2_lsb[7:0]								0000 0000
0x2C	vp_2_msb	RO	2	vp_2_msb[7:0]								0000 0000
0x2D	detresp_2	RO	2	p_2_detres[7:0]								0000 0000

Notes:

1. Register addresses not listed in the table are reserved and should not be written to.
2. The PORT column indicates which ports are associated with each register. For example, “2” means the register is associated with Port 2 only; “Global” refers to slave-level status and control registers.

Table 9. Si3454 Registers (Continued)

Register		R/W	Port[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr[1]	Name											Auto Tied to DGND
Port 3 Registers												
0x30	evnp_3	RO	3	t_{LIM_3}	t_{CUT_3}	t_{START_3}	dis_3	cls_3	det_3	pwrgd_3	pwrena_3	0000 0000
0x31	evnp_3_cor	COR	3	t_{LIM_3}	t_{CUT_3}	t_{START_3}	dis_3	cls_3	det_3	pwrgd_3	pwrena_3	0000 0000
0x32	statp_3	RO	3	Reserved	class_3[2:0]			Reserved	detect_3[2:0]			0000 0000
0x33	pwrstatp_3	RO	3	Reserved	Reserved	Reserved	Reserved	fetbad_3	pongpd_3	pg_3	pe_3	0000 0000
0x34	confp_3	R/W	3	legen_3	midsp_3	disena_3	priority_3	classena_3	detena_3	opmd_3[1:0]		0000 0000
0x35	tlimp_3	R/W	3	Reserved	hpen_3	pongen_3	Reserved	t_{LIM_3}[3:0]				0000 0000
0x36	icutp_3	R/W	3	Reserved	cutrng_3	I_{cut_3}[5:0]						0101 0100
0x37	pb_p_3	WO	3	Reserved	Reserved	Reserved	rst_3	cls_3	det_3	off_3	on_3	0000 0000
0x39	ip_3_lsb	RO	3	ip_3_lsb[7:0]								0000 0000
0x3A	ip_3_msb	RO	3	ip_3_msb[7:0]								0000 0000
0x3B	vp_3_lsb	RO	3	vp_3_lsb[7:0]								0000 0000
0x3C	vp_3_msb	RO	3	vp_3_msb[7:0]								0000 0000
0x3D	detresp_3	RO	3	p_3_detres[7:0]								0000 0000

Notes:

1. Register addresses not listed in the table are reserved and should not be written to.
2. The PORT column indicates which ports are associated with each register. For example, “2” means the register is associated with Port 2 only; “Global” refers to slave-level status and control registers.

Table 9. Si3454 Registers (Continued)

Register		R/W	Port[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr[1]	Name											Auto Tied to DGND
Port 4 Registers												
0x40	evnp_4	RO	4	t_{LIM_4}	t_{CUT_4}	t_{START_4}	dis_4	cls_4	det_4	pwrgd_4	pwrena_4	0000 0000
0x41	evnp_4_cor	COR	4	t_{LIM_4}	t_{CUT_4}	t_{START_4}	dis_4	cls_4	det_4	pwrgd_4	pwrena_4	0000 0000
0x42	statp_4	RO	4	Reserved	class_4[2:0]			Reserved	detect_4[2:0]			0000 0000
0x43	pwrstatp_4	RO	4	Reserved	Reserved	Reserved	Reserved	fetbad_4	pongpd_4	pg_4	pe_4	0000 0000
0x44	confp_4	R/W	4	legen_4	midsp_4	disena_4	priority_4	classena_4	detena_4	opmd_4[1:0]		0000 0000
0x45	tlimp_4	R/W	4	Reserved	hpen_4	pongen_4	Reserved	t_{LIM_4}[3:0]				0000 0000
0x46	icutp_4	R/W	4	Reserved	cutrng_4	I_{cut_4}[5:0]						0101 0100
0x47	pb_p_4	WO	4	Reserved	Reserved	Reserved	rst_4	cls_4	det_4	off_4	on_4	0000 0000
0x49	ip_4_lsb	RO	4	ip_4_lsb[7:0]								0000 0000
0x4A	ip_4_msb	RO	4	ip_4_msb[7:0]								0000 0000
0x4B	vp_4_lsb	RO	4	vp_4_lsb[7:0]								0000 0000
0x4C	vp_4_msb	RO	4	vp_4_msb[7:0]								0000 0000
0x4D	detresp_4	RO	4	p_4_detres[7:0]								0000 0000

Notes:

1. Register addresses not listed in the table are reserved and should not be written to.
2. The PORT column indicates which ports are associated with each register. For example, “2” means the register is associated with Port 2 only; “Global” refers to slave-level status and control registers.

4.2. Detailed Register Descriptions

Note that, in the following Register Definition Descriptions, the term “set” means that a bit is a logical 1 (or high) value, and the term “clear” means that a bit is a logical 0 (or low) value.

4.2.1. Interrupt Registers

These registers either report (0x00) or mask (0x01) interrupts. The Si3454 monitors all interrupt sources and sets the appropriate bit(s) in the **int** register (0x00).

The **intmask** register (0x01) controls the masking of groups of events, enabling or blocking those events from affecting the state of the INT pin. The **intmask** register only affects the INT pin behavior.

4.2.1.1. Interrupt Status Register (Address 0x00)

Read only. When set to logic 1 by various interrupt events, bits in this register report the source of a particular interrupt. Assuming the corresponding bit in the **intmask** register is set, when bits in this register are asserted, the INT pin is asserted (pulled to ground). Each bit of the bottom nibble (the 4 least significant bits) in this register is the logical OR of all bits in the corresponding port’s event register (**evnp**_x: 0x10, 0x20, 0x30, 0x40) bits. The upper nibble (the 4 most significant bits) in this register reflects the status of the upper nibble bits of the **evn_global** register (0x02). Clearing bits in the **int** register requires that the corresponding bits in the **evn_global** register (0x02) or all bits in the corresponding port event registers be cleared. Alternatively, all bits in the **int** register can be cleared by setting bit 7 in the **pb_global** register (0x0B) to a logical 1 value. The INT pin can be deasserted by setting bit 6 in the **pb_global** register (0x0B) to a logical 1 value. Additional detail is found in the register description below.

Register		**R/W**	**Port**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset State**
Addr	**Name**											**Auto tied to DGND**
0x00	Int	RO	Global	overtemp	fetbad	uvlo3	uvlo48	p_4_ev	p_3_ev	p_2_ev	p_1_ev	0010 0000
Bit	**Name**	**Function**										
7	overtemp	Interrupt status bit for over temperature event.										
		0:	the “overtemp” bit is not set in the **evn_global** register.									
		1:	the “overtemp” bit is set in the **evn_global** register.									
6	fetbad	Interrupt status bit for external MOSFET failure event.										
		0:	the “fetbad” bit is not set in the **evn_global** register.									
		1:	the “fetbad” bit is set in the **evn_global** register.									
5	uvlo3	Interrupt status bit for VDD Over Voltage Lock Out failure event.										
		0:	the “uvlo3” bit is not set in the **evn_global** register.									
		1:	the “uvlo3” bit is set in the **evn_global** register.									
4	uvlo48	Interrupt status bit for VPWR Over Voltage Lock Out failure event.										
		0:	the “uvlo48” bit is not set in the **evn_global** register.									
		1:	the “uvlo48” bit is set in the **evn_global** register.									

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto tied to DGND
0x00	Int	RO	Global	overtemp	fetbad	uvlo3	uvlo48	p_4_ev	p_3_ev	p_2_ev	p_1_ev	0010 0000
Bit	**Name**	**Function**										
3	p_4_ev	Interrupt status bit for Port 4 events.										
		0:	Port 4 has no active event.									
		1:	Port 4 has at least one active event.									
2	p_3_ev	Interrupt status bit for Port 3 events.										
		0:	Port 3 has no active event.									
		1:	Port 3 has at least one active event.									
1	p_2_ev	Interrupt status bit for Port 2 events.										
		0:	Port 2 has no active event.									
		1:	Port 2 has at least one active event.									
0	p_1_ev	Interrupt status bit for Port 1 events.										
		0:	Port 1 has no active event.									
		1:	Port 1 has at least one active event.									

4.2.1.2. Interrupt Mask Register (0x01)

Writing a logic 1 to any bit in the **intmask** register allows the specified event type to propagate to the INT pin. Writing a logical 0 to any bit of the **intmask** register stops the specified event type from propagating to the INT pin. The INT pin can be de-asserted by setting bit 6 in the **pb_global** register (0x0B) to a logical 1 value. Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto tied to DGND
0x01	intmask	R/W	Global	status	ifault	startfault	dis	class	det	pwrgd	pwrena	1000 0000

Bit	Name	Function	
7	status	Interrupt mask bit for overtemp, FETBAD, UVLO3 and UVLO48 global events.	
		0:	Disables the overtemp, FETBAD, UVLO3 and UVLO48 events in the **evn_global** register from propagating to the INT pin.
		1:	Enables the overtemp, FETBAD, UVLO3 and UVLO48 events in the **evn_global** register to propagate to the INT pin.
6	ifault	Interrupt mask bit for Tcut and Tlim events on all ports.	
		0:	Disables the Tcut and Tlim events from propagating to the INT pin.
		1:	Enables the Tcut and Tlim events to propagate to the INT pin.
5	startfault	Interrupt mask bit for Start Fault event on all ports.	
		0:	Disables the Start Fault event from propagating to the INT pin.
		1:	Enables the Start Fault event to propagate to the INT pin.
4	dis	Interrupt mask bit for disconnect event on all ports.	
		0:	Disables the disconnect event from propagating to the INT pin.
		1:	Enables the disconnect event to propagate to the INT pin.
3	class	Interrupt mask bit for classification completed event on all ports.	
		0:	Disables the classification completed event from propagating to the INT pin.
		1:	Enables the classification completed event to propagate to the INT pin.
2	det	Interrupt mask bit for detection completed event on all ports.	
		0:	Disables the detection completed event from propagating to the INT pin.
		1:	Enables the detection completed event to propagate to the INT pin.
1	pwrgd	Interrupt mask bit for the Power Good event on all ports.	
		0:	Disables the Power Good event from propagating to the INT pin.
		1:	Enables the Power Good event to propagate to the INT pin.
0	pwrena	Interrupt mask bit for the Power Enabled event on all ports.	
		0:	Disables the Power Enabled event from propagating to the INT pin.
		1:	Enables the Power Enabled event to propagate to the INT pin.

4.2.2. Global Event Register and Global Event COR (0x02, 0x03)

Device-related events can be polled using these registers. The content of register 0x03 is identical to that of 0x02, however, if 0x03 is read, both registers will clear momentarily. The register bits are set again every few milliseconds if the fault is still present. Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto tied to DGND
0x02	evn_global	RO	Global	overtemp	fetbad	uvlo3	uvlo48	tsd	Reserved	Reserved	Reserved	0010 0000

Bit	Name	Function
7	Overtemp	Over temperature event bit.
		When the part's die temperature is above the over-temperature threshold (135 °C) the “overtemp” bit is set until register 0x03 is read. All ports are powered down as described in paragraph 3.2.2.4, point 1, if the shut-down on over-temperature feature is not disabled with the “tsddisa” bit (Bit 5 is zero in the config register).
		0: The part's die temperature is under the over-temperature threshold (135 °C).
		1: The part's die temperature is above the over-temperature threshold (135 °C).
6	fetbad	External MOSFET failure event bit.
		When there is a leaky FET on any port then the “fetbad” (bit 6) will be set. It will remain set until specifically cleared by reading the corresponding COR register (0x03). The leaky FET test is performed at the start of a detection cycle. Note that the “fetbad_x” bit in the individual port’s powerstatp_x registers are updated at the beginning of each detection cycle. See the “Bad FET Measurement” parameter in Table 1 for test limits.
		0: The detection process found the external MOSFET operating correctly.
		1: The detection process found the external MOSFET is damaged.
5	uvlo3	VDD Over Voltage Lock Out failure event bit
		Indicates a VDD supply fault event. This event bit remain latched until cleared by reading the COR register (0x03), and only “good” to “bad” transitions are reported. **Notes:** **1.** Measured values, such as temperature, port voltages, and currents are inaccurate if VDD<2.6 V. **2.** Until VDD exceeds 2.8 V, all ports are powered down as described in paragraph 3.2.2.4, point 2. Writing to the confp_x, tlimp_x, icutp_x and pb_p_x registers is prohibited.
		0: VDD > 2.8 V (Typ).
		1: VDD < 2.8 V (Typ).
4	uvlo48	VPWR Over Voltage Lock Out failure event bit.
		Indicates a VPWR supply fault event. This event bit remain latched until cleared by reading the COR register (0x03), and only “good” to “bad” transitions are reported. This event has hysteresis between 32 V and 44 V. **Note:** Until VPWR exceeds 44V, all ports are powered down as described in paragraph 3.2.2.4, point 2. Writing to the confp_x, tlimp_x, icutp_x and pb_p_x registers is prohibited.
		0: VPWR > 44 V (TYP).
		1: VPWR < 32 V (TYP) if VPWR is decreasing; VPWR < 44V if VPWR is increasing.

3	tsd	Thermal shutdown event bit.	
		Set to a logical 1 value when all powered ports have been shut down due to an over-temperature condition. This event bit remains latched until cleared by reading the COR register (0x03).	
		0:	The part's die temperature is under the over-temperature threshold if the shutdown on over-temperature is enabled; otherwise, it is under the safe-temperature threshold.
		1:	All powered ports have been shut down due to the fact that the part's die temperature is above the over-temperature or the safe-temperature threshold.
2:0	Reserved		

4.2.3. Global Status Registers

These registers provide status information (I^2C address, Die Temperature, VPWR Voltage) valid for the full device.

4.2.3.1. Status (0x05)

This register provides information about global (all four ports) status. Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x05	Status	RO	Global	Reserved	Reserved	slave_addr[4:0]				Reserved	auto	0000 0000
Bit	**Name**	**Function**										
7	Reserved											
6:2	slave_addr[4:0]	I^2C slave address.										
		This field is comprised of the state of the 4 address selection pins A[3:0] (sampled once after reset).										
1	Reserved											
0	auto	Initial status of the AUTO pin (sampled once after reset).										

4.2.3.2. Temperature (0x06)

This register provides information about the die temperature. The actual temperature can be calculated using the following equation:

T = –20 + N x 0.652 °C, where N is the binary value contained in this register.

The resulting temperature is in the range of –20 to 146.3 °C

4.2.3.3. VPWR Voltage (0x07, 0x08)

VPWR voltage can be accessed via registers 0x07 and 0x08. The voltage measurement are 16-bit words, divided into two bytes: the Most Significant Byte (MSB, register 0x08) contains the upper 8 bits; and the Least Significant Byte (LSB, register 0x07) contains the lower 8 bits. Reading the lower byte latches the upper byte until it is read, to assure they are both from the same sample; therefore, the lower byte should always be read first. After concatenating the upper and lower bytes, multiply by 5.835 mV/count to obtain the VPWR voltage.

4.2.4. Global Configuration Registers

The device related configuration is related to all ports and can be set using these registers.

4.2.4.1. config (0x0A)

Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x0A	config	R/W	Global	intena	detchg	tsddisa	wddis[3:0]				wdstat	1001 0110

Bit	Name	Function	
7	intena	Enable or disable the interrupt pin.	
		0:	The INT pin is asserted when there is an interrupt event which is not masked by the **intmask** register.
		1:	The INT pin is not active and remains unasserted (logic level 1).
6	detchg	Detect event reporting control bit	
		0:	The detection complete event bits , as reported by “det_x” (bit 2) of the evnp_x (0x10, 0x20, 0x30, 0x40) registers, are set every time a detection cycle concludes.
		1:	The detection complete event bits are only set if there is a change in the result from the last detection.
5	tsddisa	Disable shutdown on over-temperature event	
		0:	The powered ports will be shut down when the part's die temperature is above the over-temperature threshold (135 °C).
		1:	The powered ports will be shut down when the part's die temperature is above the safe-temperature threshold (146 °C).
4:1	wddis[3:0]	Watchdog timer control	
		The watchdog timer monitors the SCL pin and is reset by transitions on either edge. If the timer is not reset for approximately 2.5 seconds, all ports will be powered off, and the WD status bit will be set. The WD status bit (‘wdstat’; bit 0) can only be cleared by writing a zero to this bit or by a RESET. The Watchdog timer is disabled by writing a 1011b to the WD disable field. The POR reset value of WD disable is 1011b (disabled). The WD timer can be enabled by writing any (non-1011b) value to this field; for example, writing 0000b will enable the WD timer.	
0	wdstat	Watchdog status bit.	
		0:	The watchdog timer is either not running (disabled) or has not timed out.
		1:	The watchdog timer has timed out.

4.2.4.2. Global PushButton Register (0x0B)

This is a write only register.

Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x0B	pb_global	WO	Global	intclr	pinclr	lowpri	swrst	Reserved	Reserved	rstall	offall	0000 0000
Bit	**Name**	**Function**										
7	intclr	Clear interrupt status.										
		1:	All bits in the int register will be cleared.									
6	pinclr	Clear INT pin										
		1:	De-assert the INT pin. Setting Bit 6 to a logical 1 value does not clear any interrupt sources.									
5	lowpri	Turn off the low priority ports										
		1:	Turn off any already-powered low priority ports (as identified by the per-port **confp_x** register "priority" bits).									
4	swrst	Software reset										
		1:	Resets the ports and registers completely. All ports and registers are reset to their default state. The **config** register is not reset; this register controls shared resources (INT pin, watch-dog timer). The MCU is not reset (setting the "swrst" bit is not equivalent to a HW reset caused by the RESET/ pin).									
3	Reserved											
2	Reserved											
1	rstall	Single bit control to reset all ports otherwise leaving register settings intact.										
		1:	The ports are reset to the shutdown state as it is described in section 3.2.2.3, point 2.									
0	offall	Single bit control to turn off all ports.										
		1:	The ports are turned off as it is described in section 3.2.2.3, point 1.									

4.2.4.3. Device ID and Revision Registers (0x0C, 0x0D, 0x0E)

These Registers are Read only.

Register 0x0C is the device identification and silicon revision register. The "Device_ID" bitfield is 0001b for Si3454 devices. The "Si_Revision" bitfield indicates the silicon revision number and contains 0000b.

Register 0x0D is the firmware revision register. Firmware revision is coded as two bytes with only decimal characters. As an example: Revision 0.3 would be coded as 0x03. See "6. Ordering Guide" for the current Firmware Revision number.

Register 0x0E is the Manufacturer ID and Device Version register. The Manufacturer ID for Silicon Labs is 0100b. The Device Version is 0001b.

4.2.5. Port-Specific Registers

Per-port events, status information, and configuration settings are grouped together in the register set. Each port has its own register group with exactly the same content.

4.2.5.1. Event Register (evnp_x; 0x10, 0x20, 0x30, 0x40)

This Register is Read only, and each bit has relevance only when it is set.

If any bit is set in this register, then the corresponding p_x_ev bit in the **int** register (0x00) is also set.

The INT pin will also be asserted if the corresponding mask bit in the **intmask** register (0x01) is set. For example, if the “pwrgd” mask bit in the **intmask** register is set, then when the “pwrgd_x” bit (Bit 1 of **evnp**_x) becomes one, the INT pin will be asserted.

*Exception: bit 6 and bit 7 of this register have common mask bit 6 (called “ifault”) in the **intmask** register (0x01), so the INT pin will be asserted if the ifault mask bit is set in the **intmask** register and any of the tcut_x or the tlim_x bits becomes one.*

When a bit in this register is set, it latches, and only clears when the corresponding **evnp**_x_cor (Clear-on-Read) register is read at the following addresses: **0x11, 0x21, 0x31, 0x41**.

Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x10, 0x20, 0x30, 0x40	evnp_x	RO	1, 2, 3, 4	t_{LIM_x}	t_{CUT_x}	t_{START_x}	dis_x	cls_x	det_x	pwrgd_x	pwrena_x	0000 0000

Bit	Name	Function	
7	t_{LIM_x}	I_{LIM} fault event bit	
		1:	I_{LIM} fault (alternatively called a current limit timeout, with symbol t_{LIM}) has occurred on the port.
6	t_{CUT_x}	t_{CUT} fault event bit	
		1:	I_{CUT} fault (alternatively called a cutoff current timeout, with symbol t_{CUT}) has occurred on the port.
5	t_{START_x}	t_{START} fault event bit	
		1:	The port is shut down at the end of the t_{START} interval due to an overload, which is in turn indicated by Pgood not being true at the end of t_{START}.
4	dis_x	Disconnect event bit	
		1:	The (already turned ON) port has been disconnected due to missing an MPS (Maintain Power Signature) test.
3	cls_x	Classification complete event bit	
		1:	One Classification cycle for the corresponding port has completed. Note: In Semi-auto mode, when this bit read as logical one, this indicates that the Class Status bitfield in the Port Status registers (**statp**_**x**) are valid.
2	det_x	Detection complete event bit	
		1:	One Detection cycle for the corresponding port has completed. Note: In Semi-auto mode, when this bit read as logical one, this indicates that the Detect Status bitfield in the Port Status registers (**statp**_**x**) are valid.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x10, 0x20, 0x30, 0x40	evnp_x	RO	1, 2, 3, 4	t_{LIM_x}	t_{CUT_x}	t_{START_x}	dis_x	cls_x	det_x	pwrgd_x	pwrena_x	0000 0000
Bit	**Name**	**Function**										
1	pwrgd_x	Power Good event bit.										
		1:	The port's Power Good status bit (Bit 1 in the **powerstatp_x** register) has changed.									
0	pwrena_x	Power Enabled event bit.										
		1:	The port's Power Enable status bit (Bit 0 in the **powerstatp_x** register) has changed.									

4.2.5.2. Status Register (statp_x; 0x12, 0x22, 0x32, 0x42)

This Register is Read only.

Detection and classification status are reported in this register. The encoding is listed in Table 9.

The "detect_$x_{[2:0]}$" bit field shows the detection status and similarly the "class_$x_{[2:0]}$" bit field shows the classification status.

Table 10. Classification and Detection Encoding

Code	Class Status	Detection Status
000b	Unknown—POR value and also value after a port is disconnected.	Unknown—POR value and also value after a port is disconnected.
001b	Class 1	Short circuit
010b	Class 2	Capacitive[1]
011b	Class 3	Rlow
100b	Class 4	Rgood
101b	Reserved	Rhigh
110b	Class 0	Open circuit
111b	Over current	PSE to PSE[2]

Notes:
1. Capacitive status is reported when the load capacitance is bigger than 0.5 µF (Cpd > 0.5 µF).
2. The Si3454 is capable of detecting whether it is cross-connected to another PSE controller of a different type. In this case, the PSE to PSE Status is reported. Detection of another PSE is based on verifying the voltage level on the output (DRAINn pin) during the detection cycle.

In Semi-Auto and Auto modes, the classification process is not initiated unless Rgood is reported. In this case, the classification status can be unknown, or it can be the last classification status after the last Rgood.

4.2.5.3. Power Status Register (pwrstatp_x; 0x13, 0x23, 0x33, 0x43)

This Register is Read only.

Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x13, 0x23, 0x33, 0x43	pwrstatp_x	RO	1, 2, 3, 4	Reserved	type2flt_x[2:0]			fetbad_x	pongpd_x	pg_x	pe_x	0000 0000

Bit	Name	Function	
7	Reserved		
6:4	type2flt_x[2:0]	Detection and classification extended status (see the table below for the encoding).	
3	fetbad_x	External MOSFET failure event bit.	
		0:	The detection process found the external MOSFET operating correctly.
		1:	The detection process found the external MOSFET is possibly damaged.
2	pongpd_x	Type 2 classification status.	
		0:	Either not Type 2 PD, or the 2-event classification was not successful.
		1:	2-event classification has occurred.
1	pg_x	Power Good status.	
		0:	The voltage on the DRAINx pin is >2 V of AGND; due to an overload or if the port is turned off for any reason.
		1:	The voltage on the DRAINx pin is within ~2 V of AGND, i.e.: the port voltage is almost equal to VPWR (within 2 V).
0	pe_x	Power Enable status.	
		0:	The port is turned off for any reason (overload, disconnect, or pushbutton).
		1:	The port is powered.

Further details for type2flt_x bitfield encoding are described in Table 11.

Table 11. type2flt_x Bitfield Encoding

Code	Det/Cls Status
000	unknown
001	Detect and 2-event classification was successful
010	Invalid detection
011	Classification overcurrent
100	2-event classification current mismatch

4.2.5.4. Configuration Register (confp_x; 0x14, 0x24, 0x34, 0x44)

This register controls the Port configuration including its operation mode.

Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x14, 0x24, 0x34, 0x44	confp_x	R/W	1, 2, 3, 4	legen_x	midsp_x	disena_x	priority_x	classena_x	detena_x	opmd_x[1:0]		0000 0000

Bit	Name	Function	
7	legen_x	Legacy PD detection enable	
		0:	Only IEEE standard 802.3at-compliant PD signatures are recognized during detection
		1:	The detection status of a PD with large common-mode capacitance is reported as valid (code 100b in the **stat-p_x** register). Note that this behavior does not comply with the IEEE standard while this bit is set because the IEEE standard specifically declares these legacy PDs to be invalid.
6	midsp_x	midspan functionality support enable	
		Controls the lenght of the delay after each detection cycle before initiating the next detection cycle	
		0:	back off delay = ~400ms
		1:	back off delay > 2s
5	disena_x	DC disconnect enable	
		0:	no active monitoring for the disconnection of a PD
		1:	active monitoring for the disconnection of a PD
4	priority_x	Port shutdown priority when the SHDN pin is asserted	
		If there is a minimum 5 µs low pulse on pin 36 (SHDN), then any port with the priority bit set to 1 (low priority) will be shut down if it is ON (previously OFF ports are unaffected). This action is equivalent to a pushbutton power off as it is described in paragraph 3.2.2.3, point 1 A high priority port or a port that is not turned on is unaffected by SHDN. Port turn off is enforced for any port with the priority bit set to 1 (low priority) as long as SHDN is asserted. When SHDN is de-asserted, port configuration remains intact; however, detect and classify control bits were cleared during the SHDN assertion, and thus must be re-enabled.	
		0:	The port's priority is High
		1:	The port's priority is Low

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x14, 0x24, 0x34, 0x44	confp_x	R/W	1, 2, 3, 4	legen_x	midsp_x	disena_x	priority_x	classena_x	detena_x	opmd_x[1:0]		0000 0000

Bit	Name	Function	
3	classena_x	Classification enable	
		This bit has effect only in the Auto and semi-Auto modes. It enables repeated classification, to be performed on the port. If the port is turned on, then classification will not be attempted. If this bit is set, the port automatically performs and repeats the classification cycle following the successful detection cycles. In Auto-mode, the port will turn on after a successful detection if classification is not enabled. Each time a classification cycle is completed, the result is indicated in the status register (statp_x; addresses 0x12, 0x22, 0x32, 0x42 for ports 1–4, respectively). Each classification cycle consists either one or two pulses, depending on the state of the corresponding 'pongen_x' bit (tlimp_x; registers 0x15, 0x25, 0x35 and 0x45 for ports 1–4, respectively) at the time the classification cycle is initiated: • If pongen=1 the classification cycle consists of one or two pulses in accordance with the IEEE 802.3at requirements for a Type 2 PSE; the second pulse occurs if the PD presented a class 4 signature during the first pulse. • If pongen=0 the classification cycle consists of one pulse in accordance with the IEEE 802.3at requirements for a Type 1 PSE. Note: a Type 1 PSE is equivalent to a PSE built to the original IEEE 802.3af spec. When a port is in Auto mode the ICUT and ILIM are set automatically after the port successfully powers up. The levels for ICUT and ILIM depend on the class of the PD as shown in Table 11. This bit will also be set if the Classification pushbutton bit is set.	
		0:	Continuous classification is disabled
		1:	Continuous classification is enabled
2	detena_x	Detection enable	
		This bit has effect only in the Auto and semi-Auto modes. It enables repeated detection, to be performed on the port. If the port is turned on, then detection will not be attempted. If this bit is set, the port automatically performs and repeats the detection cycle. In Auto-mode, the port will turn on after a successful detection, even if classification is not enabled. Each time a detection cycle is completed, the result is indicated in the status register (statp_x; addresses 0x12, 0x22, 0x32, 0x42 for ports 1–4, respectively). This bit will also be set if the detection pushbutton bit is set.	
		0:	Continuous detection is disabled
		1:	Continuous detection is enabled
1:0	opmd_x[1:0]	Port operation mode configuration	
		This bitfield sets the operation mode of the port. Any time a port is set to Shutdown or Manual mode, the detect and classification enable bits in this register are reset. In shutdown mode, the pushbuttons will not result in an action. Putting a port in Shutdown mode clears the port status registers.	
		00:	Shutdown
		01:	Manual
		10:	Semi-Auto
		11:	Auto

4.2.5.5. Current Limit Register (tlimp_x; 0x15, 0x25, 0x35, 0x45)

Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x15, 0x25, 0x35, 0x45	tlimp_x	R/W	1, 2, 3, 4	Reserved	hpen_x	pongen_x	Reserved	t_{LIM_x}[3:0]				0000 0000

Bit	Name	Function	
7	Reserved		
6	hpen_x	High Power Enable	
		This bit controls the current limit and foldback setting for the port	
		0:	The I_{LIM} threshold is 425 mA ± 5%.
		1:	The I_{LIM} threshold is 850 mA ± 5%.
5	pongen_x	2-event calssification enable.	
		0:	The classification cycle consists of one pulse in accordance with the IEEE 802.3at requirements for a Type 1 PSE.
		1:	The classification cycle consists of one or two pulses in accordance with the IEEE 802.3at requirements for a Type 2 PSE; the second pulse occurs if the PD presented a class 4 signature during the first pulse.
4	Reserved		
3:0	t_{LIM_x}[3:0]	Current limit time	
		The T_{lim} Timer duration is 1.71 ms (typ) times the value of 't_{LIM_x}[3:0]' bitfield, rounded to the nearest msec. Possible returned values in this register are: 0, 2, 3, 5, 7, 9, 10, 12, 14, 15, 17, 19, 21, 22, 24 26. When this field is written to 0, the T_{lim} timer is disabled, and the T_{cut} timer limits the duration of overloads to 60 ms.	

4.2.5.6. Cutoff Current Register (icutp_x; 0x16, 0x26, 0x36, 0x46)

This register controls the cutoff current threshold (I_{CUT}) on the port.

Bit 6 "cutrng_x" controls the cutoff current scaling.

Bits 5:0 ("t_{cut_x}[5:0]") set the I_{CUT}. The conversion scale is: 37.5 mA/count when cutrng = 0; 18.75 mA/count when cutrng = 1.

4.2.5.7. Pushbutton Register (pb_p_x; 0x17, 0x27, 0x37, 0x47)

This Register is Write only.

Additional details can be found in the register description below.

Register		R/W	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
Addr	Name											Auto Tied to DGND
0x17, 0x27, 0x37, 0x47	pb_p_x	WO	1, 2, 3, 4	Reserved	Reserved	Reserved	rst_x	cls_x	det_x	off_x	on_x	0000 0000

Bit	Name	Function	
7	Reserved		
6	Reserved		
5	Reserved		
4	rst_x	Reset the port	
		1:	Resets the port to the shutdown state, and all associated events and configurations are cleared. Please refer to Step 2 in “3.2.2.3. HOST Controlled Port Turn OFF” for further details
3	cls_x	Turn on classification	
		1:	Provide a single classification cycle in manual mode. If it is used in semi-auto mode, then the “classena_x” bit of the **confp_x** register will automatically be set (i.e. this action will turn on repeated classification for the port).
2	det_x	Turn on detection	
		1:	Provide a single detection cycle in manual mode. If it is used in semi-auto mode, then the “detena_x” bit of the **confp_x** register will automatically be set (i.e. this action will turn on repeated detection for the port).
1	off_x	Turn off the port	
		1:	Please refer to Step 1 in “3.2.2.3. HOST Controlled Port Turn OFF” for further details
0	on_x	Turn on the port	
		1:	Please refer to “3.2.2.1. HOST Controlled Port Turn ON” for further details

4.2.6. Port-Specific Parametric Measurements Registers

These registers provide real time port voltage, current and detection resistance measurements.

4.2.6.1. Port Current and Voltage (0x19-0x1C, 0x29-0x2C, 0x39-0x3C, 0x49-0x4C)

Once a channel is powered on, port voltage and port current can be accessed via registers 0x19 through 0x1C (using port 1 as an example). These registers do not give valid information for a port that is off. Each measurement of voltage is the average of 16 consecutive 10-bit samples taken at 3 ms intervals. Port current is updated once per 100 ms, and the update is the average of all (up to 400) samples taken in the prior 100 ms interval.

The voltage and current measurements are 16-bit words, divided into two bytes: the Most Significant Byte (MSB) contains the upper 8 bits; and the Least Significant Byte (LSB) contains the lower 8 bits. Reading the lower byte latches the upper byte to assure they are both from the same sample; therefore, the lower byte should always be read first. After concatenating the upper and lower bytes, the following conversion factors are used to derive the meaning of the readings: for current measurements multiply by 122.07 µA/count; and, for voltage measurements, multiply by 5.835 mV/count.

4.2.6.2. Port Detection Resistance (detresp_x; 0x1D, 0x2D, 0x3D, 0x4D)

This register contains an approximate resistance value (in kOhm), measured during the rising voltage period of the detection cycle.

4.2.6.3. VPWR Voltage (0x07, 0x08)

VPWR voltage can be accessed via registers 0x07 and 0x08. The voltage measurement are 16-bit words, divided into two bytes: the Most Significant Byte (MSB, register 0x08) contains the upper 8 bits; and the Least Significant Byte (LSB, register 0x07) contains the lower 8 bits. Reading the lower byte latches the upper byte until it is read, to assure they are both from the same sample; therefore, the lower byte should always be read first. After concatenating the upper and lower bytes multiply by 5.835 mV/count to obtain the VPWR voltage.

4.2.6.4. Supply Event and Supply Event CoR (0x0A, 0x0B)

When there is a leaky FET on any port, bit6 will be set. It will remain set until specifically cleared with a CoR. The leaky FET test is performed at the start of a detection cycle. See the “Bad FET Measurement” parameter in Table 1 for test limits.

The event register, 0x0A, indicates a VDD or VPWR supply fault or over-temperature event. The supply event's bits are latched until cleared, but only “good” to “bad” transitions are reported.

VDD UVLO: set if VDD goes below 2.8 V (TYP). All ports are powered down when this event occurs.
Note: Measured values, such as temperature, port voltages, and currents, are inaccurate if VDD<2.6 V.

In the event of thermal shutdown, the Overtemp bit is set until CoR occurs. Content of register 0x0B is identical to that of 0x0A, however, if 0x0B is read, both registers will clear momentarily. The register bits are set again every few milliseconds if the fault is still present.

5. Pin Descriptions

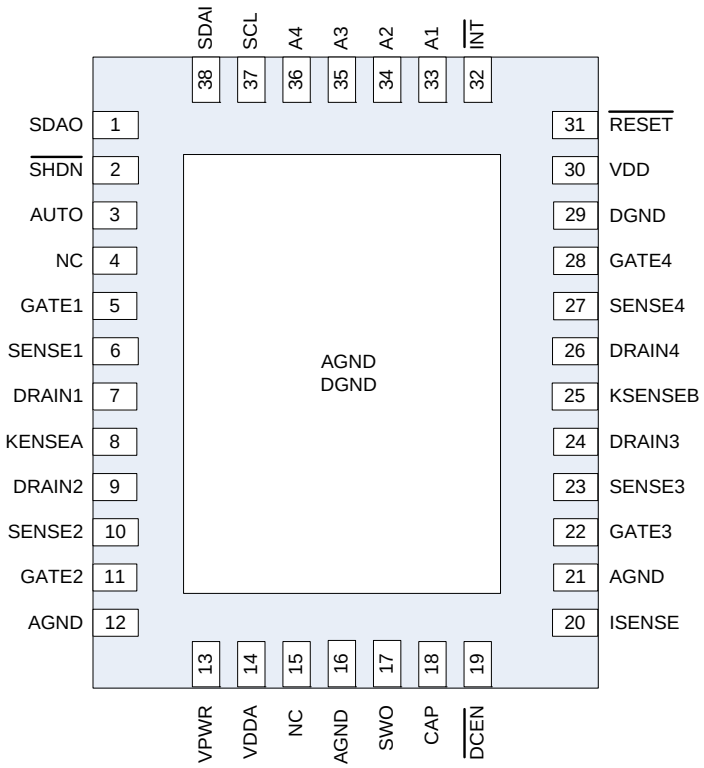


Table 12. Pin Descriptions

Pin #	Name	Type	Description
1	SDAO	Digital output (open drain)	Serial data output. This open drain output pin is intended to drive data isolators directly. Tie SDAO and SDAI together if a 2-wire version of the I^2C bus is available.
2	$\overline{\text{SHDN}}$	Digital input with 25 µA pull-up to VDD	This signal, when driven low, will initiate a shutdown of low-priority ports. **Note:** When the chip is in Auto mode, this pin should be left unconnected.
3	AUTO	Analog input with 25 µA pull-up to VDD	Tie to DGND for Manual or Semi-Auto Mode, or leave floating or tied to VDD for default Auto Mode. This pin can also be resistor programmed for other startup configurations.
4, 15	NC	No Connect	No connections or nets allowed. Leave floating.
5 11 22 28	GATE1 GATE2 GATE3 GATE4	Analog output	Gate drive outputs to external MOSFETs. Connect the GATEn outputs to the external MOSFET gate node gate. A 50 µA pull-up source is used to turn on the external MOSFET. When a current limit is detected, the GATEn voltage is reduced to maintain constant current through the external MOSFET. If the fault timer limit is reached, GATEn pulls down, shutting off the external MOSFET. GATEn will clamp to 11.5 V (typical) above AGND. If the port is unused, leave the GATEn pin disconnected or tie to AGND.

Table 12. Pin Descriptions (Continued)

Pin #	Name	Type	Description
6 10 23 27	SENSE1 SENSE2 SENSE3 SENSE4	Analog input	Current sense inputs for external MOSFETs. The SENSEn pin measures current through an external 0.25 Ω resistor tied between the AGND supply rail and the SENSEn input. If the I_{CUT} limit (the overcurrent limit) is exceeded, the current limit fault timer is incremented. If the voltage across the sense resistor subsequently triggers (the overcurrent limit), the voltage driven onto the GATEn pin is modulated to provide constant current through the external MOSFET. Tie the SENSEn pin to AGND when the port is not used. To accommodate 802.3at (PoE Plus) classification, both the I_{CUT} and Ilim values can be scaled.
7 9 24 26	DRAIN1 DRAIN2 DRAIN3 DRAIN4	Analog input with 25 µA pull-up to VPWR	MOSFET drain output voltage sense. The Power Good bit is set on each port when the voltage between DRAINn and AGND drops below 2 V (typical). DRAINn pins should be left floating if the port is unused.
8	KSENSA	Input	Kelvin points for accurate measurement of voltage across 0.25 Ω sense resistor for ports 1 and 2.
12, 16, 21, ePAD	AGND	Analog ground	Ground connection for VPWR supply. DGND and AGND are tied together inside the Si3454 package
13	VPWR	Analog power	Positive PoE voltage (+44 to +56 V) relative to AGND.
14	VDDA	Analog power	3.3 V supply to the analog side; tied with VDD at the PCB level.
17	SWO	Output	Gate driver output for the external MOSFET component of the dc-dc converter. If using only the local regulator of the part, tie SWO to VPWR. If not using the dc-dc converter or local regulator, leave this pin floating.
18	CAP	Input	Input from the dc-dc converter. This elevated voltage can be bussed to up to five additional Si3454s or Si3459s where it will be down-regulated to VDD for local use.
19	$\overline{\text{DCEN}}$	Digital input with 25 µA pull-up to VDD	Tie DCEN to DGND to enable the dc-dc converter and local regulator. If using only the local regulator of the part, DCEN must also be tied to DGND. If not using the dc-dc converter or local regulator, leave this pin floating.
20	ISENSE	Input	Current sense input for dc-dc converter to detect overcurrent and short circuit conditions.
25	KSENSB	Input	Kelvin points for accurate measurement of voltage across 0.25 Ω sense resistor for ports 3 and 4.
29, ePAD	DGND	Digital ground	Ground connection for 3.3 V digital supply (VDD). DGND and AGND are tied together inside the Si3454 package.

Table 12. Pin Descriptions (Continued)

Pin #	Name	Type	Description
30	VDD	Digital power	3.3 V digital supply (relative to DGND). Bypass VDD with a 0.1 µF capacitor to DGND as close as possible to the Si3454 power supply pins; tied with VDDA.
31	$\overline{\text{RESET}}$	Digital input with 25 µA pull-up to VDD	Active low device reset input. Generally, RESET is used at initial power up. If RESET is asserted (pulled to DGND), the MCU is disabled, all internal registers of the device are set to their default (power-up) state, and all output ports are shut off. Valid RESET timing pulses must be >10 µs. If RESET is not used, RESET should either be tied directly to VDD or through a 10 kΩ resistor to VDD.
32	$\overline{\text{INT}}$	Digital output (open drain)	Interrupt output. This open drain output pin is asserted low (to DGND) if a fault condition occurs on any of the four ports. The state of $\overline{\text{INT}}$ is updated for use by the host controller between valid I^2C commands. **Note:** When the chip is in Auto mode, this pin should be left unconnected.
33 34 35 36	A0 A1 A2 A3	Digital input with 25 µA pull-up to VDD	I^2C address input. Used to set the base I2C address for the Si3454 in the following (binary) format: 010[A3][A2][A1][A0]. The three MSB bits of the address are set to 010. Address values are latched after the deassertion of RESETB or when VDD ramps and VPWR exceeds the UVLO threshold voltage. Each address pin should be floating (internal pull-up pulls high) or tied to either VDD or DGND.
37	SCL	Digital input	Serial clock input. Should be tied directly to the SCL (clock) connection on the I^2C bus.
38	SDAI	Digital input with 25 µA pull-up to VDD	Serial data input. Tie SDAO and SDAI together if a two-wire version of the I^2C bus is available.

6. Ordering Guide

Ordering Part Number*	Product Revision	Firmware Revision	Firmware Revision Notes	Package	Temperature Range (Ambient)
Si3454-B01-IM	B	1.2	See "10. Firmware Revision Release Notes" on page 55.	38-pin QFN RoHS-compliant	–40 to 85 °C
***Note:** Add an “R” to the end of the part number for tape and reel option (e.g., Si3454-B01-IM or Si3454-B01-IMR).					

7. Package Outline

Figure 13 illustrates the package details for the Si3454. Table 13 lists the values for the dimensions shown in the illustration. The Si3454 is packaged in an industry-standard, RoHS-compliant, 38-pin QFN package. The lead plating material is matte tin.

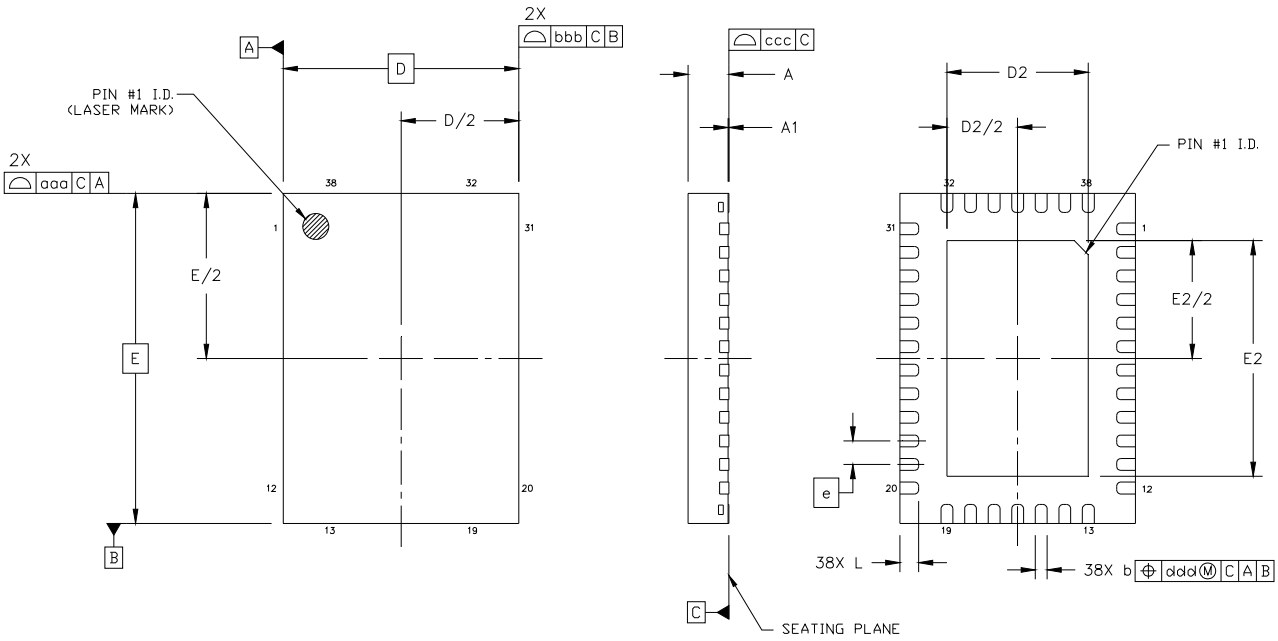


Figure 13. Package Drawing

Table 13. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC.	
D2	2.90	3.00	3.10
e		0.50 BSC.	
E		7.00 BSC.	
E2	4.90	5.00	5.10
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Recommended Land Pattern

Figure 14 illustrates the land pattern details for the Si3454. Table 14 lists the values for the dimensions shown in the illustration.

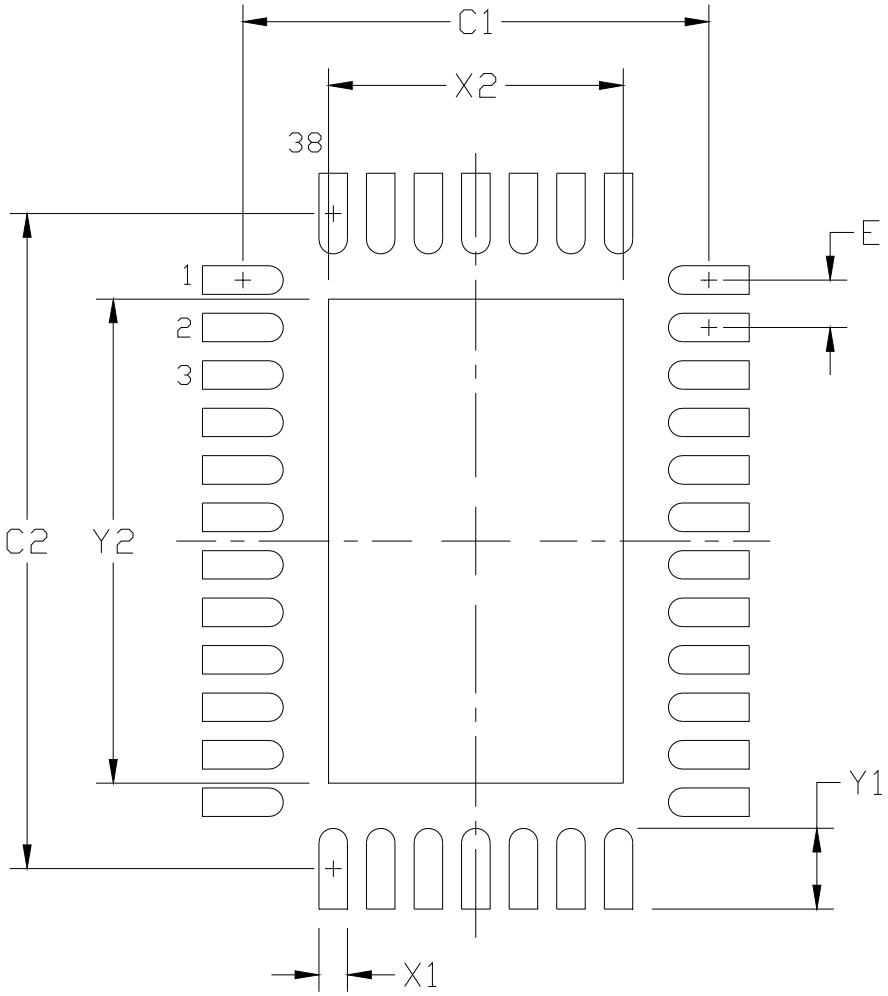


Figure 14. Si3454 Recommended Land Pattern

Table 14. PCB Land Pattern Dimensions

Symbol	mm
C1	4.90
C2	6.90
E	0.50
X1	0.30
Y1	0.85
X2	3.10
Y2	5.10

Notes:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

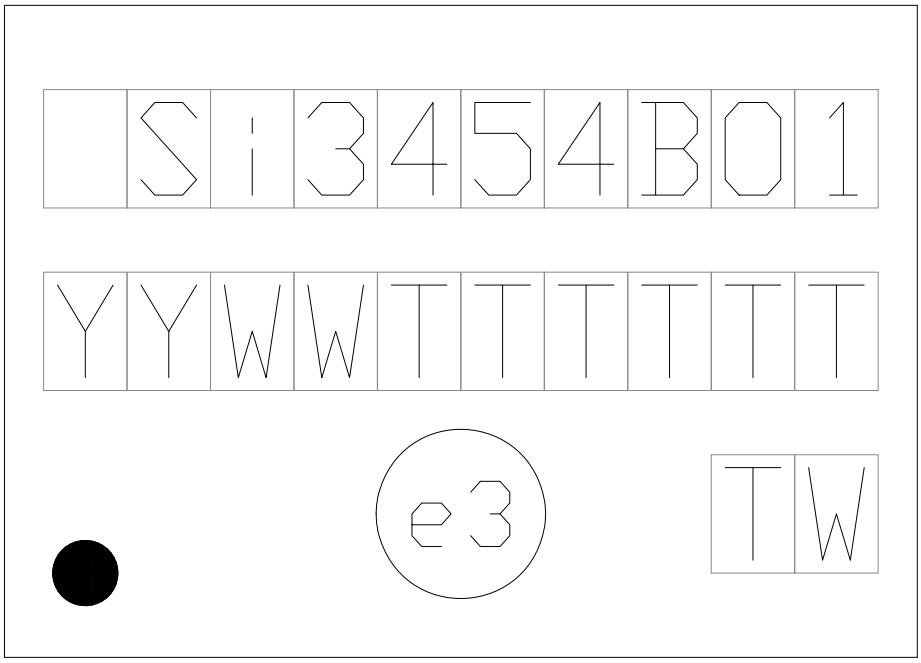
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
7. A 4x2 array of 1.0 mm square openings on 1.3 mm pitch should be used for the center ground pad to achieve a target of ~50% solder coverage.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Marking

9.1. Si3454 Top Marking (QFN)



9.2. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Bottom-Left-Justified	
Line 1 Mark Format:	Device Part Number	Si3454B01
Line 2 Mark Format:	YY = Year WW = Work Week TTTTTT = Mfg Code	Year and Work Week of Assembly Manufacturing Code
Line 3 Mark Format:	Circle = 1.3 mm Diameter Country of Origin	“e3” Pb-Free Symbol TW = Taiwan

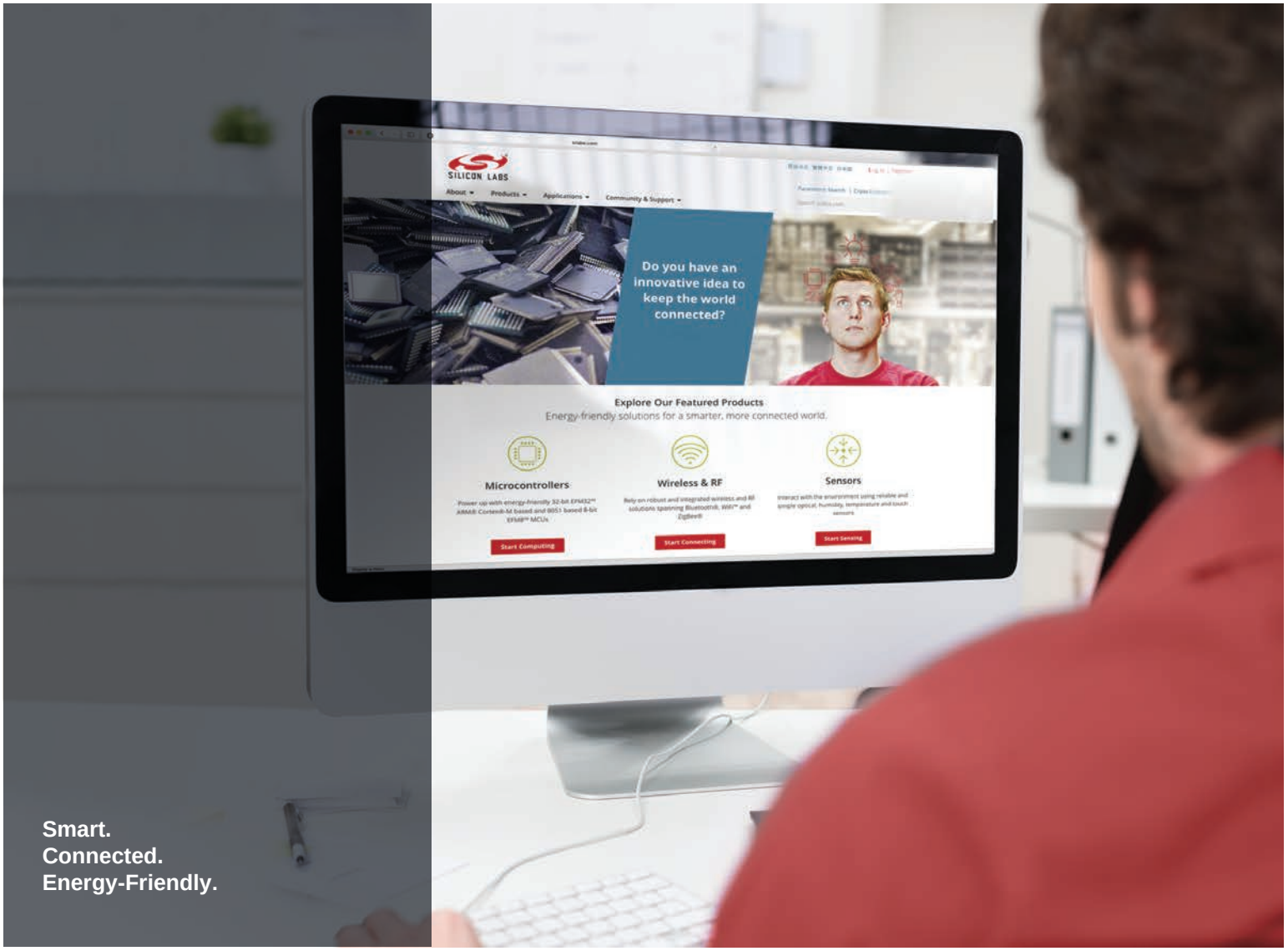
10. Firmware Revision Release Notes

- Initial release

Document Change List

Revision 1.0 to Revision 1.1

- Updated Table 1 to reduce minimum voltage on “Voltage Difference Between any GATEn and AGND Pin” and to increase maximum current on Bad FET Measurement IPORTn parameters.
- Updated Table 2 to expand Regulator Output Voltage Mix and Max slightly.
- Updated Table 3 to increase Input Leakage IIH Max by 1 µA.
- Updated icutp_x register default values in Table 8 on page 19.
- Updated the default value (reset state; Auto tied to DGND) of the icutp_x registers (0x16, 0x26, 0x36, 0x46) to 0101 0100.



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