Si2165

Multi-Standard DVB-T and DVB-C Demodulator

Description

The Si2165 is a compact standalone DVB-T/C digital TV demodulator ideally matching Silicon Labs' Si2170/1/2 new hybrid high-performance silicon tuner product family. The analog front-end consists of two ADCs with wide dynamic range (12-bit) to allow operation with standard IF (~36 MHz), Low-IF, or Zero-IF inputs. This enables the use of the Si2165 with any TV tuner, either metal can or silicon tuner based.

The multi-standard demodulator supports all modes of DVB-T (EN 300 744), including hierarchical modes. The Si2165 also supports ITU J.83 annex A/C and DVB-C (EN 300 429), including a user-configurable 31-tap equalizer. In addition to DVB-T's legacy modes, the Si2165 also complies with DVB-H (EN 300 744 Annex F) specificities: 4K FFT, extended TPS, "native" and "in-depth" deinterleavers. The Si2165 is able to receive DVB-H programs in fixed receiver applications (without decoding the additional MPE FEC layer).

An embedded 32-bit DSP controls device operation. Sophisticated on-chip algorithms ensure optimum reception even under difficult channel conditions, such as echoes outside the guard interval, pre-echoes, or strong impulse noise. For ease-of-use, DSP firmware is preloaded into ROM (device is immediately active at powerup). Nevertheless, there is a possibility of downloading additional patch code via the I^2C interface (e.g., to adjust the demodulator to unexpected conditions or reception impairments).

Thanks to proprietary features, the Si2165 supports ultra-fast channel scanning for VHF/UHF terrestrial and cable DTV channels. For supported tuners, the Quickscan algorithm for blindscan is running onto the embedded DSP (in order to limit the host CPU load) and is provided as a downloadable patch file.

Serial or parallel master MPEG TS output modes are supported. Furthermore, a TS slave parallel mode is available via a GPIF port and provides a glueless interface to Silicon Labs' MCU devices with embedded USB interface. The user can optionally program a 32-PID hardware filter to reduce the output TS bit rate.

An internal I^2C pass-through logic switch acts as an I^2C repeater. This provides a "quiet" I^2C bus to the RF front end.

A maximum of six general-purpose inputs/outputs are available; three GPIOs also feature Δ/Σ and interrupt output capabilities.

Best-in-class demodulation performance is achieved while still maintaining very low-power operation.

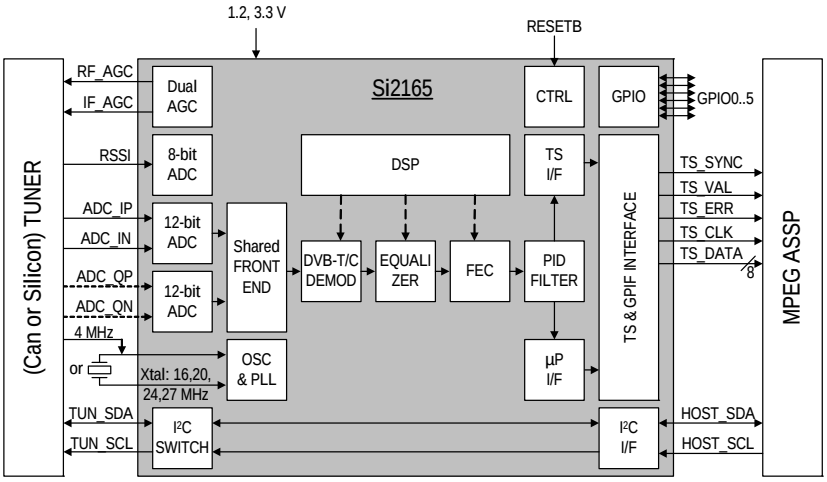
The Si2165 guarantees a low-cost system implementation due to its minimal BOM and very small package footprint.

Features

- DVB-T (ETSI EN 300 744) demodulator & FEC decoder
- ITU J.83 Annex A/C and DVB-C (EN 300 429) compliant demodulator & FEC decoder
- NorDig Unified 2.0, D-Book & C-Book 4.0 compliant
- Suitable for low power design: 140 mW (typical, 36 MHz IF sampling mode)
- Dual 12-bit ADCs: accept 1st IF, low IF, or zero-IF inputs
- DVB-T channel bandwidth: 5, 6, 7, 8 MHz
- DVB-C symbol rate: 1 to 7.2 MBaud
- DSP-based synchronization and control with embedded ROM code avoids need for code download at startup
- Supports patch code downloads for in-field upgradeability
- Independent AGC controls (for IF & RF), plus RSSI measurement
- ACI filtering: fixed 8 MHz SAW filter even for 7 MHz channel
- Advanced performance for SFN networks
- Impulsive noise protection algorithm
- Ultra fast automatic UHF/VHF band scanning (QuickScan)
- Master TS output modes, parallel or serial (with tri-state function)
- Slave TS parallel output: external device polls data from an embedded FIFO, providing a seamless interface to any USB controller.
- On-chip PID filtering to reduce TS output bit rate.
- Up to six GPIOs
- Two 5 V tolerant I^2C control buses (host-side, tuner-side) with on-chip I^2C repeater
- 4, 16, 20, 24, or 27 MHz clock/crystal reference
- 3.3 and 1.2 V power supplies only
- Very compact QFN-36, 5 x 6 mm, RoHS compliant package

Applications

- Digital terrestrial and cable STB, NIM, and iDTV set
- Personal Video Recorder (DVD or HDD-based)
- Digital terrestrial and cable PC-TV tuner peripheral

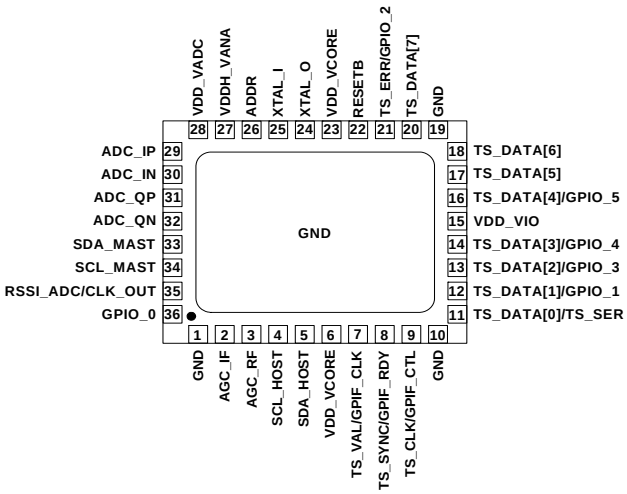


Selected Electrical Specifications

Parameter	Min	Typ	Max	Unit
General				
Ambient Temperature	0	25	85	°C
Power-up Time	—	—	10	ms
I^2C Speed (Host side)	<1	—	400	kHz
Input Clock or Supported Xtal Frequency	—	4[1]/16/20/24/27	—	MHz
VDD_VCORE Supply	1.14	1.20	1.26	V
VDD_VIO Supply[2]	1.62	1.80 to 3.30	3.60	V
VDD_VADC Supply	1.14	1.20	1.26	V
VDDH_VANA Supply	3.00	3.30	3.60	V
Input ADC (2 x 12-bits)				
Input Differential Voltage Range	—	1	—	Vpp
ZIF Mode Sampling Clock	18.5	48	60	MHz
IF Sub-sampling Mode Clock	18.5	27	32.5	MHz
IF Over-sampling Mode Clock	37	48	60	MHz
System Clock	—	—	85	MHz
TS Output Rates				
Serial Mode Clock (DVB-T or DVB-C Mode)	—	—	65	MHz
Power Consumption				
DVB-T 8 MHz, IF Mode (adc_clk@56 MHz), Parallel TS	—	140	—	mW
DVB-C, IF Mode, SR = 6.9 MBaud , 256 QAM (adc_clk@56 MHz), Parallel TS	—	120	—	mW
Total Stand-by Power Consumption	—	13	—	mW

Notes:
1. Clock only.
2. 5 V tolerant I^2C bus requires VDD_VIO supply set @ 3.3 V.

Pin Assignments



5 x 6 mm SLP QFN-36 Package Information