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32

SH7032, SH7034
Hardware Manual

Renesas 32-Bit RISC Microcomputer
SuperH™ RISC engine Family/SH7030 Series

SH7032	HD6417032
SH7034	HD6477034
	HD6437034
	HD6417034
SH7034B	HD6437034B
	HD6417034B

Hardware Manual

Rev. 7.00
Revision Date: Jan 31, 2006

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Preface

The SH7032 and SH7034 are microprocessors that integrate peripheral functions necessary for system configuration with a 32-bit internal architecture SH1-DSP CPU as its core.

The SH7032 and SH7034's on-chip peripheral functions include an interrupt controller, timers, serial communication interfaces, a user break controller (UBC), a bus state controller (BSC), a direct memory access controller (DMAC), and I/O ports, making it ideal for use as a microcomputer in electronic devices that require high speed together with low power consumption.

Intended Readership: This manual is intended for users undertaking the design of an application system using the SH7032 and SH7034. Readers using this manual require a basic knowledge of electrical circuits, logic circuits, and microcomputers.

Purpose: The purpose of this manual is to give users an understanding of the hardware functions and electrical characteristics of the SH7032 and SH7034. Details of execution instructions can be found in the SH-1, SH-2, SH-DSP Software Manual, which should be read in conjunction with the present manual.

Using this Manual:

- For an overall understanding of the SH7032 and SH7034's functions
  Follow the Table of Contents. This manual is broadly divided into sections on the CPU, system control functions, peripheral functions, and electrical characteristics.
- For a detailed understanding of CPU functions
  Refer to the separate publication SH-1, SH-2, SH-DSP Software Manual.
  Note on bit notation: Bits are shown in high-to-low order from left to right.

Related Material: The latest information is available at our Web Site. Please make sure that you have the most up-to-date information available.
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User's Manuals on the SH7032 and SH7034:

Manual Title	Document No.
SH7032 and SH7034 Hardware Manual	This manual
SH-1, SH-2, SH-DSP Software Manual	REJ09B0171-0500

Users manuals for development tools:

Manual Title	Document No.
C/C++ Complier, Assembler, Optimized Linkage Editor User's Manual	REJ10B0152-0101
Simulator Debugger Users Manual	REJ10B0210-0200
High-performance Embedded Workshop Users Manual	REJ10J0886-0300

Application Note:

Manual Title	Document No.
C/C++ Complier	REJ05B0463-0300

Organization of This Manual

Table 1 describes how this manual is organized. Figure 1 shows the relationships between the sections within this manual.

Table 1 Manual Organization

Category	Section Title		Abbreviation	Contents
Overview	1.	Overview	—	Features, internal block diagram, pin layout, pin functions
CPU	2.	CPU	CPU	Register configuration, data structure. instruction features, instruction types, instruction lists
Operating Modes	3.	Operating Modes	—	MCU mode, PROM mode
Internal Modules	4.	Exception Handling	—	Resets, address errors, interrupts, trap instructions, illegal instructions
	5.	Interrupt Controller	INTC	NMI interrupts, user break interrupts, IRQ interrupts, on-chip module interrupts
	6.	User Break Controller	UBC	Break address and break bus cycle selection
Clock	7.	Clock Pulse Generator	CPG	Crystal pulse generator, duty correction circuit
Buses	8.	Bus State Controller	BSC	Division of memory space, DRAM interface, refresh, wait state control, parity control
	9.	Direct Memory Access Controller	DMAC	Auto request, external request, on-chip peripheral module request, cycle steal mode, burst mode
Timers	10.	16-Bit Integrated Timer Pulse Unit	ITU	Waveform output mode, input capture function, counter clear function, buffer operation, PWM mode, complementary PWM mode, reset synchronized mode, synchronized operation, phase counting mode, compare match output mode
	11.	Programmable Timing Pattern Controller	TPC	Compare match output triggers, non-overlap operation
	12.	Watchdog Timer	WDT	Watchdog timer mode, interval timer mode

Category	Section	Title	Abbreviation	Contents
Data Processing	13.	Serial Communication Interface	SCI	Asynchronous mode, synchronous mode, multiprocessor communication function
	14.	A/D Converter	A/D	Single mode, scan mode, activation by external trigger
Pins	15.	Pin Function Controller	PFC	Pin function selection
	16.	Parallel I/O Ports	I/O	I/O ports
Memory	17.	ROM	ROM	PROM mode, high-speed programming system
	18.	RAM	RAM	On-chip RAM
Power-Down State	19.	Power-Down State	—	Sleep mode, standby mode
Electrical Characteristics	20.	Electrical Characteristics	—	Absolute maximum ratings, AC characteristics, DC characteristics, operation timing

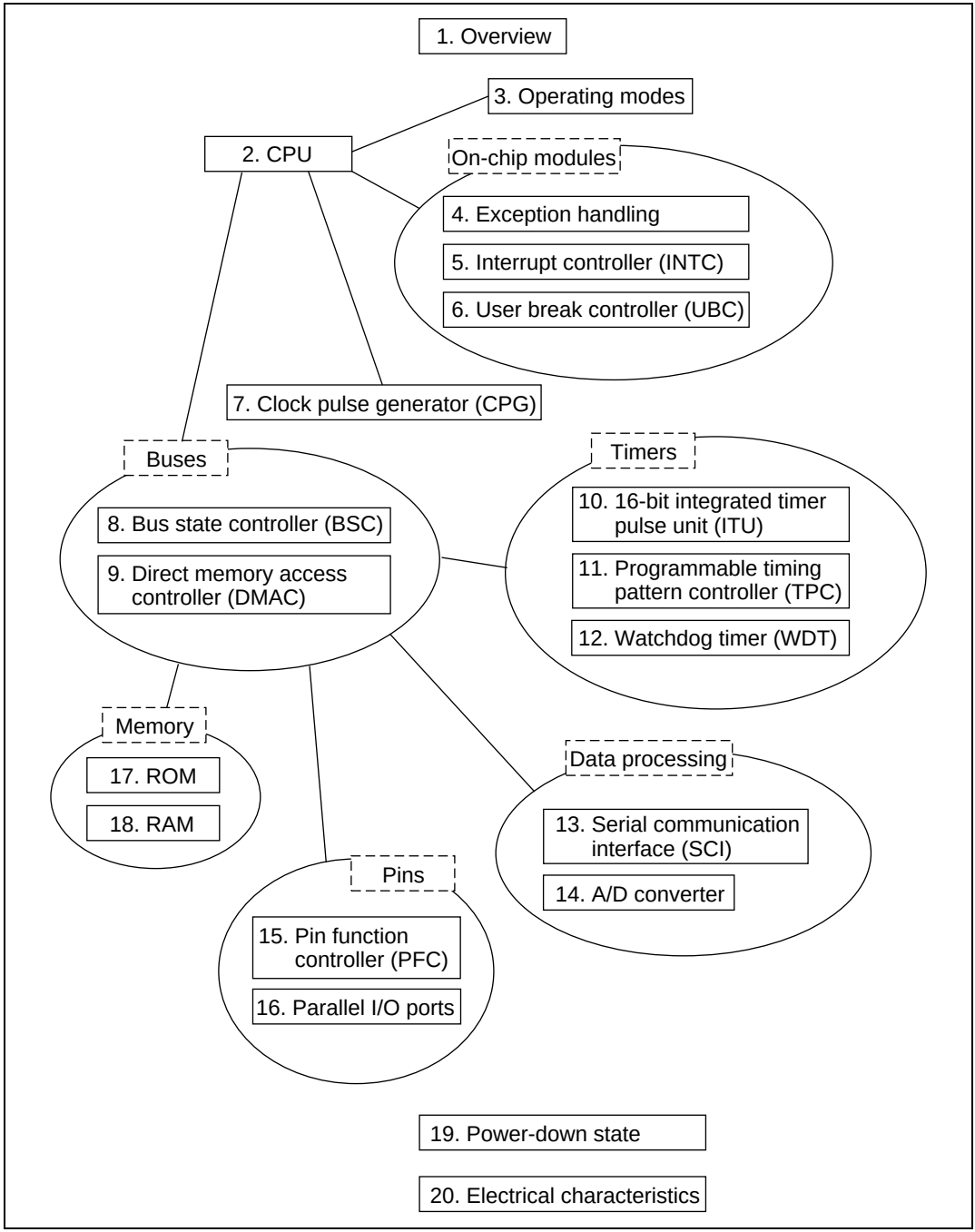


Figure 1 Manual Organization

Addresses of On-Chip Peripheral Module Registers

The on-chip peripheral module registers are located in the on-chip peripheral module space (area 5: H'5000000–H'5FFFFFF), but since the actual register space is only 512 bytes, address bits A23–A9 are ignored. 32k shadow areas in 512 byte units that contain exactly the same contents as the actual registers are thus provided in the on-chip peripheral module space.

In this manual, register addresses are specified as though the on-chip peripheral module registers were in the 512 bytes H'5FFFE00–H'5FFFFFF. Only the values of the A27–A24 and A8–A0 bits are valid; the A23–A9 bits are ignored. When area H'5000000–H'50001FF is accessed, for example, the result will be the same as when area H'5FFFE00–H'5FFFFFF is accessed. For more details, see Section 8.3.5, Area Descriptions: Area 5.

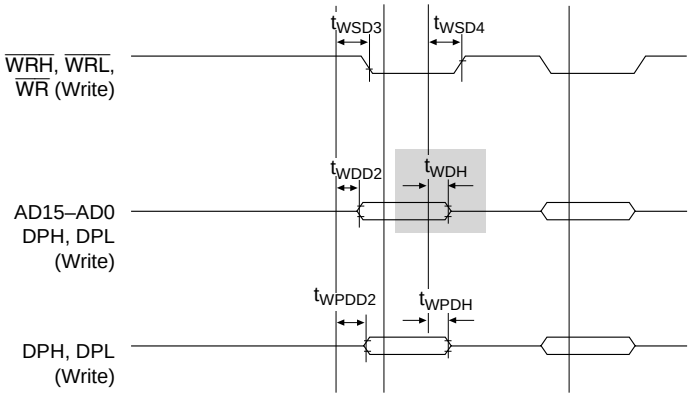
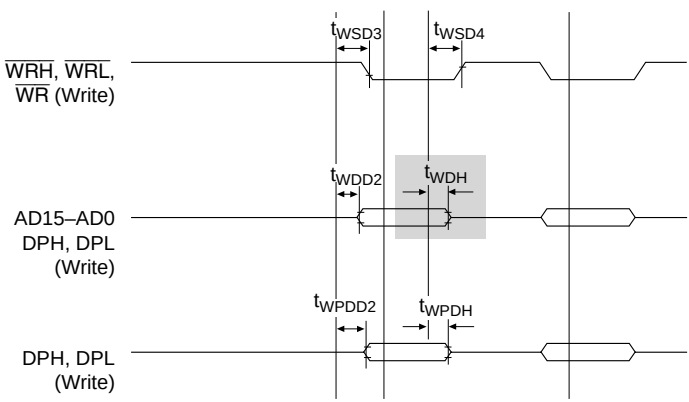
List of Items Revised or Added for This Version

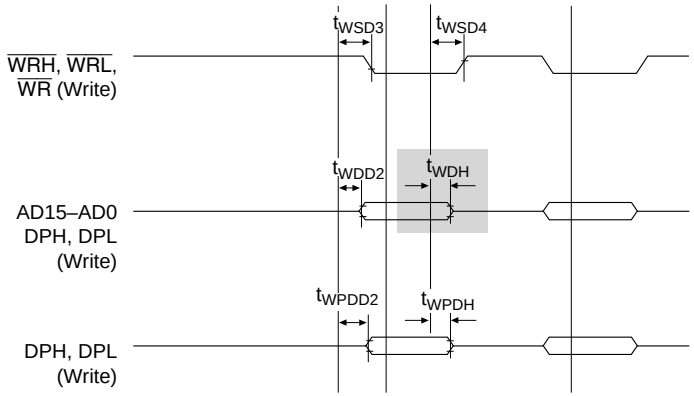
Item	Page	Revision (See Manual for Details)
All	—	• All references to Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names changed to Renesas Technology Corp. • Designation for categories changed from “series” to “group” • Changes due to change in package codes. FP-112 → PRQP0112JA-A FP-120 → PTQP0120LA-A
1.1 SuperH Microcomputer Features Table 1.2 Product Lineup	6	Table amended

Product Number	On-Chip ROM	Operating Voltage	Operating Frequency	Temperature Range	Model	Marking Model No.*2	Package
SH7032	ROMless	5.0 V	2 to 20 MHz	-20 to +75 C	HD6417032F20	HD6417032F20	112-pin plastic QFP (PRQP0112JA-A)
				-40 to +85 C	HD6417032FI20	HD6417032FI20	
		3.3 V	2 to 12.5 MHz	-20 to +75 C	HD6417032VF12	HD6417032VF12	
				-40 to +85 C	HD6417032VFI12	HD6417032VFI12	
SH7034	PROM	5.0 V	2 to 20 MHz	-20 to +75 C	HD6477034F20	HD6477034F20	112-pin plastic QFP (PRQP0112JA-A)
				-40 to +85 C	HD6477034FI20	HD6477034FI20	
		3.3 V	2 to12.5 MHz	-20 to +75 C	HD6477034VF12	HD6477034VF12	
		5.0 V	2 to 20 MHz	-20 to +75 C	HD6477034X20	HD6477034TE20	120-pin plastic TQFP (PTQP0120LA-A)

2.3.2 Addressing Modes Table 2.8 Addressing Modes and Effective Addresses	27	Table amended PC relative addressing added to Rn.
2.3.3 Instruction Formats Table 2.9 Instruction Formats	28	Table amended m format added to mmmm: PC relative using Rm
2.4.1 Instruction Set by Classification Table 2.11 Instruction Code Format	33	Note amended ∗ Scaling (×1, ×2, ×4) is performed based on the operand size of the instruction.

Item	Page	Revision (See Manual for Details)
2.4.1 Instruction Set by Classification Table 2.13 Arithmetic Instructions	37	Table amended **Instruction** / **Instruction Code** / **Operation** / **Execution Cycles** / **T Bit** MAC.W @Rm+,@Rn+ / 0100nnnnmmmm1111 / Signed operation of (Rn) × (Rm) + MAC → MAC 16 × 16 + 42 → 42-bit / 3/(2)* / — MULS Rm,Rn / 0010nnnnmmmm1111 / Signed operation of Rn × Rm → MAC 16 × 16 → 32-bit / 1–3* / — MULU Rm,Rn / 0010nnnnmmmm1110 / Unsigned operation of Rn × Rm → MAC 16 × 16 → 32-bit / 1–3* / —
2.4.2 Operation Code Map Table 2.18 Operation Code Map	42, 43	Table amended **Instruction Code** / **Fx: 0000** / **Fx: 0001** / **Fx: 0010** / **Fx: 0011–1111** **MSB** **LSB** / **MD: 00** / **MD: 01** / **MD: 10** / **MD: 11** 0000 0000 Fx 1001 / NOP / DIV0U 0000 Rn Fx 1001 / MOVT Rn 0110 Rn Rm 10MD / SWAP.B Rm,Rn / SWAP.W Rm,Rn / NEGC Rm,Rn / NEG Rm,Rn
8.5.3 Wait State Control	151	Description amended Regardless of the state of the $\overline{\text{WAIT}}$ signal, when the RW1 bit, the number of wait states selected by CBR refresh wait state insertion bits 1 and 0 (RLW1, RLW0) in the refresh control register (RCR) are inserted into the CAS-before-RAS refresh cycle.
10.4.5 Reset-Synchronized PWM Mode Figure 10.31 Procedure for Selecting Reset-Synchronized PWM Mode	273	Description of PFC setting added
10.4.6 Complementary PWM Mode Figure 10.33 Procedure for Selecting Complementary PWM Mode	276	Description of PFC setting added

Item	Page	Revision (See Manual for Details)
20.1.3 AC Characteristics (3) Bus Timing Figure 20.9 Basic Bus Cycle: Two-State Access	486	Note amended Note 2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) – t_{RDS}.
Figure 20.12 (b) DRAM Bus Cycle (Short-Pitch, High-Speed Page Mode: Write)	490	Figure amended 
20.1.3 AC Characteristics (3) Bus Timing Figure 20.22 Basic Bus Cycle: Two-State Access	502	Note amended Note 2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) – t_{RDS}.
Figure 20.25 (b) DRAM Bus Cycle (Short-Pitch, High-Speed Page Mode: Write)	506	Figure amended 

Item	Page	Revision (See Manual for Details)
20.2.3 AC Characteristics (3) Bus Timing Figure 20.53 Basic Bus Cycle: Two-State Access	538	Note amended Note 2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) – t_{RDS}.
Figure 20.56 (b) DRAM Bus Cycle (Short-Pitch, High-Speed Page Mode: Write)	542	Figure amended 

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Section 1 Overview

1.1 SuperH Microcomputer Features

SuperH microcomputers (SH7000 series) comprise a new generation of reduced instruction set computers (RISC) in which a Renesas-original CPU and the peripheral functions required for system configuration are integrated onto a single chip.

The CPU has a RISC-type instruction set. Most instructions can be executed in one system clock cycle, which strikingly improves instruction execution speed. In addition, the CPU has a 32-bit internal architecture for enhanced data-processing ability. As a result, the CPU enables high-performance systems to be constructed with advanced functionality at low cost, even in applications such as realtime control that require very high speeds, an impossibility with conventional microcomputers.

SH microcomputers include peripheral functions such as large-capacity ROM, RAM, a direct memory access controller (DMAC), timers, a serial communication interface (SCI), an A/D converter, an interrupt controller (INTC), and I/O ports. External memory access support functions enable direct connection to SRAM and DRAM. These features can drastically reduce system cost.

For on-chip ROM, masked ROM or electrically programmable ROM (PROM) can be selected. The PROM version can be programmed by users with a general-purpose PROM programmer.

Table 1.1 lists the features of the SH microcomputers (SH7032 and SH7034).

Table 1.1 Features of the SH7032 and SH7034 Microcomputers

Feature	Description
CPU	Original Renesas architecture
	32-bit internal data paths
	General-register machine: Sixteen 32-bit general registers Three 32-bit control registers Four 32-bit system registers
	RISC-type instruction set: Instruction length: 16-bit fixed length for improved code efficiency Load-store architecture (basic arithmetic and logic operations are executed between registers) Delayed unconditional branch instructions reduce pipeline disruption Instruction set optimized for C language
	Instruction execution time: one instruction/cycle (50 ns/instruction at 20-MHz operation)
	Address space: 4 Gbytes available in the architecture
	On-chip multiplier: multiplication operations (16 bits × 16 bits → 32 bits) executed in 1–3 cycles, and multiplication/accumulation operations (16 bits × 16 bits + 42 bits → 42 bits) executed in 2–3 cycles
	Five-stage pipeline
Operating modes	Operating modes: On-chip ROMless mode On-chip ROM mode (SH7034 only)
	Processing states: Power-on reset state Manual reset state Exception handling state Program execution state Power-down state Bus-released state
	Power-down states: Sleep mode Software standby mode

Feature	Description
Interrupt controller (INTC)	Nine external interrupt pins (NMI, $\overline{\text{IRQ0}}$–$\overline{\text{IRQ7}}$)
	Thirty-one internal interrupt sources
	Sixteen programmable priority levels
User break controller (UBC)	Generates an interrupt when the CPU or DMAC generates a bus cycle with specified conditions
	Simplifies configuration of an on-chip debugger
Clock pulse generator (CPG)	On-chip clock pulse generator (maximum operating frequency: 20 MHz): 20-MHz pulses can be generated from a 20-MHz crystal with a duty cycle correcting circuit
Bus state controller (BSC)	Supports external memory access: Sixteen-bit external data bus
	Address space divided into eight areas with the following preset features: Bus size (8 or 16 bits) Number of wait cycles can be defined by user. Type of area (external memory area, DRAM area, etc.) — Simplifies connection to ROM, SRAM, DRAM, and peripheral I/O When the DRAM area is accessed: — $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals for DRAM are output — Tp cycles can be generated to assure RAS precharge time — Address multiplexing is supported internally, so DRAM can be connected directly Chip select signals ($\overline{\text{CS0}}$ to $\overline{\text{CS7}}$) are output for each area
	DRAM refresh function: Programmable refresh interval Supports CAS-before-RAS refresh and self-refresh modes
	DRAM burst access function: Supports high-speed access modes for DRAM
	Wait cycles can be inserted by an external WAIT signal
	One-stage write buffer improves the system performance
	Data bus parity can be generated and checked

Feature	Description
Direct memory access controller (DMAC) (4 channels)	Permits DMA transfer between the following modules:
	External memory
	External I/O
	On-chip memory
	Peripheral on-chip modules (except DMAC)
	DMA transfer can be requested from external pins, on-chip SCI, on-chip timers, and on-chip A/D converter
	Cycle-steal mode or burst mode
	Channel priority level is selectable
	Channels 0 and 1: dual or single address transfer mode is selectable; external request sources are supported; channels 2 and 3: dual address transfer mode, internal request sources only
16-bit integrated timer pulse unit (ITU)	Ten types of waveforms can be output
	Input pulse width and cycle can be measured
	PWM mode: pulse output with 0–100% duty cycle (maximum resolution: 50 ns)
	Complementary PWM mode: can output a maximum of three pairs of non-overlapping PWM waveforms
	Phase counting mode: can count up or down according to the phase of an external two-phase clock
Timing pattern controller (TPC)	Maximum 16-bit output (4 bits × 4 channels) can be output
	Non-overlap intervals can be established between pairs of waveforms
	Timing-source timer is selectable
Watchdog timer (WDT) (1 channel)	Can be used as watchdog timer or interval timer
	Timer overflow can generate an internal reset, external signal, or interrupt
	Power-on reset or manual reset can be selected as the internal reset
Serial communication interface (SCI) (2 channels)	Asynchronous or synchronous mode is selectable
	Can transmit and receive simultaneously (full duplex)
	On-chip baud rate generator in each channel
	Multiprocessor communication function
A/D converter	Ten bits × 8 channels
	Can be externally triggered
	Variable reference voltage

Feature	Description
I/O ports	Total of 40 I/O lines (32 input/output lines, 8 input-only lines):
	Port A: 16 input/output lines (input or output can be selected for each bit)
	Port B: 16 input/output lines (input or output can be selected for each bit)
	Port C: 8 input lines
Large on-chip memory	SH7034 (on-chip ROM version): 64-kbyte electrically programmable ROM or masked ROM, and 4-kbyte RAM
	SH7032 (ROMless version): 8-kbyte RAM
	32-bit data can be accessed in one clock cycle

Table 1.2 Product Lineup

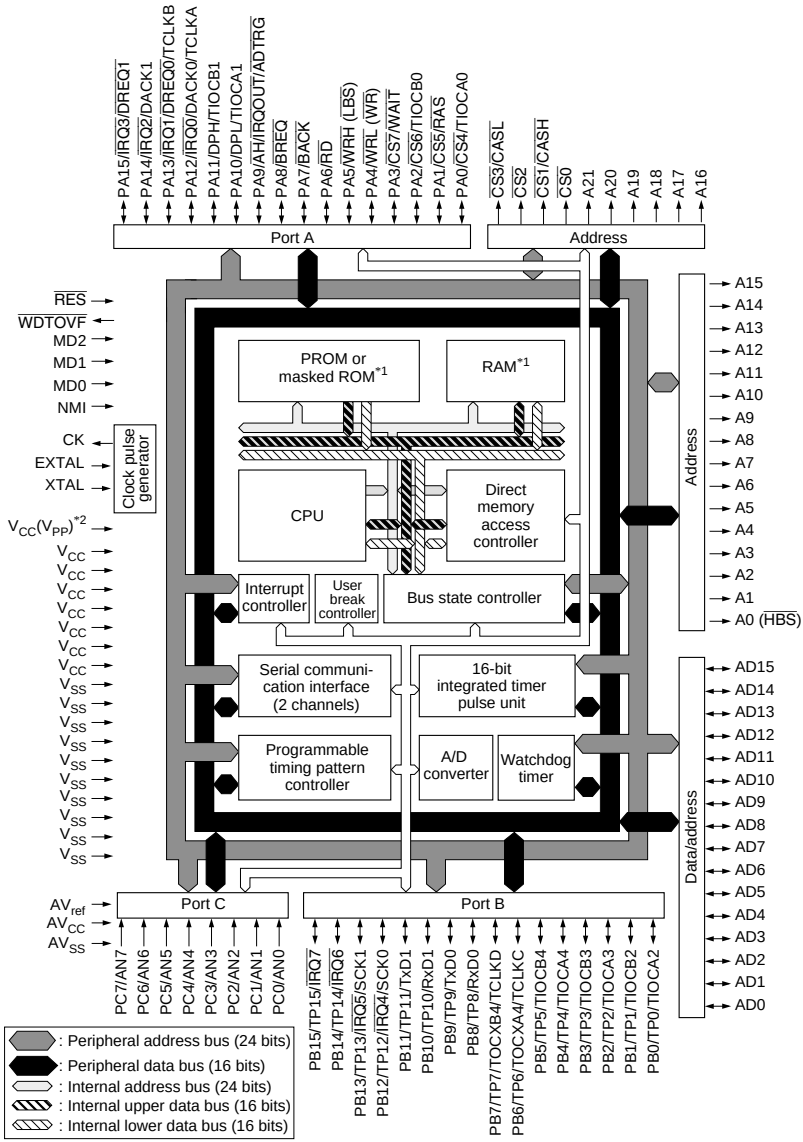
Product Number	On-Chip ROM	Operating Voltage	Operating Frequency	Temperature Range	Model	Marking Model No.*2	Package
SH7032	ROMless	5.0 V	2 to 20 MHz	-20 to +75°C	HD6417032F20	HD6417032F20	112-pin plastic QFP (PRQP0112JA-A)
				-40 to +85°C	HD6417032FI20	HD6417032FI20	
		3.3 V	2 to 12.5 MHz	-20 to +75°C	HD6417032VF12	HD6417032VF12	
				-40 to +85°C	HD6417032VFI12	HD6417032VFI12	
SH7034	PROM	5.0 V	2 to 20 MHz	-20 to +75°C	HD6477034F20	HD6477034F20	112-pin plastic QFP (PRQP0112JA-A)
				-40 to +85°C	HD6477034FI20	HD6477034FI20	
		3.3 V	2 to12.5 MHz	-20 to +75°C	HD6477034VF12	HD6477034VF12	
		5.0 V	2 to 20 MHz	-20 to +75°C	HD6477034X20	HD6477034TE20	120-pin plastic TQFP (PTQP0120LA-A)
	Mask ROM	5.0 V	2 to 20 MHz	-20 to +75°C	HD6437034AF20	HD6437034AF20	112-pin plastic QFP (PRQP0112JA-A)
				-40 to +85°C	HD6437034AFI20	HD6437034AFI20	
		3.3 V	2 to 12.5 MHz	-20 to +75°C	HD6437034AVF12	HD6437034AF12	
				-40 to +85°C	HD6437034AVFI12	HD6437034AFI12	
		5.0 V	2 to 20 MHz	-20 to +75°C	HD6437034AX20	HD6437034ATE20	120-pin plastic TQFP (PTQP0120LA-A)
				-40 to +85°C	HD6437034AXI20	HD6437034ATEI20	
		3.3 V	2 to 12.5 MHz	-20 to +75°C	HD6437034AVX12	HD6437034ATE12	
				-40 to +85°C	HD6437034AVXI12	HD6437034ATEI12	
	ROMless	5.0 V	2 to 20 MHz	-20 to +75°C	HD6417034F20	HD6417034F20	112-pin plastic QFP (PRQP0112JA-A)
				-40 to +85°C	HD6417034FI20	HD6417034FI20	
		3.3 V	2 to 12.5 MHz	-20 to +75°C	HD6417034VF12	HD6417034VF12	
				-40 to +85°C	HD6417034VFI12	HD6417034VFI12	
		5.0 V	2 to 20 MHz	-20 to +75°C	HD6417034X20	HD6417034TE20	120-pin plastic TQFP (PTQP0120LA-A)
				-40 to +85°C	HD6417034XI20	HD6417034TEI20	
		3.3 V	2 to 12.5 MHz	-20 to +75°C	HD6417034VX12	HD6417034VTE12	
				-40 to +85°C	HD6417034VXI12	HD6417034VTEI12	

Product Number	On-Chip ROM	Operating Voltage	Operating Frequency	Temperature Range	Model	Marking Model No.*2	Package
SH7034B*1	Mask ROM	3.3 V	4 to 12.5 MHz	-20 to +75°C	HD6437034BVF12	6437034B(***)F	112-pin plastic QFP (PRQP0112JA-A)
				-40 to +85°C	HD6437034BVFW12	6437034B(***)FW	
				-20 to +75°C	HD6437034BVX12	6437034B(***)X	120-pin plastic TQFP (PTQP0120LA-A)
				-40 to +85°C	HD6437034BVXW12	6437034B(***)XW	
	ROMless	3.3 V	4 to 20 MHz	-20 to +75°C	HD6417034BVF20	HD6417034BVF20	112-pin plastic QFP (PRQP0112JA-A)
				-40 to +85°C	HD6417034BVFW20	HD6417034BVFW20	
				-20 to +75°C	HD6417034BVX20	6417034BVTE20	120-pin plastic TQFP (PTQP0120LA-A)
				-40 to +85°C	HD6417034BVXW20	6417034BVTEW20	

Notes: 1. The electrical characteristics of the SH7034B mask ROM version and SH7034 PROM version are different.

2. For mask ROM versions, (***) is the ROM code.

1.2 Block Diagram

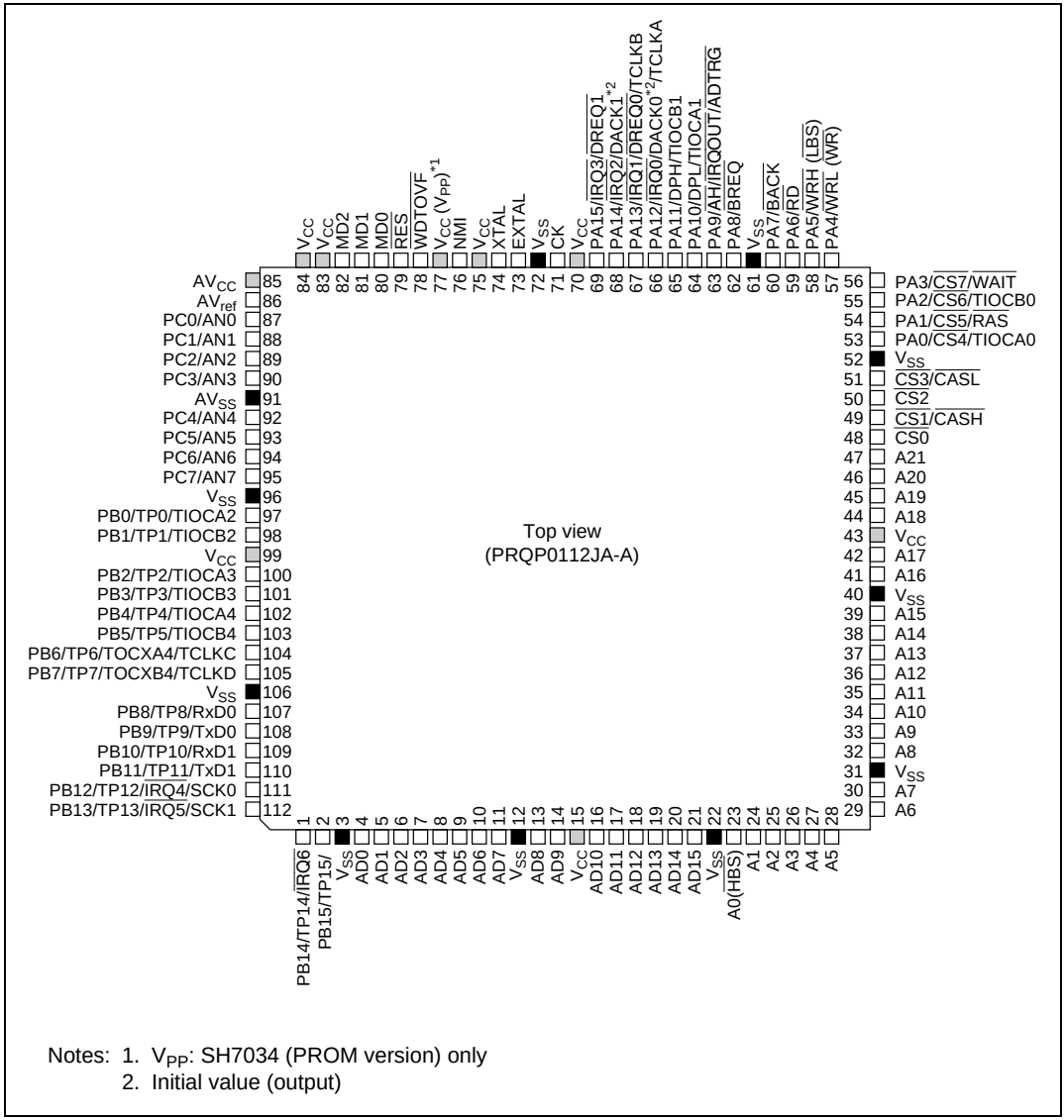


Notes: 1. The SH7032 has 8 kB of RAM and no PROM or masked ROM. The SH7034 has 4 kB of RAM and 64 kB of PROM or masked ROM.
2. VPP: SH7034 (PROM version)

Figure 1.1 Block Diagram

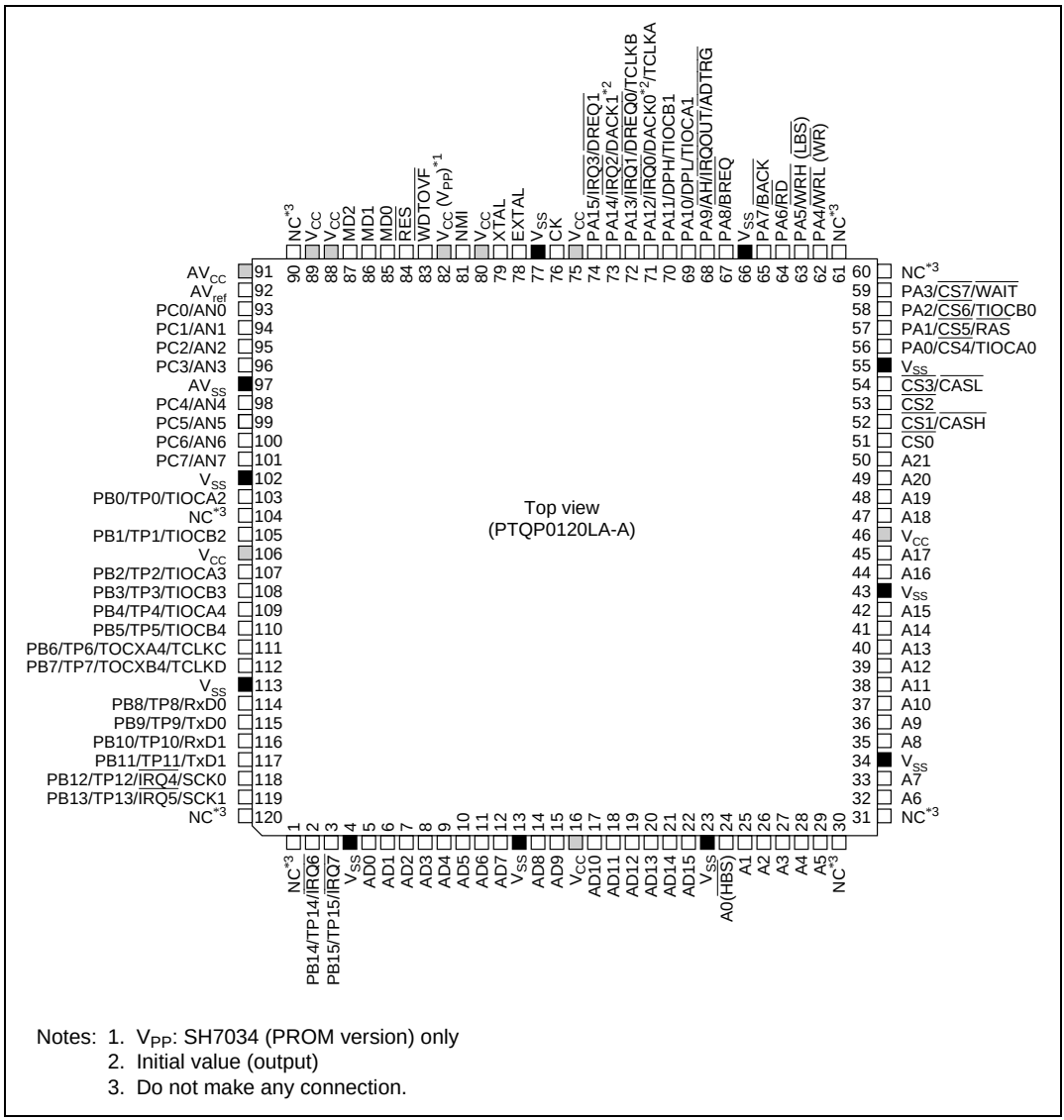
1.3 Pin Descriptions

1.3.1 Pin Arrangement



Notes: 1. V_{PP}: SH7034 (PROM version) only
2. Initial value (output)

Figure 1.2 Pin Arrangement (PRQP0112JA-A)



Notes: 1. V_{PP}: SH7034 (PROM version) only
2. Initial value (output)
3. Do not make any connection.

Figure 1.3 Pin Arrangement (PTQP0120LA-A)

1.3.2 Pin Functions

Table 1.3 describes the pin functions.

Table 1.3 Pin Functions

Type	Symbol	Pin No. (PRQP0112 JA-A)	Pin No. (PTQP0120 LA-A)	I/O	Name and Function
Power	V_{CC}	15, 43, 70, 75, 77*, 83, 84, 99	16, 46, 75, 80, 82*, 88, 89, 106	I	Power: Connected to the power supply. Connect all V_{CC} pins to the system power supply . The chip will not operate if any V_{CC} pin is left unconnected.
	V_{SS}	3, 12, 22, 31, 40, 52, 61, 72, 96, 106	4, 13, 23, 34, 43, 55, 66, 77, 102, 113	I	Ground: Connected to ground. Connect all V_{SS} pins to the system ground. The chip will not operate if any V_{SS} pin is left unconnected.
	V_{PP}	77*	82*	I	PROM programming power supply: Connected to the power supply (V_{CC}) during normal operation. Apply +12.5 V when programming the PROM in the SH7034 (PROM version).
Clock	EXTAL	73	78	I	External clock: Connected to a crystal resonator or external clock input having the same frequency as the system clock (CK).
	XTAL	74	79	I	Crystal: Connected to a crystal resonator with the same frequency as the system clock (CK). If an external clock is input at the EXTAL pin, leave XTAL open.
	CK	71	76	O	System clock: Supplies the system clock (CK) to peripheral devices.
System control	$\overline{RES}$	79	84	I	Reset: Low input causes a power-on reset if NMI is high, or a manual reset if NMI is low.
	$\overline{WDTOVF}$	78	83	O	Watchdog timer overflow: Overflow output signal from the watchdog timer.
	$\overline{BREQ}$	62	67	I	Bus request: Driven low by an external device to request bus ownership.
	$\overline{BACK}$	60	65	O	Bus request acknowledge: Indicates that bus ownership has been granted to an external device. By receiving the $\overline{BACK}$ signal, a device that has sent a $\overline{BREQ}$ signal can confirm that it has been granted the bus.

Note: * Pin 77 is V_{CC} in the SH7032 and SH7034 (masked ROM version), and V_{PP} in the SH7034 (PROM version).

Type	Symbol	Pin No. (PRQP0112JA-A)	Pin No. (PTQP0120LA-A)	I/O	Name and Function
Operating mode control	MD2, MD1, MD0	82, 81, 80	87, 86, 85	I	Mode select: Selects the operating mode. Do not change these inputs while the chip is operating. The following table lists the possible operating modes and their corresponding MD2–MD0 values.

MD2	MD1	MD0	Operating Mode	On-Chip ROM	Bus Size in Area 0
0	0	0	MCU mode	Disabled	8 bits
0	0	1			16 bits
0	1	0		Enabled*1	
0	1	1	(Reserved)		
1	0	0			
1	0	1			
1	1	0			
1	1	1	PROM mode*2		

Type	Symbol	Pin No. (PRQP0112JA-A)	Pin No. (PTQP0120LA-A)	I/O	Name and Function
Interrupts	NMI	76	81	I	Nonmaskable interrupt: Nonmaskable interrupt request signal. The rising or falling edge can be selected for signal detection.
	$\overline{IRQ0}$–$\overline{IRQ7}$	66–69, 111, 112, 1, 2	71–74, 118, 119, 2, 3	I	Interrupt request 0–7: Maskable interrupt request signals. Level input or edge-triggered input can be selected.
	$\overline{IRQOUT}$	63	68	O	Slave interrupt request output: Indicates occurrence of an interrupt while the bus is released.
Address bus	A21–A0	47–44, 42, 41, 39–32, 30–23	50–47, 45, 44, 42–35, 33, 32, 29–24	O	Address bus: Outputs addresses.
Data bus	AD15–AD0	21–16, 14, 13, 11–4	22–17, 15, 14, 12–5	I/O	Data bus: 16-bit bidirectional data bus that is multiplexed with the lower 16 bits of the address bus.
	DPH	65	70	I/O	Upper data bus parity: Parity data for D15–D8.
	DPL	64	69	I/O	Lower data bus parity: Parity data for D7–D0.

Notes: 1. Use prohibited in the SH7032 and SH7034 ROM-less versions.
2. Can be used in the SH7034 PROM version.

Type	Symbol	Pin No. (PRQP0112JA-A)	Pin No. (PTQP0120LA-A)	I/O	Name and Function
Bus control (cont)	$\overline{WAIT}$	56	59	I	Wait: Requests the insertion of wait states (T_W) into the bus cycle when the external address space is accessed.
	$\overline{RAS}$	54	57	O	Row address strobe: DRAM row-address strobe timing signal.
	$\overline{CASH}$	49	52	O	Column address strobe high: DRAM column-address strobe timing signal. Output to access the upper eight data bits.
	$\overline{CASL}$	51	54	O	Column address strobe low: DRAM column-address strobe timing. Output to access the lower eight data bits.
	$\overline{RD}$	59	64	O	Read: Indicates reading of data from an external device.
	$\overline{WRH}$	58	63	O	Upper write: Indicates write access to the upper eight bits of an external device.
	$\overline{WRL}$	57	62	O	Lower write: Indicates write access to the lower eight bits of an external device.
	$\overline{CS0}$–$\overline{CS7}$	48–51, 53–56	51–54, 56–59	O	Chip select 0–7: Chip select signals for accessing external memory and devices.
	$\overline{AH}$	63	68	O	Address hold: Address hold timing signal for a device using a multiplexed address/data bus.
	$\overline{HBS}$, $\overline{LBS}$	23, 58	24, 63	O	Upper/lower byte strobe: Upper and lower byte strobe signals. (Also used as $\overline{WRH}$ and A0.)
	$\overline{WR}$	57	62	O	Write: Brought low during write access. (Also used as $\overline{WRL}$.)
DMAC	$\overline{DREQ0}$, $\overline{DREQ1}$	67, 69	72, 74	I	DMA transfer request (channels 0 and 1): Input pins for external DMA transfer requests.
	DACK0, DACK1	66, 68	71, 73	O	DMA transfer acknowledge (channels 0 and 1): Indicates that DMA transfer is acknowledged.
16-bit integrated timer pulse unit (ITU)	TIOCA0, TIOCB0	53, 55	56, 58	I/O	ITU input capture/output compare (channel 0): Input capture or output compare pins.
	TIOCA1, TIOCB1	64, 65	69, 70	I/O	ITU input capture/output compare (channel 1): Input capture or output compare pins.
	TIOCA2, TIOCB2	97, 98	103, 105	I/O	ITU input capture/output compare (channel 2): Input capture or output compare pins.
	TIOCA3, TIOCB3	100, 101	107, 108	I/O	ITU input capture/output compare (channel 3): Input capture or output compare pins.

Type	Symbol	Pin No. (PRQP0112JA-A)	Pin No. (PTQP0120LA-A)	I/O	Name and Function
16-bit integrated timer pulse unit (ITU)	TIOCA4, TIOCB4	102, 103	109, 110	I/O	ITU input capture/output compare (channel 4): Input capture or output compare pins.
	TOCXA4, TOCXB4	104, 105	111, 112	O	ITU output compare (channel 4): Output compare pins.
	TCLKA–TCLKD	66, 67, 104, 105	71, 72, 111, 112	I	ITU timer clock input: External clock input pins for ITU counters.
Timing pattern controller (TPC)	TP15–TP0	2, 1, 112–107, 105–100, 98, 97	3, 2, 119–114, 112–107, 105, 103	O	Timing pattern output 15-0: Timing pattern output pins.
Serial communication interface (SCI)	TxD0, TxD1	108, 110	115, 117	O	Transmit data (channels 0 and 1): Transmit data output pins for SCI0 and SCI1.
	RxD0, RxD1	107, 109	114, 116	I	Receive data (channels 0 and 1): Receive data input pins for SCI0 and SCI1.
	SCK0, SCK1	111, 112	118, 119	I/O	Serial clock (channels 0 and 1): Clock input/output pins for SCI0 and SCI1.
A/D converter	AN7–AN0	95–92, 90–87	101–98, 96–93	I	Analog input: Analog signal input pins.
	$\overline{\text{ADTRG}}$	63	68	I	A/D trigger input: External trigger input for starting A/D conversion.
	AV_{ref}	86	92	I	Analog reference power supply: Input pin for the analog reference voltage.
	AV_{CC}	85	91	I	Analog power supply: Power supply pin for analog circuits. Connect to the V_{CC} potential.
	AV_{SS}	91	97	I	Analog ground: Power supply pin for analog circuits. Connect to the V_{SS} potential.
I/O ports	PA15–PA0	69–62, 60–53	74–67, 65–62, 59–56	I/O	Port A: 16-bit input/output pins. Input or output can be selected individually for each bit.
	PB15–PB0	2, 1, 112–107, 105–100, 98, 97	3, 2, 119–114, 112–107, 105, 103	I/O	Port B: 16-bit input/output pins. Input or output can be selected individually for each bit.
	PC7–PC0	95–92, 90–87	101–98, 96–93	I	Port C: 8-bit input pins.

1.3.3 Pin Layout by Mode

Table 1.4 Pin Layout by Mode

Pin No. (PRQP0112JA-A)	Pin No. (PTQP0120LA-A)	MCU Mode	PROM Mode (SH7034 PROM Version)	Pin No. (PRQP0112JA-A)	Pin No. (PTQP0120LA-A)	MCU Mode	PROM Mode (SH7034 PROM Version)
—	1	NC	NC	30	33	A7	A7
1	2	PB14/TP14/$\overline{\text{IRQ6}}$	NC	31	34	V_{SS}	V_{SS}
2	3	PB15/TP15/$\overline{\text{IRQ7}}$	NC	32	35	A8	A8
3	4	V_{SS}	V_{SS}	33	36	A9	$\overline{\text{OE}}$
4	5	AD0	D0	34	37	A10	A10
5	6	AD1	D1	35	38	A11	A11
6	7	AD2	D2	36	39	A12	A12
7	8	AD3	D3	37	40	A13	A13
8	9	AD4	D4	38	41	A14	A14
9	10	AD5	D5	39	42	A15	A15
10	11	AD6	D6	40	43	V_{SS}	V_{SS}
11	12	AD7	D7	41	44	A16	A16
12	13	V_{SS}	V_{SS}	42	45	A17	V_{CC}
13	14	AD8	NC	43	46	V_{CC}	V_{CC}
14	15	AD9	NC	44	47	A18	V_{CC}
15	16	V_{CC}	V_{CC}	45	48	A19	NC
16	17	AD10	NC	46	49	A20	NC
17	18	AD11	NC	47	50	A21	NC
18	19	AD12	NC	48	51	$\overline{\text{CS0}}$	NC
19	20	AD13	NC	49	52	$\overline{\text{CS1}}$/$\overline{\text{CASH}}$	NC
20	21	AD14	NC	50	53	$\overline{\text{CS2}}$	NC
21	22	AD15	NC	51	54	$\overline{\text{CS3}}$/$\overline{\text{CASL}}$	NC
22	23	V_{SS}	V_{SS}	52	55	V_{SS}	V_{SS}
23	24	A0 ($\overline{\text{HBS}}$)	A0	53	56	PA0/$\overline{\text{CS4}}$/TIOCA0	NC
24	25	A1	A1	54	57	PA1/$\overline{\text{CS5}}$/$\overline{\text{RAS}}$	NC
25	26	A2	A2	55	58	PA2/$\overline{\text{CS6}}$/TIOCB0	$\overline{\text{PGM}}$
26	27	A3	A3	56	59	PA3/$\overline{\text{CS7}}$/$\overline{\text{WAIT}}$	$\overline{\text{CE}}$
27	28	A4	A4	—	60	NC	NC
28	29	A5	A5	—	61	NC	NC
—	30	NC	NC	57	62	PA4/$\overline{\text{WRL}}$ ($\overline{\text{WR}}$)	NC
—	31	NC	NC	58	63	PA5/$\overline{\text{WRH}}$ ($\overline{\text{LBS}}$)	NC
29	32	A6	A6	59	64	PA6/$\overline{\text{RD}}$	NC

Pin No. (PRQP0112 JA-A)	Pin No. (PTQP0120 LA-A)	MCU Mode	PROM Mode (SH7034 PROM Version)	Pin No. (PRQP0112 JA-A)	Pin No (PTQP0120 LA-A)	MCU Mode	PROM Mode (SH7034 PROM Version)
60	65	PA7/$\overline{\text{BACK}}$	NC	87	93	PC0/AN0	V_{SS}
61	66	V_{SS}	V_{SS}	88	94	PC1/AN1	V_{SS}
62	67	PA8/$\overline{\text{BREQ}}$	NC	89	95	PC2/AN2	V_{SS}
63	68	PA9/$\overline{\text{AH}}$/$\overline{\text{IRQOUT}}$/ $\overline{\text{ADTRG}}$	NC	90	96	PC3/AN3	V_{SS}
64	69	PA10/DPL/ TIOCA1	NC	91	97	AV_{SS}	V_{SS}
65	70	PA11/DPH/ TIOCB1	NC	92	98	PC4/AN4	V_{SS}
66	71	PA12/$\overline{\text{IRQ0}}$/ DACK0/TCLKA	NC	93	99	PC5/AN5	V_{SS}
67	72	PA13/$\overline{\text{IRQ1}}$/ $\overline{\text{DREQ0}}$/TCLKB	NC	94	100	PC6/AN6	V_{SS}
68	73	PA14/$\overline{\text{IRQ2}}$/ DACK1	NC	95	101	PC7/AN7	V_{SS}
69	74	PA15/$\overline{\text{IRQ3}}$/ $\overline{\text{DREQ1}}$	NC	96	102	V_{SS}	V_{SS}
70	75	V_{CC}	V_{CC}	97	103	PB0/TP0/TIOCA2	NC
71	76	CK	NC	—	104	NC	NC
72	77	V_{SS}	V_{SS}	98	105	PB1/TP1/TIOCB2	NC
73	78	EXTAL	NC	99	106	V_{CC}	V_{CC}
74	79	XTAL	NC	100	107	PB2/TP2/TIOCA3	NC
75	80	V_{CC}	V_{CC}	101	108	PB3/TP3/TIOCB3	NC
76	81	NMI	A9	102	109	PB4/TP4/TIOCA4	NC
77	82	V_{CC}	V_{PP}	103	110	PB5/TP5/TIOCB4	NC
78	83	$\overline{\text{WDTOVF}}$	NC	104	111	PB6/TP6/ TOCXA4/TCLKC	NC
79	84	$\overline{\text{RES}}$	V_{SS}	105	112	PB7/TP7/ TOCXB4/TCLKD	NC
80	85	MD0	V_{CC}	106	113	V_{SS}	V_{SS}
81	86	MD1	V_{CC}	107	114	PB8/TP8/RxD0	NC
82	87	MD2	V_{CC}	108	115	PB9/TP9/TxD0	NC
83	88	V_{CC}	V_{CC}	109	116	PB10/TP10/RxD1	NC
84	89	V_{CC}	V_{CC}	110	117	PB11/TP11/TxD1	NC
—	90	NC	NC	111	118	PB12/TP12/$\overline{\text{IRQ4}}$/ SCK0	NC
85	91	AV_{CC}	V_{CC}	112	119	PB13/TP13/$\overline{\text{IRQ5}}$/ SCK1	NC
86	92	AV_{ref}	V_{CC}	—	120	NC	NC

Section 2 CPU

2.1 Register Configuration

The register set consists of sixteen 32-bit general registers, three 32-bit control registers, and four 32-bit system registers.

2.1.1 General Registers (Rn)

General registers Rn consist of sixteen 32-bit registers (R0–R15). General registers are used for data processing and address calculation. Register R0 also functions as an index register. For some instructions, the R0 register must be used. Register R15 functions as a stack pointer to save or restore status registers (SR) and the program counter (PC) during exception handling.

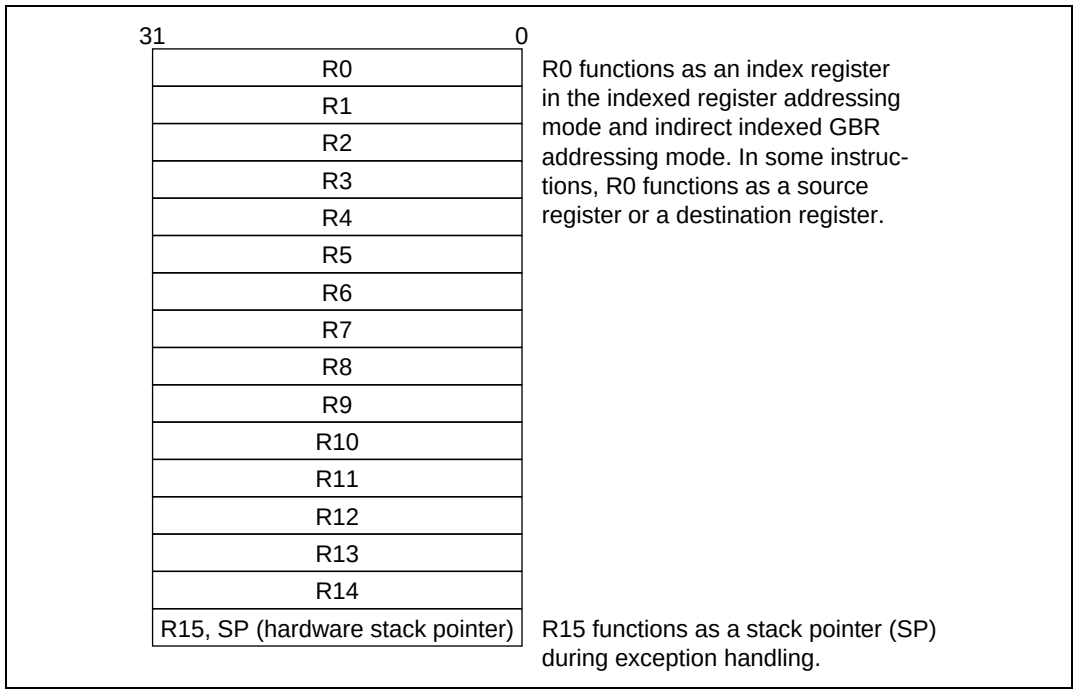


Figure 2.1 General Registers (Rn)

2.1.2 Control Registers

Control registers consist of the 32-bit status register (SR), global base register (GBR), and vector base register (VBR). The status register indicates processing states. The global base register functions as a base address for the indirect GBR addressing mode to transfer data to the registers of on-chip supporting modules. The vector base register functions as the base address of the exception vector area including interrupts.

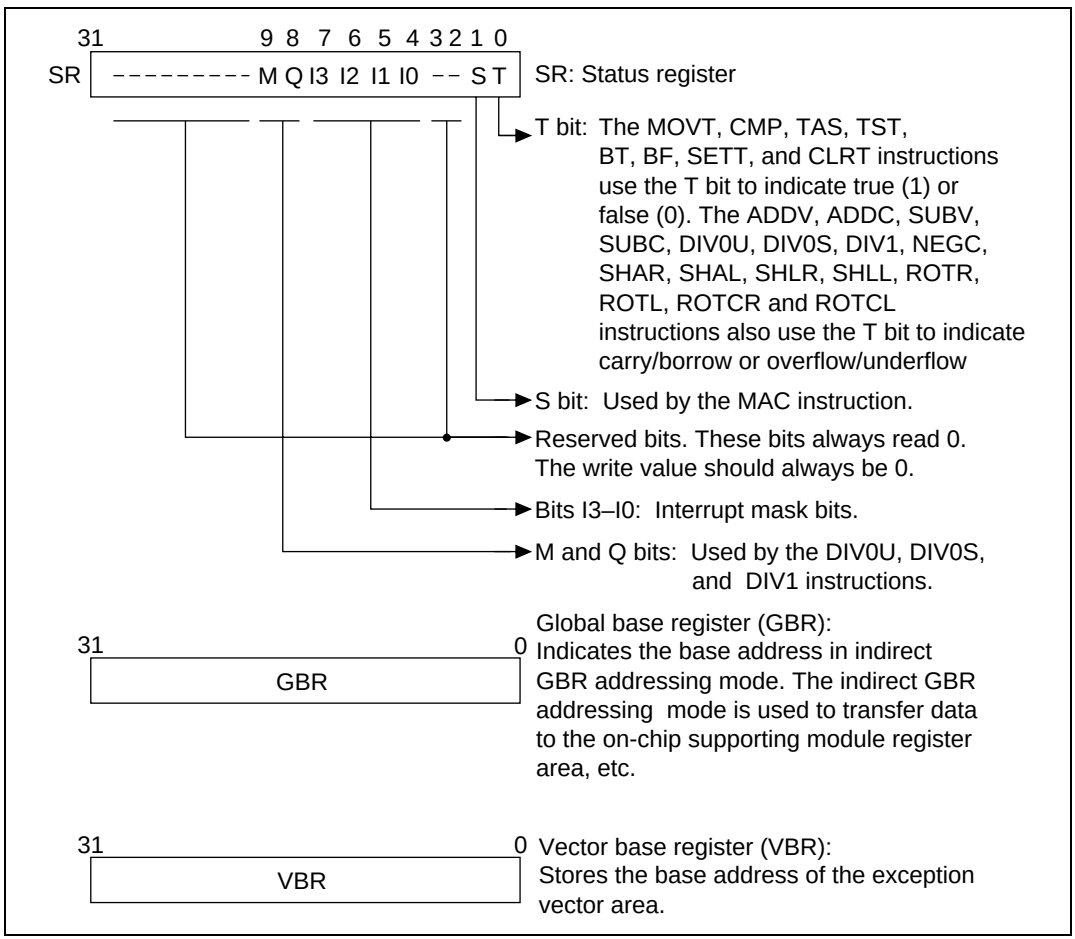


Figure 2.2 Control Registers

2.1.3 System Registers

System registers consist of four 32-bit registers: multiply and accumulate registers high and low (MACH and MACL), procedure register (PR), and program counter (PC). The multiply and accumulate registers store the results of multiply and accumulate operations. The procedure register stores the return address for a subroutine procedure. The program counter stores program addresses to control the flow of the processing.

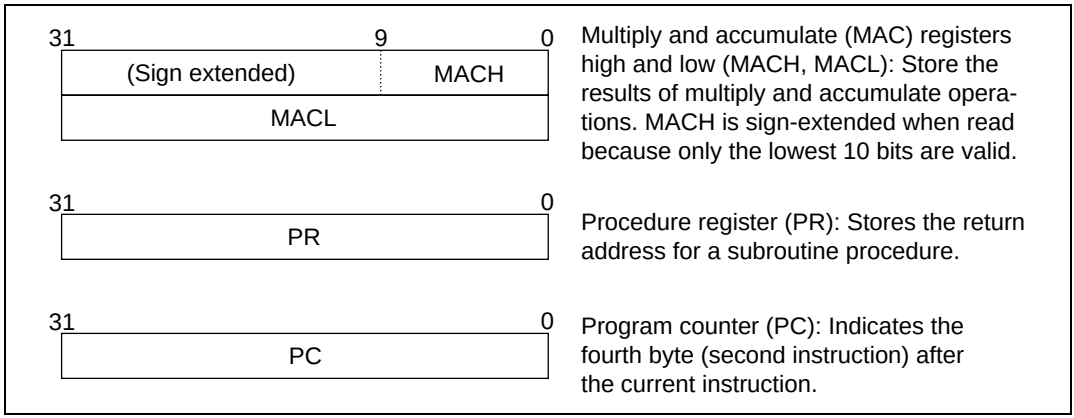


Figure 2.3 System Registers

2.1.4 Initial Values of Registers

Table 2.1 lists the values of the registers after reset.

Table 2.1 Initial Values of Registers

Classification	Register	Initial Value
General registers	R0–R14	Undefined
	R15 (SP)	Value of the stack pointer in the vector address table
Control registers	SR	Bits I3–I0 are 1111(H'F), reserved bits are 0, and other bits are undefined
	GBR	Undefined
	VBR	H'00000000
System registers	MACH, MACL, PR	Undefined
	PC	Value of the program counter in the vector address table

2.2 Data Formats

2.2.1 Data Format in Registers

Register operands are always longwords (32 bits). When the memory operand is only a byte (8 bits) or a word (16 bits), it is sign-extended into a longword when stored into a register (figure 2.4).

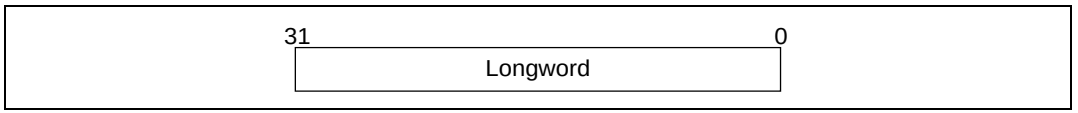


Figure 2.4 Data Format in Registers

2.2.2 Data Format in Memory

Memory data formats are classified into bytes, words, and longwords. Byte data can be accessed from any address, but an address error will occur if an attempt is made to access word data starting from an address other than 2n or longword data starting from an address other than 4n. In such cases, the data accessed cannot be guaranteed. The hardware stack area, which is referred to by the hardware stack pointer (SP, R15), uses only longword data starting from address 4n because this area stores the program counter and status register (figure 2.5).

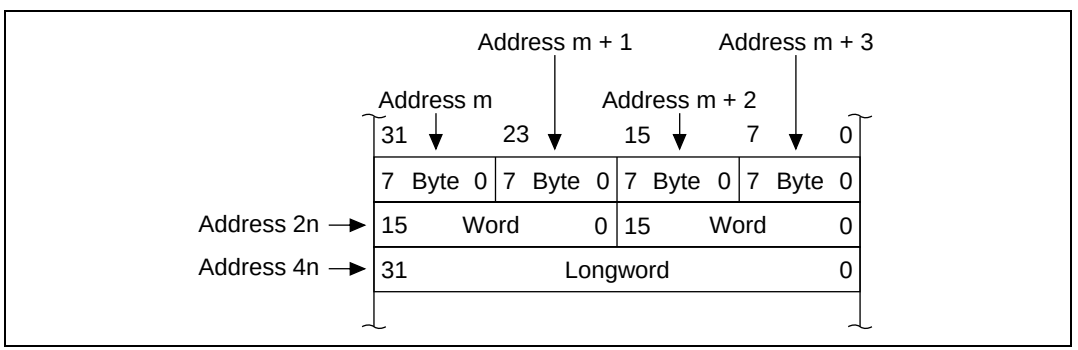


Figure 2.5 Data Format in Memory

2.2.3 Immediate Data Format

Byte (8-bit) immediate data is located in the instruction code. Immediate data accessed by the MOV, ADD, and CMP/EQ instructions is sign-extended and is handled in registers as longword data. Immediate data accessed by the TST, AND, OR, and XOR instructions is zero-extended and is handled as longword data. Consequently, AND instructions with immediate data always clear the upper 24 bits of the destination register.

Word or longword immediate data is not located in the instruction code but rather is stored in a memory table. The memory table is accessed by an immediate data transfer instruction (MOV) using the PC relative addressing mode with displacement.

2.3 Instruction Features

2.2.1 RISC-Type Instruction Set

All instructions are RISC type. Their features are as follows:

16-Bit Fixed Length: Every instruction is 16 bits long, making program coding much more efficient.

One Instruction/Cycle: Basic instructions can be executed in one cycle using a pipeline system. One-cycle instructions are executed in 50 ns at 20 MHz.

Data Length: Longword is the standard data length for all operations. Memory can be accessed in bytes, words, or longwords. Byte or word data accessed from memory is sign-extended and handled as longword data. Immediate data is sign-extended for arithmetic operations or zero-extended for logic operations (handled as longword data).

Table 2.2 Sign Extension of Word Data

SH7000 Series CPU	Description	Conventional CPUs

`MOV.W @(disp,PC),R1`
`ADD R1,R0`
`.....`
`.DATA.W H'1234`
	Data is sign-extended to 32 bits, and R1 becomes H'00001234. It is next operated upon by an ADD instruction.	`ADD.W #H'1234,R0`

Note: The address of the immediate data is accessed by @(disp, PC).

Load-Store Architecture: Basic operations are executed between registers. For operations that involve memory, data is loaded into to the registers and executed (load-store architecture). Instructions such as AND that manipulate bits, however, are executed directly in memory.

Delayed Branch Instructions: Unconditional branch instructions are delayed. Pipeline disruption during branching is reduced by first executing the instruction that follows the branch instruction, and then branching. See the SH-1/SH-2/SH-DSP Software Manual for details.

Table 2.3 Delayed Branch Instructions

SH7000 Series CPU		Description	Conventional CPU	
BRA	TRGET	Executes an ADD before branching to TRGET.	ADD.W	R1,R0
ADD	R1,R0		BRA	TRGET

Multiplication/Accumulation Operation: The five-stage pipeline system and the on-chip multiplier enable 16-bit × 16-bit → 32-bit multiplication operations to be executed in 1–3 cycles. 16-bit × 16-bit + 42-bit → 42-bit multiplication/accumulation operations can be executed in 2–3 cycles.

T bit: T bit (in the status register) is set according to the result of a comparison, and in turn is the condition (True/False) that determines if the program will branch. The T bit in the status register is only changed by selected instructions, thus improving the processing speed.

Table 2.4 T Bit

SH7000 Series CPU		Description	Conventional CPU	
CMP/GE	R1,R0	T bit is set when R0 ≥ R1. The program branches to TRGET0 when R0 ≥ R1 and to TRGET1 when R0<R1.	CMP.W	R1,R0
BT	TRGET0		BGE	TRGET0
BF	TRGET1		BLT	TRGET1
ADD	#–1,R0	T bit is not changed by ADD. T bit is set when R0 = 0. The program branches if R0 = 0.	SUB.W	#1,R0
TST	R0,R0		BEQ	TRGET
BT	TRGET			

Immediate Data: Byte (8-bit) immediate data is located in the instruction code. Word or longword immediate data is not located in instruction codes but is stored in a memory table. The memory table is accessed by an immediate data transfer instruction (MOV) using the PC relative addressing mode with displacement.

Table 2.5 Immediate Data Accessing

Classification	SH7000 Series CPU	Conventional CPU
8-bit immediate	`MOV #H'12,R0`	`MOV.B #H'12,R0`

16-bit immediate	`MOV.W @(disp,PC),R0`
	`.........`
	`.DATA.W H'1234`
		`MOV.W #H'1234,R0`

32-bit immediate	`MOV.L @(disp,PC),R0`
	`.........`
	`.DATA.L H'12345678`
		`MOV.L #H'12345678, R0`

Note: The address of the immediate data is accessed by @(disp, PC).

Absolute Address: When data is accessed by absolute address, the value already in the absolute address is placed in the memory table. By loading the immediate data when the instruction is executed, that value is transferred to the register and the data is accessed in the indirect register addressing mode.

Table 2.6 Absolute Address Accessing

Classification	SH7000 Series CPU	Conventional CPU

Absolute address	`MOV.L @(disp,PC),R1`
	`MOV. B @R1,R0`
	`.........`
	`.DATA.L H'12345678`
		`MOV.B @H'12345678,R0`

Note: The address of the immediate data is accessed by @(disp, PC).

16/32-Bit Displacement: When data is accessed by 16-bit or 32-bit displacement, the pre-existing displacement value is placed in the memory table. By loading the immediate data when the instruction is executed, that value is transferred to the register and the data is accessed in the indirect indexed register addressing mode.

Table 2.7 Accessing by Displacement

Classification	SH7000 Series CPU	Conventional CPU

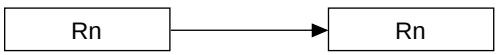
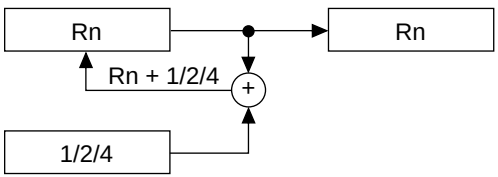
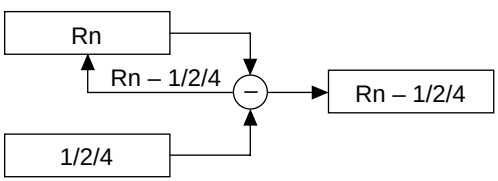
16-bit displacement	`MOV.W @(disp,PC),R0`
	`MOV.W @(R0,R1),R2`
	`.........`
	`.DATA.W H'1234`
		`MOV.W @(H'1234,R1),R2`

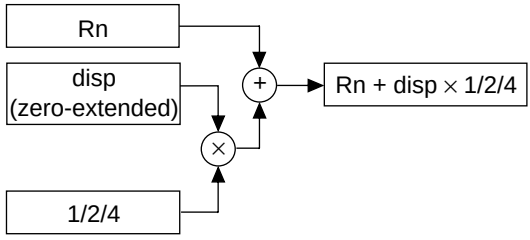
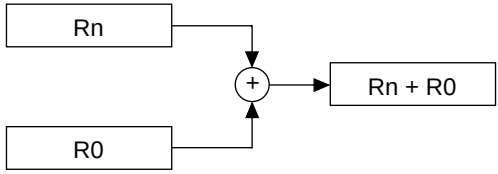
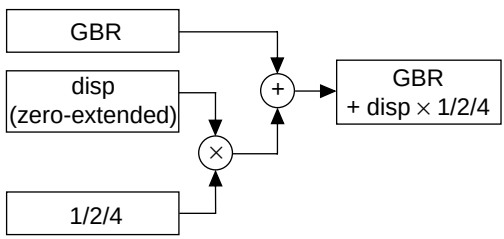
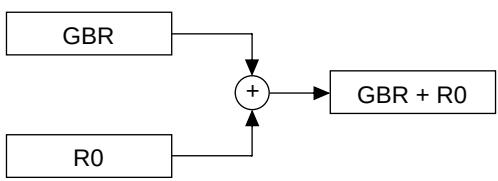
Note: The address of the immediate data is accessed by @(disp, PC).

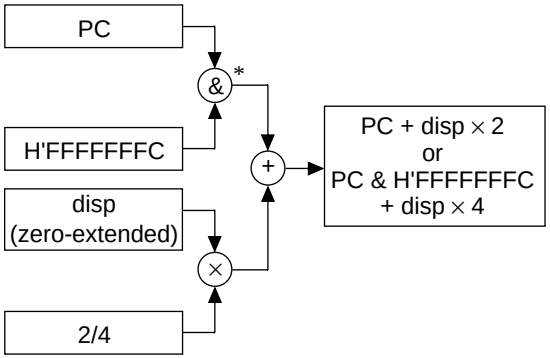
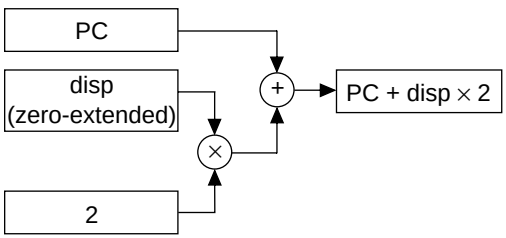
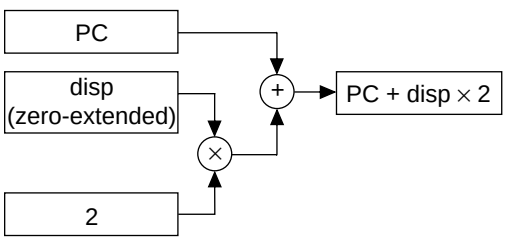
2.3.2 Addressing Modes

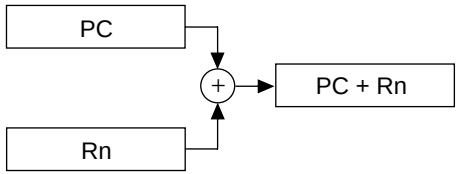
Addressing modes and effective address calculation are described in table 2.8.

Table 2.8 Addressing Modes and Effective Addresses

Addressing Mode	Mnemonic Expression	Effective Addresses Calculation	Equation
Direct register addressing	Rn	The effective address is register Rn. (The operand is the contents of register Rn.)	—
Indirect register addressing	@Rn	The effective address is the contents of register Rn. 	Rn
Post-increment indirect register addressing	@Rn +	The effective address is the contents of register Rn. A constant is added to the contents of Rn after the instruction is executed. 1 is added for a byte operation, 2 for a word operation, and 4 for a longword operation. 	Rn (After the instruction is executed) Byte: Rn + 1 → Rn Word: Rn + 2 → Rn Longword: Rn + 4 → Rn
Pre-decrement indirect register addressing	@–Rn	The effective address is the value obtained by subtracting a constant from Rn. 1 is subtracted for a byte operation, 2 for a word operation, and 4 for a longword operation. 	Byte: Rn – 1 → Rn Word: Rn – 2 → Rn Longword: Rn – 4 → Rn (Instruction executed with Rn after calculation)

Addressing Mode	Mnemonic Expression	Effective Addresses Calculation	Equation
Indirect register addressing with displace-ment	@(disp:4, Rn)	The effective address is Rn plus a 4-bit displacement (disp). disp is zero-extended, and remains the same for a byte operation, is doubled for a word operation, and is quadrupled for a longword operation. 	Byte: Rn + disp Word: Rn + disp × 2 Longword: Rn + disp × 4
Indirect indexed register addressing	@(R0, Rn)		Rn + R0
Indirect GBR addressing with displace-ment	@(disp:8, GBR)	The effective address is the GBR value plus an 8-bit displacement (disp). The value of disp is zero-extended, and remains the same for a byte operation, is doubled for a word operation, and is quadrupled for a longword operation. 	Byte: GBR + disp Word: GBR + disp × 2 Longword: GBR + disp × 4
Indirect indexed GBR addressing	@(R0, GBR)	The effective address is the GBR value plus the R0 value. 	GBR + R0

Addressing Mode	Mnemonic Expression	Effective Addresses Calculation	Equation
PC relative addressing with displacement	@(disp:8, PC)	The effective address is the PC value plus an 8-bit displacement (disp). disp is zero-extended, is doubled for a word operation, and is quadrupled for a longword operation. For a longword operation, the lowest two bits of the PC are masked.  *: For longword	Word: PC + disp × 2 Longword: PC & H'FFFFFFFC + disp × 4
PC relative addressing	disp:8	The effective address is the PC value sign-extended with an 8-bit displacement (disp), doubled, and added to the PC.  	PC + disp × 2
	disp:12	The effective address is the PC value sign-extended with a 12-bit displacement (disp), doubled, and added to the PC.  	PC + disp × 2

Addressing Mode	Mnemonic Expression	Effective Addresses Calculation	Equation
PC relative addressing	Rn	The effective address is the PC value plus Rn. 	PC + Rn
Immediate addressing	#imm:8	The 8-bit immediate data (imm) for the TST, AND, OR, and XOR instructions is zero-extended.	—
	#imm:8	The 8-bit immediate data (imm) for the MOV, ADD, and CMP/EQ instructions is sign-extended.	—
	#imm:8	Immediate data (imm) for the TRAPA instruction is zero-extended and is quadrupled.	—

2.3.3 Instruction Formats

The instruction format refers to the source operand and the destination operand. The meaning of the operand depends on the instruction code. Symbols are as follows.

xxxx Instruction code

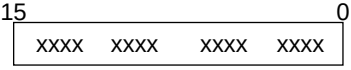
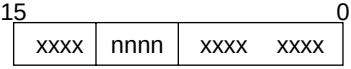
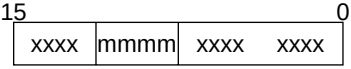
mmmm Source register

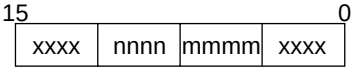
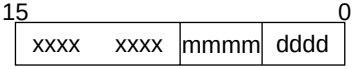
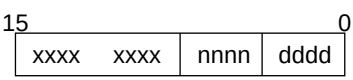
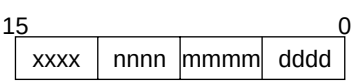
nnnn Destination register

iiii Immediate data

dddd Displacement

Table 2.9 Instruction Formats

Instruction Format	Source Operand	Destination Operand	Example
0 format 	—	—	NOP
n format 	—	nnnn: Register direct	MOVT Rn
	Control register or system register	nnnn: Register direct	STS MACH,Rn
	Control register or system register	nnnn: Register indirect with pre-decrement	STC.L SR,@-Rn
m format 	mmmm: Register direct	Control register or system register	LDC Rm,SR
	mmmm: Register indirect with post-increment	Control register or system register	LDC.L @Rm+,SR
	mmmm: Register indirect	—	JMP @Rm
	mmmm: PC relative using Rm	—	BRAF Rm

Instruction Format	Source Operand	Destination Operand	Example
nm format 	mmmm: Register direct	nnnn: Register direct	ADD Rm,Rn
	mmmm: Register direct	nnnn: Register indirect	MOV.L Rm,@Rn
	mmmm: Register indirect with post-increment (multiply-and-accumulate) nnnn: Register indirect with post-increment (multiply-and-accumulate)*	MACH, MACL	MAC.W @Rm+,@Rn+
	mmmm: Register indirect with post-increment	nnnn: Register direct	MOV.L @Rm+,Rn
	mmmm: Register direct	nnnn: Register indirect with pre-decrement	MOV.L Rm,@-Rn
	mmmm: Register direct	nnnn: Indexed register indirect	MOV.L Rm,@(R0,Rn)
md format 	mmmmdddd: Register indirect with displacement	R0 (Register direct)	MOV.B @(disp,Rn),R0
nd4 format 	R0 (Register direct)	nnnndddd: Register indirect with displacement	MOV.B R0,@(disp,Rn)
nmd format 	mmmm: Register direct	nnnndddd: Register indirect with displacement	MOV.L Rm,@(disp,Rn)
	mmmmdddd: Register indirect with displacement	nnnn: Register direct	MOV.L @(disp,Rm),Rn

Instruction Format	Source Operand	Destination Operand	Example
d format 15 0 xxxx xxxx dddd dddd	dddddddd: GBR indirect with displacement	R0 (Register direct)	MOV.L @(disp,GBR),R0
	R0 (Register direct)	dddddddd: GBR indirect with displacement	MOV.L R0,@(disp,GBR)
	dddddddd: PC relative with displacement	R0 (Register direct)	MOVA @(disp,PC),R0
	dddddddd: PC relative	—	BF label
d12 format 15 0 xxxx dddd dddd dddd	ddddddddddddd: PC relative	—	BRA label (label = disp + PC)
nd8 format 15 0 xxxx nnnn dddd dddd	dddddddd: PC relative with displacement	nnnn: Register direct	MOV.L @(disp,PC),Rn
i format 15 0 xxxx xxxx iiii iiii	iiiiiiii: Immediate	Indexed GBR indirect	AND.B #imm,@(R0,GBR)
	iiiiiiii: Immediate	R0 (Register direct)	AND #imm,R0
	iiiiiiii: Immediate	—	TRAPA #imm
ni format 15 0 xxxx nnnn iiii iiii	iiiiiiii: Immediate	nnnn: Register direct	ADD #imm,Rn

Note: * In multiply-and-accumulate instructions, nnnn is the source register.

2.4 Instruction Set

2.4.1 Instruction Set by Classification

Table 2.10 lists instructions by classification.

Table 2.10 Classification of Instructions

Classification	Types	Operation Code	Function	Number of Instructions
Data transfer	5	MOV	Data transfer, immediate data transfer, supporting module data transfer, structure data transfer	39
		MOVA	Effective address transfer	
		MOVT	T bit transfer	
		SWAP	Swap of upper and lower bytes	
		XTRCT	Extraction of the middle of registers connected	
Arithmetic operations	17	ADD	Binary addition	28
		ADDC	Binary addition with carry	
		ADDV	Binary addition with overflow check	
		CMP/cond	Comparison	
		DIV1	Division	
		DIV0S	Initialization of signed division	
		DIV0U	Initialization of unsigned division	
		EXTS	Sign extension	
		EXTU	Zero extension	
		MAC	Multiplication and accumulation	
		MULS	Signed multiplication	
		MULU	Unsigned multiplication	
		NEG	Negation	
		NEGC	Negation with borrow	
		SUB	Binary subtraction	
		SUBC	Binary subtraction with carry	
		SUBV	Binary subtraction with underflow check	
Logic operations	6	AND	Logical AND	14
		NOT	Bit inversion	
		OR	Logical OR	
		TAS	Memory test and bit set	

Classification	Types	Operation Code	Function	Number of Instructions
Logic operations (cont)	6	TST	Logical AND and T bit set	14
		XOR	Exclusive OR	
Shift	10	ROTL	One-bit left rotation	14
		ROTR	One-bit right rotation	
		ROTCL	One-bit left rotation with T bit	
		ROTCR	One-bit right rotation with T bit	
		SHAL	One-bit arithmetic left shift	
		SHAR	One-bit arithmetic right shift	
		SHLL	One-bit logical left shift	
		SHLLn	n-bit logical left shift	
		SHLR	One-bit logical right shift	
		SHLRn	n-bit logical right shift	
Branch	7	BF	Conditional branch (T = 0)	7
		BT	Conditional branch (T = 1)	
		BRA	Unconditional branch	
		BSR	Branch to subroutine procedure	
		JMP	Unconditional branch	
		JSR	Branch to subroutine procedure	
		RTS	Return from subroutine procedure	
System control	11	CLRT	T bit clear	31
		CLRMAC	MAC register clear	
		LDC	Load to control register	
		LDS	Load to system register	
		NOP	No operation	
		RTE	Return from exception handling	
		SETT	T bit set	
		SLEEP	Shift into power-down mode	
		STC	Store control register data	
		STS	Store system register data	
		TRAPA	Trap exception handling	
Total	56			133

The following tables (arranged by instruction classification) show instruction codes, operations, and execution states, using the format shown below.

Table 2.11 Instruction Code Format

Item	Format	Explanation
Instruction mnemonic	`OP.Sz SRC,DEST`	OP: Operation code Sz: Size SRC: Source DEST: Destination Rm: Source register Rn: Destination register imm: Immediate data disp: Displacement*
Instruction code	MSB ↔ LSB	mmmm: Source register nnnn: Destination register 0000: R0 0001: R1 ..... 1111: R15 iiii: Immediate data dddd: Displacement
Operation summary	→, ← (xx) M/Q/T & | ^ ~ <<n, >>n	Direction of transfer Memory operand Flag bits in SR Logical AND of each bit Logical OR of each bit Exclusive OR of each bit Logical NOT of each bit n-bit shift
Execution cycle		Value when no wait states are inserted
		Instruction execution cycles: The execution cycles shown in the table are minimums. The actual number of cycles may be increased: 1. When contention occurs between instruction fetches and data access, or 2. When the destination register of the load instruction (memory → register) and the register used by the next instruction are the same.
T bit		Value of T bit after instruction is executed
	—	No change

Notes: * Scaling (×1, ×2, ×4) is performed based on the operand size of the instruction.

Table 2.12 Data Transfer Instructions

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
MOV	#imm,Rn	1110nnnniiiiiiii	#imm → Sign extension → Rn	1	—
MOV.W	@(disp,PC),Rn	1001nnnndddddddd	(disp × 2 + PC) → Sign extension → Rn	1	—
MOV.L	@(disp,PC),Rn	1101nnnndddddddd	(disp × 4 + PC) → Rn	1	—
MOV	Rm,Rn	0110nnnnmmmm0011	Rm → Rn	1	—
MOV.B	Rm,@Rn	0010nnnnmmmm0000	Rm → (Rn)	1	—
MOV.W	Rm,@Rn	0010nnnnmmmm0001	Rm → (Rn)	1	—
MOV.L	Rm,@Rn	0010nnnnmmmm0010	Rm → (Rn)	1	—
MOV.B	@Rm,Rn	0110nnnnmmmm0000	(Rm) → Sign extension → Rn	1	—
MOV.W	@Rm,Rn	0110nnnnmmmm0001	(Rm) → Sign extension → Rn	1	—
MOV.L	@Rm,Rn	0110nnnnmmmm0010	(Rm) → Rn	1	—
MOV.B	Rm,@–Rn	0010nnnnmmmm0100	Rn–1 → Rn, Rm → (Rn)	1	—
MOV.W	Rm,@–Rn	0010nnnnmmmm0101	Rn–2 → Rn, Rm → (Rn)	1	—
MOV.L	Rm,@–Rn	0010nnnnmmmm0110	Rn–4 → Rn, Rm → (Rn)	1	—
MOV.B	@Rm+,Rn	0110nnnnmmmm0100	(Rm) → Sign extension → Rn, Rm + 1 → Rm	1	—
MOV.W	@Rm+,Rn	0110nnnnmmmm0101	(Rm) → Sign extension → Rn, Rm + 2 → Rm	1	—
MOV.L	@Rm+,Rn	0110nnnnmmmm0110	(Rm) → Rn, Rm + 4 → Rm	1	—
MOV.B	R0,@(disp,Rn)	10000000nnnndddd	R0 → (disp + Rn)	1	—
MOV.W	R0,@(disp,Rn)	10000001nnnndddd	R0 → (disp × 2 + Rn)	1	—
MOV.L	Rm,@(disp,Rn)	0001nnnnmmmmdddd	Rm → (disp × 4 + Rn)	1	—
MOV.B	@(disp,Rm),R0	10000100mmmmdddd	(disp + Rm) → Sign extension → R0	1	—

Instruction	Instruction Code	Operation	Execution Cycles	T Bit
MOV.W @(disp,Rm),R0	10000101mmmmdddd	(disp × 2 + Rm) → Sign extension → R0	1	—
MOV.L @(disp,Rm),Rn	0101nnnnmmmmdddd	(disp × 4 + Rm) → Rn	1	—
MOV.B Rm,@(R0,Rn)	0000nnnnmmmm0100	Rm → (R0 + Rn)	1	—
MOV.W Rm,@(R0,Rn)	0000nnnnmmmm0101	Rm → (R0 + Rn)	1	—
MOV.L Rm,@(R0,Rn)	0000nnnnmmmm0110	Rm → (R0 + Rn)	1	—
MOV.B @(R0,Rm),Rn	0000nnnnmmmm1100	(R0 + Rm) → Sign extension → Rn	1	—
MOV.W @(R0,Rm),Rn	0000nnnnmmmm1101	(R0 + Rm) → Sign extension → Rn	1	—
MOV.L @(R0,Rm),Rn	0000nnnnmmmm1110	(R0 + Rm) → Rn	1	—
MOV.B R0,@(disp,GBR)	11000000dddddddd	R0 → (disp + GBR)	1	—
MOV.W R0,@(disp,GBR)	11000001dddddddd	R0 → (disp × 2 + GBR)	1	—
MOV.L R0,@(disp,GBR)	11000010dddddddd	R0 → (disp × 4 + GBR)	1	—
MOV.B @(disp,GBR),R0	11000100dddddddd	(disp + GBR) → Sign extension → R0	1	—
MOV.W @(disp,GBR),R0	11000101dddddddd	(disp × 2 + GBR) → Sign extension → R0	1	—
MOV.L @(disp,GBR),R0	11000110dddddddd	(disp × 4 + GBR) → R0	1	—
MOVA @(disp,PC),R0	11000111dddddddd	disp × 4 + PC → R0	1	—
MOVT Rn	0000nnnn00101001	T → Rn	1	—
SWAP.B Rm,Rn	0110nnnnmmmm1000	Rm → Swap the bottom two bytes → Rn	1	—
SWAP.W Rm,Rn	0110nnnnmmmm1001	Rm → Swap two consecutive words → Rn	1	—
XTRCT Rm,Rn	0010nnnnmmmm1101	Rm: Center 32 bits of Rn → Rn	1	—

Table 2.13 Arithmetic Instructions

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
ADD	Rm,Rn	0011nnnnmmmm1100	Rn + Rm → Rn	1	—
ADD	#imm,Rn	0111nnnniiiiiiii	Rn + imm → Rn	1	—
ADDC	Rm,Rn	0011nnnnmmmm1110	Rn + Rm + T → Rn, Carry → T	1	Carry
ADDV	Rm,Rn	0011nnnnmmmm1111	Rn + Rm → Rn, Overflow → T	1	Overflow
CMP/EQ	#imm,R0	10001000iiiiiiii	If R0 = imm, 1 → T	1	Comparison result
CMP/EQ	Rm,Rn	0011nnnnmmmm0000	If Rn = Rm, 1 → T	1	Comparison result
CMP/HS	Rm,Rn	0011nnnnmmmm0010	If Rn ≥ Rm with unsigned data, 1 → T	1	Comparison result
CMP/GE	Rm,Rn	0011nnnnmmmm0011	If Rn ≥ Rm with signed data, 1 → T	1	Comparison result
CMP/HI	Rm,Rn	0011nnnnmmmm0110	If Rn > Rm with unsigned data, 1 → T	1	Comparison result
CMP/GT	Rm,Rn	0011nnnnmmmm0111	If Rn > Rm with signed data, 1 → T	1	Comparison result
CMP/PZ	Rn	0100nnnn00010001	If Rn ≥ 0, 1 → T	1	Comparison result
CMP/PL	Rn	0100nnnn00010101	If Rn > 0, 1 → T	1	Comparison result
CMP/STR	Rm,Rn	0010nnnnmmmm1100	If Rn and Rm have an equivalent byte, 1 → T	1	Comparison result
DIV1	Rm,Rn	0011nnnnmmmm0100	Single-step division (Rn/Rm)	1	Calculation result
DIV0S	Rm,Rn	0010nnnnmmmm0111	MSB of Rn → Q, MSB of Rm → M, M ^ Q → T	1	Calculation result
DIV0U		0000000000011001	0 → M/Q/T	1	0
EXTS.B	Rm,Rn	0110nnnnmmmm1110	A byte in Rm is sign-extended → Rn	1	—

Instruction	Instruction Code	Operation	Execution Cycles	T Bit
EXTS.W Rm,Rn	0110nnnnmmmm1111	A word in Rm is sign-extended → Rn	1	—
EXTU.B Rm,Rn	0110nnnnmmmm1100	A byte in Rm is zero-extended → Rn	1	—
EXTU.W Rm,Rn	0110nnnnmmmm1101	A word in Rm is zero-extended → Rn	1	—
MAC.W @Rm+,@Rn+	0100nnnnmmmm1111	Signed operation of (Rn) × (Rm) + MAC → MAC 16 × 16 + 42 → 42-bit	3/(2)*	—
MULS Rm,Rn	0010nnnnmmmm1111	Signed operation of Rn × Rm → MAC 16 × 16 → 32-bit	1–3*	—
MULU Rm,Rn	0010nnnnmmmm1110	Unsigned operation of Rn × Rm → MAC 16 × 16 → 32-bit	1–3*	—
NEG Rm,Rn	0110nnnnmmmm1011	0–Rm → Rn	1	—
NEGC Rm,Rn	0110nnnnmmmm1010	0–Rm–T → Rn, Borrow → T	1	Borrow
SUB Rm,Rn	0011nnnnmmmm1000	Rn–Rm → Rn	1	—
SUBC Rm,Rn	0011nnnnmmmm1010	Rn–Rm–T → Rn, Borrow → T	1	Borrow
SUBV Rm,Rn	0011nnnnmmmm1011	Rn–Rm → Rn, Underflow → T	1	Underflow

Note: * The normal minimum number of cycles (numbers in parenthesis represent the number of cycles when there is contention with preceding or following instructions).

Table 2.14 Logic Operation Instructions

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
AND	Rm,Rn	0010nnnnmmmm1001	Rn & Rm → Rn	1	—
AND	#imm,R0	11001001iiiiiiii	R0 & imm → R0	1	—
AND.B	#imm,@(R0,GBR)	11001101iiiiiiii	(R0 + GBR) & imm → (R0 + GBR)	3	—
NOT	Rm,Rn	0110nnnnmmmm0111	~Rm → Rn	1	—
OR	Rm,Rn	0010nnnnmmmm1011	Rn | Rm → Rn	1	—
OR	#imm,R0	11001011iiiiiiii	R0 | imm → R0	1	—
OR.B	#imm,@(R0,GBR)	11001111iiiiiiii	(R0 + GBR) | imm → (R0 + GBR)	3	—
TAS.B	@Rn	0100nnnn00011011	If (Rn) is 0, 1 → T; 1 → MSB of (Rn)	4	Test result
TST	Rm,Rn	0010nnnnmmmm1000	Rn & Rm; if the result is 0, 1 → T	1	Test result
TST	#imm,R0	11001000iiiiiiii	R0 & imm; if the result is 0, 1 → T	1	Test result
TST.B	#imm,@(R0,GBR)	11001100iiiiiiii	(R0 + GBR) & imm; if the result is 0, 1 → T	3	Test result
XOR	Rm,Rn	0010nnnnmmmm1010	Rn ^ Rm → Rn	1	—
XOR	#imm,R0	11001010iiiiiiii	R0 ^ imm → R0	1	—
XOR.B	#imm,@(R0,GBR)	11001110iiiiiiii	(R0 + GBR) ^ imm → (R0 + GBR)	3	—

Table 2.15 Shift Instructions

Instruction	Instruction Code	Operation	Execution Cycles	T Bit
ROTL Rn	0100nnnn00000100	T ← Rn ← MSB	1	MSB
ROTR Rn	0100nnnn00000101	LSB → Rn → T	1	LSB
ROTCL Rn	0100nnnn00100100	T ← Rn ← T	1	MSB
ROTCR Rn	0100nnnn00100101	T → Rn → T	1	LSB
SHAL Rn	0100nnnn00100000	T ← Rn ← 0	1	MSB
SHAR Rn	0100nnnn00100001	MSB → Rn → T	1	LSB
SHLL Rn	0100nnnn00000000	T ← Rn ← 0	1	MSB
SHLR Rn	0100nnnn00000001	0 → Rn → T	1	LSB
SHLL2 Rn	0100nnnn00001000	Rn<<2 → Rn	1	—
SHLR2 Rn	0100nnnn00001001	Rn>>2 → Rn	1	—
SHLL8 Rn	0100nnnn00011000	Rn<<8 → Rn	1	—
SHLR8 Rn	0100nnnn00011001	Rn>>8 → Rn	1	—
SHLL16 Rn	0100nnnn00101000	Rn<<16 → Rn	1	—
SHLR16 Rn	0100nnnn00101001	Rn>>16 → Rn	1	—

Table 2.16 Branch Instructions

Instruction	Instruction Code	Operation	Execution Cycles	T Bit
BF label	10001011dddddddd	If T = 0, disp × 2 + PC → PC; if T = 1, nop	3/1*	—
BT label	10001001dddddddd	If T = 1, disp × 2 + PC → PC; if T = 0, nop	3/1*	—
BRA label	1010dddddddddddd	Delayed branch, disp × 2 + PC → PC	2	—
BSR label	1011dddddddddddd	Delayed branch, PC → PR, disp × 2 + PC → PC	2	—
JMP @Rm	0100mmmm00101011	Delayed branch, Rm → PC	2	—
JSR @Rm	0100mmmm00001011	Delayed branch, PC → PR, Rm → PC	2	—
RTS	0000000000001011	Delayed branch, PR → PC	2	—

Note: * The execution state is three cycles when program branches, and one cycle when program does not branch.

Table 2.17 System Control Instructions

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
CLRT		0000000000001000	0 → T	1	0
CLRMAC		0000000000101000	0 → MACH, MACL	1	—
LDC	Rm,SR	0100mmmm00001110	Rm → SR	1	LSB
LDC	Rm,GBR	0100mmmm00011110	Rm → GBR	1	—
LDC	Rm,VBR	0100mmmm00101110	Rm → VBR	1	—
LDC.L	@Rm+,SR	0100mmmm00000111	(Rm) → SR, Rm + 4 → Rm	3	LSB
LDC.L	@Rm+,GBR	0100mmmm00010111	(Rm) → GBR, Rm + 4 → Rm	3	—
LDC.L	@Rm+,VBR	0100mmmm00100111	(Rm) → VBR, Rm + 4 → Rm	3	—
LDS	Rm,MACH	0100mmmm00001010	Rm → MACH	1	—
LDS	Rm,MACL	0100mmmm00011010	Rm → MACL	1	—
LDS	Rm,PR	0100mmmm00101010	Rm → PR	1	—
LDS.L	@Rm+,MACH	0100mmmm00000110	(Rm) → MACH, Rm + 4 → Rm	1	—
LDS.L	@Rm+,MACL	0100mmmm00010110	(Rm) → MACL, Rm + 4 → Rm	1	—
LDS.L	@Rm+,PR	0100mmmm00100110	(Rm) → PR, Rm + 4 → Rm	1	—
NOP		0000000000001001	No operation	1	—
RTE		0000000000101011	Delayed branch, stack area → PC/SR	4	—
SETT		0000000000011000	1 → T	1	1
SLEEP		0000000000011011	Sleep	3*	—
STC	SR,Rn	0000nnnn00000010	SR → Rn	1	—
STC	GBR,Rn	0000nnnn00010010	GBR → Rn	1	—
STC	VBR,Rn	0000nnnn00100010	VBR → Rn	1	—
STC.L	SR,@–Rn	0100nnnn00000011	Rn–4 → Rn, SR → (Rn)	2	—
STC.L	GBR,@–Rn	0100nnnn00010011	Rn–4 → Rn, GBR → (Rn)	2	—
STC.L	VBR,@–Rn	0100nnnn00100011	Rn–4 → Rn, VBR → (Rn)	2	—
STS	MACH,Rn	0000nnnn00001010	MACH → Rn	1	—

Note: * The number of execution states before the chip enters the sleep state.

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
STS	MACL,Rn	0000nnnn00011010	MACL → Rn	1	—
STS	PR,Rn	0000nnnn00101010	PR → Rn	1	—
STS.L	MACH,@–Rn	0100nnnn00000010	Rn–4 → Rn, MACH → (Rn)	1	—
STS.L	MACL,@–Rn	0100nnnn00010010	Rn–4 → Rn, MACL → (Rn)	1	—
STS.L	PR,@–Rn	0100nnnn00100010	Rn–4 → Rn, PR → (Rn)	1	—
TRAPA	#imm	11000011iiiiiiii	PC/SR → stack area, (imm × 4 + VRR) → PC	8	—

Notes: The execution cycles shown in the table are minimums.

The actual number of cycles may be increased:

1. When contention occurs between instruction fetches and data access
2. When the destination register of the load instruction (memory → register) and the register used by the next instruction are the same.

2.4.2 Operation Code Map

Table 2.18 shows an operation code map.

Table 2.18 Operation Code Map

Instruction Code				Fx: 0000	Fx: 0001	Fx: 0010	Fx: 0011–1111
MSB			LSB	MD: 00	MD: 01	MD: 10	MD: 11
0000	Rn	Fx	0000				
0000	Rn	Fx	0001				
0000	Rn	Fx	0010	STC SR,Rn	STC GBR,Rn	STC VBR,Rn	
0000	Rn	Fx	0011				
0000	Rn	Rm	01MD	MOV.B Rm, @(R0,Rn)	MOV.W Rm, @(R0,Rn)	MOV.L Rm, @(R0,Rn)	
0000	0000	Fx	1000	CLRT	SETT	CLRMAC	
0000	0000	Fx	1001	NOP	DIV0U		
0000	0000	Fx	1010				
0000	0000	Fx	1011	RTS	SLEEP	RTE	
0000	Rn	Fx	1000				
0000	Rn	Fx	1001			MOVT Rn	
0000	Rn	Fx	1010	STS MACH,Rn	STS MACL,Rn	STS PR,Rn	
0000	Rn	Rm	1011				
0000	Rn	Rm	11MD	MOV.B @(R0,Rm),Rn	MOV.W @(R0,Rm),Rn	MOV.L @(R0,Rm),Rn	
0001	Rn	Rm	disp	MOV.L Rm,@(disp:4,Rn)			
0010	Rn	Rm	00MD	MOV.B Rm,@Rn	MOV.W Rm,@Rn	MOV.L Rm,@Rn	
0010	Rn	Rm	01MD	MOV.B Rm,@-Rn	MOV.W Rm,@-Rn	MOV.L Rm,@-Rn	DIV0S Rm,Rn
0010	Rn	Rm	10MD	TST Rm,Rn	AND Rm,Rn	XOR Rm,Rn	OR Rm,Rn
0010	Rn	Rm	11MD	CMP/STR Rm,Rn	XTRCT Rm,Rn	MULU Rm,Rn	MULS Rm,Rn
0011	Rn	Rm	00MD	CMP/EQ Rm,Rn		CMP/HS Rm,Rn	CMP/GE Rm,Rn
0011	Rn	Rm	01MD	DIV1 Rm,Rn		CMP/HI Rm,Rn	CMP/GT Rm,Rn
0011	Rn	Rm	10MD	SUB Rm,Rn		SUBC Rm,Rn	SUBV Rm,Rn
0011	Rn	Rm	11MD	ADD Rm,Rn		ADDC Rm,Rn	ADDV Rm,Rn
0100	Rn	Fx	0000	SHLL Rn		SHAL Rn	
0100	Rn	Fx	0001	SHLR Rn	CMP/PZ Rn	SHAR Rn	
0100	Rn	Fx	0010	STS.L MACH, @–Rn	STS.L MACL, @–Rn	STS.L PR, @–Rn	

Instruction Code				Fx: 0000	Fx: 0001	Fx: 0010	Fx: 0011–1111
MSB			**LSB**	**MD: 00**	**MD: 01**	**MD: 10**	**MD: 11**
0100	Rn	Fx	0011	STC.L SR,@–Rn	STC.L GBR,@–Rn	STC.L VBR,@–Rn	
0100	Rn	Fx	0100	ROTL Rn		ROTCL Rn	
0100	Rn	Fx	0101	ROTR Rn	CMP/PL Rn	ROTCR Rn	
0100	Rm	Fx	0110	LDS.L @Rm+,MACH	LDS.L @Rm+,MACL	LDS.L @Rm+,PR	
0100	Rm	Fx	0111	LDC.L @Rm+,SR	LDC.L @Rm+,GBR	LDC.L @Rm+,VBR	
0100	Rn	Fx	1000	SHLL2 Rn	SHLL8 Rn	SHLL16 Rn	
0100	Rn	Fx	1001	SHLR2 Rn	SHLR8 Rn	SHLL16 Rn	
0100	Rm	Fx	1010	LDS Rm,MACH	LDS Rm,MACL	LDS Rm,PR	
0100	Rm/Rn	Fx	1011	JSR @Rm	TAS.B @Rn	JMP @Rm	
0100	Rm	Fx	1100				
0100	Rm	Fx	1101				
0100	Rn	Fx	1110	LDC Rm,SR	LDC Rm,GBR	LDC Rm,VBR	
0100	Rn	Rm	1111	MAC.W @Rm+,@Rn+			
0101	Rn	Rm	disp	MOV.L @(disp:4,Rm),Rn			
0110	Rn	Rm	00MD	MOV.B @Rm,Rn	MOV.W @Rm,Rn	MOV.L @Rm,Rn	MOV Rm,Rn
0110	Rn	Rm	01MD	MOV.B @Rm+,Rn	MOV.W @Rm+,Rn	MOV.L @Rm+,Rn	NOT Rm,Rn
0110	Rn	Rm	10MD	SWAP.B Rm,Rn	SWAP.W Rm,Rn	NEGC Rm,Rn	NEG Rm,Rn
0110	Rn	Rm	11MD	EXTU.B Rm,Rn	EXTU.W Rm,Rn	EXTS.B Rm,Rn	EXTS.W Rm,Rn
0111	Rn	imm		ADD #imm:8,Rn			
1000	00MD	Rn	disp	MOV.B R0, @(disp:4,Rn)	MOV.W R0, @(disp:4,Rn)		
1000	01MD	Rm	disp	MOV.B @(disp:4, Rm),R0	MOV.W @(disp:4, Rm),R0		
1000	10MD	imm/disp		CMP/EQ #imm:8,R0	BT disp:8		BF disp:8
1000	11MD	imm/disp					
1001	Rn	disp		MOV.W @(disp:8,PC),Rn			
1010	disp			BRA disp:12			
1011	disp			BSR disp:12			

Instruction Code			Fx: 0000	Fx: 0001	Fx: 0010	Fx: 0011–1111
MSB	LSB		MD: 00	MD: 01	MD: 10	MD: 11
1100	00MD	imm/disp	MOV.B R0,@(disp:8,GBR)	MOV.W R0,@(disp:8,GBR)	MOV.L R0,@(disp:8,GBR)	TRAPA #imm:8
1100	01MD	disp	MOV.B @(disp:8,GBR),R0	MOV.W @(disp:8,GBR),R0	MOV.L @(disp:8,GBR),R0	MOVA @(disp:8,PC),R0
1100	10MD	imm	TST #imm:8,R0	AND #imm:8,R0	XOR #imm:8,R0	OR #imm:8,R0
1100	11MD	imm	TST.B #imm:8,@(R0,GBR)	AND.B #imm:8,@(R0,GBR)	XOR.B #imm:8,@(R0,GBR)	OR.B #imm:8,@(R0,GBR)
1101	Rn	disp	MOV.L @(disp:8,PC),Rn			
1110	Rn	imm	MOV #imm:8,Rn			
1111		...				

2.5 CPU State

2.5.1 State Transitions

The CPU has five processing states: reset, exception handling, bus-released, program execution and power-down. The transitions between the states are shown in figure 2.6. For more information on the reset and exception handling states, see section 4, Exception Handling. For details on the power-down state, see section 19, Power-Down State.

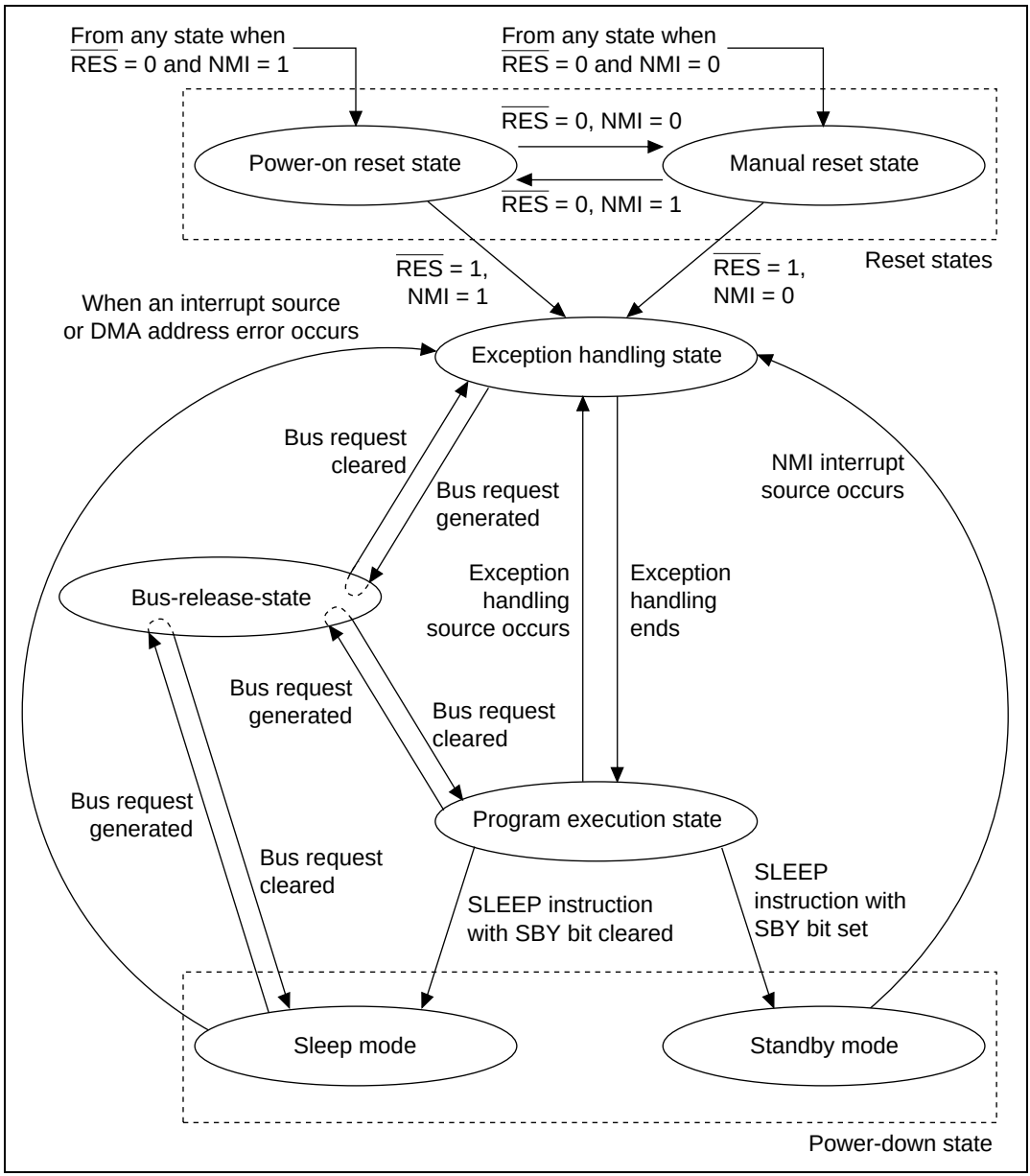


Figure 2.6 Transitions Between Processing States

Reset State: In the reset state the CPU is reset. This occurs when the $\overline{\text{RES}}$ pin level goes low. When the NMI pin is high, the result is a power-on reset; when it is low, a manual reset will occur. When turning on the power, be sure to carry out a power-on reset.

In a power-on reset, all CPU internal states and on-chip supporting module registers are initialized. In a manual reset, all CPU internal states and on-chip supporting module registers, with the exception of the bus state controller (BSC) and pin function controller (PFC), are initialized. In a manual reset, the BSC is not initialized, so refresh operations will continue.

Exception Handling State: Exception handling is a transient state that occurs when the CPU's processing state flow is altered by exception handling sources such as resets or interrupts.

In a reset, the initial values of the program counter PC (execution start address) and stack pointer SP are fetched from the exception vector table and stored; the CPU then branches to the execution start address and execution of the program begins.

For an interrupt, the stack pointer (SP) is accessed and the program counter (PC) and status register (SR) are saved to the stack area. The exception handling routine start address is fetched from the exception vector table; the CPU then branches to that address and the program starts executing, thereby entering the program execution state.

Program Execution State: In the program execution state, the CPU sequentially executes the program.

Power-Down State: In the power-down state, CPU operation halts and power consumption decreases. The SLEEP instruction places the CPU in the power-down state. This state has two modes: sleep mode and standby mode.

Bus-Released State: In the bus-released state, the CPU releases the bus to the device that has requested it.

2.5.2 Power-Down State

In addition to the ordinary program execution states, the CPU also has a power-down state in which CPU operation halts and power consumption is reduced There are two power-down state modes: sleep mode and standby mode.

Sleep Mode: When the standby bit SBY (in the standby control register, SBYCR) is cleared to 0 and a SLEEP instruction is executed, the CPU switches from program execution state to sleep mode. In sleep mode, the CPU halts and the contents of its internal registers and the data in on-chip RAM are stored. The on-chip supporting modules other than the CPU do not halt in sleep mode.

Sleep mode is cleared by a reset, any interrupt, or a DMA address error; the CPU returns to ordinary program execution state through the exception handling state.

Software Standby Mode: To enter standby mode, set standby bit SBY (in the standby control register, SBYCR) to 1 and execute a SLEEP instruction. In standby mode, all CPU, on-chip supporting module and oscillator functions are halted. CPU internal register contents and on-chip RAM data are held.

Standby mode is cleared by a reset or an external NMI interrupt. For resets, the CPU returns to the ordinary program execution state through the exception handling state when placed in a reset state during the oscillator settling time. For NMI interrupts, the CPU returns to the ordinary program execution state through the exception handling state after the oscillator settling time has elapsed. In this mode, power consumption drops markedly, since the oscillator stops.

Table 2.19 Power-Down State

		State						
Mode	**Conditions**	**Clock**	**CPU**	**On-Chip Supporting Modules**	**CPU Regi-sters**	**RAM**	**I/O Ports**	**Canceling**
Sleep mode	Execute SLEEP instruction with SBY bit cleared to 0 in SBYCR	Run	Halted	Run	Held	Held	Held	1. Interrupt 2. DMA address error 3. Power-on reset 4. Manual reset
Standby mode	Execute SLEEP instruction with SBY bit set to 1 in SBYCR	Halted	Halted	Halted and initialized*	Held	Held	Held or high-Z* (select-able)	1. NMI 2. Power-on reset 3. Manual reset

Note: * Differs depending on the supporting module and pin.

Section 3 Operating Modes

3.1 Types of Operating Modes and Their Selection

The SH7032 microcomputer operates in one of two operating modes (modes 0 and 1) and the SH7034 operates in one of four operating modes (modes 0, 1, 2, and 7). Modes 0 and 1 differ in the bus width of memory area 0. The mode is selected by the mode pins (MD2–MD0) as indicated in table 3.1. Do not change the mode selection while the chip is operating.

Table 3.1 Operating Mode Selection

	Pin Settings				
Operating Mode	**MD2**	**MD1**	**MD0**	**Mode Name**	**Bus Width of Area 0**
Mode 0*2	0	0	0	MCU mode 0	8 bits
Mode 1*2	0	0	1	MCU mode 1	16 bits
Mode 2	0	1	0	MCU mode 2	On-chip ROM
Mode 7*1	1	1	1	PROM mode	—

Notes: 1. SH7034 PROM version only
2. Only modes 0 and 1 are available in the SH7032 and SH7034 ROMless version.

3.2 Operating Mode Descriptions

3.2.1 Mode 0 (MCU Mode 0)

In mode 0, memory area 0 has an eight-bit bus width. For the memory map, see section 8, Bus State Controller (BSC).

3.2.2 Mode 1 (MCU Mode 1)

In mode 1, memory area 0 has a 16-bit bus width.

3.2.3 Mode 2 (MCU Mode 2)

In mode 2, memory area 0 is assigned to the on-chip ROM. Mode 2 should only be set for the product is the SH7034.

3.2.4 Mode 7 (PROM Mode)

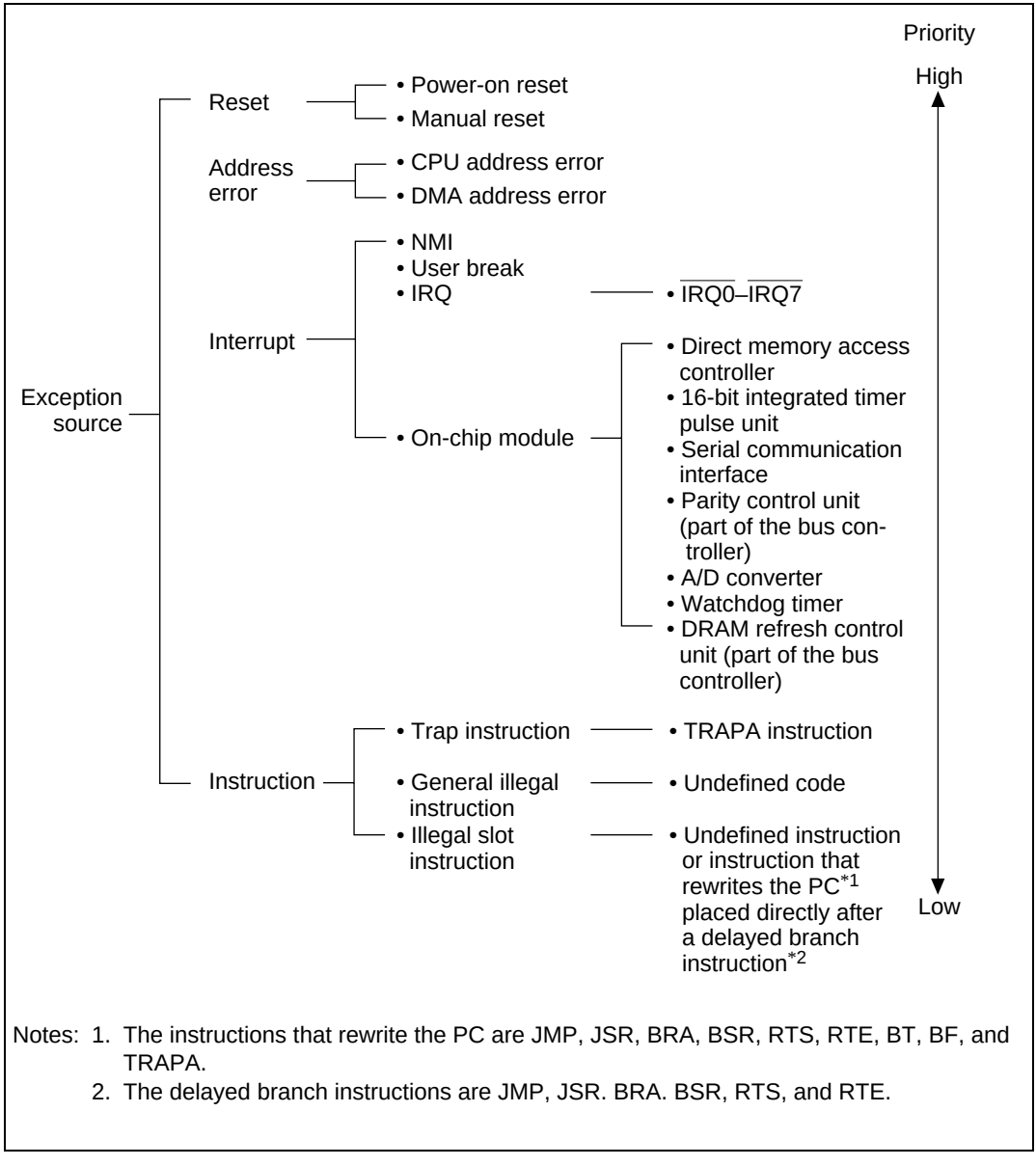
Mode 7 is a PROM mode. In this mode, the PROM can be programmed. For details, see section 17, ROM. Mode 7 should only be set for the SH7034 (PROM version).

Section 4 Exception Handling

4.1 Overview

4.1.1 Exception Handling Types and Priorities

As figure 4.1 indicates, exception handling may be caused by a reset, address error, interrupt, or instruction. Exception sources are prioritized as indicated in figure 4.1. If two or more exceptions occur simultaneously, they are accepted and handled in the priority order shown.



Notes: 1. The instructions that rewrite the PC are JMP, JSR, BRA, BSR, RTS, RTE, BT, BF, and TRAPA.
2. The delayed branch instructions are JMP, JSR. BRA. BSR, RTS, and RTE.

Figure 4.1 Exception Source Types and Priority

4.1.2 Exception Handling Operation

Exception sources are detected at the times indicated in table 4.1, whereupon handling starts.

Table 4.1 Exception Source Detection and Start of Handling

Exception Type		Source Detection and Start of Handling
Reset	Power-on	Low-to-high transition at $\overline{\text{RES}}$ pin when NMI is high
	Manual	Low-to-high transition at $\overline{\text{RES}}$ pin when NMI is low
Address error		Detected when instruction is decoded and starts after the instruction that was executing prior to this point is completed.
Interrupt		Detected when instruction is decoded and starts after the instruction that was executing prior to this point is completed.
Instruction	Trap instruction	Starts when a trap instruction (TRAPA) is executed.
	General illegal instruction	Starts when undefined code is decoded at a position other than directly after a delayed branch instruction (a delay slot).
	Illegal slot instruction	Starts when undefined code or an instruction that rewrites the PC is decoded directly after a delayed branch instruction (in a delay slot).

When exception handling begins, the CPU operates as follows:

Resets: The initial values of the program counter (PC) and stack pointer (SP) are read from the exception vector table (the respective PC and SP values are H'00000000 and H'00000004 for a power-on reset and H'00000008 and H'0000000C for a manual reset). For more information on the exception vector table, see section 4.1.3, Exception Vector Table. Next, the vector base register (VBR) is cleared to zero and interrupt mask bits (I3–I0) in the status register (SR) are set to 1111. Program execution starts from the PC address read from the exception vector table.

Address Errors, Interrupts and Instructions: SR and PC are pushed onto the stack indicated in R15. For interrupts, the interrupt priority level is written in the interrupt mask bits (I3–I0). For address errors and instructions, bits I3–I0 are not affected. Next, the start address is fetched from the exception vector table, and program execution starts from this address.

4.1.3 Exception Vector Table

Before exception handling can execute, the exception vector table must be set in memory. The exception vector table holds the start addresses of exception handling routines (the table for reset exception handling stores initial PC and SP values). Different vector numbers and vector table address offsets are assigned to different exception sources. The vector table addresses are calculated from the corresponding vector numbers and vector address offsets. In exception handling, the exception handling routine start address is fetched from the exception vector table indicated by this vector table address.

Table 4.2 lists vector numbers and vector table address offsets. Table 4.3 shows how vector table addresses are calculated.

Table 4.2 Exception Vector Table

Exception Source		Vector Number	Vector table Address Offset
Power-on reset	PC	0	H'00000000–H'00000003
	SP	1	H'00000004–H'00000007
Manual reset	PC	2	H'00000008–H'0000000B
	SP	3	H'0000000C–H'0000000F
General illegal instruction		4	H'00000010–H'00000013
(Reserved for system use)		5	H'00000014–H'00000017
Illegal slot instruction		6	H'00000018–H'0000001B
(Reserved for system use)		7	H'0000001C–H'0000001F
		8	H'00000020–H'00000023
CPU address error		9	H'00000024–H'00000027
DMA address error		10	H'00000028–H'0000002B
Interrupts	NMI	11	H'0000002C–H'0000002F
	User break	12	H'00000030–H'00000033
(Reserved for system use)		13–31	H'00000034–H'00000037 to H'0000007C–H'0000007F
Trap instruction (user vectors)		32–63	H'00000080–H'00000083 to H'000000FC–H'000000FF
Interrupts	IRQ0	64	H'00000100–H'00000103
	IRQ1	65	H'00000104–H'00000107
	IRQ2	66	H'00000108–H'0000010B
	IRQ3	67	H'0000010C–H'0000010F
	IRQ4	68	H'00000110–H'00000113
	IRQ5	69	H'00000114–H'00000117
	IRQ6	70	H'00000118–H'0000011B
	IRQ7	71	H'0000011C–H'0000011F
	On-chip modules*	72–255	H'00000120–H'00000123 to H'000003FC–H'000003FF

Note: * See table 5.3, Interrupt Exception Vectors and Rankings, in section 5, Interrupt Controller (INTC), for details on vector numbers and vector table address offsets of individual on-chip supporting module interrupts.

Table 4.3 Calculation of Exception Vector Table Addresses

Exception Source	Calculation of Vector Table Address
Reset	(Vector table address) = (vector table address offset) = (vector number) × 4
Address error, interrupt, instructions	(Vector table address) = VBR + (vector table address offset) = VBR + (vector number) × 4

Note: VBR: Vector base register. For vector table address offsets and vector numbers, see table 4.2.

4.2 Resets

4.2.1 Reset Types

A reset is the highest-priority exception. There are two types of reset: power-on reset and manual reset. As table 4.4 shows, a power-on reset initializes the internal state of the CPU and all registers of the on-chip supporting modules. A manual reset initializes the internal state of the CPU and all registers of the on-chip supporting modules except the bus state controller (BSC), pin function controller (PFC), and I/O ports (I/O).

Table 4.4 Reset Types

	Transition Conditions		Internal State	
Reset	**NMI**	**RES**	**CPU**	**On-Chip Supporting Modules**
Power-on Reset	High	Low	Initialized	Initialized
Manual Reset	Low	Low	Initialized	All initialized except BSC, PFC, and I/O

4.2.2 Power-On Reset

When the NMI pin is high, a low input at the $\overline{\text{RES}}$ pin drives the chip into the power-on reset state. The $\overline{\text{RES}}$ pin should be driven low while the clock pulse generator (CPG) is stopped (or while the CPG is operating during the oscillation settling time) for at least 20 t_{cyc} to assure that the chip is reset. A power-on reset initializes the internal state of the CPU and all registers of the on-chip supporting modules. For pin states in the power-on reset state, see appendix B, Pin States.

While the NMI pin remains high, if the $\overline{\text{RES}}$ pin is held low for a certain time then driven high in the power-on state, power-on reset exception handling begins. The CPU then:

1. Reads the start address (initial PC value) from the exception vector table.
2. Reads the initial stack pointer value (SP) from the exception vector table.
3. Clears the vector base register (VBR) to H'00000000, and sets interrupt mask bits I3–I0 in the status register (SR) to H'F (1111).
4. Loads the values read from the exception vector table into the PC and SP and starts program execution.

A power-on reset must be executed when turning on power.

4.2.3 Manual Reset

When the NMI pin is high, a low input at the $\overline{\text{RES}}$ pin drives the chip into the manual reset state. To ensure that the chip is properly reset, drive the $\overline{\text{RES}}$ pin low for at least 20 t_{cyc}. A manual reset initializes the internal state of the CPU and all registers of the on-chip supporting modules except the bus state controller, pin function controller, and I/O ports. Since a manual reset does not affect the bus state controller, the DRAM refresh control function operates even if the manual reset state continues for a long time. When a manual reset is performed during the bus cycle, manual reset exception handling is deferred until the end of the bus cycle. The manual reset thus cannot be used to abort the bus cycle. For the pin states during the manual reset state, see appendix B, Pin States.

While the NMI pin remains low, if the $\overline{\text{RES}}$ pin is held low for a certain time then driven high in the manual reset state, manual reset exception handling begins. The CPU carries out the same operations as for a power-on reset.

4.3 Address Errors

4.3.1 Address Error Sources

Address errors occur during instruction fetches and data reading/writing as shown in table 4.5.

Table 4.5 Address Error Sources

	Bus Cycle		
Type	**Bus Master**	**Operation**	**Address Error**
Instruction fetch	CPU	Instruction fetch from even address	None (normal)
		Instruction fetch from odd address	Address error
		Instruction fetch from outside on-chip supporting module space	None (normal)
		Instruction fetch from on-chip supporting module space	Address error
Data read/write	CPU or DMAC	Access to word data from even address	None (normal)
		Access to word data from odd address	Address error
		Access to longword data aligned on longword boundary	None (normal)
		Access to longword data not aligned on longword boundary	Address error
		Access to word or byte data in on-chip supporting module space*	None (normal)
		Access to longword data in 16-bit on-chip supporting module space*	None (normal)
		Access to longword data in 8-bit on-chip supporting module space*	Address error

Note: * See section 8, Bus State Controller (BSC), for details on the on-chip supporting module space.

4.3.2 Address Error Exception Handling

When an address error occurs, address error exception handling starts after both the bus cycle that caused the address error and the instructions that were being executed at that time, have been completed. The CPU then:

1. Pushes SR onto the stack.
2. Pushes the program counter onto the stack. The PC value saved is the start address of the instruction following the last instruction to be executed.
3. Fetches the exception handling routine start address from the exception vector table for the address error that occurred and starts program execution from that address. The branch that occurs here is not a delayed branch.

4.4 Interrupts

4.4.1 Interrupt Sources

Table 4.6 lists the types of interrupt exception handling sources (NMI, user break, IRQ, on-chip supporting module).

Table 4.6 Interrupt Sources

Interrupt	Requesting Pin or Module	Number of Sources
NMI	NMI pin (external input)	1
User break	User break controller	1
IRQ	$\overline{\text{IRQ0}}$–$\overline{\text{IRQ7}}$ pin (external input)	8
On-chip supporting module	Direct Memory Access Controller	4
	16-bit integrated timer pulse unit	15
	Serial communication interface	8
	A/D converter	1
	Watchdog timer	1
	Bus state controller	2

Each interrupt source has a different vector number and vector address offset value. See table 5.3, Interrupt Exception Vectors and Rankings, in section 5, Interrupt Controller (INTC), for details on vector numbers and vector table address offsets.

4.4.2 Interrupt Priority Rankings

Interrupt sources are assigned priorities. When multiple interrupts occur at the same time, the interrupt controller (INTC) ascertains their priorities and starts exception handling based on its findings. Priorities from 16–0 can be assigned, with 0 the lowest level and 16 the highest. NMI has priority level 16 and cannot be masked. NMI is always accepted. The user break priority level is 15. The IRQ and on-chip supporting module interrupt priority levels can be set in interrupt priority level registers A–E (IPRA–IPRE) as shown in table 4.7. Priority levels 0–15 can be set. See section 5.3.1, Interrupt Priority Registers A-E (IPRA–IPRE), for details.

Table 4.7 Interrupt Priority Rankings

Type	Priority	Comments
NMI	16	Fixed and unmaskable
User break	15	Fixed
IRQ and on-chip supporting modules	0–15	Set in interrupt priority level registers A–E (IPRA–IPRE)

4.4.3 Interrupt Exception Handling

When an interrupt is generated, the INTC ascertains the interrupt ranking. NMI is always accepted, but other interrupts are only accepted if their ranking is higher than the ranking set in the interrupt mask bits (I3–I0) of SR.

When an interrupt is accepted, interrupt exception handling begins. In the interrupt exception handling sequence, the SR and PC values are pushed onto the stack, and the priority level of the accepted interrupt is copied to the interrupt mask level bits (I3–I0) in SR. In NMI exception handling, the priority ranking is 16 but the value 15 (H'F) is stored in I3–I0. The exception handling routine start address for the accepted interrupt is fetched from the exception vector table and the program branches to that address and starts executing. For further information on interrupts, see section 5.4, Interrupt Operation.

4.5 Instruction Exceptions

4.5.1 Types of Instruction Exceptions

Table 4.8 shows the three types of instruction that start exception handling (trap instructions, illegal slot instructions, and general illegal instructions).

Table 4.8 Types of Instruction Exceptions

Type	Source Instruction	Comments
Trap instruction	TRAPA	—
Illegal slot instruction	Undefined code or instruction that rewrites the PC located immediately after a delayed branch instruction (delay slot)	Delayed branch instructions are: JMP, JSR, BRA, BSR, RTS, RTE. Instructions that rewrite the PC are: JMP, JSR, BRA, BSR, RTS, RTE, BT, BF, and TRAPA
General illegal instructions	Undefined code in other than delay slot	—

4.5.2 Trap Instruction

Trap instruction exception handling is carried out when a trap instruction (TRAPA) is executed. The CPU then:

1. Saves the status register by pushing register contents onto the stack.
2. Pushes the program counter value onto the stack. The PC value saved is the start address of the next instruction after the TRAPA instruction.
3. Reads the exception handling routine start address from the vector table corresponding to the vector number specified in the TRAPA instruction, branches to that address, and starts program execution. The branch is not a delayed branch.

4.5.3 Illegal Slot Instruction

An instruction located immediately after a delayed branch instruction is called an “instruction placed in a delay slot.” If an undefined instruction is located in a delay slot, illegal slot instruction exception handling begins executing when the undefined code is decoded. Illegal slot instruction exception handling also begins when the instruction located in the delay slot is an instruction that rewrites the program counter. In this case, exception handling begins when the instruction that rewrites the PC is decoded. The CPU performs illegal slot exception handling as follows:

1. Saves the status register onto the stack.
2. Pushes the program counter value onto the stack. The PC value saved is the branch destination address of the delayed branch instruction immediately before the instruction that contains the undefined code or rewrites the PC.
3. Fetches the exception handling routine start address from the vector table corresponding to the exception that occurred, branches to that address, and starts executing the program. The branch is not a delayed branch.

4.5.4 General Illegal Instructions

If an undefined instruction located other than in a delay slot (immediately after a delayed branch instruction) is decoded, general illegal instruction exception handling is executed. The CPU follows the same procedure as for illegal slot exception handling, except that the program counter (PC) value pushed on the stack in general illegal instruction exception handling is the start address of the illegal instruction with the undefined code.

4.6 Cases in which Exceptions are Not Accepted

In some cases, address errors and interrupts that directly follow a delayed branch instruction or interrupt-disabled instruction are not accepted immediately. Table 4.9 lists these cases. When this occurs, the exception is accepted when an instruction that can accept the exception is decoded.

Table 4.9 Cases in which Exceptions are Not Accepted

	Exception Source	
Case	**Address Error**	**Interrupt**
Immediately after delayed branch instruction*1	X	X
Immediately after interrupt-disabled instruction*2	O	X

X: Not accepted

O: Accepted

Notes: 1. Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE

2. Interrupt-disabled instructions: LDC, LDC.L, STC, STC.L, LDS, LDS.L, STS, STS.L

4.6.1 Immediately after Delayed Branch Instruction

Address errors and interrupts are not accepted when an instruction in a delay slot immediately following a delayed branch instruction is decoded. The delayed branch instruction and the instruction in the delay slot are therefore always executed one after the other. Exception handling is never inserted between them.

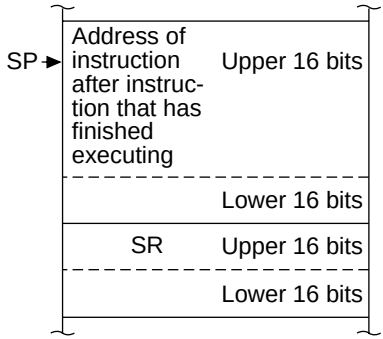
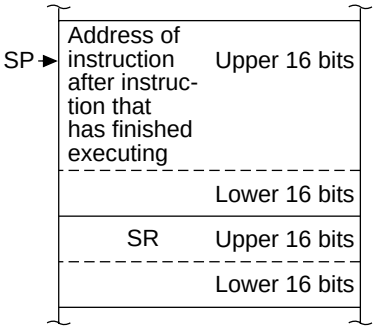
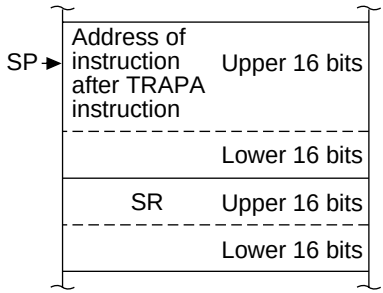
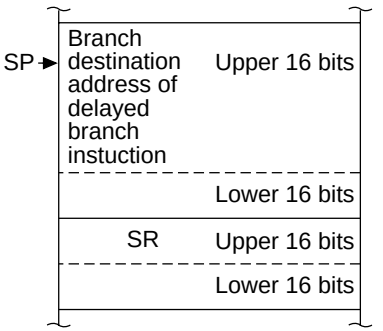
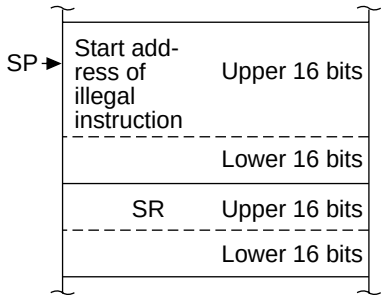
4.6.2 Immediately after Interrupt-Disabling Instruction

Interrupts are not accepted when the instruction immediately following an interrupt-disabled instruction is decoded. Address errors are accepted, however.

4.7 Stack Status after Exception Handling

Table 4.10 shows the stack after exception handling.

Table 4.10 Stack after Exception Handling

Type	Stack Status	Type	Stack Status
Address error		Interrupt	
Trap instruction		Illegal slot instruction	
General illegal instruction			

Note: Stack status is based on a bus width of 16 bits.

4.8 Notes

4.8.1 Value of the Stack Pointer (SP)

An address error occurs if the stack is accessed for exception handling when the value of the stack pointer (SP) is not a multiple of four. Therefore, a multiple of four should always be stored in the SP.

4.8.2 Value of the Vector Base Register (VBR)

An address error occurs if the vector table is accessed for exception handling when the value of the vector base register (VBR) is not a multiple of four. Therefore, VBR should always be set to a multiple of four.

4.8.3 Address Errors Caused by Stacking During Address Error Exception Handling

If the stack pointer is not a multiple of four, address errors will occur in the exception handling (interrupt, etc.) stacking. After the exception handling ends, the CPU will then shift to address error exception handling. An address error will also occur during the address error exception handling stacking, but the CPU is set up to ignore the address error so that it can avoid an infinite series of address errors. This allows it to shift program control to the address error exception handling routine and handle the error.

When an address error does occur in exception handling stacking, the stacking bus cycle (write) is executed. In SR and PC stacking, four is subtracted from each of the SPs so the SP values are not multiples of four after stacking either. Since the address value output during stacking is the SP value, the address that produced the error is exactly what is output. In such cases, the stacked write data will be undefined.

Section 5 Interrupt Controller (INTC)

5.1 Overview

The interrupt controller (INTC) determines the priority of interrupt sources and controls interrupt requests to the CPU. INTC has registers for assigning priority levels to interrupt sources. These registers handle interrupt requests according to user-specified priorities.

5.1.1 Features

The interrupt controller has the following features:

- 16 settable priority levels: Five interrupt priority registers can set 16 levels of interrupt priorities for IRQ and on-chip supporting module interrupt sources.
- NMI noise canceller function: INTC has an NMI input level bit that indicates the NMI pin status. By reading this bit in the interrupt exception handling routine, the pin status can be checked for use in a noise canceller function.
- The interrupt controller can notify external devices (via the $\overline{\text{IRQOUT}}$ pin) that an on-chip interrupt has occurred. In this way an external device can, for example, be informed if an on-chip interrupt occurs while the chip is operating in bus-released mode and the bus has been requested.

5.1.2 Block Diagram

Figure 5.1 shows a block diagram of the interrupt controller.

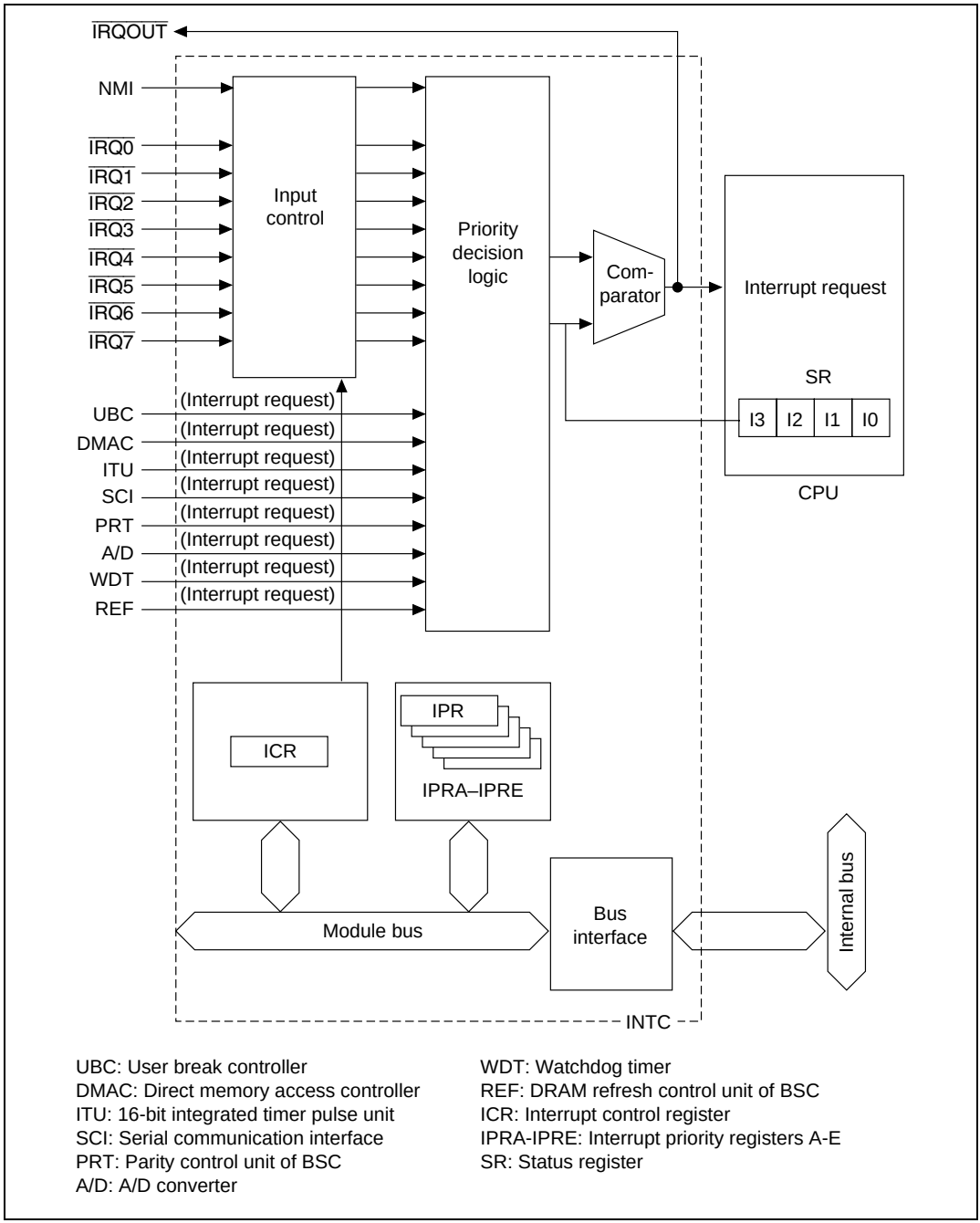


Figure 5.1 Block Diagram of Interrupt Controller

5.1.3 Pin Configuration

INTC pins are summarized in table 5.1.

Table 5.1 INTC Pin Configuration

Name	Abbr.	I/O	Function
Nonmaskable interrupt input pin	NMI	I	Inputs a non-maskable interrupt request signal.
Interrupt request input pins	$\overline{\text{IRQ0}}$–$\overline{\text{IRQ7}}$	I	Inputs maskable interrupt request signals.
Interrupt request output pin	$\overline{\text{IRQOUT}}$	O	Outputs a signal indicating an interrupt source has occurred.

5.1.4 Registers

The interrupt controller has six registers as listed in table 5.2. These registers are used for setting interrupt priority levels and controlling the detection of external interrupt input signals.

Table 5.2 Interrupt Controller Register Configuration

Name	Abbr.	R/W	Address*2	Initial Value	Bus width
Interrupt priority register A	IPRA	R/W	H'5FFFF84	H'0000	8, 16, 32
Interrupt priority register B	IPRB	R/W	H'5FFFF86	H'0000	8, 16, 32
Interrupt priority register C	IPRC	R/W	H'5FFFF88	H'0000	8, 16, 32
Interrupt priority register D	IPRD	R/W	H'5FFFF8A	H'0000	8, 16, 32
Interrupt priority register E	IPRE	R/W	H'5FFFF8C	H'0000	8, 16, 32
Interrupt control register	ICR	R/W	H'5FFFF8E	*1	8, 16, 32

Notes: 1. H'8000 when pin NMI is high, H'0000 when pin NMI is low.
2. Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.

5.2 Interrupt Sources

There are four types of interrupt sources: NMI, user break, IRQ, and on-chip supporting module interrupts.

Interrupt rankings are expressed as priority levels (0–16), with 0 the lowest and 16 the highest. An interrupt set to level 0 is masked.

5.2.1 NMI Interrupts

NMI is the highest-priority interrupt (level 16) and is always accepted. Input at the NMI pin is edge-sensed. Either the rising or falling edge can be selected by setting the NMI edge select bit (NMIE) in the interrupt control register (ICR). NMI interrupt exception handling sets the interrupt mask level bits (I3–I0) in the status register (SR) to level 15.

5.2.2 User Break Interrupt

A user break interrupt occurs when a break condition is satisfied in the user break controller (UBC). A user break interrupt has priority level 15. User break interrupt exception handling sets the interrupt mask level bits (I3–I0) in the status register (SR) to level 15. For further details on the user break interrupt, see section 6, User Break Controller (UBC).

5.2.3 IRQ Interrupts

IRQ interrupts are requested by input from pins $\overline{\text{IRQ0}}$–$\overline{\text{IRQ7}}$. IRQ sense select bits 0–7 (IRQ0S–IRQ7S) in the interrupt control register (ICR) can select low-level sensing or falling-edge sensing for each pin independently. Interrupt priority registers A and B (IPRA and IPRB) can select priority levels from 0–15 for each pin. IRQ interrupt exception handling sets the interrupt mask level bits (I3–I0) in the status register (SR) to the priority level value of the IRQ interrupt that was accepted.

5.2.4 On-Chip Interrupts

On-chip interrupts are interrupts generated by the following 6 on-chip supporting modules:

- Direct memory access controller (DMAC)
- 16-bit integrated timer pulse unit (ITU)
- Serial communication interface (SCI)
- Bus state controller (BSC)
- A/D converter (A/D)
- Watchdog timer (WDT)

A different interrupt vector is assigned to each interrupt source, so the exception handling routine does not have to decide which interrupt has occurred. Priority levels 0–15 can be assigned to individual on-chip supporting module in interrupt priority registers C–E (IPRC–IPRE). On-chip interrupt exception handling sets the interrupt mask level bits (I3–I0) in the status register (SR) to the priority level value of the on-chip interrupt that was accepted.

5.2.5 Interrupt Exception Vectors and Priority Rankings

Table 5.3 lists the vector numbers, vector table address offsets, and interrupt priority order of the interrupt sources.

Each interrupt source is allocated a different vector number and vector table address offset. The vector table address is calculated from this vector number and address offset. In interrupt exception handling, the exception handling routine start address is fetched from the vector table indicated by this vector table address. See table 4.3, Calculation of Exception Vector Table Address, in section 4, Exception Handling, for details on this calculation.

Arbitrary interrupt priority levels between 0 and 15 can be assigned to IRQ and on-chip supporting module interrupt sources by setting interrupt priority registers A–E (IPRA–IPRE) for each pin or module. The interrupt sources for IPRC–IPRE, however, must be ranked in the order listed under Priority Within Module in table 5.3 and cannot be changed. A reset assigns priority level 0 to IRQ and on-chip supporting module interrupts. If the same priority level is assigned to two or more interrupt sources, and interrupts from those sources occur simultaneously, their priority order is the default priority order indicated at the right in table 5.3.

Table 5.3 Interrupt Exception Vectors and Rankings

Interrupt Source		Interrupt Priority Order (Initial Value)	IPR (Bit Numbers)	Priority Within Module	Vector No.	Address Offset in Vector Table	Default Priority Order
NMI		16	—	—	11	H'0000002C–H'0000002F	High
User break		15	—	—	12	H'00000030–H'00000033	↑
IRQ0		0–15 (0)	IPRA (15–12)	—	64	H'00000100–H'00000103	
IRQ1		0–15 (0)	IPRA (11–8)	—	65	H'00000104–H'00000107	
IRQ2		0–15 (0)	IPRA (7–4)	—	66	H'00000108–H'0000010B	
IRQ3		0–15 (0)	IPRA (3–0)	—	67	H'0000010C–H'0000010F	
IRQ4		0–15 (0)	IPRB (15–12)	—	68	H'00000110–H'00000113	
IRQ5		0–15 (0)	IPRB (11–8)	—	69	H'00000114–H'00000117	
IRQ6		0–15 (0)	IPRB (7–4)	—	70	H'00000118–H'0000011B	
IRQ7		0–15 (0)	IPRB (3–0)	—	71	H'0000011C–H'0000011F	
DMAC0	DEI0	0–15 (0)	IPRC (15–12)	3	72	H'00000120–H'00000123	
	Reserved			2	73	H'00000124–H'00000127	
DMAC1	DEI1			1	74	H'00000128–H'0000012B	
	Reserved			0	75	H'0000012C–H'0000012F	
DMAC2	DEI2	0–15 (0)	IPRC (11–8)	3	76	H'00000130–H'00000133	
	Reserved			2	77	H'00000134–H'00000137	
DMAC3	DEI3			1	78	H'00000138–H'0000013B	
	Reserved			0	79	H'0000013C–H'0000013F	
ITU0	IMIA0	0–15 (0)	IPRC (7–4)	3	80	H'00000140–H'00000143	
	IMIB0			2	81	H'00000144–H'00000147	
	OVI0			1	82	H'00000148–H'0000014B	
	Reserved			0	83	H'0000014C–H'0000014F	
ITU1	IMIA1	0–15 (0)	IPRC (3–0)	3	84	H'00000150–H'00000153	
	IMIB1			2	85	H'00000154–H'00000157	
	OVI1			1	86	H'00000158–H'0000015B	
	Reserved			0	87	H'0000015C–H'0000015F	
ITU2	IMIA2	0–15 (0)	IPRD (15–12)	3	88	H'00000160–H'00000163	
	IMIB2			2	89	H'00000164–H'00000167	
	OVI2			1	90	H'00000168–H'0000016B	↓
	Reserved			0	91	H'0000016C–H'0000016F	Low

Interrupt Source		Interrupt Priority Order (Initial Value)	IPR (Bit Numbers)	Priority Within Module	Vector No.	Address Offset in Vector Table	Default Priority Order
ITU3	IMIA3	0–15 (0)	IPRD (11–8)	3	92	H'00000170–H'00000173	High
	IMIB3			2	93	H'00000174–H'00000177	↑
	OVI3			1	94	H'00000178–H'0000017B	
	Reserved			0	95	H'0000017C–H'0000017F	
ITU4	IMIA4	0–15 (0)	IPRD (7–4)	3	96	H'00000180–H'00000183	
	IMIB4			2	97	H'00000184–H'00000187	
	OVI4			1	98	H'00000188–H'0000018B	
	Reserved			0	99	H'0000018C–H'0000018F	
SCI0	ERI0	0–15 (0)	IPRD (3–0)	3	100	H'00000190–H'00000193	
	RxI0			2	101	H'00000194–H'00000197	
	TxI0			1	102	H'00000198–H'0000019B	
	TEI0			0	103	H'0000019C–H'0000019F	
SCI1	ERI1	0–15 (0)	IPRE (15–12)	3	104	H'000001A0–H'000001A3	
	RxI1			2	105	H'000001A4–H'000001A7	
	TxI1			1	106	H'000001A8–H'000001AB	
	TEI1			0	107	H'000001AC–H'000001AF	
PRT*[1]	PEI	0–15 (0)	IPRE (11–8)	3	108	H'000001B0–H'000001B3	
A/D	ITI			2	109	H'000001B4–H'000001B7	
	Reserved			1	110	H'000001B8–H'000001BB	
	Reserved			0	111	H'000001BC–H'000001BF	
WDT	ITI	0–15 (0)	IPRE (7–4)	3	112	H'000001C0–H'000001C3	
REF*[2]	CMI			2	113	H'000001C4–H'000001C7	
	Reserved			1	114	H'000001C8–H'000001CB	
	Reserved			0	115	H'000001CC–H'000001CF	
Reserved		—	—	—	116 to 255	H'000001D0–H'000001D3 to H'000003FC–H'000003FF	↓ Low

Notes: 1. PRT: Parity control unit of bus state controller.
2. REF: DRAM refresh control unit of bus state controller.

5.3 Register Descriptions

5.3.1 Interrupt Priority Registers A–E (IPRA–IPRE)

The five registers IPRA–IPRE are 16-bit read/write registers that assign priority levels from 0–15 to the IRQ and on-chip supporting module interrupt sources. Interrupt request sources are mapped onto IPRA–IPRE as shown in table 5.4.

Bit	15	14	13	12	11	10	9	8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 5.4 Interrupt Request Sources and IPRA-IPRE

Register	Bits 15–12	Bits 11–8	Bits 7–4	Bits 3–0
IPRA	IRQ0	IRQ1	IRQ2	IRQ3
IPRB	IRQ4	IRQ5	IRQ6	IRQ7
IPRC	DMAC0, DMAC1	DMAC2, DMAC3	ITU0	ITU1
IPRD	ITU2	ITU3	ITU4	SCI0
IPRE	SCI1	PRT*[1], A/D	WDT, REF*[2]	(Reserved)*[3]

Notes: 1. PRT: Parity control unit of bus state controller. See section 8, Bus State Controller (BSC), for details.
2. REF: DRAM refresh control unit of bus controller. See section 8, Bus State Controller (BSC), for details.
3. Always read as 0. Always write 0 in reserved bits.

As indicated in table 5.4, four $\overline{\text{IRQ}}$ pins or four groups of on-chip supporting modules are assigned to each interrupt priority register. The priority levels for the four pins or groups can be set by setting the corresponding 4-bit groups of bits 15–12, bits 11–8, bits 7–4, and bits 3–0 (of IPRA–IPRE) with values in the range of H'0 (0000) to H'F (1111). Setting H'0 gives interrupt priority level 0 (the lowest). Setting H'F gives level 15 (the highest). When two on-chip supporting modules are assigned to the same bits (DMAC0 and DMAC1, or DMAC2 and DMAC3, or the parity control unit and the A/D converter, or the watchdog timer and DRAM refresh control unit),

those two modules have the same priority. A reset initializes IPRA–IPRE to H'0000. These registers are not initialized in standby mode.

5.3.2 Interrupt Control Register (ICR)

ICR is a 16-bit register that sets the input detection mode of external interrupt input pins NMI and $\overline{\text{IRQ0}}$–$\overline{\text{IRQ7}}$, and indicates the input signal level at the NMI pin. A reset initializes ICR but standby mode does not.

Bit:	15	14	13	12	11	10	9	8
	NMIL	—	—	—	—	—	—	NMIE
Initial value	*	0	0	0	0	0	0	0
Read/Write	R	—	—	—	—	—	—	R/W

Bit	7	6	5	4	3	2	1	0
	IRQ0S	IRQ1S	IRQ2S	IRQ3S	IRQ4S	IRQ5S	IRQ6S	IRQ7S
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * When NMI input is high: 1; when NMI input is low: 0

Bit 15—NMI input level (NMIL): NMIL sets the level of the signal input at the NMI pin. NMIL cannot be modified. The NMI input level can be read to determine the NMI pin level.

Bit 15: NMIL	Description
0	NMI input level is low
1	NMI input level is high

Bits 14–9—Reserved: These bits are always read as 0. The write value should always be 0.

Bit 8—NMI Edge Select (NMIE): NMIE selects whether the falling or rising edge of the interrupt request signal at the NMI pin is sensed.

Bit 8: NMIE	Description	
0	Interrupt is requested on falling edge of NMI input	(Initial value)
1	Interrupt is requested on rising edge of NMI input	

Bits 7–0—IRQ0–IRQ7 Sense Select (IRQ0S–IRQ7S): IRQ0–IRQ7 select whether the falling edge or low level of the $\overline{\text{IRQ}}$ inputs is sensed at pins $\overline{\text{IRQ0}}$–$\overline{\text{IRQ7}}$.

Bits 7–0: IRQ0S–IRQ7S	Description	
0	Interrupt is requested when $\overline{\text{IRQ}}$ input is low	(Initial value)
1	Interrupt is requested on falling edge of $\overline{\text{IRQ}}$ input	

5.4 Interrupt Operation

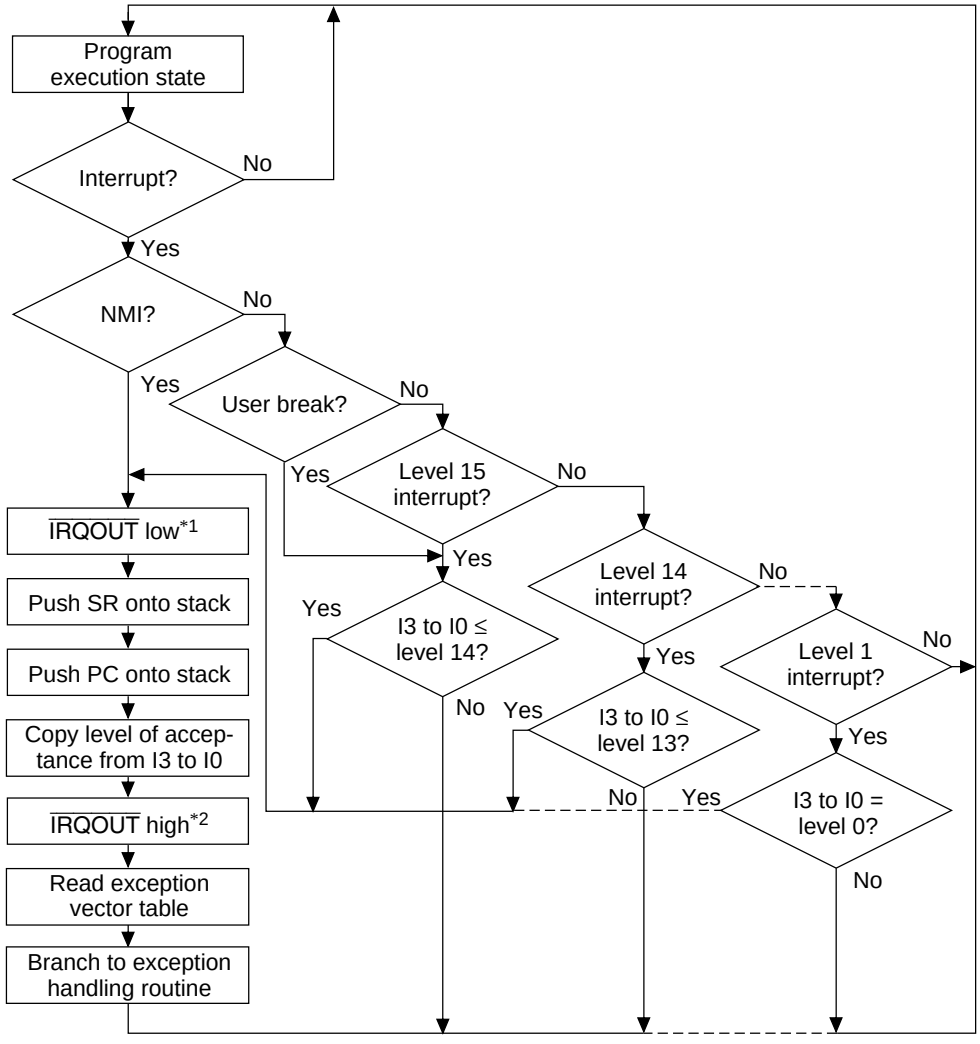
5.4.1 Interrupt Sequence

The sequence of interrupt operations is described below. Figure 5.2 shows a flowchart of the operations up to acceptance of the interrupt.

1. The interrupt request sources send interrupt request signals to the interrupt controller.
2. The interrupt controller selects the highest-priority interrupt among the interrupt requests sent, following the priority order indicated in table 5.3 and the levels set in interrupt priority registers A–E (IPRA–IPRE). Lower priority interrupts are ignored*. If two interrupts with the same priority level are requested simultaneously, or if there are multiple interrupts occurring within a single module, the interrupt with the highest default priority or priority within module as indicated in table 5.3 is selected.
3. The interrupt controller compares the priority level of the selected interrupt request with the interrupt mask level bits (I3–I0) in the CPU's status register (SR). If the request priority level is equal to or less than the interrupt mask level, the request is ignored. If the request priority level is higher than the interrupt mask level, the interrupt controller accepts the request and sends an interrupt request signal to the CPU.
4. When the interrupt controller accepts an interrupt request, it drives $\overline{\text{IRQOUT}}$ pin low.
5. The CPU detects the interrupt request sent from the interrupt controller when it decodes the next instruction to be executed. Instead of executing that instruction, the CPU starts interrupt exception handling. (See figure 5.4.)
6. In interrupt exception handling, first SR and PC are pushed onto the stack.
7. The priority level of the accepted interrupt is copied to the interrupt mask level bits (I3–I0) in the status register (SR).
8. When the accepted interrupt is level-sensed or from an on-chip supporting module, the $\overline{\text{IRQOUT}}$ pin returns to the high level. If the accepted interrupt is edge-sensed, the $\overline{\text{IRQOUT}}$ pin returns to the high level when the instruction to be executed by the CPU in (5) is replaced by the interrupt exception handling. If the interrupt controller has accepted another interrupt (of a level higher than the current interrupt), however, the $\overline{\text{IRQOUT}}$ pin remains low.

9. The CPU accesses the exception vector table at the entry for the vector number of the accepted interrupt, reads the start address of the exception handling routine, branches to that address, and starts executing the program there. This branch is not delayed.

Note: * A request for an external interrupt (IRQ) designated as edge-detected is held pending once only. An external interrupt designated as level-detected is held pending as long as the interrupt request continues, but if the request is cleared before the CPU next accepts an interrupt, the interrupt request is regarded as not having been made.
Interrupt requests from on-chip supporting modules are level requests. When the status flag in a particular module is set, an interrupt is requested. For details, see the descriptions of the individual modules. Note that the interrupt request will be continued unless an operation described in "Clearing Conditions" is performed.



I3 to I0: Interrupt mask bits of status register

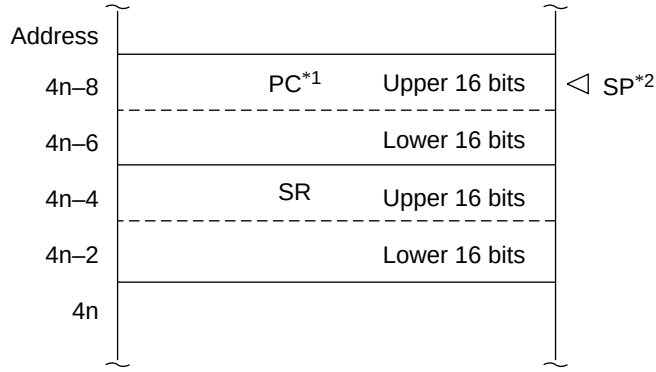
Notes: 1. $\overline{\text{IRQOUT}}$ is the same signal as the interrupt request signal to the CPU (figure 5.1). The $\overline{\text{IRQOUT}}$ pin returns to the high level when the interrupt controller has accepted the interrupt of a level higher than that specified by bits I3 to I0 in the CPU's status register.

2. If the accepted interrupt is edge-sensed, the $\overline{\text{IRQOUT}}$ pin returns to the high level when the instruction to be executed by the CPU is replaced by interrupt exception handling (before the status register is saved to the stack). If the interrupt controller has accepted another interrupt of a level higher than the current interrupt, and has sent an interrupt request to the CPU, however, the $\overline{\text{IRQOUT}}$ pin remains low.

Figure 5.2 Flowchart of Interrupt Operation

5.4.2 Stack after Interrupt Exception Handling

Figure 5.3 shows the stack after interrupt exception handling.



Notes: Bus width is 16 bits.
1. PC stores the start address of the next instruction (return instruction) after the executed instruction.
2. The value of SP must always be a multiple of four.

Figure 5.3 Stack after Interrupt Exception Handling

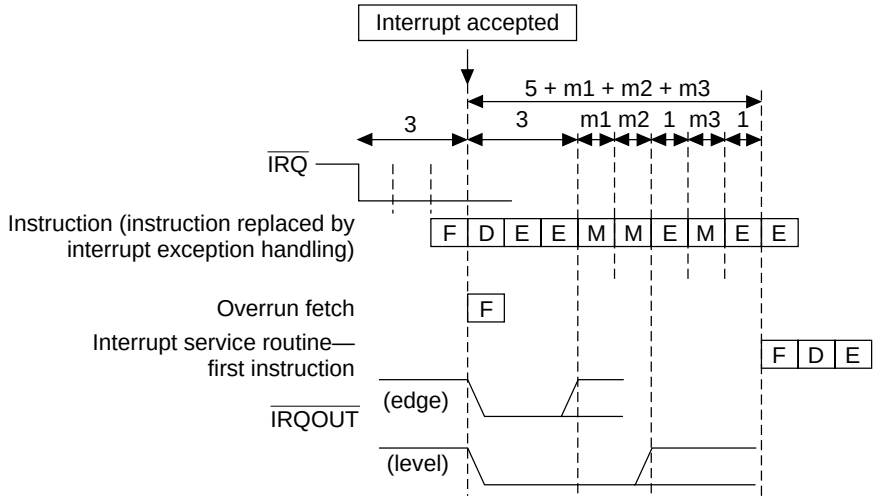
5.5 Interrupt Response Time

Table 5.5 shows the interrupt response time, which is the time from the occurrence of an interrupt request until interrupt exception handling starts and fetching of the first instruction of the interrupt handling routine begins. Figure 5.4 shows the pipeline when an IRQ interrupt is accepted.

Table 5.5 Interrupt Response Time

		Number of States		
Item		NMI or On-Chip Interrupt	IRQ	Notes
Interrupt priority decision and comparison with SR mask bit		2	3	
Wait for completion of sequence currently being executed by CPU		X (≥ 0)		The longest sequence is the interrupt or address error exception handling sequence: X = 4 + m1 + m2 + m3 + m4. If an interrupt-masking instruction follows, however, the time may be longer.
Time from interrupt exception handling (saving PC and SR and fetching vector address) until fetching of first instruction of interrupt handling routine starts		5 + m1 + m2 + m3		
Interrupt response	Total	7 + m1 + m2 + m3	8 + m1 + m2 + m3	
	Minimum	10	11	0.50–0.55 µs at 20 MHz
	Maximum	11 + 2(m1 + m2 + m3) + m4	12 + 2(m1 + m2 + m3) + m4	(m1 = m2 = m3 = m4 = 1) 0.90–0.95 µs at 20 MHz

Notes: m1–m4 are the number of states needed for the following memory accesses:
m1: SR save cycle (longword write)
m2: PC save cycle (longword write)
m3: Vector address read cycle (longword read)
m4: Fetch start instruction of interrupt handling routine



When m1 = m2 = m3, the interrupt response time is 11 cycles.

F	(Instruction fetch)	Instruction fetched from memory where program is stored.
D	(Instruction decoding)	The fetched instruction is decoded.
E	(Instruction execution)	Data operations and address calculations are performed according to the decoded results.
M	(Memory access)	Data in memory is accessed.

Note: For the interrupt acceptance timing, see table 4.1, Exception Source Detection and Start of Handling, in section 4.1.2, Exception Handling Operation.

Figure 5.4 Example of Pipelining in IRQ Interrupt Acceptance

5.6 Usage Notes

When the following operations are performed in the order shown when a pin to which IRQ input is assigned is designated as a general input pin by the pin function controller (PFC) and inputs a low-level signal, the IRQ falling edge is detected, and an interrupt request is detected, immediately after the setting in (b) is performed:

- An interrupt control register (ICR) setting is made so that an interrupt is detected at the falling edge of IRQ. …(a)
- The function of pins to which IRQ input is assigned is switched from general input to IRQ input by a pin function controller (PFC) setting. …(b)

Therefore, when switching the pin function from general input pin to IRQ input, the pin function controller (PFC) setting should be changed to IRQ input while the pin to which IRQ input is assigned is high.

Section 6 User Break Controller (UBC)

6.1 Overview

The user break controller (UBC) simplifies the debugging of user programs. Break conditions are set in the UBC and a user break interrupt request is sent to the CPU in response to the contents of a CPU or DMAC bus cycle. This function can implement an effective self-monitoring debugger, enabling a program to be debugged by itself without using a large in-circuit emulator.

6.1.1 Features

- The following break conditions can be set:
  - Address
  - CPU cycle or DMA cycle
  - Instruction fetch or data access
  - Read or write
  - Operand size (longword access, word access, or byte access)
- When break conditions are met, a user break interrupt is generated. A user-created user break interrupt exception routine can then be executed.
- When a break is set to a CPU instruction fetch, the break occurs just before the fetched instruction.

6.1.2 Block Diagram

Figure 6.1 shows a block diagram of the user break controller.

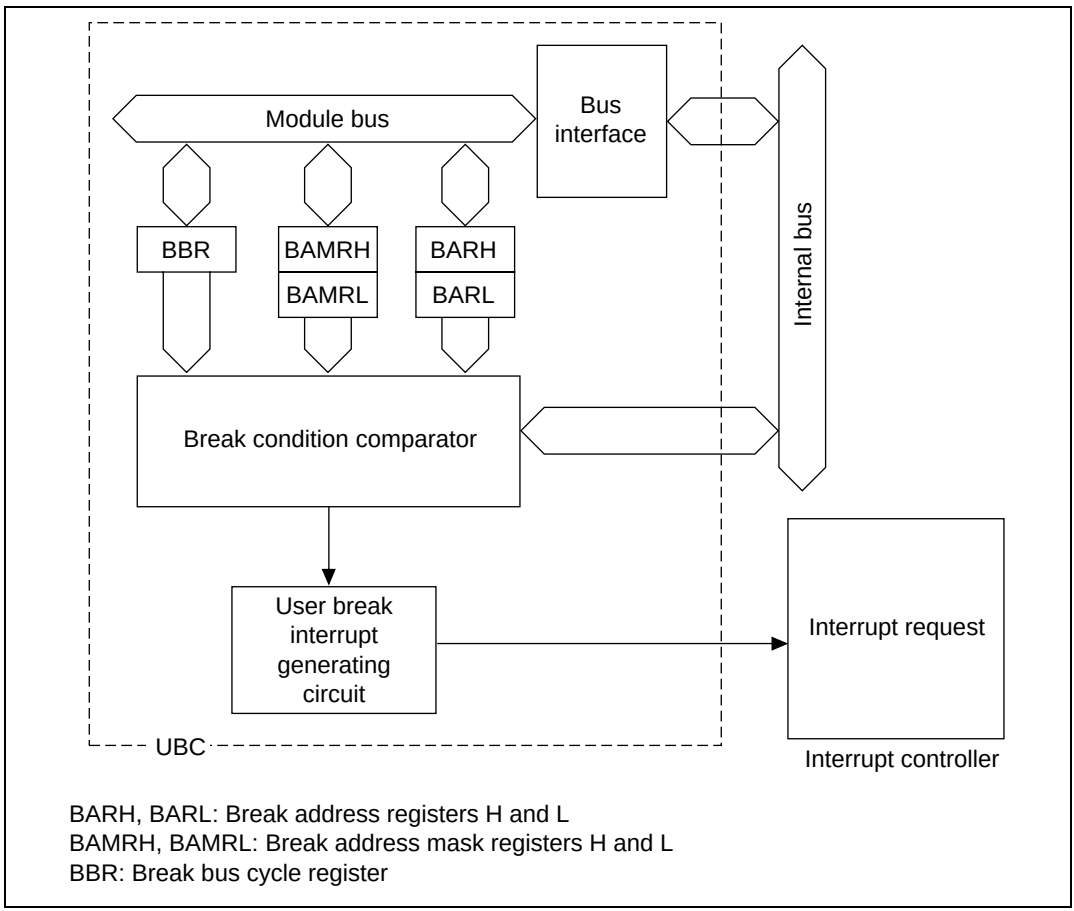


Figure 6.1 Block Diagram of User Break Controller

6.1.3 Register Configuration

The user break controller has five registers as listed in table 6.1. These registers are used for setting break conditions.

Table 6.1 User Break Controller Registers

Name	Abbr.	R/W	Address*	Initial Value	Bus width
Break address register high	BARH	R/W	H'5FFFF90	H'0000	8, 16, 32
Break address register low	BARL	R/W	H'5FFFF92	H'0000	8, 16, 32
Break address mask register high	BAMRH	R/W	H'5FFFF94	H'0000	8, 16, 32
Break address mask register low	BAMRL	R/W	H'5FFFF96	H'0000	8, 16, 32
Break bus cycle register	BBR	R/W	H'5FFFF98	H'0000	8, 16, 32

Note: * Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.

6.2 Register Descriptions

6.2.1 Break Address Registers (BAR)

There are two break address registers—break address register H (BARH) and break address register L (BARL)—that together form a single group. Both are 16-bit read/write registers. BARH stores the upper bits (bits 31–16) of the address of the break condition. BARL stores the lower bits (bits 15–0) of the address of the break condition. A reset initializes both BARH and BARL to H'0000. They are not initialized in standby mode.

BARH: Break address register H.

Bit	15	14	13	12	11	10	9	8
	BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BARH Bits 15–0—Break Address 31–16 (BA31–BA16): BA31–BA16 store the upper bit values (bits 31–16) of the address of the break condition.

BARL: Break address register L.

Bit	15	14	13	12	11	10	9	8
	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BARL Bits 15–0—Break Address 15–0 (BA15–BA0): BA15–BA0 store the lower bit values (bits 15–0) of the address of the break condition.

6.2.2 Break Address Mask Register (BAMR)

The two break address mask registers—break address mask register H (BAMRH) and break address mask register L (BARML)—together form a single group. Both are 16-bit read/write registers. BAMRH determines which of the bits in the break address set in BARH are masked. BAMRL determines which of the bits in the break address set in BARL are masked. A reset initializes BAMRH and BARML to H'0000. They are not initialized in standby mode.

BAMRH: Break address mask register H.

Bit	15	14	13	12	11	10	9	8
	BAM31	BAM30	BAM29	BAM28	BAM27	BAM26	BAM25	BAM24
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BAM23	BAM22	BAM21	BAM20	BAM19	BAM18	BAM17	BAM16
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BAMRH bits 15–0—Break Address Mask 31–16 (BAM31–BAM16): BAM31–BAM16 specify whether bits BA31–BA16 of the break address set in BARH are masked or not.

BAMRL: Break address mask register L.

Bit	15	14	13	12	11	10	9	8
	BAM15	BAM14	BAM13	BAM12	BAM11	BAM10	BAM9	BAM8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BAM7	BAM6	BAM5	BAM4	BAM3	BAM2	BAM1	BAM0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BAMRL bits 15–0—Break Address Mask 15–0 (BAM15–BAM0)): BAM15–BAM0 specify whether bits BA15–BA0 of the break address set in BARH are masked or not.

Bits 15–0:

BAMn	Description	
0	Break address bit BAn is included in the break condition	(Initial value)
1	Break address bit BAn is not included in the break condition	

n = 31–0

6.2.3 Break Bus Cycle Register (BBR)

The break bus cycle register (BBR) is a 16-bit read/write register that selects the following four break conditions:

- CPU cycle or DMA cycle
- Instruction fetch or data access
- Read or write
- Operand size (byte, word, longword)

A reset initializes BBR to H'0000. It is not initialized in standby mode.

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
	CD1	CD0	ID1	ID0	RW1	RW0	SZ1	SZ0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 15–8—Reserved: These bits are always read as 0. The write value should always be 0.

Bits 7 and 6—CPU Cycle/DMA Cycle Select (CD1 and CD0): CD1 and CD0 select whether to break on CPU and/or DMA bus cycles.

Bit 7: CD1	Bit 6: CD0	Description	
0	0	No break interrupt occurs	(Initial value)
	1	Break only on CPU cycles	
1	0	Break only on DMA cycles	
	1	Break on both CPU and DMA cycles	

Bits 5 and 4—Instruction Fetch/Data Access Select (ID1, ID0): ID1 and ID0 select whether to break on instruction fetch and/or data access bus cycles.

Bit 5: ID1	Bit 4: ID0	Description	
0	0	No break interrupt occurs	(Initial value)
	1	Break only on instruction fetch cycles	
1	0	Break only on data access cycles	
	1	Break on both instruction fetch and data access cycles	

Bits 3 and 2—Read/Write Select (RW1, RW0): RW1 and RW0 select whether to break on read and/or write access cycles.

Bit 3: RW1	Bit 2: RW0	Description	
0	0	No break interrupt occurs	(Initial value)
	1	Break only on read cycles	
1	0	Break only on write cycles	
	1	Break on both read and write cycles	

Bits 1 and 0 —Operand Size Select (SZ1, SZ0): SZ1 and SZ0 select the bus cycle operand size as a break condition.

Bit 1: SZ1	Bit 0: SZ0	Description	
0	0	Operand size is not a break condition	(Initial value)
	1	Break on byte access	
1	0	Break on word access	
	1	Break on longword access	

Note: When setting a break on an instruction fetch, clear the SZ0 bit to 0. All instructions will be considered to be accessed as words (even those instructions in on-chip memory for which two instructions can be fetched simultaneously in a single bus cycle). Instruction fetch is by word access and CPU/DMAC data access is by the specified operand size. The access is not determined by the bus width of the space being accessed.

6.3 Operation

6.3.1 Flow of User Break Operation

The flow from setting of break conditions to user break interrupt exception handling is described below.

1. Break conditions are set in the break address register (BAR), break address mask register (BAMR), and break bus cycle register (BBR). Set the break address in BAR, the address bits to be masked in BAMR and the type of break bus cycle in BBR. When even one of the BBR groups (CPU cycle/DMA cycle select bits (CD1, CD0), instruction fetch/data access select bits (ID1, ID0), read/write select bits (RW1, RW0)) is set to 00 (no user break interrupt), there will be no user break even when all other conditions are consistent. To use a user break interrupt, set conditions for all three pairs.
2. The UBC checks to see if the set conditions are satisfied, using the system shown in figure 6.2. When the break conditions are satisfied, the UBC sends a user break interrupt request to the interrupt controller.
3. On receiving the user break interrupt request, the interrupt controller checks its priority level. The user break interrupt has priority level 15, so it is accepted only if the interrupt mask level in bits I3–I0 in the status register (SR) is 14 or lower. When the I3–I0 bit level is 15, the user break interrupt cannot be accepted, but is held pending until user break interrupt exception handling is carried out. NMI exception handling sets I3–I0 to level 15, so a user break cannot occur during the NMI handling routine unless the NMI handling routine itself begins by reducing I3–I0 to level 14 or lower. Section 5, Interrupt Controller (INTC), describes the handling of priority levels in greater detail.
4. INTC sends a request signal for a user break interrupt to the CPU. When the CPU receives it, it starts user break interrupt exception handling. Section 5.4, Interrupt Operation, describes interrupt exception handling in more detail.

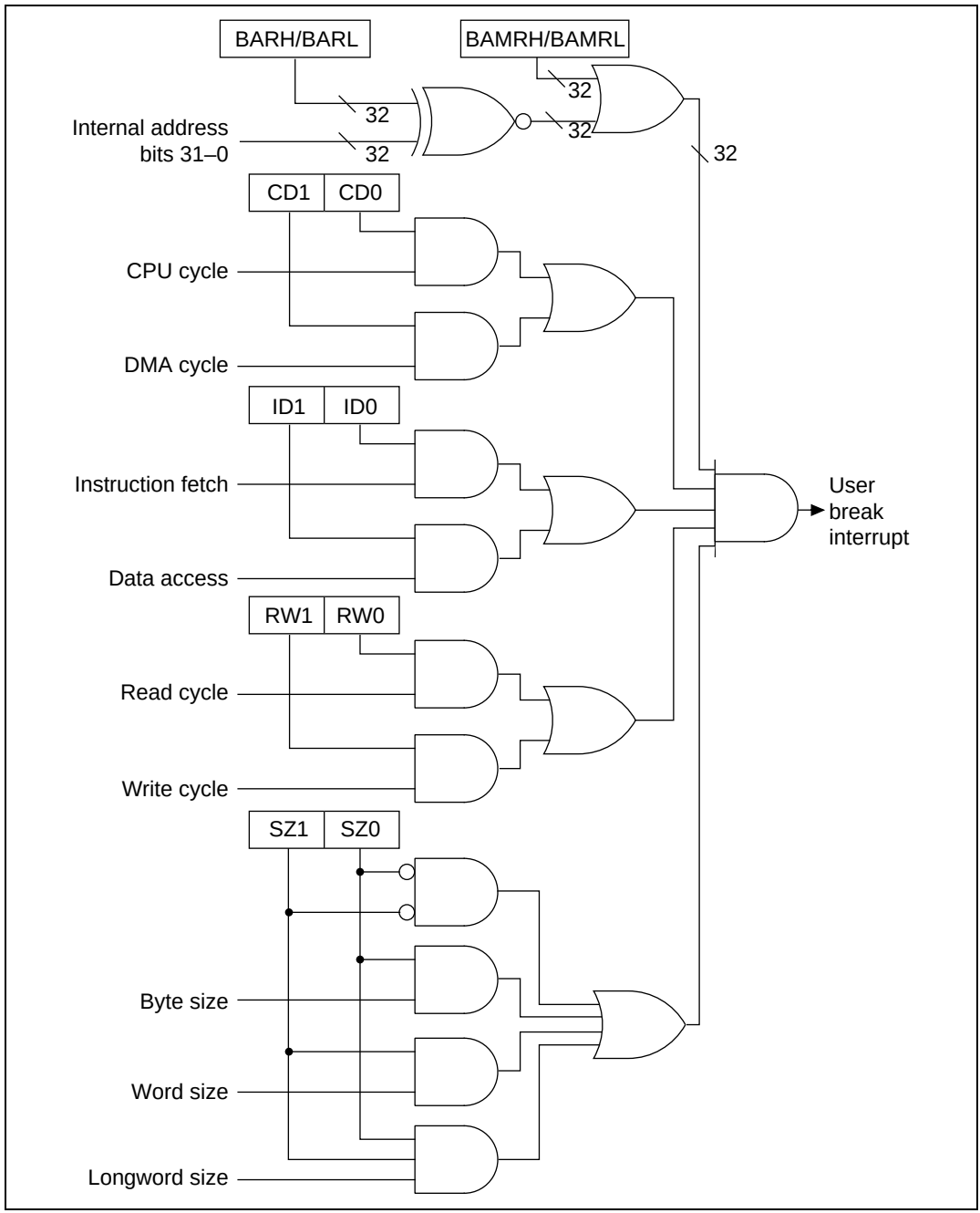


Figure 6.2 Break Condition Logic

6.3.2 Break on Instruction Fetch Cycles to On-Chip Memory

On-chip memory (on-chip ROM (SH7034 only) and RAM) is always accessed 32 bits each bus cycle. Two instructions are therefore fetched in a bus cycle from on-chip memory . Although only a single bus cycle occurs for the two-instruction fetch, a break can be set on either instruction by placing the corresponding address in the break address registers (BAR). In other words, to break the second of the two instructions fetched, set its start address in the BAR. The break will then occur after the first instruction executes.

6.3.3 Program Counter (PC) Value Saved in User Break Interrupt Exception Processing

Break on Instruction Fetch: The program counter (PC) value saved in user break interrupt exception processing for an instruction fetch is the address set as the break condition. The user break interrupt is generated before the fetched instruction is executed. If a break condition is set on the fetch cycle of a delayed slot instruction immediately following a delayed branch instruction or on the fetch cycle of an instruction that follows an interrupt-disabling instruction, however, the user break interrupt is not accepted immediately, so the instruction is executed. The user break interrupt is not accepted until immediately after that instruction. The PC value that will be saved is the start address of the next instruction that is able to accept the interrupt.

Break on Data Access (CPU/DMAC): The program counter (PC) value is the top address of the next instruction after the last executed instruction at the time when the user break exception processing is activated. When data access (CPU/DMAC) is set as a break condition, the place where the break will occur cannot be specified exactly. The break will occur at the instruction fetched close to where the data access that is to receive the break occurs.

6.4 Setting User Break Conditions

CPU Instruction Fetch Bus Cycle:

- Register settings: BARH = H'0000, BARL = H'0404, BBR = H'0054
  Conditions set: Address = H'00000404, bus cycle = CPU, instruction fetch, read (operand size not included in conditions)

  A user break interrupt will occur immediately before the instruction at address H'00000404. If the instruction at address H'00000402 can accept an interrupt, the user break exception handling will be executed after that instruction is executed. The instruction at H'00000404 will not be executed. The value saved to the PC is H'00000404.
- Register settings: BARH = H'0015, BARL = H'389C, BBR = H'0058
  Conditions set: Address = H'0015389C, bus cycle = CPU, instruction fetch, write (operand size not included in conditions)

  No user break interrupt occurs, because no instruction fetch cycle is ever a write cycle.
- Register settings: BARH = H'0003, BARL = H'0147, BBR = H'0054

  Conditions set: Address = H'00030147, bus cycle = CPU, instruction fetch, read (operand size not included in conditions)

  No user break interrupt occurs, because instructions are always fetched from even addresses. If the first fetched address after a branch is odd and a user break is set on this address, however, user break exception handling will be carried out after address error exception handling.

CPU Data Access Bus Cycle:

- Register settings: BARH = H'0012, BARL = H'3456, BBR = H'006A
  Conditions set: Address = H'00123456, bus cycle = CPU, data access, write, word
  A user break interrupt occurs when word data is written to address H'00123456.
- Register settings: BARH = H'00A8, BARL = H'0391, BBR = H'0066
  Conditions set: Address = H'00A80391, bus cycle = CPU, data access, read, word
  No user break interrupt occurs, because word data access is always to an even address.

DMA Cycle:

- Register setting: BARH = H'0076, BARL = H'BCDC, BBR = H'00A7
  Conditions set: Address = H'0076BCDC, bus cycle = DMA, data access, read, longword
  A user break interrupt occurs when longword data is read from address H'0076BCDC.
- Register setting: BARH = H'0023, BARL = H'45C8, BBR = H'0094
  Conditions set: Address = H'002345C8, bus cycle = DMA, instruction fetch, read (operand size not included)
  No user break interrupt occurs, because a DMA cycle includes no instruction fetch.

6.5 Notes

6.5.1 On-Chip Memory Instruction Fetch

Two instructions are simultaneously fetched from on-chip memory. If a break condition is set on the second of these two instructions but the contents of the UBC break condition registers are changed so as to alter the break condition immediately after the first of the two instructions is fetched, a user break interrupt will still occur when the second instruction is fetched.

6.5.2 Instruction Fetch at Branches

When a conditional branch instruction or TRAPA instruction causes a branch, instructions are fetched and executed as follows:

1. Conditional branch instruction, branch taken: BT, BF
   Instruction fetch cycles: Conditional branch fetch → Next-instruction overrun fetch → Next-but-one-instruction overrun fetch → Branch destination fetch
   Instruction execution: Conditional branch instruction execution → Branch destination instruction execution
2. TRAPA instruction, branch taken: TRAPA
   Instruction fetch cycles: TRAPA instruction fetch → Next-instruction overrun fetch → Next-but-one-instruction overrun fetch → Branch destination fetch
   Instruction execution: TRAPA instruction execution → Branch destination instruction execution

When a conditional branch instruction or TRAPA instruction causes a branch, the branch destination will be fetched after the next instruction or the one after that does an overrun fetch. When the next instruction or the one after that is set as a break condition, a branch will result in the generation of a user break interrupt at the next instruction or the instruction after that, neither of which instructions will be executed.

6.5.3 Instruction Fetch Break

If a break is attempted at the task A return destination instruction fetch, task B is activated before the UBC interrupt by interrupt B generated during task A processing, and the UBC interrupt is handled after the interrupt B exception handling.

1. Cause

   The SH7032/SH7034 chip operates as follows.

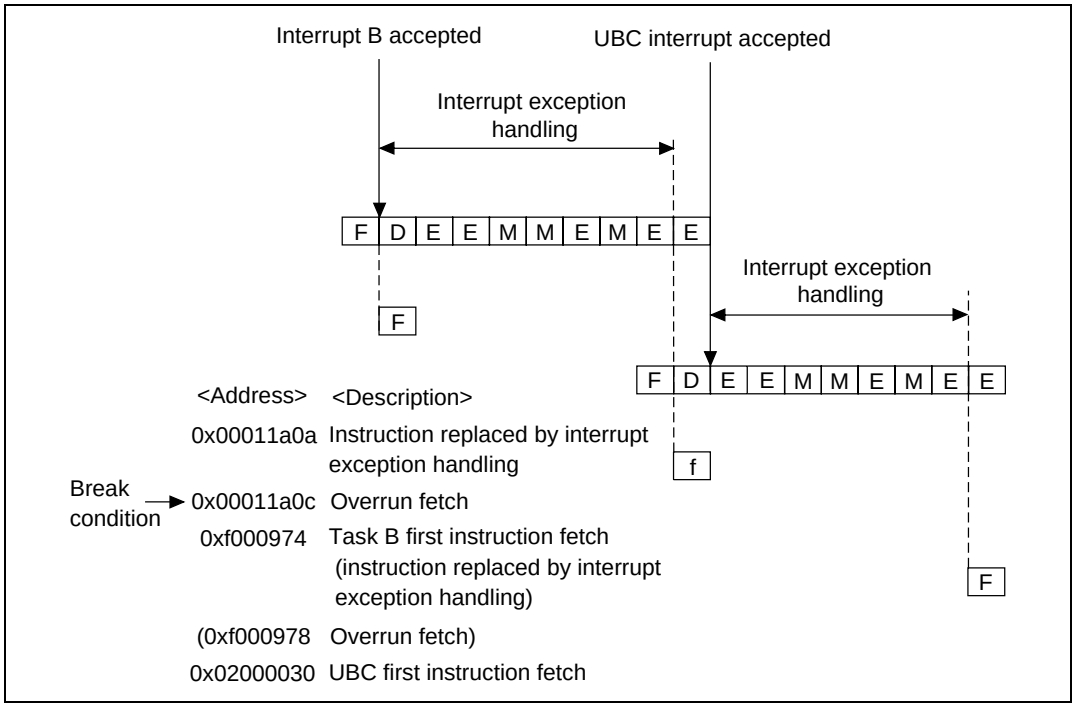


Figure 6.3 UBC Operation

It actually takes at least two cycles for the UBC interrupt generated by the address 0x00011a0c instruction fetch cycle to be sent to the interrupt controller and interrupt exception handling to begin. However, as shown in figure 6.3, when the UBC interrupt is generated, previously generated interrupt B initiated by task B is accepted first, and the UBC interrupt is accepted after completion of the interrupt B exception handling.

2. Remedy

   There is no way of preventing this operation by hardware. A software solution, such as the use of a flag, must be employed.

Section 7 Clock Pulse Generator (CPG)

7.1 Overview

The SuperH microcomputer has a built-in clock pulse generator (CPG) that supplies the chip and external devices with a clock pulse. The CPG makes the chip run at the oscillation frequency of the crystal resonator. The CPG consists of an oscillator and a duty cycle correction circuit (figure 7.1). The CPG can be made to generate a clock signal by connecting it to a crystal resonator or by inputting an external clock. (The CPG is halted in standby mode.)

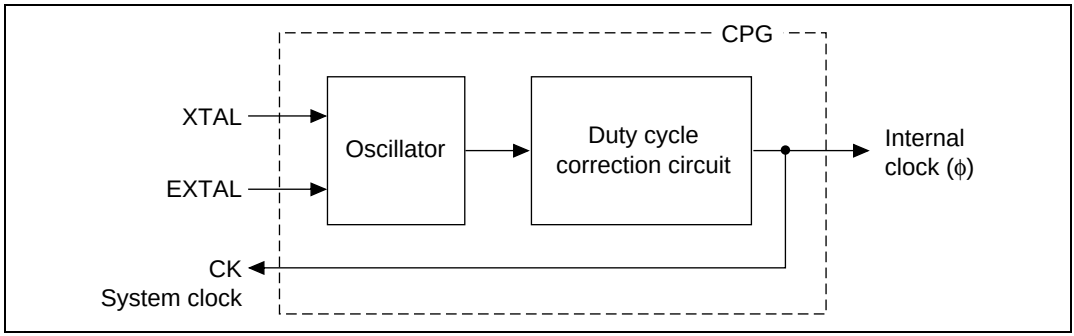


Figure 7.1 Block Diagram of Clock Pulse Generator

7.2 Clock Source

Clock pulses can be supplied from a connected crystal resonator or an external clock.

7.2.1 Connecting a Crystal Resonator

Circuit Configuration: A crystal resonator can be connected as shown in figure 7.2. Use the damping resistance Rd shown in table 7.1. Use an AT-cut parallel resonating crystal with a frequency equal to the system clock (CK) frequency. Connect load capacitors (C_{L1} and C_{L2}) as shown in the figure. The clock pulse produced by the crystal resonator and internal pulse generator is sent to the duty cycle correction circuit where its duty cycle is corrected. It is then supplied to the chip and to external devices.

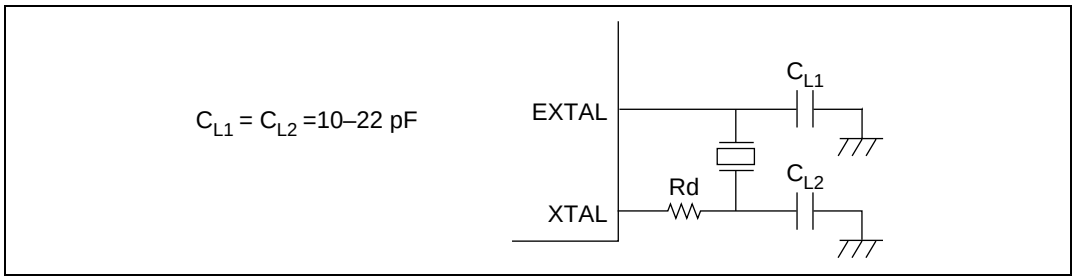


Figure 7.2 Connection of Crystal Resonator (Example)

Table 7.1 Damping Resistance

Frequency [MHz]	2	4	8	12	16	20
Rd [Ω]	1k	500	200	0	0	0

Crystal Resonator: Figure 7.3 shows an equivalent circuit of the crystal resonator. Use a crystal resonator with the characteristics listed in table 7.2.

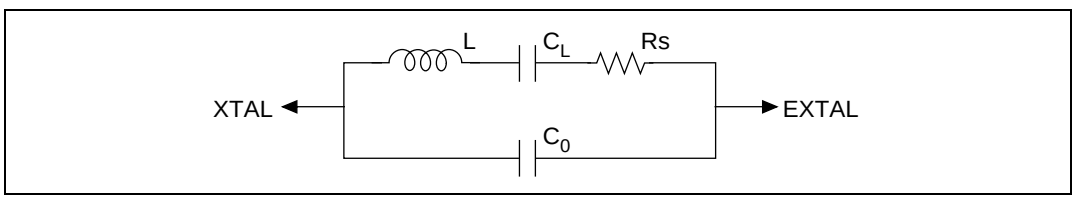


Figure 7.3 Crystal Resonator Equivalent Circuit

Table 7.2 Crystal Resonator Parameters

	Frequency (MHz)					
Parameter	**2**	**4**	**8**	**12**	**16**	**20**
Rs max [Ω]	500	120	80	60	50	40
Co max [pF]	7	7	7	7	7	7

7.2.2 External Clock Input

An external clock signal can be input at the EXTAL pin as shown in figure 7.4. The XTAL pin should be left open. The frequency must be equal to the system clock (CK) frequency. The specifications for the waveform of the external clock input are given below. Make the external clock frequency the same as the system clock (CK).

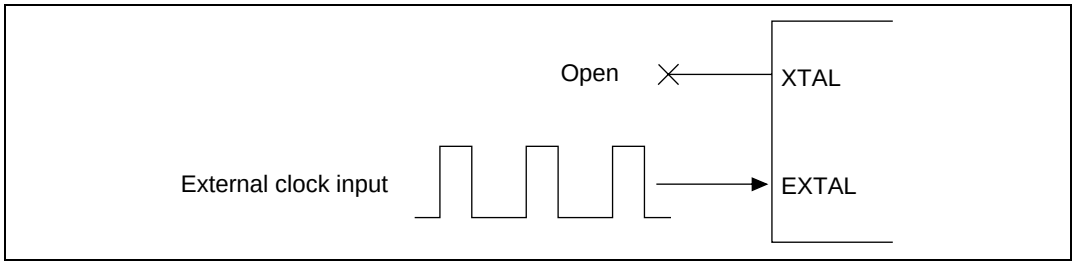


Figure 7.4 External Clock Input Method

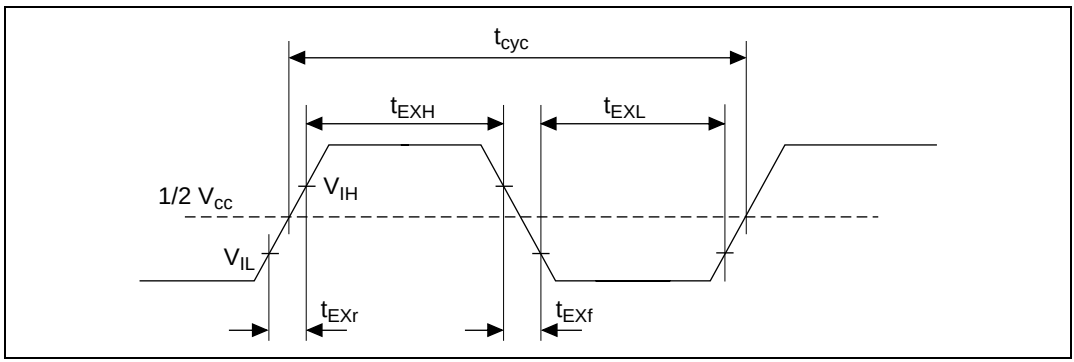


Figure 7.5 Input Clock Waveform

Table 7.3 Input Clock Specifications

	5 V Specifications (fmax = 20 MHz)*1	3.3 V Specifications (fmax = 12.5 MHz)	3.3 V Specifications (fmax = 20 MHz)*2	Unit
$t_{EXr/f}$ (V_{IL}–V_{IH})	Max = 5	Max = 10	Max = 5	ns
$t_{EXH/L}$	Min = 10	Min = 20	Min = 15	ns

Notes: 1. Except SH7034B
2. SH7034B only

7.3 Usage Notes

Board Design: When designing the board, place the crystal resonator and its load capacitors as close as possible to the XTAL and EXTAL pins. Route no other signal lines near the XTAL and EXTAL pin signal lines to prevent induction from interfering with correct oscillation. See figure 7.6.

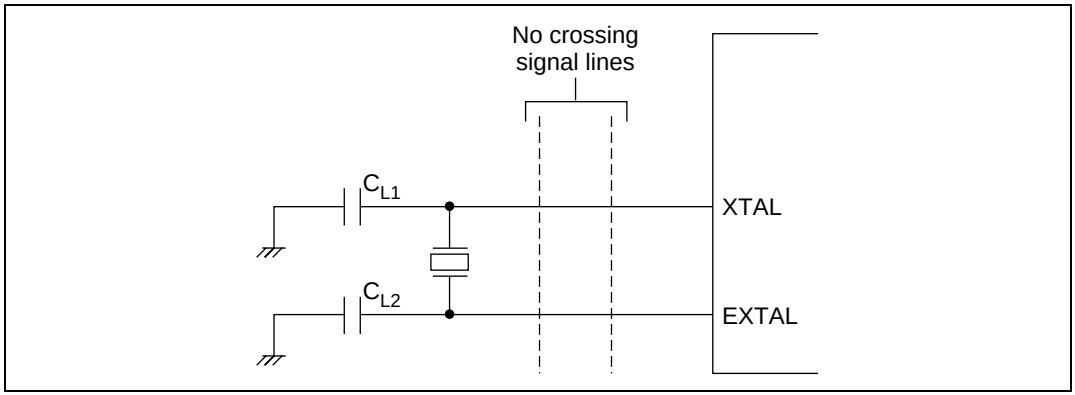
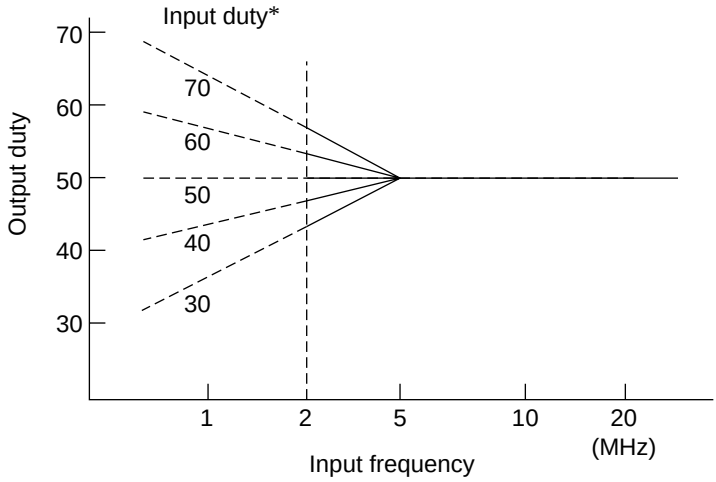


Figure 7.6 Precaution on Oscillator Circuit Board Design

Duty Cycle Correction Circuit: Duty cycle corrections are conducted for an input clock over 5 MHz. Duty cycles may not be corrected for a clock of under 5 MHz, but AC characteristics for the high-level pulse width (t_{CH}) and low-level pulse width (t_{CL}) of the clock are satisfied, and the chip will operate normally. Figure 7.7 shows the standard characteristics of duty cycle correction. This duty cycle correction circuit is not for correcting transient fluctuations and jitter in the input clock.

Thus, it takes several tens of microseconds to obtain a stable clock after duty cycle correction is performed.



Note: * With the SH7034B, compensation is performed in the input duty range of 60% to 40%.

Figure 7.7 Duty Cycle Correction Circuit Standard Characteristics

Section 8 Bus State Controller (BSC)

8.1 Overview

The bus state controller (BSC) divides address space and outputs control signals for all kinds of memory and peripheral chips. BSC functions enable the chip to be connected directly to DRAM, SRAM, ROM, and peripheral chips without the use of external circuits, simplifying system design and allowing high-speed data transfer in a compact system.

8.1.1 Features

The BSC has the following features:

- Address space is divided into eight areas
  - A maximum 4-Mbyte linear address space for each of eight areas, 0–7 (area 1 can be up to 16-Mbyte linear space when set for DRAM). (The space that can actually be used varies with the type of memory connected.)
  - Bus width (8 bits or 16 bits) can be selected by access address
  - On-chip ROM and RAM is accessed in one cycle (32 bits wide)
  - Wait states can be inserted using the $\overline{\text{WAIT}}$ pin
  - Wait state insertion can be controlled by software. Register settings can be used to specify the insertion of 1–4 cycles for areas 0, 2, and 6 (long wait function)
  - The type of memory connected can be specified for each area
  - Outputs control signals for accessing the memory and peripheral chips connected to the area
- Direct interface to DRAM
  - Multiplexes row/column addresses according to DRAM capacity
  - Two types of byte access signals (dual-CAS system and dual-WE system)
  - Supports burst operation (high-speed page mode)
  - Supports CAS-before-RAS refresh and self-refresh
- Access control for all memory and peripheral chips
  - Address/data multiplex function
- Parallel execution of external writes etc. with internal access (warp mode)
- Supports parity check and generation for data bus
  - Odd parity/even parity selectable
  - Interrupt request generated for parity error (PEI interrupt request signal)

- Refresh counter can be used as an interval timer
  — Interrupt request generated at compare match (CMI interrupt request signal)

8.1.2 Block Diagram

Figure 8.1 shows a block diagram of the bus state controller.

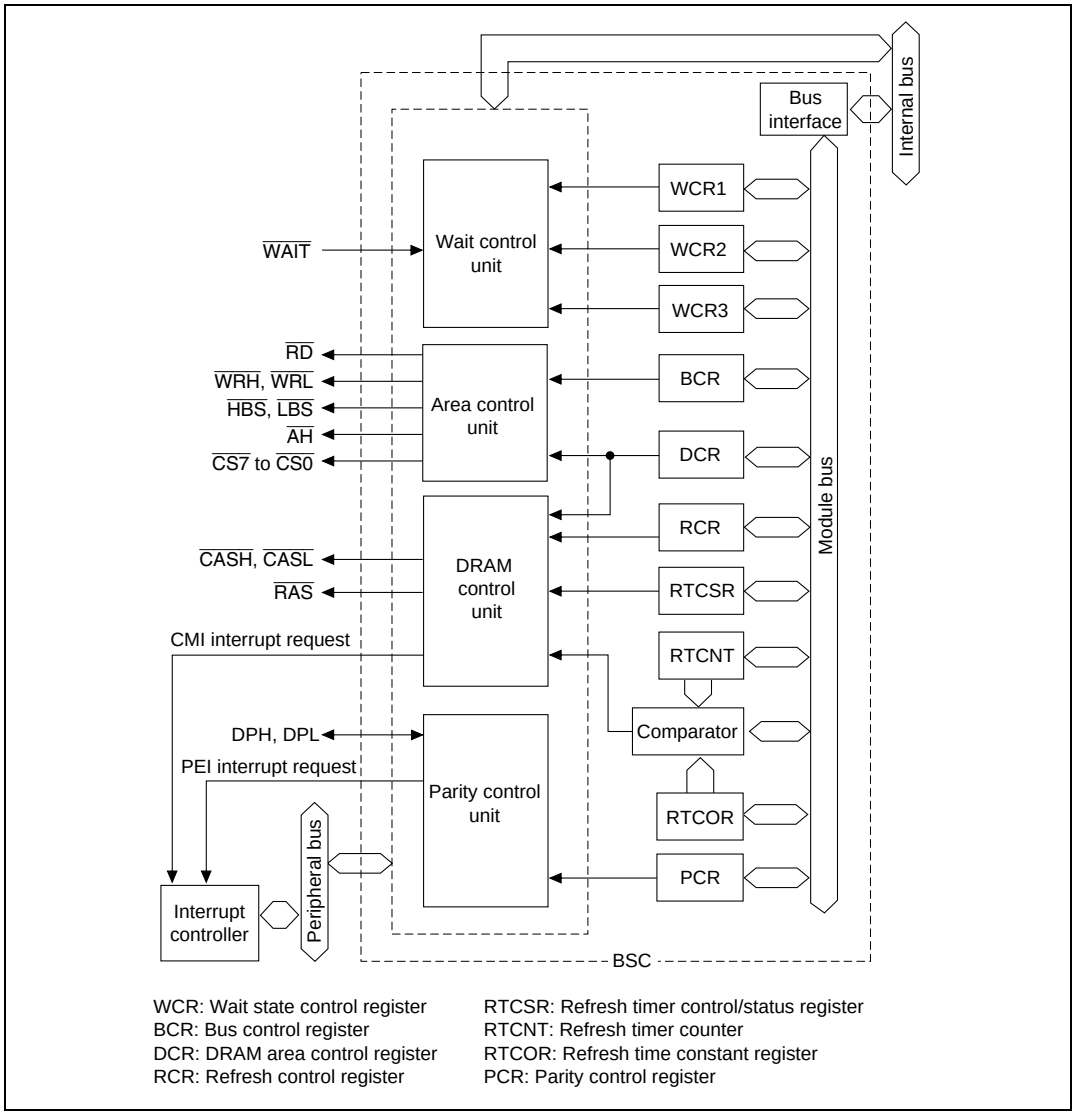


Figure 8.1 Block Diagram of BSC

8.1.3 Pin Configuration

Table 8.1 shows the BSC pin configuration.

Table 8.1 Pin Configuration

Name	Abbreviation	I/O	Function
Chip select 7–0	$\overline{CS7}$–$\overline{CS0}$	O	Chip select signal that indicates the area being accessed
Read	$\overline{RD}$	O	Strobe signal that indicates the read cycle
High write	$\overline{WRH}$	O	Strobe signal that indicates write cycle to upper 8 bits
Low write	$\overline{WRL}$	O	Strobe signal that indicates write cycle to lower 8 bits
Write	$\overline{WR}$*1	O	Strobe signal that indicates write cycle
High byte strobe	$\overline{HBS}$*2	O	Strobe signal that indicates access to upper 8 bits
Low byte strobe	$\overline{LBS}$*3	O	Strobe signal that indicates access to lower 8 bits
Row address strobe	$\overline{RAS}$	O	DRAM row address strobe signal
High column address strobe	$\overline{CASH}$	O	Column address strobe signal for accessing the upper 8 bits of the DRAM
Low column address strobe	$\overline{CASL}$	O	Column address strobe signal for accessing the lower 8 bits of the DRAM
Address hold	$\overline{AH}$	O	Signal for holding the address for address/data multiplexing
Wait	$\overline{WAIT}$	I	Wait state request signal
Address bus	A21–A0	O	Address output
Data bus	AD15–AD0	I/O	Data I/O. During address/data multiplexing, address output and data input/output
Data bus parity high	DPH	I/O	Parity data I/O for upper byte
Data bus parity low	DPL	I/O	Parity data I/O for lower byte

Notes: 1. Doubles with the $\overline{WRL}$ pin. (Selected by the BAS bit in BCR. See section 8.2.1, Bus Control Register (BCR), for details.)
2. Doubles with the A0 pin. (Selected by the BAS bit in BCR. See section 8.2.1, Bus Control Register (BCR), for details.)
3. Doubles with the $\overline{WRH}$ pin. (Selected by the BAS bit in BCR. See section 8.2.1, Bus Control Register (BCR), for details.)

8.1.4 Register Configuration

The BSC has ten registers (listed in table 8.2) which control space division, wait states, DRAM interface, and parity check.

Table 8.2 Register Configuration

Name	Abbr.	R/W	Initial Value	Address*1	Bus width
Bus control register	BCR	R/W	H'0000	H'5FFFFA0	8,16,32
Wait state control register 1	WCR1	R/W	H'FFFF	H'5FFFFA2	8,16,32
Wait state control register 2	WCR2	R/W	H'FFFF	H'5FFFFA4	8,16,32
Wait state control register 3	WCR3	R/W	H'F800	H'5FFFFA6	8,16,32
DRAM area control register	DCR	R/W	H'0000	H'5FFFFA8	8,16,32
Parity control register	PCR	R/W	H'0000	H'5FFFFAA	8,16,32
Refresh control register	RCR	R/W	H'0000	H'5FFFFAC	8,16,32*2
Refresh timer control/status register	RTCSR	R/W	H'0000	H'5FFFFAE	8,16,32*2
Refresh timer counter	RTCNT	R/W	H'0000	H'5FFFFB0	8,16,32*2
Refresh time constant register	RTCOR	R/W	H'00FF	H'5FFFFB2	8,16,32*2

Notes: 1. Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.
2. Write only with word transfer instructions. See section 8.2.11, Notes on Register Access, for details on writing.

8.1.5 Overview of Areas

The SH microprocessors have a 32-bit address space in the architecture, but the upper 4 bits are ignored. Table 8.3 outlines the space divisions. As shown, the space is divided into areas 0–7 according to the value of the upper addresses.

Each area is allocated a specific type of space. When the area is accessed, a strobe signal that matches the type of area space is generated. This allocates peripheral chips and memory devices according to the type of the area spaces and allows them to be directly linked to this chip. Some areas are of a fixed type based on their address while others can be selected in registers.

Area 0 can be used as an on-chip ROM space or external memory space in the SH7034. In the SH7032, it can only be used as external memory space. Area 1 can be used as DRAM space or external memory space. DRAM space enables direct connection to DRAM and outputs $\overline{RAS}$, $\overline{CAS}$ and multiplexed addresses. Areas 2–4 can only be used as external memory space. Area 5 can be used as on-chip supporting module space or external memory space. Area 6 can be used as address/data multiplexed I/O space or external memory space. For address/data multiplexed I/O space, an address and data are multiplexed and input/output from pins AD15–AD0. Area 7 can be used as on-chip RAM space or external memory space.

The bus width of the data bus is basically switched between 8 bits and 16 bits according to the value of address bit A27. For the following areas, however, the bus width is determined by conditions other than the A27 bit value.

- On-chip ROM space in area 0: Always 32 bits
- External memory space in area 0: 8 bits when MD0 pin is 0, 16 bits when the pin is 1
- On-chip supporting module space in area 5: 8 bits when the A8 address bit is 0, 16 bits when it is 1
- Area 6: If A27 = 0, area 6 is 8 bits when the A14 address bit is 0, 16 bits when A14 is 1
- On-chip RAM space in area 7: Always 32 bits

See table 8.6 in section 8.3, Address Space Subdivision, for more information on how the space is divided.

Table 8.3 Overview of Space Divisions

Area	Address	Assignable Memory	Capacity (Linear Space)	Bus Width	CS Output
0	H'0000000–H'0FFFFFF	On-chip ROM*1	64 kB	32	—
		External memory*2	4 MB	8/16*3	$\overline{CS0}$
1	H'1000000–H'1FFFFFF	External memory	4 MB	8	$\overline{CS1}$
		DRAM*4	16 MB	8	$\overline{RAS}$ $\overline{CAS}$
2	H'2000000–H'2FFFFFF	External memory	4 MB	8	$\overline{CS2}$
3	H'3000000–H'3FFFFFF	External memory	4 MB	8	$\overline{CS3}$
4	H'4000000–H'4FFFFFF	External memory	4 MB	8	$\overline{CS4}$
5	H'5000000–H'5FFFFFF	On-chip supporting modules	512 B	8/16*5	—
6	H'6000000–H'6FFFFFF	External memory*7	4 MB	8/16*6	$\overline{CS6}$
		Multiplexed I/O	4 MB		
7	H'7000000–H'7FFFFFF	External memory	4 MB	8	$\overline{CS7}$
0	H'8000000–H'8FFFFFF	On-chip ROM*1	64 kB	32	—
		External memory*2	4 MB	8/16*3	$\overline{CS0}$
1	H'9000000–H'9FFFFFF	External memory	4 MB	16	$\overline{CS1}$
		DRAM*4	16 MB	16	$\overline{RAS}$ $\overline{CAS}$
2	H'A000000–H'AFFFFFF	External memory	4 MB	16	$\overline{CS2}$
3	H'B000000–H'BFFFFFF	External memory	4 MB	16	$\overline{CS3}$
4	H'C000000–H'CFFFFFF	External memory	4 MB	16	$\overline{CS4}$
5	H'D000000–H'DFFFFFF	External memory	4 MB	16	$\overline{CS5}$
6	H'E000000–H'EFFFFFF	External memory	4 MB	16	$\overline{CS6}$
7	H'F000000–H'FFFFFFF	On-chip RAM	8 kB*8, 4 kB*9	32	—

Notes:
1. When MD2–MD0 pins are 010 (SH7034)
2. When MD2–MD0 pins are 000 or 001
3. Select with MD0 pin
4. Select with DRAME bit in BCR
5. Divided into 8-bit and 16-bit space according to value of address bit A8. (Longword accesses are inhibited, however, for on-chip supporting modules with bus widths of 8 bits. Some on-chip supporting modules with bus widths of 16 bits also have registers that are only byte-accessible and registers for which byte access is inhibited. For details, see the sections on the individual modules.)
6. Divided into 8-bit space and 16-bit space by value of address bit A14
7. Select with IOE bit in BCR
8. For SH7032
9. For SH7034

8.2 Register Descriptions

8.2.1 Bus Control Register (BCR)

The bus control register (BCR) is a 16-bit read/write register that selects the functions of areas and status of bus cycles. It is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or in standby mode.

Bit	15	14	13	12	11	10	9	8
	DRAME	IOE	WARP	RDDTY	BAS	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	—	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit 15—DRAM Enable Bit (DRAME): DRAME selects whether area 1 is used as an external memory space or DRAM space. 0 sets it as external memory space and 1 sets it as DRAM space. The setting of the DRAM area control register is valid only when this bit is set to 1.

Bit 15: DRAME	Description	
0	Area 1 is external memory space	(Initial value)
1	Area 1 is DRAM space	

Bit 14—Multiplexed I/O Enable Bit (IOE): IOE selects whether area 6 is used as external memory space or an address/data multiplexed I/O area. 0 sets it as external memory space and 1 sets it as address/data multiplexed I/O space. With address/data multiplexed I/O space, the address and data are multiplexed and input/output is from AD15–AD0.

Bit 14: IOE	Description	
0	Area 6 is external memory space	(Initial value)
1	Area 6 is an address/data multiplexed I/O area	

Bit 13—Warp Mode Bit (WARP): WARP selects warp or normal mode. 0 sets normal mode and 1 sets warp mode. In warp mode, some external accesses are carried out in parallel with internal access.

Bit 13: WARP	Description
0	Normal mode: External and internal accesses are not performed simultaneously (Initial value)
1	Warp mode: External and internal accesses are performed simultaneously

Bit 12—RD Duty (RDDTY): RDDTY selects 35% or 50% of the T1 state as the high-level duty cycle ratio of signal $\overline{RD}$. 0 sets 50%, 1 sets 35%.

Bit 12: RDDTY	Description
0	$\overline{RD}$ signal high-level duty cycle is 50% of T1 state (Initial value)
1	$\overline{RD}$ signal high-level duty cycle is 35% of T1 state

Bit 11—Byte Access Select (BAS): BAS selects whether byte access control signals are $\overline{WRH}$, $\overline{WRL}$, and A0, or $\overline{LBS}$, $\overline{WR}$ and $\overline{HBS}$ during word space accesses. When this bit is cleared to 0, $\overline{WRH}$, $\overline{WRL}$, and A0 signals are valid; when set to 1, $\overline{LBS}$, $\overline{WR}$, and $\overline{HBS}$ signals are valid.

Bit 11: BAS	Description
0	$\overline{WRH}$, $\overline{WRL}$, and A0 enabled (Initial value)
1	$\overline{LBS}$, $\overline{WR}$, and $\overline{HBS}$ enabled

Bits 10–0—Reserved: These bits are always read as 0. The write value should always be 0.

8.2.2 Wait State Control Register 1 (WCR1)

Wait state control register 1 is a 16-bit read/write register that controls the number of states for accessing each area and whether wait states are used. WCR1 is initialized to H'FFFF by a power-on reset. It is not initialized by a manual reset or in standby mode.

Bit	15	14	13	12	11	10	9	8
	RW7	RW6	RW5	RW4	RW3	RW2	RW1	RW0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	WW1	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	R/W	—

Bits 15–8—Wait State Control During Read (RW7–RW0): RW7–RW0 determine the number of states in read cycles for each area and whether or not to sample the signal input from the $\overline{\text{WAIT}}$ pin. Bits RW7–RW0 correspond to areas 7–0, respectively. If a bit is cleared to 0, the $\overline{\text{WAIT}}$ signal is not sampled during the read cycle for the corresponding area. If it is set to 1, sampling takes place.

For the external memory spaces of areas 1, 3–5, and 7, read cycles are completed in one state when the corresponding bits are cleared to 0. When they are set to 1, the number of wait states is 2 plus the $\overline{\text{WAIT}}$ signal value. For the external memory space of areas 0, 2, and 6, read cycles are completed in one state plus the number of long wait states (set in wait state controller 3 (WCR3)) when the corresponding bits are cleared to 0. When they are set to 1, the number of wait states is 1 plus the long wait state; when the $\overline{\text{WAIT}}$ signal is low as well, a wait state is inserted.

The DRAM space (area 1) finishes the column address output cycle in one state (short pitch) when the RW1 bit is 0, and in 2 states plus the $\overline{\text{WAIT}}$ signal value (long pitch) when RW1 is 1. When RW1 is set to 1, the number of wait states selected in wait state insertion bits 1 and 0 (RLW0 and RLW1) for CAS-before-RAS (CBR) refresh in the refresh control register (RCR) are inserted during the CBR refresh cycle, regardless of the status of the $\overline{\text{WAIT}}$ signal.

The read cycle of the address/data multiplexed I/O space (area 6) is 4 states plus the wait states from the $\overline{\text{WAIT}}$ signal, regardless of the setting of the RW6 bit. The read cycle of the on-chip supporting module space (area 5) finishes in 3 states, regardless of the setting of the RW5 bit, and the $\overline{\text{WAIT}}$ signal is not sampled. The read cycles of on-chip ROM (area 0) and on-chip RAM (area

7) finish in 1 state, regardless of the settings of bits RW0 and RW7. The $\overline{\text{WAIT}}$ signal is not sampled for either.

Table 8.4 summarizes read cycle state information.

Table 8.4 Read Cycle States

		Read Cycle States				
		External Memory Space			Internal Space	
Bits 15–8: RW7–RW0	$\overline{\text{WAIT}}$ Pin Input Signal	External Memory Space	DRAM Space	Multi-plexed I/O	On-Chip Supporting Modules	On-Chip ROM and RAM
0	Not sampled during read cycle*1	Areas 1, 3–5,7: 1 state, fixed Areas 0, 2, 6: 1 state + long wait state	Column address cycle: 1 state, fixed (short pitch)	4 states + wait states from $\overline{\text{WAIT}}$	3 states, fixed	1 state, fixed
1	Sampled during read cycle (Initial value)	Areas 1, 3–5, 7: 2 states + wait states from $\overline{\text{WAIT}}$ Areas 0, 2, 6: 1 state + long wait state + wait state from $\overline{\text{WAIT}}$	Column address cycle: 2 states + wait state from $\overline{\text{WAIT}}$ (long pitch)*2			

Notes: 1. Sampled in the address/data multiplexed I/O space
2. During a CBR refresh, the $\overline{\text{WAIT}}$ signal is ignored and the wait state from the RLW1 and RLW0 bits in RCR is inserted.

Bits 7–2—Reserved: These bits are always read as 1. The write value should always be 1.

Bit 1—Wait State Control During Write (WW1): WW1 determines the number of states in write cycles for the DRAM space (area 1) and whether or not to sample the $\overline{\text{WAIT}}$ signal. When the DRAM enable bit (DRAME) in BCR is set to 1 and area 1 is being used as DRAM space, clearing WW1 to 0 makes the column address output cycle finish in 1 state (short pitch). When WW1 is set to 1, it finishes in 2 states plus the wait states from the $\overline{\text{WAIT}}$ signal (long pitch).

Note: Write 0 to WW1 only when area 1 is used as DRAM space (DRAME bit in BCR is 1). Never write 0 to WW1 when area 1 is used as external memory space (DRAME is 0).

Bit 1: WW1	DRAM Space (DRAME = 1)	Area 1 External Memory Space (DRAME = 0)
0	Column address cycle: 1 state (short pitch)	Setting inhibited
1	Column address cycle: 2 states + wait state from $\overline{\text{WAIT}}$ (long pitch) (Initial value)	2 states + wait state from $\overline{\text{WAIT}}$

Bit 0—Reserved: This bit is always read as 1. The write value should always be 1.

8.2.3 Wait State Control Register 2 (WCR2)

Wait state control register 2 is a 16-bit read/write register that controls the number of states for accessing each area with a DMA single address mode transfer and whether wait states are used. WCR2 is initialized to H'FFFF by a power-on reset. It is not initialized by a manual reset or in standby mode.

Bit	15	14	13	12	11	10	9	8
	DRW7	DRW6	DRW5	DRW4	DRW3	DRW2	DRW1	DRW0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	DWW7	DWW6	DWW5	DWW4	DWW3	DWW2	DWW1	DWW0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 15–8—Wait State Control During Single-Mode DMA Transfer (DRW7–DRW0): DRW7–DRW0 determine the number of states in single-mode DMA memory read cycles for each area and whether or not to sample the $\overline{\text{WAIT}}$ signal. Bits DRW7–DRW0 correspond to areas 7–0, respectively. If a bit is cleared to 0, the $\overline{\text{WAIT}}$ signal is not sampled during the single-mode DMA memory read cycle for the corresponding area. If it is set to 1, sampling takes place.

For the external memory spaces of areas 1, 3–5, and 7, single-mode DMA memory read cycles are completed in one state when the corresponding bits are cleared to 0. When they are set to 1, the number of wait states is 2 plus the wait states from the $\overline{\text{WAIT}}$ signal. For the external memory space of areas 0, 2, and 6, single-mode DMA memory read cycles are completed in one state plus the long wait state number (set in wait state controller 3 (WCR3)) when the corresponding bits are cleared to 0. When they are set to 1, the number of wait states is 1 plus the long wait state; when the $\overline{\text{WAIT}}$ signal is low as well, a wait state is inserted.

The DRAM space (area 1) finishes the column address output cycle in one state (short pitch) when the DRW1 bit is 0, and in 2 states plus the wait states from the $\overline{\text{WAIT}}$ signal (long pitch) when DRW1 is 1. The single-mode DMA memory read cycle of the address/data multiplexed I/O space (area 6) is 4 states plus the wait states from the $\overline{\text{WAIT}}$ signal, regardless of the setting of the DRW6 bit.

Table 8.5 Single-Mode DMA Memory Read Cycle States (External Memory Space)

		Single-Mode DMA Memory Read Cycle States (External Memory Space)		
Bits 15–8: DRW7–DRW0	**$\overline{\text{WAIT}}$ Pin Input Signal**	**External Memory Space**	**DRAM Space**	**Multiplexed I/O**
0	Not sampled during single-mode DMA memory read cycle*	Areas 1, 3–5,7: 1 state, fixed Areas 0, 2, 6: 1 state + long wait state	Column address cycle: 1 state, fixed (short pitch)	4 states + wait states from $\overline{\text{WAIT}}$
1	Sampled during single-mode DMA memory read cycle (Initial value)	Areas 1, 3–5, 7: 2 states + wait states from $\overline{\text{WAIT}}$ Areas 0, 2, 6: 1 state + long wait state + wait state from $\overline{\text{WAIT}}$	Column address cycle: 2 states + wait state from $\overline{\text{WAIT}}$ (long pitch)	

Note: * Sampled in the address/data multiplexed I/O space.

Bits 7–0—Single-Mode DMA Memory Write Wait State Control (DWW7–DWW0): DWW7–DWW0 determine the number of states in single-mode DMA memory write cycles for each area and whether or not to sample the $\overline{\text{WAIT}}$ signal. Bits DWW7–DWW0 correspond to areas 7–0, respectively. If a bit is cleared to 0, the $\overline{\text{WAIT}}$ signal is not sampled during the single-mode DMA memory write cycle for the corresponding area. If it is set to 1, sampling takes place.

The number of states for areas accesses based on bit settings is the same as indicated for single-mode DMA memory read cycles. See bits 15–8, Wait State Control During Single-Mode DMA Memory Transfer (DRW7–DRW0), for details.

Table 8.6 summarizes single-mode DMA memory write cycle state information.

Table 8.6 Single-Mode DMA Memory Write Cycle States (External Memory Space)

		Single-Mode DMA Memory Write Cycle States (External Memory Space)		
Bits 15–8: DWW7–DWW0	**$\overline{\text{WAIT}}$ Pin Input Signal**	**External Memory Space**	**DRAM Space**	**Multiplexed I/O**
0	Not sampled during single-mode DMA memory write cycle*	Areas 1, 3–5,7: 1 state, fixed Areas 0, 2, 6: 1 state + long wait state	Column address cycle: 1 state, fixed (short pitch)	4 states + wait state from $\overline{\text{WAIT}}$
1	Sampled during single-mode DMA memory write cycle (Initial value)	Areas 1, 3–5, 7: 2 states + wait state from $\overline{\text{WAIT}}$ Areas 0, 2, 6: 1 state + long wait state + wait state from $\overline{\text{WAIT}}$	Column address cycle: 2 states + wait state from $\overline{\text{WAIT}}$ (long pitch)	

Note: * Sampled in the address/data multiplexed I/O space.

8.2.4 Wait State Control Register 3 (WCR3)

Wait state control register 3 is a 16-bit read/write register that controls $\overline{\text{WAIT}}$ pin pull-up and the insertion of long wait states. WCR3 is initialized to H'F800 by a power-on reset. It is not initialized by a manual reset or in standby mode.

Bit	15	14	13	12	11	10	9	8
	WPU	A02LW1	A02LW0	A6LW1	A6LW0	—	—	—
Initial value	1	1	1	1	1	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	—	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit 15—Wait Pin Pull-Up Control (WPU): WPU controls whether the $\overline{\text{WAIT}}$ pin is pulled up or not. When cleared to 0, the pin is not pulled up; when set to 1, it is pulled up.

Bit 15: WPU	Description	
0	$\overline{\text{WAIT}}$ pin is not pulled up	
1	$\overline{\text{WAIT}}$ pin is pulled up	(Initial value)

Bits 14 and 13—Long Wait Insertion in Areas 0 and 2, Bits 1, 0 (A02LW1 and A02LW0): A02LW1 and A02LW0 select the long wait states to be inserted (1–4 states) when accessing external memory space of areas 0 and 2.

Bit 14: A02LW1	Bit 13: A02LW0	Description
0	0	1 state inserted
	1	2 states inserted
1	0	3 states inserted
	1	4 states inserted (Initial value)

Bits 12 and 11—Long Wait Insertion in Area 6, Bits 1, 0 (A6LW1 and A6LW0): A6LW1 and A6LW0 select the long wait states to be inserted (1–4 states) when accessing external memory space of area 6.

Bit 12: A6LW1	Bit 11: A6LW0	Description
0	0	1 state inserted
	1	2 states inserted
1	0	3 states inserted
	1	4 states inserted (Initial value)

Bits 10–0—Reserved: These bits are always read as 0. The write value should always be 0.

8.2.5 DRAM Area Control Register (DCR)

The DRAM area control register (DCR) is a 16-bit read/write register that selects the type of DRAM control signal, the number of precharge cycles, the burst operation mode, and the use of address multiplexing. DCR settings are valid only when the DRAME bit in BCR is set to 1. It is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or in standby mode.

Bit	15	14	13	12	11	10	9	8
	CW2	RASD	TPC	BE	CDTY	MXE	MXC1	MXC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit 15—Dual-CAS or Dual-WE Select Bit (CW2): When accessing a 16-bit bus width space, CW2 selects the dual-CAS or the dual-WE method. When cleared to 0, the $\overline{\text{CASH}}$, $\overline{\text{CASL}}$, and $\overline{\text{WRL}}$ signals are valid ; when set to 1, the $\overline{\text{CASL}}$, $\overline{\text{WRH}}$, and $\overline{\text{WRL}}$ signals are valid. When accessing an 8-bit space, only $\overline{\text{CASL}}$ and $\overline{\text{WRL}}$ signals are valid, regardless of the CW2 setting.

Bit 15L: CW2	Description	
0	Dual-CAS: $\overline{\text{CASH}}$, $\overline{\text{CASL}}$, and $\overline{\text{WRL}}$ signals are valid	(Initial value)
1	Dual-WE: $\overline{\text{CASL}}$, $\overline{\text{WRH}}$, and $\overline{\text{WRL}}$ signals are valid	

Bit 14—RAS Down (RASD): When DRAM access pauses, RASD determines whether to keep $\overline{\text{RAS}}$ low while waiting for the next DRAM access (RAS down mode) or return it to high (RAS up mode). When cleared to 0, the $\overline{\text{RAS}}$ signal returns to high; when set to 1, it stays low.

Bit 14: RASD	Description
0	RAS up mode: Return $\overline{\text{RAS}}$ signal to high and wait for the next DRAM access (Initial value)
1	RAS down mode: Keep $\overline{\text{RAS}}$ signal low and wait for the next DRAM access

Bit 13—RAS Precharge Cycle Count (TPC): TPC selects whether the $\overline{RAS}$ signal precharge cycle (T_P) will be 1 state or 2. When TPC is cleared to 0, a 1-state precharge cycle is inserted; when 1 is set, a 2-state precharge cycle is inserted.

Bit 13: TPC	Description	
0	1-state precharge cycle inserted	(Initial value)
1	2-state precharge cycle inserted	

Bit 12—Burst Operation Enable (BE): BE selects whether or not to perform burst operation, a high-speed page mode. When burst operation is not selected (0), the row address is not compared but instead is transferred to the DRAM every time and full access is performed. When burst operation is selected (1), row addresses are compared and burst operation with the same row address as previously is performed (in this access, no row address is output and the column address and $\overline{CAS}$ signal alone are output) (high-speed page mode).

Bit 12: BE	Description	
0	Normal mode: full access	(Initial value)
1	Burst operation: high-speed page mode	

Bit 11—CAS Duty (CDTY): CDTY selects 35% or 50% of the TC state as the high-level duty ratio of the signal $\overline{CAS}$ in short-pitch access. When cleared to 0, the $\overline{CAS}$ signal high level duty is 50%; when set to 1, it is 35%.

Bit 11: CDTY	Description	
0	$\overline{CAS}$ signal high level duty cycle is 50% of the T_C state	(Initial value)
1	$\overline{CAS}$ signal high level duty cycle is 35% of the T_C state	

Bit 10—Multiplex Enable Bit (MXE): MXE determines whether or not DRAM row and column addresses are multiplexed. When cleared to 0, addresses are not multiplexed; when set to 1, they are multiplexed.

Bit 10: MXE	Description	
0	Multiplexing of row and column addresses disabled	(Initial value)
1	Multiplexing of row and column addresses enabled	

Bits 9 and 8—Multiplex Shift Count 1 and 0 (MXC1 and MXC0): Shift row addresses downward by a certain number of bits (8–10) when row and column addresses are multiplexed (MXE = 1). Regardless of the MXE bit setting, these bits also select the range of row addresses compared in burst operation.

Bit 9: MXC1	Bit 8: MXC0	Row Address Shift (MXE = 1)		Row Address Bits Compared (in Burst Operation) (MXE = 0 or 1)	
0	0	8 bits	(Initial value)	A8–A27	(Initial value)
	1	9 bits		A9–A27	
1	0	10 bits		A10–A27	
	1	Reserved		Reserved	

Bits 7–0—Reserved: These bits are always read as 0. The write value should always be 0.

8.2.6 Refresh Control Register (RCR)

The refresh control register (RCR) is a 16-bit read/write register that controls the start of refreshing and selects the refresh mode and the number of wait states during refreshing. It is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or in standby mode.

To prevent RCR from being written incorrectly, it must be written by a different method from most other registers. A word transfer operation is used, H'5A is written in the upper byte, and the actual data is written in the lower byte. For details, see section 8.2.11, Notes on Register Access.

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
	RFSHE	RMODE	RLW1	RLW0	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Bit 15–8—Reserved: These bits are always read as 0.

Bit 7—Refresh Control (RFSHE): RFSHE determines whether or not to perform DRAM refresh operations. When this bit is cleared to 0, no DRAM refresh control is performed and the refresh timer counter (RTCNT) can be used as an 8-bit interval timer. When set to 1, DRAM refresh control is performed.

Bit 7: RFSHE	Description	
0	Refresh control disabled. RTCNT can be used as an 8-bit interval timer	(Initial value)
1	Refresh control enabled	

Bit 6—Refresh Mode (RMODE): When DRAM refresh control is selected (RFSHE = 1), RMODE selects whether to perform CAS-before-RAS (CBR) refresh or self-refresh. When this bit is cleared to 0, a CBR refresh is performed at the cycle set in the refresh timer control/status register (RTCSR) and refresh time constant register (RTCOR). When set to 1, the DRAM performs a self-refresh. When refresh control is not selected (RFSHE = 0), the RMODE bit setting is not valid. When canceling self-refresh, set RMODE to 0 with RFSHE set to 1.

Bit 6: RMODE	Description	
0	CAS-before-RAS refresh	(Initial value)
1	Self-refresh	

Bits 5 and 4—CBR Refresh Wait State Insertion Bits 1 and 0 (RLW1, RLW0): These bits select the number of wait states to be inserted (1–4) during CAS-before-RAS refreshing. When CBR refresh is performed and the RW1 bit in WCR1 is set to 1, the number of wait states selected by RLW1 and RLW0 is inserted regardless of the $\overline{\text{WAIT}}$ signal. When the RW1 bit is cleared to 0, the RLW1 and RLW0 bit settings are ignored and no wait states are inserted.

Bit 5: RLW1	Bit 4: RLW0	Description	
0	0	1 state inserted	(Initial value)
	1	2 states inserted	
1	0	3 states inserted	
	1	4 states inserted	

Bits 3–0—Reserved: These bits are always read as 0. The write value should always be 0.

8.2.7 Refresh Timer Control/Status Register (RTCSR)

The refresh timer control/status register (RTCSR) is a 16-bit read/write register that selects the clock input to the refresh timer counter (RTCNT) and controls compare match interrupts (CMI). It is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or in standby mode.

To prevent RTCSR from being written incorrectly, it must be written by a different method from most other registers. A word transfer operation is used, H'A5 is written in the upper byte, and the actual data is written in the lower byte. For details, see section 8.2.11, Notes on Register Access.

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
	CMF	CMIE	CKS2	CKS1	CKS0	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	—	—

Bits 15–8—Reserved: These bits are always read as 0.

Bit 7—Compare Match Flag (CMF): Indicates whether the values of RTCNT and the refresh time constant register (RTCOR) match. When 0, the value of RTCNT and RTCOR do not match; when 1, the value of RTCNT and RTCOR match.

Bit 7: CMF	Description
0	RTCNT value does not equal RTCOR value (Initial value) To clear CMF, the CPU must read CMF after it has been set to 1, then write a 0 in this bit
1	RTCNT value is equal to RTCOR value

Bit 6—Compare Match Interrupt Enable (CMIE): Enables or disables the compare match interrupt (CMI) generated when CMF is set to 1 in RTCSR (RTCNT value = RTCOR value). When cleared to 0, the CMI interrupt is disabled; when set to 1, it is enabled.

Bit 6: CMIE	Description	
0	Compare match interrupt request (CMI) is disabled	(Initial value)
1	Compare match interrupt request (CMI) is enabled	

Bits 5–3—Clock Select Bits 2–0 (CKS2–CKS0): These bits select the clock input to RTCNT from among the seven types of clocks created by dividing the system clock (φ). When the input clock is selected with the CKS2–CKS0 bits, RTCNT starts to increment.

Bit 5: CKS2	Bit 4: CKS1	Bit 3: CKS0	Description	
0	0	0	Clock input disabled	(Initial value)
		1	φ/2	
	1	0	φ/8	
		1	φ/32	
1	0	0	φ/128	
		1	φ/512	
	1	0	φ/2048	
		1	φ/4096	

Bits 2–0—Reserved: These bits are always read as 0. The write value should always be 0.

8.2.8 Refresh Timer Counter (RTCNT)

The refresh timer counter (RTCNT) is a 16-bit read/write register that is used as an 8-bit upcounter that generates refresh or interrupt requests. When the input clock is selected by clock select bits 2–0 (CKS2–CKS0) in RTCSR, that clock makes the RTCNT start incrementing. When the values of RTCNT and the refresh time constant register (RTCOR) match, RTCNT is cleared to H'0000 and the CMF flag in RTCSR is set to 1. When the RFSHE bit in RCR is also set to 1, a CAS-before-RAS refresh is performed. When the CMIE bit in RTCSR is also set to 1, a compare match interrupt (CMI) is generated.

Bits 15–8 are reserved and are not incremented. These bits are always read as 0.

RTCNT is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or in standby mode.

To prevent RTCSR from being written incorrectly, it must be written by a different method from most other registers. A word transfer operation is used, H'69 is written in the upper byte, and the actual data is written in the lower byte. For details, see section 8.2.11, Notes on Register Access.

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.2.9 Refresh Time Constant Register (RTCOR)

The refresh time constant register (RTCOR) is a 16-bit read/write register that sets the compare match cycle used with RTCNT. The values in RTCOR and RTCNT are constantly compared. When they match, the compare match flag (CMF) is set in RTCNT and RTCSR is cleared to H'0000. If the RFSHE bit in RCR is set to 1 when this happens, a CAS-before-RAS (CBR) refresh is performed. When the CMIE bit in RTCSR is also set to 1, a compare match interrupt (CMI) is generated.

Bits 15–8 are reserved and cannot be used to set the cycle. These bits are always read as 0.

RTCOR is initialized to H'00FF by a power-on reset, but is not initialized by a manual reset or in standby mode.

To prevent RTCOR from being written incorrectly, it must be written by a different method from most other registers. A word transfer operation is used, H'96 is written in the upper byte, and the actual data is written in the lower byte. For details, see section 8.2.11, Notes on Register Access.

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.2.10 Parity Control Register (PCR)

The parity control register (PCR) is a 16-bit read/write register that selects the parity polarity and space to be parity checked. PCR is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or in standby mode.

Bit	15	14	13	12	11	10	9	8
	PEF	PFRC	PEO	PCHK1	PCHK0	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	—	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit 15—Parity Error Flag (PEF): When a parity check is carried out, PEF indicates whether a parity error has occurred. 0 indicates that no parity error has occurred; 1 indicates that a parity error has occurred.

Bit 15: PEF	Description
0	No parity error (Initial value) Cleared by reading PEF after it has been set to 1, then writing 0 in PEF
1	Parity error has occurred

Bit 14—Parity Output Force (PFRC): PFRC selects whether to produce a forced parity output for testing the parity error check function. When cleared to 0, there is no forced output; when set to 1, it produces a forced high-level output from the DPH and DPL pins when data is output, regardless of the parity.

Bit 14: PFRC	Description	
0	Parity output not forced	(Initial value)
1	High output forced	

Bit 13—Parity Polarity (PEO): PEO selects even or odd parity. When cleared to 0, parity is even; when set to 1, parity is odd.

Bit 13: PEO	Description	
0	Even parity	(Initial value)
1	Odd parity	

Bits 12 and 11—Parity Check Enable Bits 1 and 0 (PCHK1 and PCHK0): These bits determine whether or not parity is checked and generated, and select the check and generation spaces.

Bit 12: PCHK1	Bit 11: PCHK0	Description	
0	0	Parity not checked and not generated	(Initial value)
	1	Parity checked and generated only in DRAM area	
1	0	Parity checked and generated in DRAM area and area 2	
	1	Reserved	

Bits 10–0—Reserved: These bits are always read as 0. The write value should always be 0.

8.2.11 Notes on Register Access

RCR, RTCSR, RTCNT, and RTCOR differ from other registers in being more difficult to write. Data requires a password when it is written. This prevents data from being mistakenly overwritten by program overruns and so on.

Writing to RCR, RTCSR, RTCNT, and RTCOR: Use only word transfer instructions. It is not possible to write with byte transfer instructions. As figure 8.2 shows, when writing to RCR, place H'5A in the upper byte and the write data in the lower byte. When writing to RTCSR, place H'A5 in the upper byte and the write data in the lower byte. When writing to RTCNT, place H'69 in the upper byte and the write data in the lower byte. When writing to RTCOR, place H'96 in the upper byte and the write data in the lower byte. These transfers write data in the lower byte of the respective registers. If the upper byte differs from the above passwords, no writing occurs.

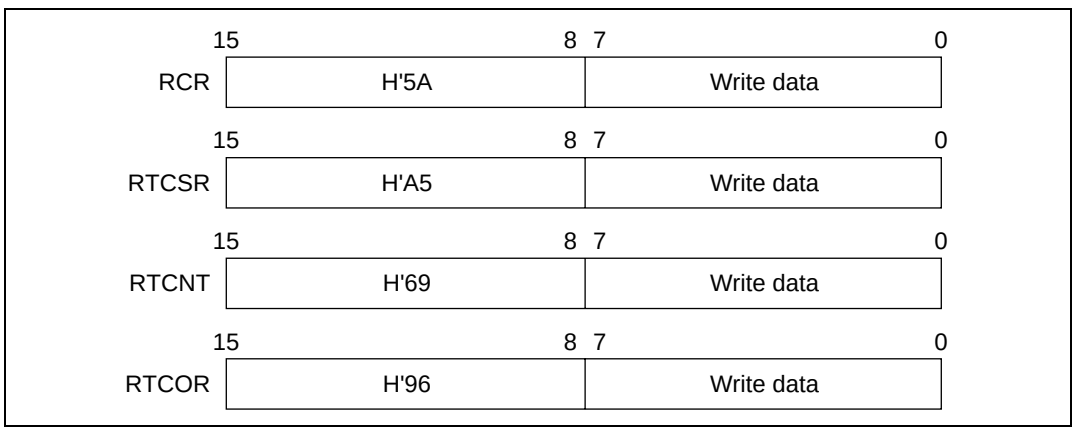


Figure 8.2 Writing to RCR, RTCSR, RTCNT, and RTCOR

Reading from RCR, RTCSR, RTCNT, and RTCOR: These registers are read like other registers. They can be read by byte and word transfer instructions. If read by word transfer, the value of the upper eight bits is H'00.

8.3 Address Space Subdivision

8.3.1 Address Spaces and Areas

Figure 8.3 shows the address format used in this chip.

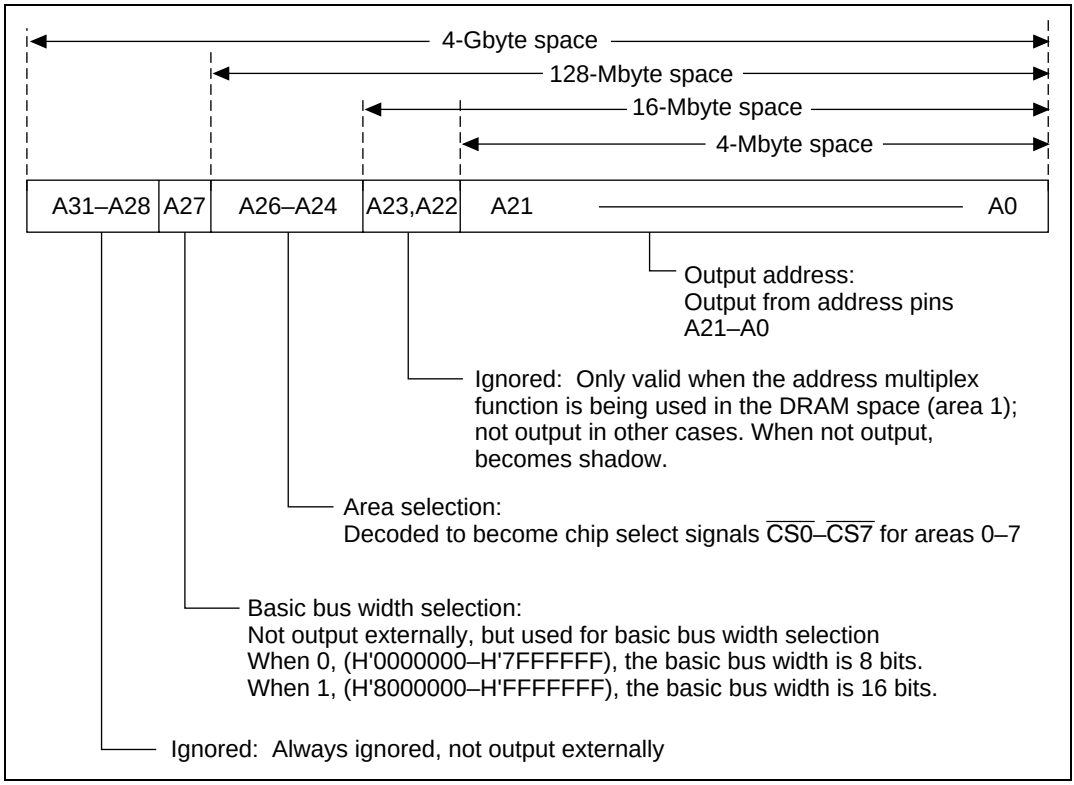


Figure 8.3 Address Format

Since this chip uses a 32-bit address, 4 Gbytes of space can be accessed in the architecture; however, the upper 4 bits (A31–A28) are always ignored and not output. Bit A27 is basically only used for switching the bus width. When the A27 bit is 0 (H'0000000–H'7FFFFFF), the bus width is 8 bits; when the A27 bit is 1 (H'8000000–H'FFFFFFF), the bus width is 16 bits. With the remaining 27 bits (A26–A0), a total of 128 Mbytes can thus be accessed.

The 128-Mbyte space is subdivided into 8 areas (areas 0–7) of 16 Mbytes each according to the values of bits A26–A24. The space with bits A26–A24 as 000 is area 0 and the space with bits A26–A24 as 111 is area 7. The A26–A24 bits are decoded and are output as the chip select signals ($\overline{CS0}$–$\overline{CS7}$) of the corresponding areas 0–7. Table 8.7 shows how the space is divided.

Table 8.7 How Space is Divided

Area	Address	Assignable Memory	Capacity (Linear Space)	Bus Width	CS Output
0	H'0000000–H'0FFFFFF	On-chip ROM*[1]	64 kB	32	—
		External memory*[2]	4 MB	8/16*[3]	$\overline{CS0}$
1	H'1000000–H'1FFFFFF	External memory	4 MB	8	$\overline{CS1}$
		DRAM*[4]	16 MB	8	$\overline{RAS}$ $\overline{CAS}$
2	H'2000000–H'2FFFFFF	External memory	4 MB	8	$\overline{CS2}$
3	H'3000000–H'3FFFFFF	External memory	4 MB	8	$\overline{CS3}$
4	H'4000000–H'4FFFFFF	External memory	4 MB	8	$\overline{CS4}$
5	H'5000000–H'5FFFFFF	On-chip supporting modules	512 B	8/16*[5]	—
6	H'6000000–H'6FFFFFF	External memory*[7]	4 MB	8/16*[6]	$\overline{CS6}$
		Multiplexed I/O	4 MB		
7	H'7000000–H'7FFFFFF	External memory	4 MB	8	$\overline{CS7}$
0	H'8000000–H'8FFFFFF	On-chip ROM*[1]	64 kB	32	—
		External memory*[2]	4 MB	8/16*[3]	$\overline{CS0}$
1	H'9000000–H'9FFFFFF	External memory	4 MB	16	$\overline{CS1}$
		DRAM*[4]	16 MB	16	$\overline{RAS}$ $\overline{CAS}$
2	H'A000000–H'AFFFFFF	External memory	4 MB	16	$\overline{CS2}$
3	H'B000000–H'BFFFFFF	External memory	4 MB	16	$\overline{CS3}$
4	H'C000000–H'CFFFFFF	External memory	4 MB	16	$\overline{CS4}$
5	H'D000000–H'DFFFFFF	External memory	4 MB	16	$\overline{CS5}$
6	H'E000000–H'EFFFFFF	External memory	4 MB	16	$\overline{CS6}$
7	H'F000000–H'FFFFFFF	On-chip RAM	8 kB*[8], 4 kB*[9]	32	—

Notes:
1. When MD2–MD0 pins are 010 (SH7034)
2. When MD2–MD0 pins are 000 or 001
3. Select with MD0 pin
4. Select with DRAME bit in BCR
5. Divided into 8-bit and 16-bit space according to value of address bit A8. (Longword accesses are inhibited, however, for on-chip supporting modules with bus widths of 8 bits. Some on-chip supporting modules with bus widths of 16 bits also have registers that are only byte-accessible and registers for which byte access is inhibited. For details, see the sections on the individual modules.)
6. Divided into 8-bit space and 16-bit space by value of address bit A14
7. Select with IOE bit in BCR
8. For SH7032
9. For SH7034

As table 8.7 shows, specific spaces such as DRAM space and address/data multiplexed I/O space are allocated to the 8 areas. Each of the spaces is equipped with the necessary interfaces. The control signals needed by DRAM and peripheral chips will be output by the chip to devices connected to an area allocated to the appropriate type of space.

8.3.2 Bus Width

The primary bus width selection for this chip is made by switching between 8 bits and 16 bits using the A27 bit. When A27 is 0, the bus width is 8 bits and data is input/output through the AD7–AD0 pins; when A27 is 1, the size is 16 bits and data is input/output through the AD15–AD0 pins for word accesses. For byte access, the upper byte is input/output through AD15–AD8 and the lower byte through AD7–AD0. When the bus width is 8 bits or byte access is being performed with a 16-bit bus width, the status of the eight AD pins that are not inputting/outputting data is as shown in appendix B, Pin States.

Bus widths are also determined by conditions other than the A27 bit for specific areas:

- Area 0 is an 8-bit external memory space when the MD2–MD0 pins are 000, a 16-bit external memory space when these bits are 001, and a 32-bit on-chip ROM space when they are 010 (the on-chip ROM is available only in the SH7034).
- Area 5 is an 8-bit on-chip supporting module space when the A27 bit and A8 bit are both 0 and a 16-bit on-chip supporting module space when the A27 bit is 0 and the A8 bit is 1. When the A27 bit is 1, it is a 16-bit external memory space.
- Area 6 has an 8-bit bus width when the A27 bit and A14 bit are both 0 and a 16-bit bus width when the A27 bit is 0 and the A14 bit is 1. When the A27 bit is 1, it is a 16-bit space.
- Area 7 is a 32-bit on-chip RAM space when the A27 bit is 1 and an 8-bit external memory space when the A27 bit is 0.

Word (16-bit) data accessed from 8-bit bus areas and longword (32-bit) data accessed from 16-bit bus areas require two consecutive accesses. Longword (32-bit) data accessed from 8-bit bus areas requires four consecutive accesses.

8.3.3 Chip Select Signals ($\overline{\text{CS0}}$–$\overline{\text{CS7}}$)

When the A26–A24 bits of the address are decoded, they become chip select signals ($\overline{\text{CS0}}$–$\overline{\text{CS7}}$) for areas 0–7. When an area is accessed, the corresponding chip select pin is driven low. Table 8.8 shows the relationship between the A26–A24 bits and the chip select signals.

Table 8.8 A26–A24 Bits and Chip Select Signals

Address				
A26	**A25**	**A24**	**Area Selected**	**Chip Select Pin Driven Low**
0	0	0	Area 0	$\overline{CS0}$
		1	Area 1	$\overline{CS1}$
	1	0	Area 2	$\overline{CS2}$
		1	Area 3	$\overline{CS3}$
1	0	0	Area 4	$\overline{CS4}$
		1	Area 5	$\overline{CS5}$
	1	0	Area 6	$\overline{CS6}$
		1	Area 7	$\overline{CS7}$

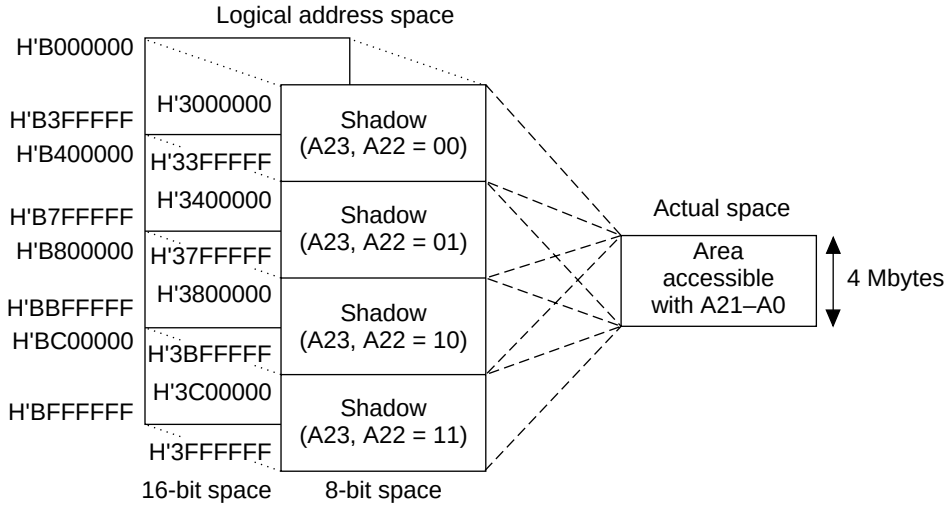
The chip select signal is output only for external accesses. When accessing the on-chip ROM (area 0), on-chip supporting modules (area 5), and on-chip RAM (area 7), the $\overline{CS0}$, $\overline{CS5}$, and $\overline{CS7}$ pins are not driven low. When accessing DRAM space (area 1), select the $\overline{RAS}$ and $\overline{CAS}$ signals with the pin function controller.

8.3.4 Shadows

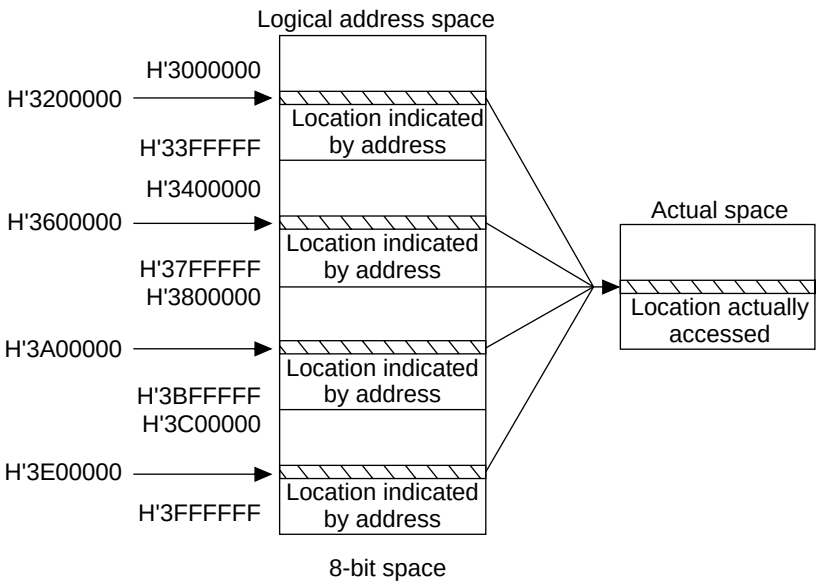
The size of each area is 16 Mbytes, which can be specified with the 24 address bits A23–A0 for 8-bit spaces and 16-bit spaces alike. Bits A23 and A22, however, output externally only when the address multiplex function is used in DRAM space (area 1); in all other cases, there is no output, so the actually accessible area for all areas is the 4 Mbytes that can be specified with the 22 bits A21–A0. Regardless of the values of A23 and A22, the same 4 Mbytes of actual space is accessed. As illustrated in figure 8.4 (a), the A23 and A22 bit regions 00, 01, 10 and 11 are called shadows of actual areas. Shadows are allocated in 4-Mbyte units for both 8-bit and 16-bit bus widths. When the same addresses H'3200000, H'3600000, H'3A00000 and H'3E00000 are specified for values A21–A0, as shown in figure 8.4 (b), the same actual space is accessed regardless of the A23 and A22 bits.

In areas whose bus widths are switchable using the A27 address bit, the shadow of the same actual space is allocated to both A27 = 0 spaces and A27 = 1 spaces (figure 8.4(a)). When the value of A27 is changed, the valid AD pins switch from AD15–AD0 to AD7–AD0, but the actual space accessed remains the same.

The spaces of on-chip ROM (area 0), DRAM (area 1), on-chip supporting modules (area 5), and on-chip RAM (area 7) have shadows of different sizes from those mentioned above. See section 8.3.5, Area Descriptions, for details.



a. Shadow allocation



b. Actual space accessed when addresses are specified

Figure 8.4 Shadows

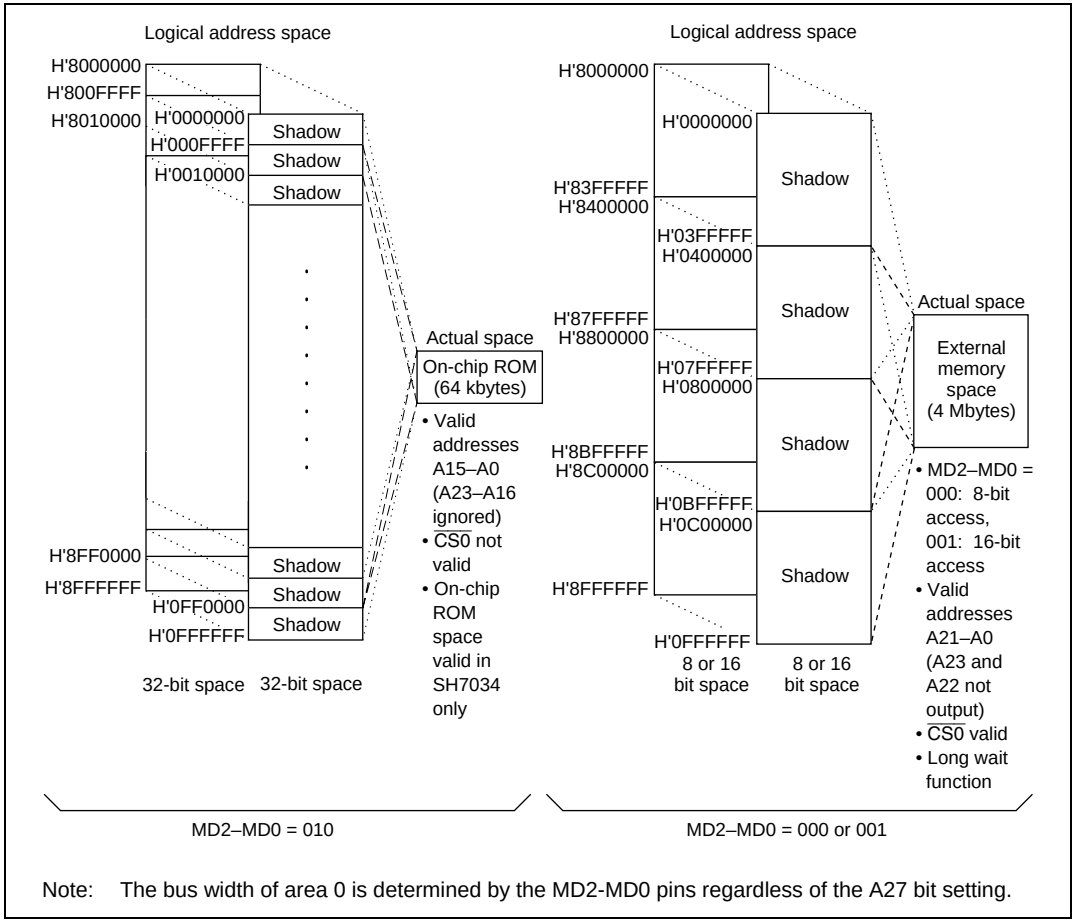
8.3.5 Area Descriptions

Area 0: Area 0 is an area with address bits A26–A24 set to 000 and an address range of H'0000000–H'0FFFFFF and H'8000000–H'8FFFFFF. Figure 8.5 shows a memory map of area 0.

Area 0 can be set for use as on-chip ROM space or external memory space with the mode pins (MD2–MD0). The MD2–MD0 pins also determine the bus width, regardless of the A27 address bit. When MD2–MD0 are 000, area 0 is an 8-bit external memory space; when they are 001, area 0 is a 16-bit external memory space; and when they are 010, it is a 32-bit on-chip ROM space. In the SH7032, area 0 can only be used as external memory space since there is no on-chip ROM, and this last setting is meaningless.

The capacity of the on-chip ROM is 64 kbytes, so bits A23–A16 are ignored in on-chip ROM space and the shadow is in 64-kbyte units. The $\overline{CS0}$ signal is disabled.

In external memory space, the A23 and A22 bits are not output and the shadow is in 4-Mbyte units. When external memory space is accessed, the $\overline{CS0}$ signal is valid. The external memory space has a long wait function, so between 1 and 4 states can be selected for the number of long waits inserted into the bus cycle using the area 0 and 2 long wait insertion bits (A02LW1, A02LW0) of wait state controller 3 (WCR3).



Note: The bus width of area 0 is determined by the MD2-MD0 pins regardless of the A27 bit setting.

Figure 8.5 Memory Map of Area 0

Area 1: Area 1 is an area with address bits A26–A24 set to 001 and an address range of H'1000000–H'1FFFFFF and H'9000000–H'9FFFFFF. Figure 8.6 shows a memory map of area 1.

Area 1 can be set for use as DRAM space or external memory space with the DRAM enable bit (DRAME) in the bus control register (BCR). When the DRAME bit is 0, area 1 is external memory space; when DRAME is 1, it is DRAM space.

In external memory space, the bus width is 8 bits when the A27 bit is 0 and 16 bits when it is 1. Bits A23 and A22 are not output and the shadow is in 4-Mbyte units. When external memory is accessed, the $\overline{CS1}$ signal is valid.

DRAM space is a type of external memory space, but it is configured especially to be connected to DRAM, so it outputs strobe signals required for this purpose. The access size is 8 bits when

address bit A27 is 0 and 16 bits when A27 is 1. When the multiplex enable bit (MXE) in the DRAM control register (DCR) is set to 1 to use the address multiplex function, bits A23–A0 are multiplexed and output from pins A15–A0, so a maximum 16-Mbyte space can be used. When DRAM space is accessed, the $\overline{CS1}$ signal is not valid and the pin function controller should be set for access with $\overline{CAS}$ ($\overline{CASH}$ and $\overline{CASL}$) and $\overline{RAS}$ signals.

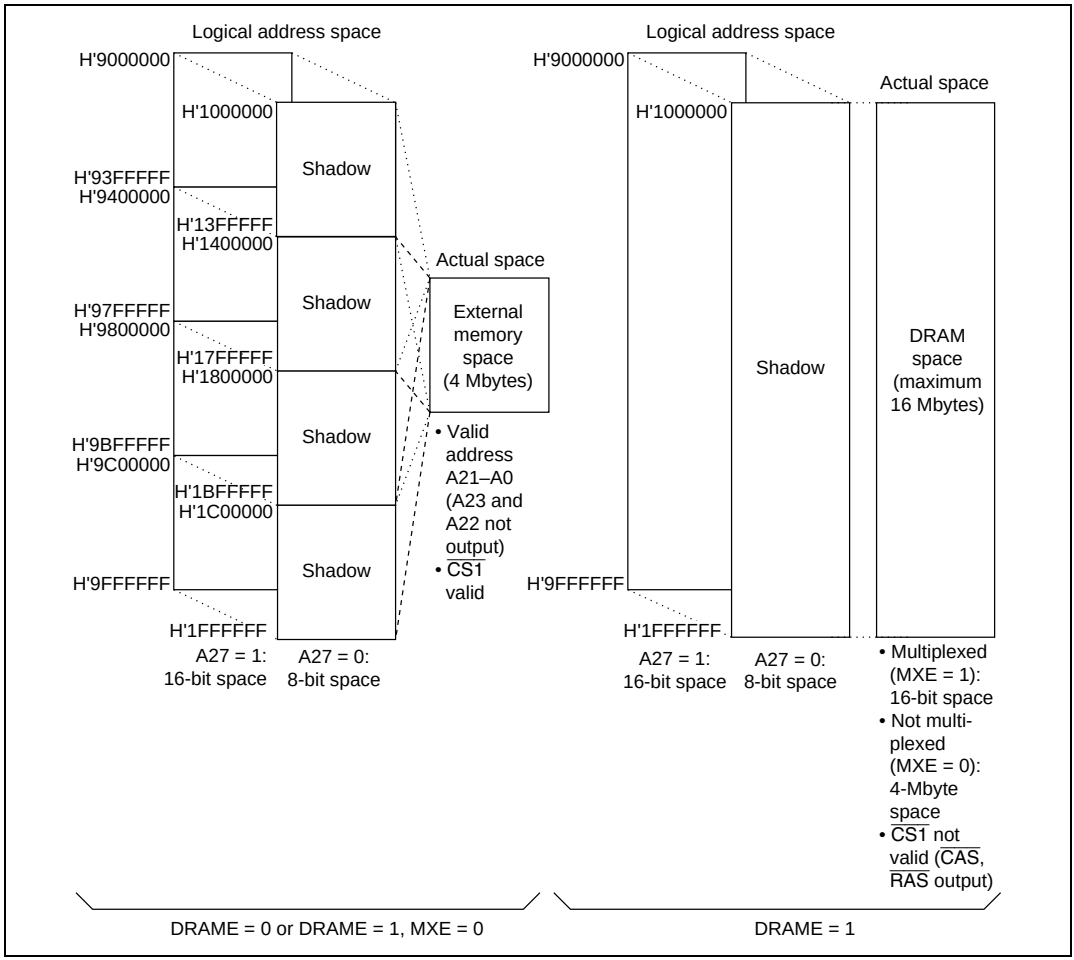


Figure 8.6 Memory Map of Area 1

Areas 2–4: Areas 2–4 are areas with address bits A26–A24 set to 010, 011, and 100, respectively, and address ranges of H'2000000–H'2FFFFFF and H'A000000–H'AFFFFFF (area 2), H'3000000–H'3FFFFFF and H'B000000–H'BFFFFFF (area 3), and H'4000000–H'4FFFFFF and H'C000000–H'CFFFFFF (area 4). Figure 8.7 shows a memory map of area 2, which is representative of areas 2–4.

Areas 2–4 are always used as external memory space. The bus width is 8 bits when the A27 bit is 0 and 16 bits when it is 1. A23 and A22 bits are not output and the shadow is in 4-Mbyte units. When areas 2–4 are accessed, the $\overline{CS2}$, $\overline{CS3}$, and $\overline{CS4}$ signals are valid. Area 2 has a long wait function, so between 1 and 4 states can be selected for the number of long waits inserted into the bus cycle using bits A02LW1 and A02LW0 in WCR3.

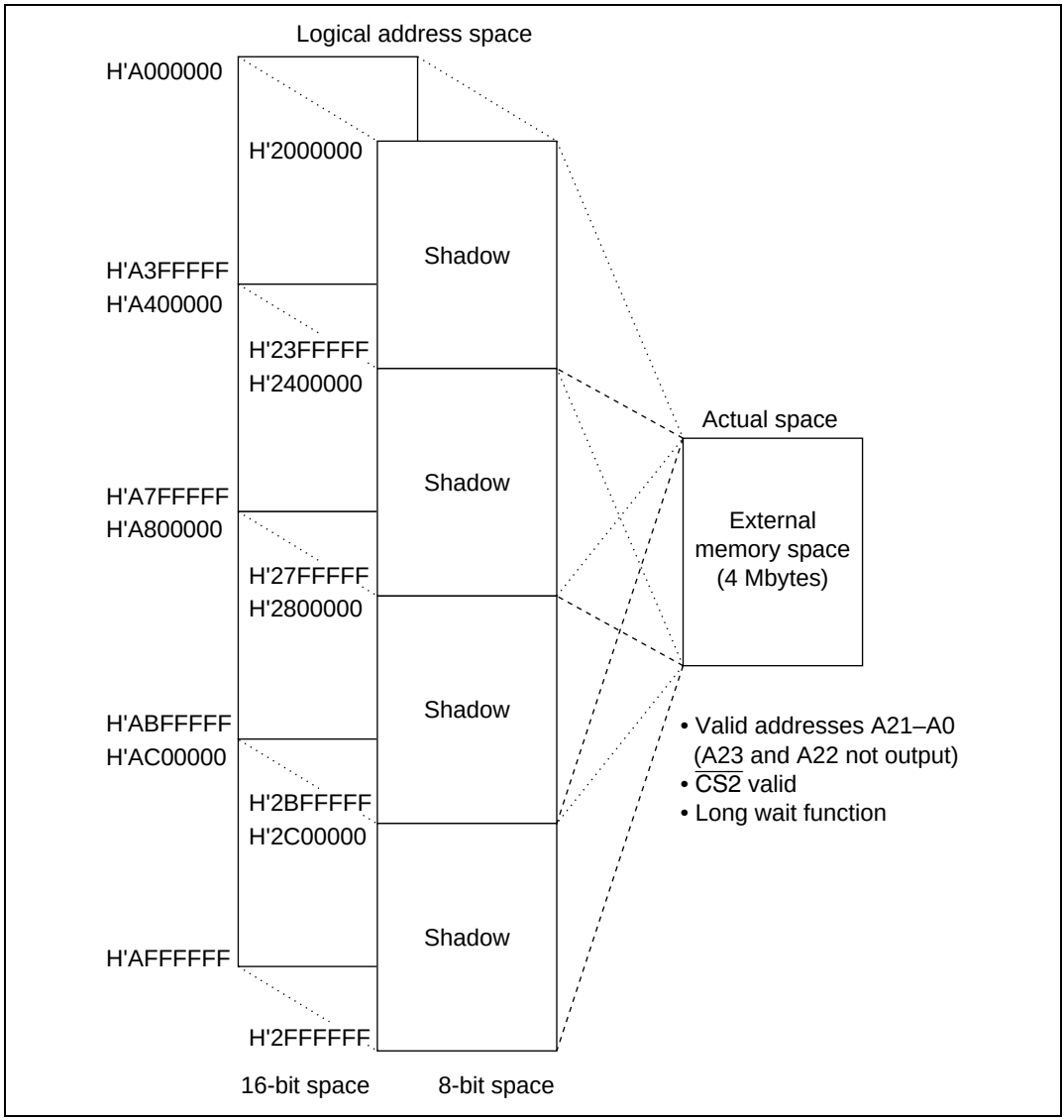
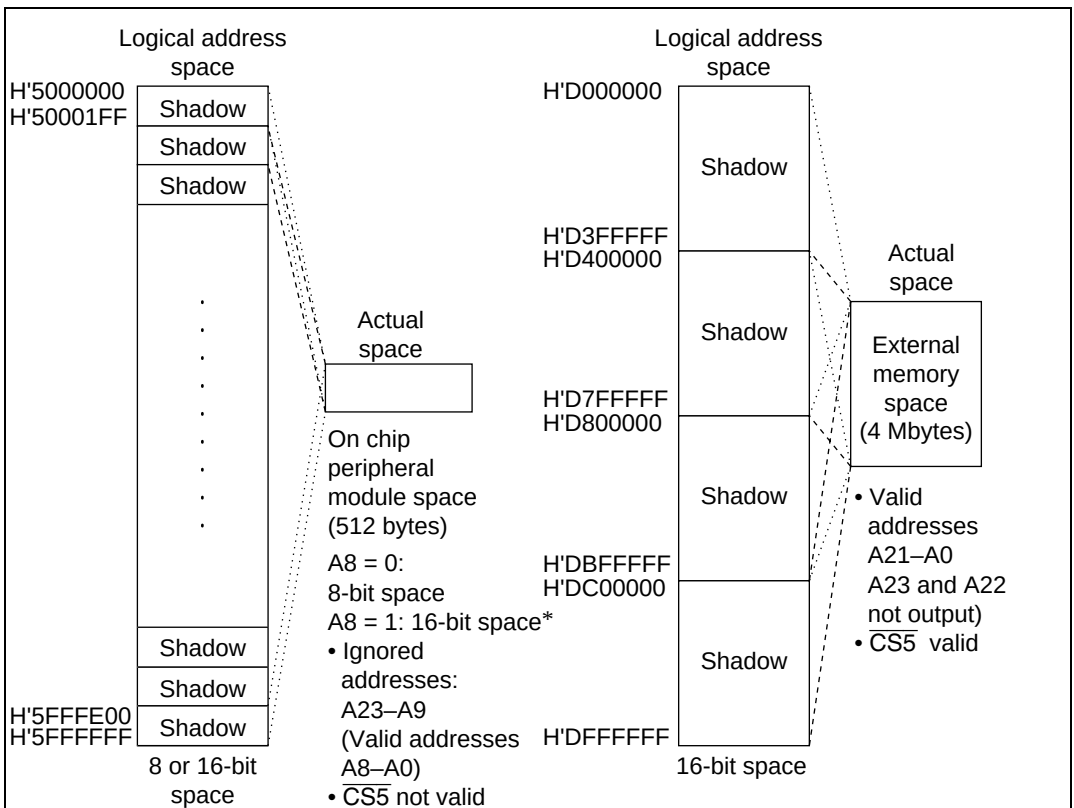


Figure 8.7 Memory Map of Area 2

Area 5: Area 5 is an area with address bits A26–A24 set to 101 and an address range of H'5000000–H'5FFFFFF and H'D000000–H'DFFFFFF. Figure 8.8 shows a memory map of area 5.

Area 5 is allocated to on-chip supporting module space when the A27 address bit is 0 and external memory space when A27 is 1. In on-chip supporting module space, bits A23–A9 are ignored and the shadows are in 512-byte units. The bus width is 8 bits when the A8 bit is 0 and 16 bits when A8 is 1. When on-chip supporting module space is accessed, the $\overline{CS5}$ signal is not valid. In external memory space, the A23 and A22 bits are not output and the shadow is in 4-Mbyte units. The bus width is always 16 bits. When external memory space is accessed, the $\overline{CS5}$ signal is valid.



Note: * Some on-chip supporting module registers can only be accessed as 8-bit registers even though they occupy 16 bits (see Appendix A).

Figure 8.8 Memory Map of Area 5

Area 6: Area 6 is an area with address bits A26–A24 set to 110 and an address range of H'6000000–H'6FFFFFF and H'E000000–H'EFFFFFF. Figure 8.9 shows a memory map of area 6.

In area 6, a space for which address bit A27 is 0 is allocated to address/data multiplexed I/O space when the multiplexed I/O enable bit (IOE) of the bus control register (BCR) is 1, and to external memory space when the IOE bit is 0. When A27 is 1, it is always external memory space.

The multiplexed I/O space is a type of external memory space but the address and data are multiplexed and output from AD15–AD0 or AD7–AD0. The bus width is 8 bits when the A14 bit is 0 and 16 bits when the A14 bit is 1. The A23 and A22 bits are not output and the shadow is in 4-Mbyte units. When multiplexed I/O space is accessed, the $\overline{CS6}$ signal is valid.

In external memory space, the bus width is 8 bits when both the A27 and A14 bits are 0 and 16 bits when the A27 bit is 0 and the A14 bit is 1. When the A27 bit is 1, it is always a 16-bit space. The A23 and A22 bits are not output and the shadow is in 4-Mbyte units. When external memory is accessed, the $\overline{CS6}$ signal is valid. The external memory space has a long wait function so between 1 and 4 states can be selected for the number of long waits inserted into the bus cycle using the area 6 long wait insertion bits (A6LW1 and A6LW0) in WCR3.

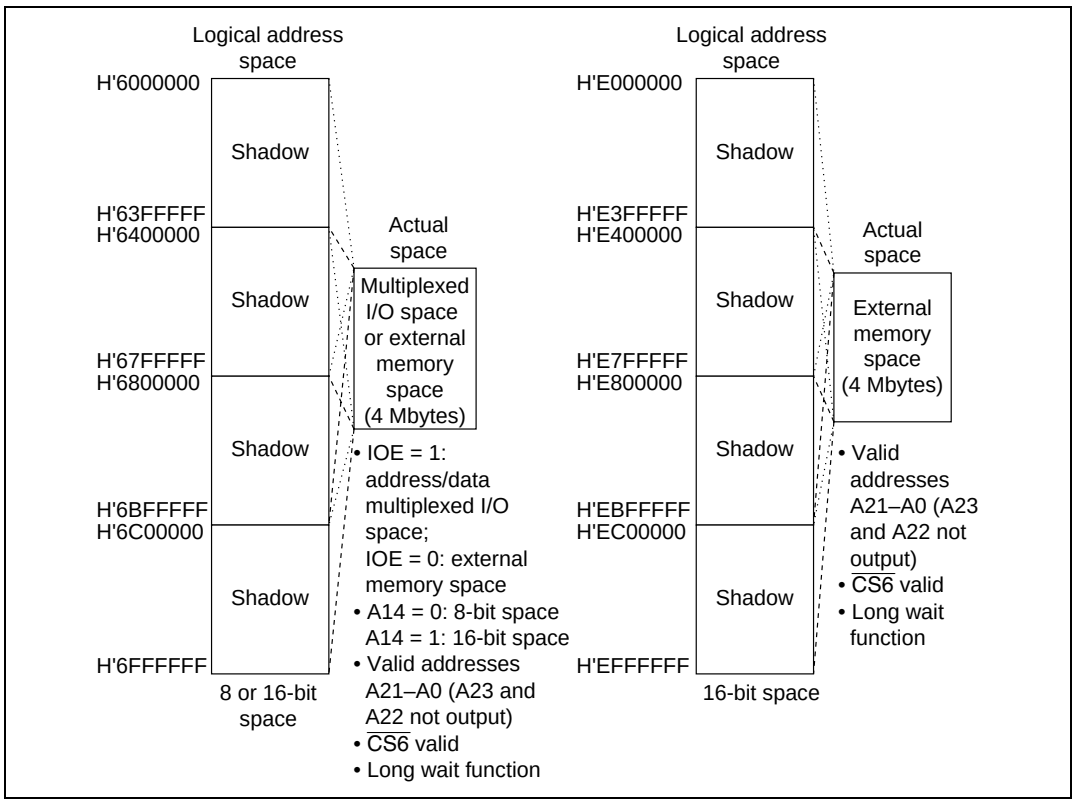


Figure 8.9 Memory Map of Area 6

Area 7: Area 7 is an area with address bits A26–A24 set to 111 and an address range of H'7000000–H'7FFFFFF and H'F000000–H'FFFFFFF. Figure 8.10 shows a memory map of area 7.

Area 7 is allocated to external memory space when A27 is 0 and on-chip RAM space when A27 is 1. In external memory space, the bus width is 8 bits. The A23 and A22 bits are not output and the shadow is in 4-Mbyte units. When external memory is accessed, the $\overline{CS7}$ signal is valid.

The on-chip RAM space has a bus width of 32 bits. In the SH7032, the on-chip RAM capacity is 8 kbytes, so A23–A13 are ignored and the shadows are in 8-kbyte units. In the SH7034, the on-chip RAM capacity is 4 kbytes, so A23–A12 are ignored and the shadows are in 4-kbyte units. During on-chip RAM access, the $\overline{CS7}$ signal is not valid.

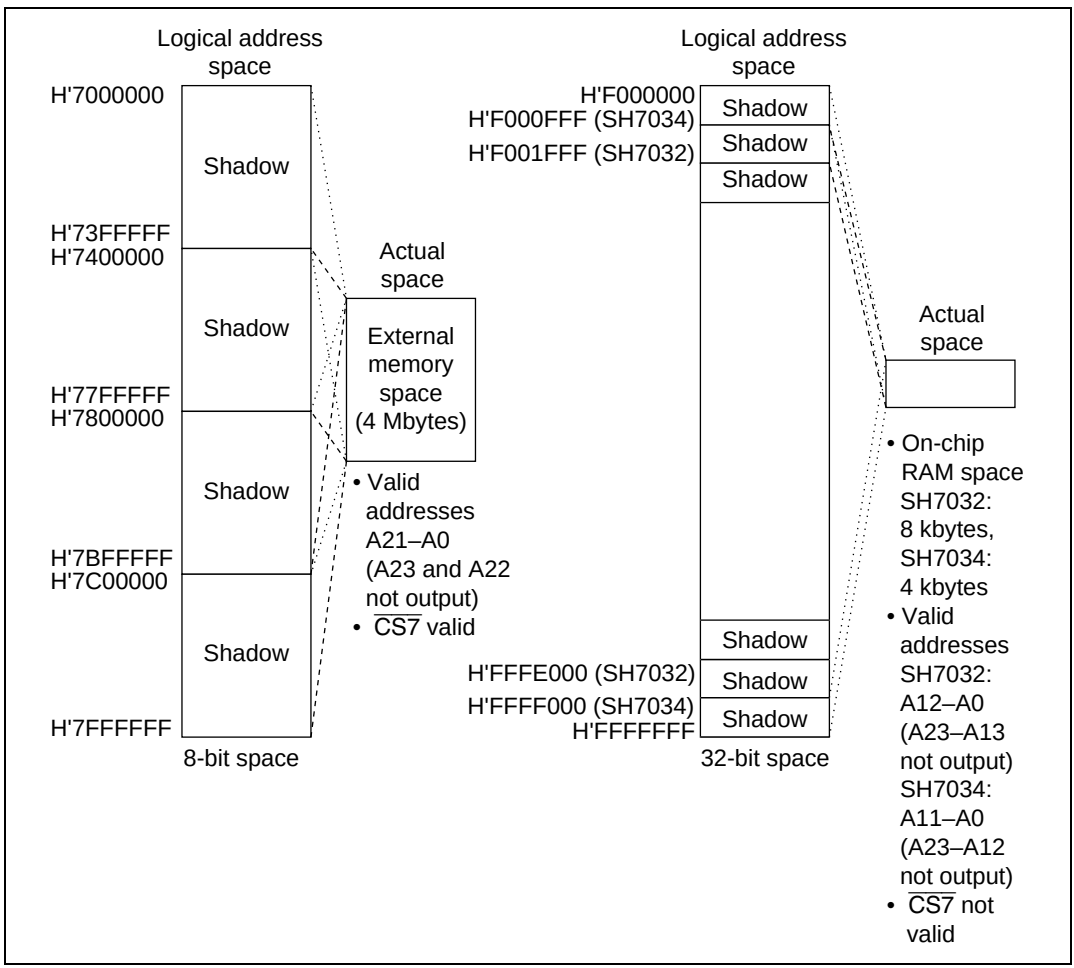


Figure 8 10 Memory Map of Area 7

8.4 Accessing External Memory Space

In external memory space, a strobe signal is output based on the assumption of a directly connected SRAM. The external memory space is allocated to the following areas:

- Area 0 (when MD2–MD0 are 000 or 001)
- Area 1 (when the DRAM enable bit (DRAME) in BCR is 0)
- Areas 2–4
- Area 5 (space where address bit A27 is 1)
- Area 6 (when the multiplexed I/O enable bit (IOE) bit in BCR is 0, or space where address bit A27 is 1)
- Area 7 (space where address bit A27 is 0)

8.4.1 Basic Timing

The bus cycle for external memory space access is 1 or 2 states. The number of states is controlled with wait states by the settings of wait state control registers 1–3 (WCR1–WCR3). For details, see section 8.4.2, Wait State Control. Figures 8.11 and 8.12 illustrate the basic timing of external memory space access.

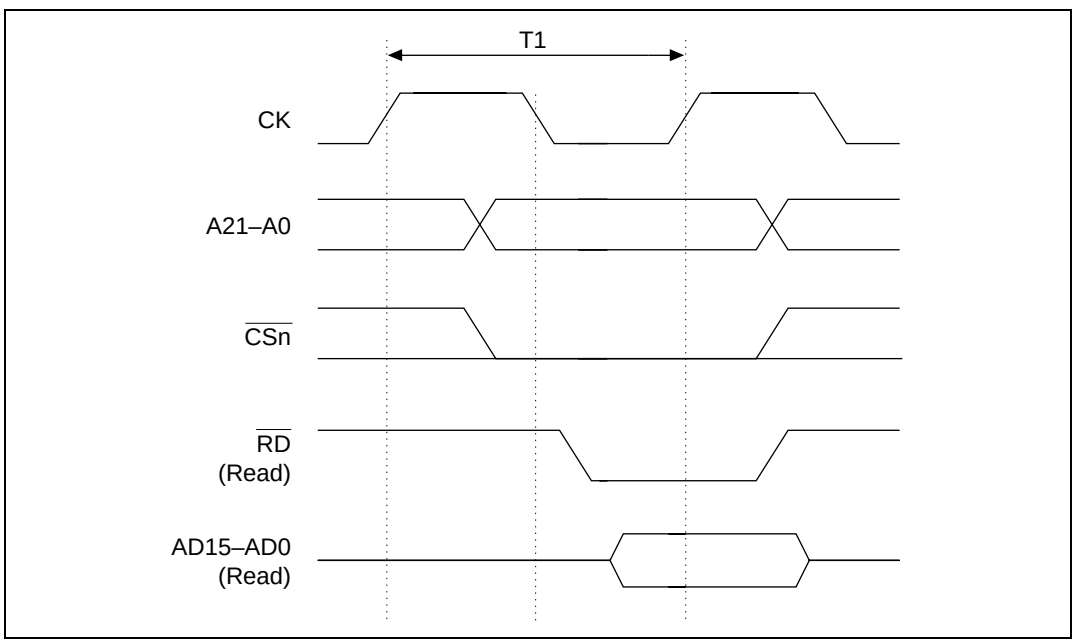


Figure 8.11 Basic Timing of External Memory Space Access (1-State Read Timing)

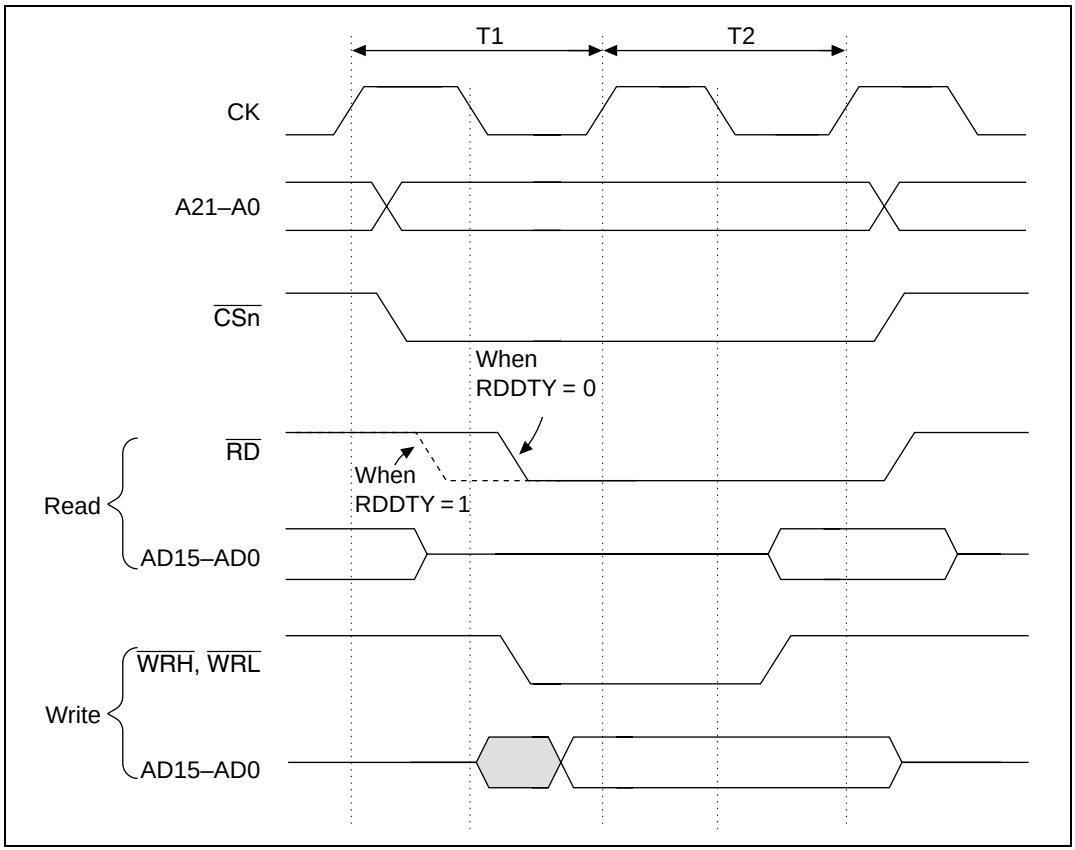


Figure 8.12 Basic Timing of External Memory Space Access (2-State Read Timing)

High-level duties of 35% and 50% can be selected for the $\overline{RD}$ signal using the RD duty bit (RDDTY) in BCR. When RDDTY is set to 1, the high-level duty is 35% of the T1 state, enabling longer access times for external devices. Only set to 1 when the operating frequency is a minimum of 10 MHz.

8.4.2 Wait State Control

The number of external memory space access states and the insertion of wait states can be controlled using the WCR1–WCR3 bits. The bus cycles that can be controlled are the CPU read cycle and the DMAC dual mode read cycle. The bus cycle that can be controlled using the WCR2 is the DMAC single-mode read/write cycle.

Table 8.9 shows the number of states and number of wait states in access cycles to external memory spaces.

Table 8.9 Number of States and Number of Wait States in Access Cycles to External Memory Spaces

	CPU Read Cycle, DMAC Dual Mode Read Cycle, DMAC Single Mode Read/Write Cycle		CPU Write Cycle and DMAC Dual Mode Write Cycle (Cannot be controlled by WCR1)*2
Area	Corresponding Bits in WCR1 and WCR2 = 0	Corresponding Bits in WCR1 and WCR2 = 1	
1, 3–5, 7	1 cycle fixed; $\overline{\text{WAIT}}$ signal ignored	2 cycles fixed + wait state from $\overline{\text{WAIT}}$ signal*3	
0, 2, 6 (long wait available)	1 cycle + long wait state, $\overline{\text{WAIT}}$ signal ignored	1 cycle + long wait state*1 + wait state from $\overline{\text{WAIT}}$ signal	

Notes: 1. The number of long wait states is set by WCR3.
2. When DRAME = 1, short pitch/long pitch is selected with the WW1 bit in WCR1.
3. Pin wait cannot be used for the CS7 and $\overline{\text{WAIT}}$ pins of area 3 because they are multiplexed.

For the CPU read cycle, DMAC dual mode read cycle, and DMAC single mode read/write cycle, the access cycle is completed in 1 state when the corresponding bits of WCR1 and WCR2 for areas 1, 3–5, and 7 are cleared to 0 and the $\overline{\text{WAIT}}$ pin input signal is not sampled. When the bits are set to 1, the $\overline{\text{WAIT}}$ signal is sampled and the number of states is 2 plus the number of wait states set by the $\overline{\text{WAIT}}$ signal. The $\overline{\text{WAIT}}$ signal is sampled at the rise of the system clock (CK) directly preceding the second state of the bus cycle and the wait states are inserted as long as the level is low. When a high level is detected, it shifts to the second state (final state). Figure 8.13 shows the wait state timing when accessing the external memory spaces of areas 1, 3, 4, 5, and 7.

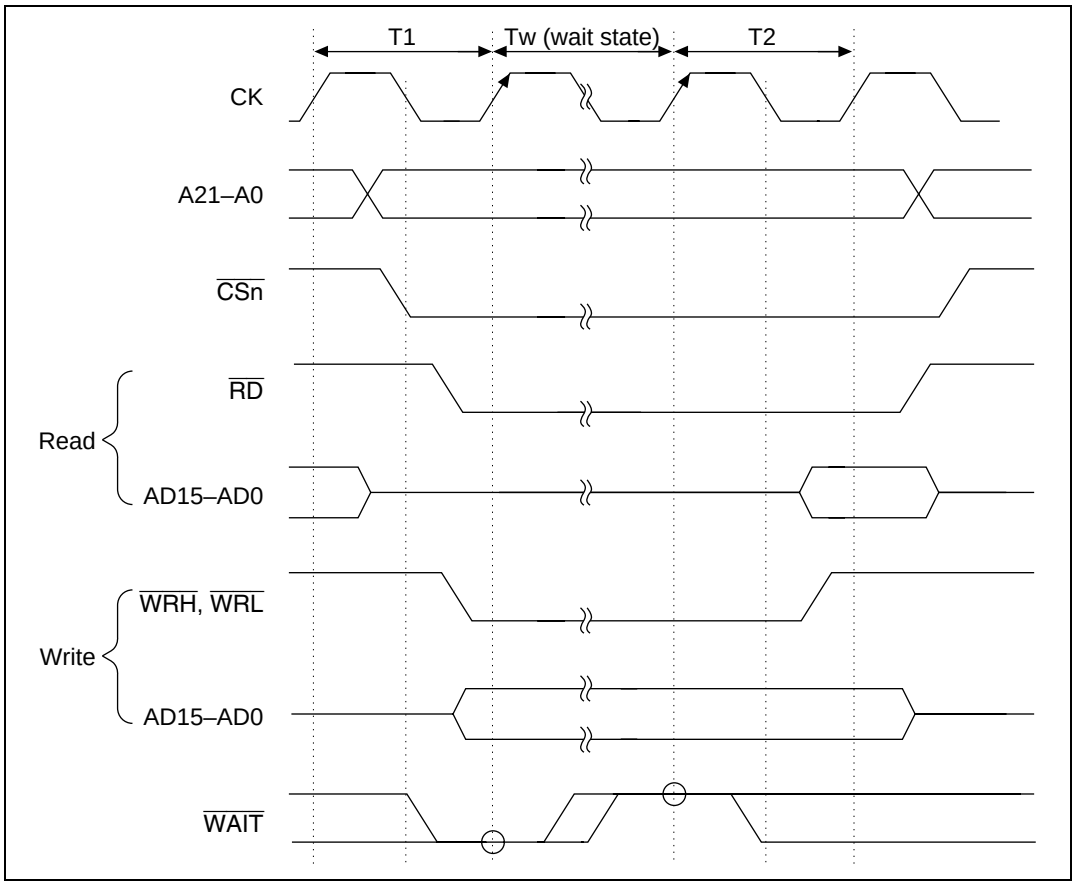


Figure 8.13 Wait State Timing for External Memory Space Access (2 States Plus Wait States from $\overline{\text{WAIT}}$ Signal)

Areas 0, 2, and 6 have long wait functions. When the corresponding bits in WCR1 and WCR2 are cleared to 0, the access cycle is 1 state plus the number of long wait states (set in WCR3, selectable between 1 and 4) and the $\overline{\text{WAIT}}$ pin input signal is not sampled. When the bits are set to 1, the $\overline{\text{WAIT}}$ signal is sampled and the number of states is 1 plus the number of long wait states plus the number of wait states set by the $\overline{\text{WAIT}}$ signal. The $\overline{\text{WAIT}}$ signal is sampled at the rise of the system clock (CK) directly preceding the last long wait state and the wait states are inserted as long as the level is low. When a high level is detected, it shifts to the final long wait state. Figure 8.14 shows the wait state timing when accessing the external memory spaces of areas 0, 2, and 6.

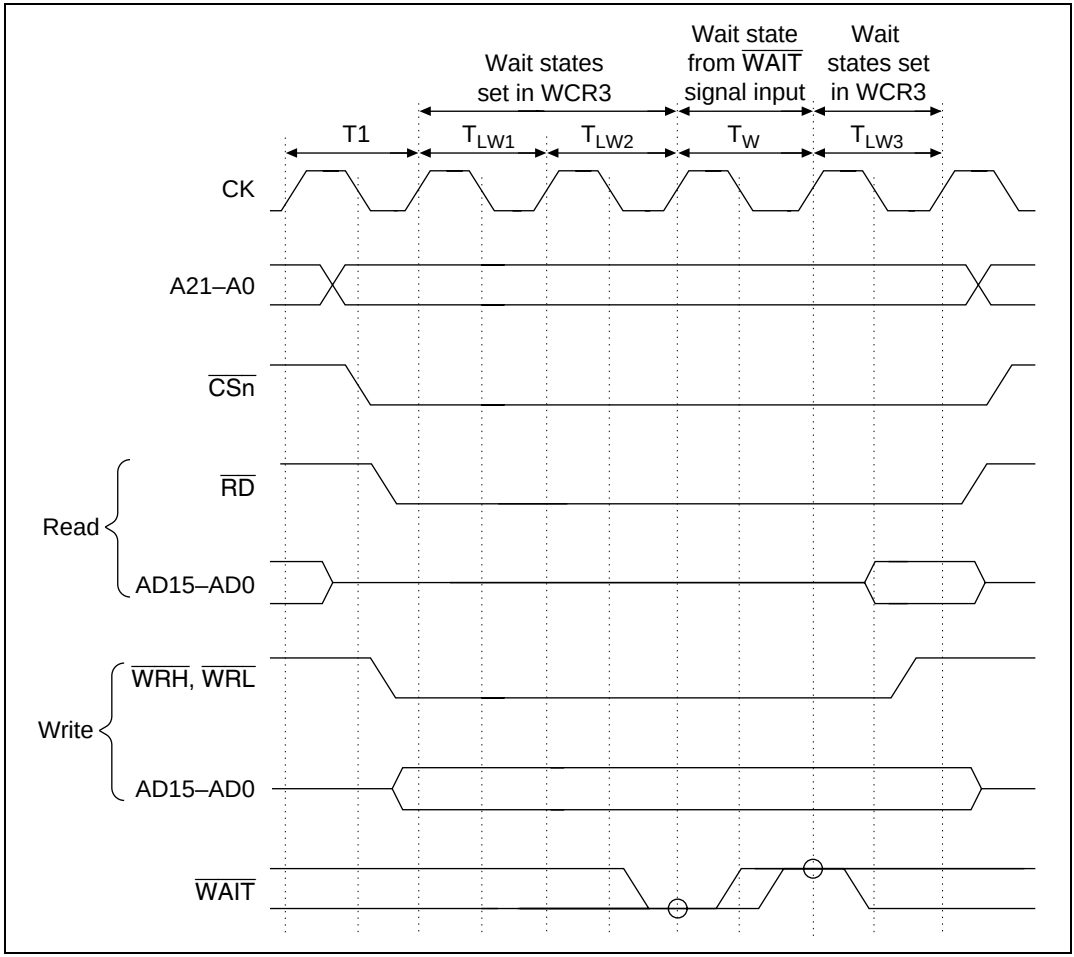


Figure 8.14 Wait State Timing for External Memory Space Access (1 State Plus Long Wait State (When Set to Insert 3 States) Plus Wait States from $\overline{\text{WAIT}}$ Signal)

For CPU write cycles and DMAC dual mode write cycles to external memory space, the number of states and wait state insertion cannot be controlled by WCR1. In areas 1, 3, 4, 5, and 7, the $\overline{\text{WAIT}}$ signal is sampled and the number of states is 2 plus the number of wait states set by the $\overline{\text{WAIT}}$ signal (figure 8.13). In areas 0, 2 and 6, the number of states is 1 state plus the number of long wait states plus the number of wait states set by the $\overline{\text{WAIT}}$ signal (figure 8.14). Do not write 0 in bits 7–2 and 0 of WCR1; only write 1. When area 1 is being used as external memory space, do not write 0 in bit 1 (WW1); always write 1.

8.4.3 Byte Access Control

The upper byte and lower byte control signals when 16-bit bus width space is being accessed can be selected from ($\overline{WRH}$, $\overline{WRL}$, A0) or ($\overline{WR}$, $\overline{HBS}$, $\overline{LBS}$). When the byte access select bit (BAS) in BCR is set to 1, the $\overline{WRH}$, $\overline{WRL}$, and A0 pins output $\overline{WR}$, $\overline{LBS}$, and $\overline{HBS}$ signals. Figure 8.15 illustrates the control signal output timing in the byte write cycle.

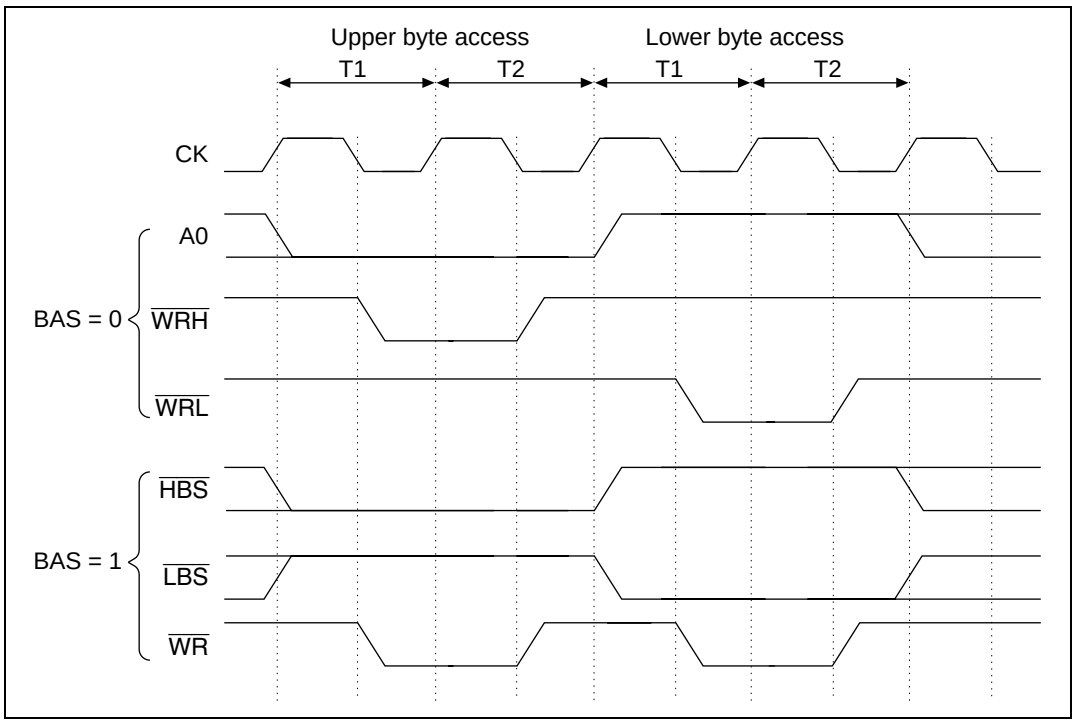


Figure 8.15 Byte Access Control Timing For External Memory Space Access (Write Cycle)

The $\overline{WRH}$, $\overline{WRL}$ system and the $\overline{HBS}$, $\overline{LBS}$ system are available as byte access signals for 16-bit space in address/data multiplexing space and external memory space.

These strobe signals are assigned to pins in the manner: A0/$\overline{HBS}$, $\overline{WRH}$/$\overline{LBS}$, $\overline{WRL}$/$\overline{WR}$, and the BAS bit in the bus control register (BCR) is used to switch specify signal sending.

Note that the byte access signals are strobe signals specifically for byte access to a 16-bit space and are not to be used for byte access to an 8-bit space. When making an access to an 8-bit space, use the A0/$\overline{HBS}$ pin as A0 irrespective of the BAS bit value to use the $\overline{WRL}$/$\overline{WR}$ pin as the $\overline{WR}$ pin, and avoid using the $\overline{WRH}$/$\overline{LBS}$ pin.

8.5 DRAM Interface Operation

When the DRAM enable bit (DRAME) in BCR is set to 1, area 1 becomes DRAM space and the DRAM interface function is available, which permits direct connection of this chip to DRAMs.

8.5.1 DRAM Address Multiplexing

When the multiplex enable bit (MXE) in the DRAM area control register (DCR) is set to 1, row addresses and column addresses are multiplexed. This allows DRAMs that require multiplexing of row and column addresses to be connected directly to an SH microprocessor without additional multiplexing circuits. When addresses are multiplexed (MXE = 1), setting of the DCR's multiplex shift bits (MXC1, MXC0) allows selection of eight, nine and ten-bit row address shifting. Table 8.10 illustrates the relationship between the MXC1/MXC0 bits and address multiplexing.

Table 8.10 Relationship between Multiplex Shift Count Bits (MXC1, MXC0) and Address Multiplexing

	8-Bit Shift		9-Bit Shift		10-Bit Shift	
Output Pin	**Output Row Address**	**Output Column Address**	**Output Row Address**	**Output Column Address**	**Output Row Address**	**Output Column Address**
A21	Undefined	A21	Undefined	A21	Undefined	A21
A20	Value	A20	Value	A20	Value	A20
A19		A19		A19		A19
A18		A18		A18		A18
A17		A17		A17		A17
A16		A16		A16		A16
A15	A23	A15		A15		A15
A14	A22	A14	A23	A14		A14
A13	A21	A13	A22	A13	A23	A13
A12	A20	A12	A21	A12	A22	A12
A11	A19	A11	A20	A11	A21	A11
A10	A18	A10	A19	A10	A20	A10
A9	A17	A9	A18	A9	A19	A9
A8	A16	A8	A17	A8	A18	A8
A7	A15	A7	A16	A7	A17	A7
A6	A14	A6	A15	A6	A16	A6
A5	A13	A5	A14	A5	A15	A5
A4	A12	A4	A13	A4	A14	A4
A3	A11	A3	A12	A3	A13	A3
A2	A10	A2	A11	A2	A12	A2
A1	A9	A1	A10	A1	A11	A1
A0	A8	A0	A9	A0	A10	A0

Note: The MXC1=1, MX0=1 setting is reserved, and must not be used.

For example, when MXC1 and MXC0 are set to 00 and an 8-bit shift is selected, the A23–A8 address bit values are output to pins A15–A0 the row address. The values for A21–A16 are undefined. The values of bits address A21–A0 are output to pins A21–A0 as the column address. Figure 8.16 depicts address multiplexing with an 8-bit shift.

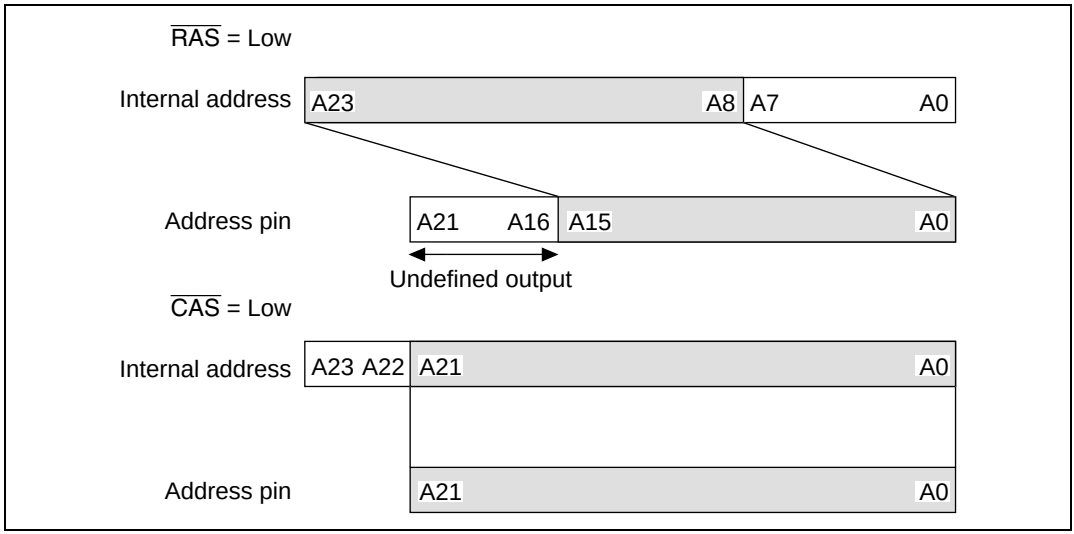


Figure 8.16 Address Multiplexing States (8-Bit Shift)

8.5.2 Basic Timing

There are two types of DRAM accesses: short pitch and long pitch. Short pitch or long pitch can be selected for the respective bus cycles using the RW1 and WW1 bits in WCR1 and the DRW1 and DWW1 bits in WCR2. When the corresponding bits are cleared to 0, DRAM access is short pitch and column address output occurs in 1 state. When these bits are 1, DRAM access is long pitch and column address output occurs in 2 states. Figure 8.17 shows short pitch timing; figure 8.18 shows long pitch timing.

The high-level duty of the $\overline{CAS}$ signal can also be selected between 50% and 35% of the T_c state when access is short pitch. By setting the CDTY bit to 1, the high level duty becomes 35% and the DRAM access time can be lengthened. Only set to 1 when the operating frequency is a minimum of 10 MHz.

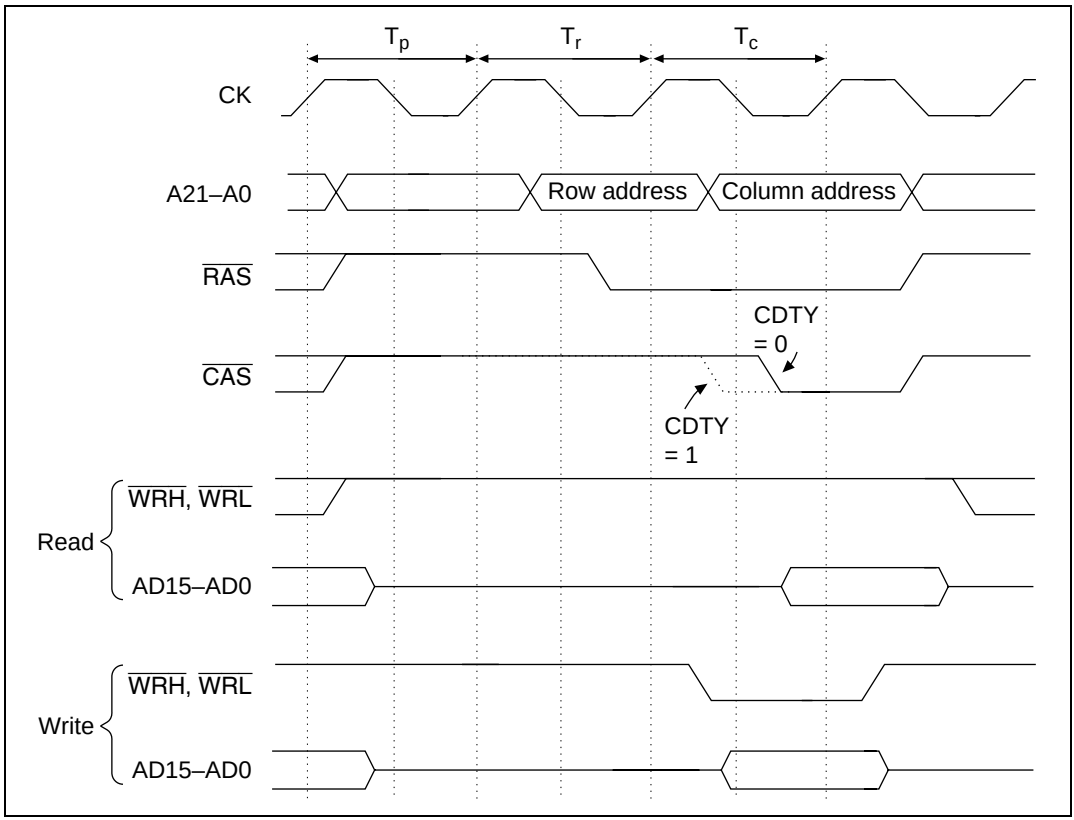


Figure 8.17 Short Pitch Access Timing

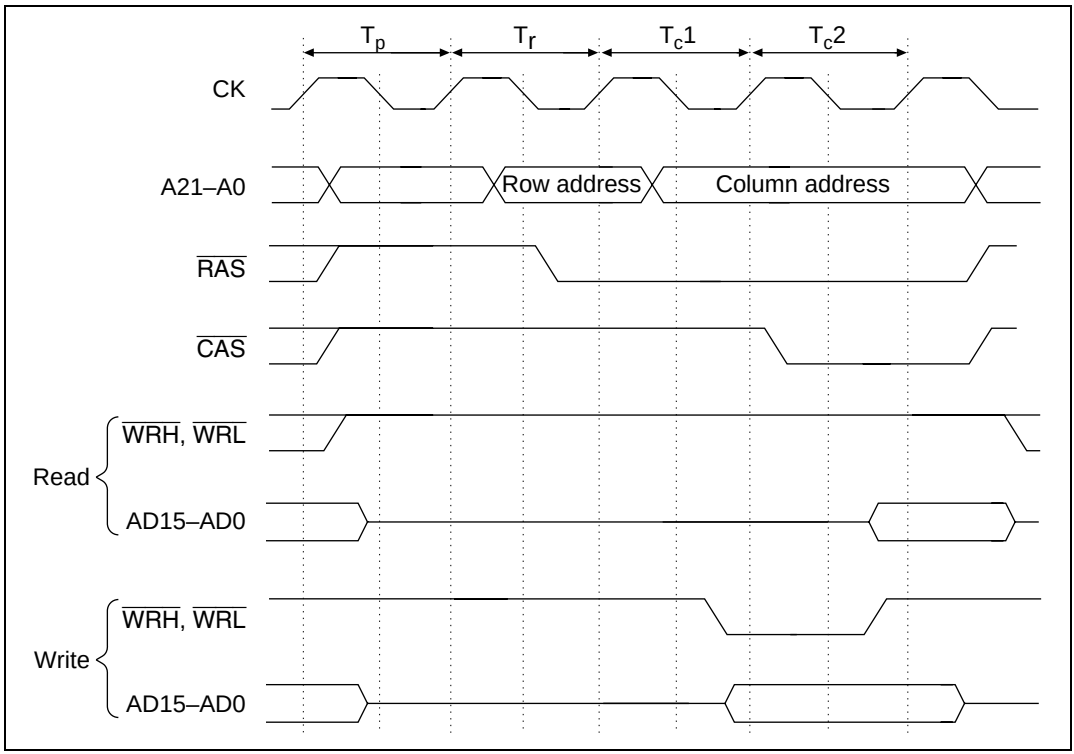


Figure 8.18 Long Pitch Access Timing

8.5.3 Wait State Control

Precharge State Control: When the microprocessor clock frequency is raised and the cycle period shortened, 1 cycle may not always be sufficient for the precharge time for the $\overline{RAS}$ signal when the DRAM is accessed. The BSC allows the precharge cycle to be set to 1 state or 2 states using the RAS signal precharge cycles bit (TPC) in DCR. When the TPC bit is 0, the precharge cycle is 1 state; when TPC is 1, the precharge cycle is 2 states. Figure 8.19 shows the timing when the precharge cycle is 2 states.

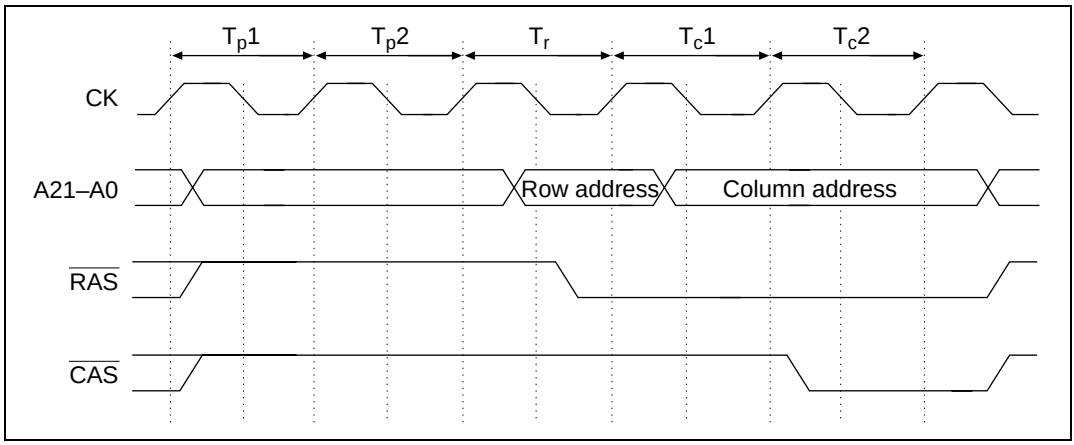


Figure 8.19 Precharge Timing (Long Pitch)

Control of Insertion of Wait States Using the $\overline{\text{WAIT}}$ Pin Input Signal: The number of wait states inserted into the DRAM access cycle can be controlled by setting WCR1 and WCR2. When the corresponding bits in WCR1 and WCR2 are cleared to 0, the column address output cycle ends in 1 state and no wait states are inserted. When the bit is 1, the $\overline{\text{WAIT}}$ pin input signal is sampled on the rise of the system clock (CK) directly preceding the second state of the column address output cycle and the wait state is inserted as long as the level is low. When a high level is detected, it shifts to the second state. Figure 8.20 shows the wait state timing in a long pitch bus cycle.

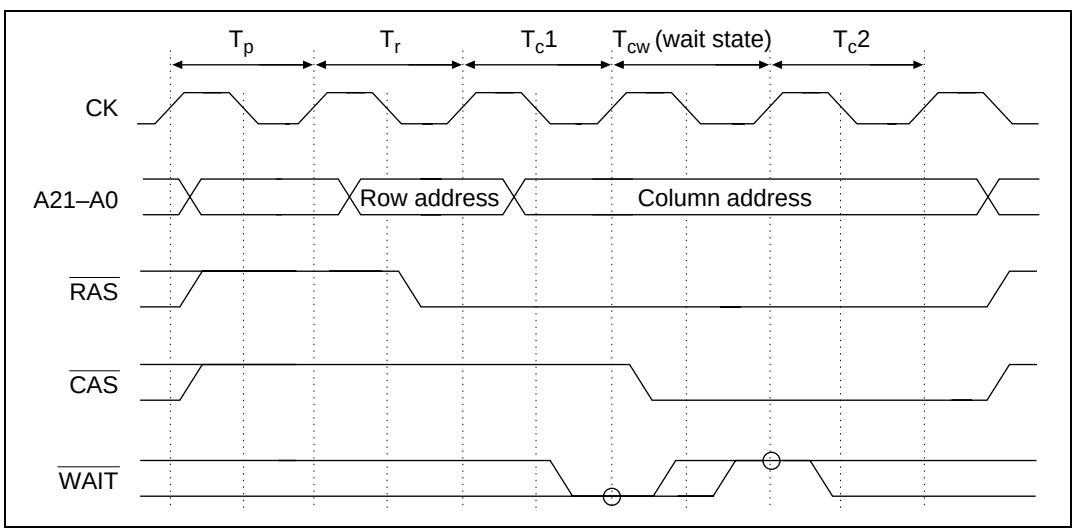


Figure 8.20 Wait State Timing during DRAM Access (Long Pitch)

Regardless of the state of the $\overline{\text{WAIT}}$ signal, when the RW1 bit, the number of wait states selected by CBR refresh wait state insertion bits 1 and 0 (RLW1, RLW0) in the refresh control register (RCR) are inserted into the CAS-before-RAS refresh cycle.

8.5.4 Byte Access Control

16-bit width and 18-bit width DRAMs require different types of byte control signals for access. By setting the dual CAS signals/dual WE signals select bit (CW2) in DCR, the BSC allows selection of either the dual CAS signal or dual WE signal system of control signals. When 16-bit space is being accessed and the CW2 bit is cleared to 0 for dual CAS signals, $\overline{\text{CASH}}$, $\overline{\text{CASL}}$, and $\overline{\text{WRL}}$ signals are output; when CW2 is set to 1 for dual WE signals, the $\overline{\text{CASL}}$, $\overline{\text{WRH}}$, and $\overline{\text{WRL}}$ signals are output. When accessing 8-bit space, $\overline{\text{WRL}}$ and $\overline{\text{CASL}}$ are output regardless of the CW2 setting.

Figure 8.21 shows the control timing of the upper byte write cycle (short pitch) in 16-bit space.

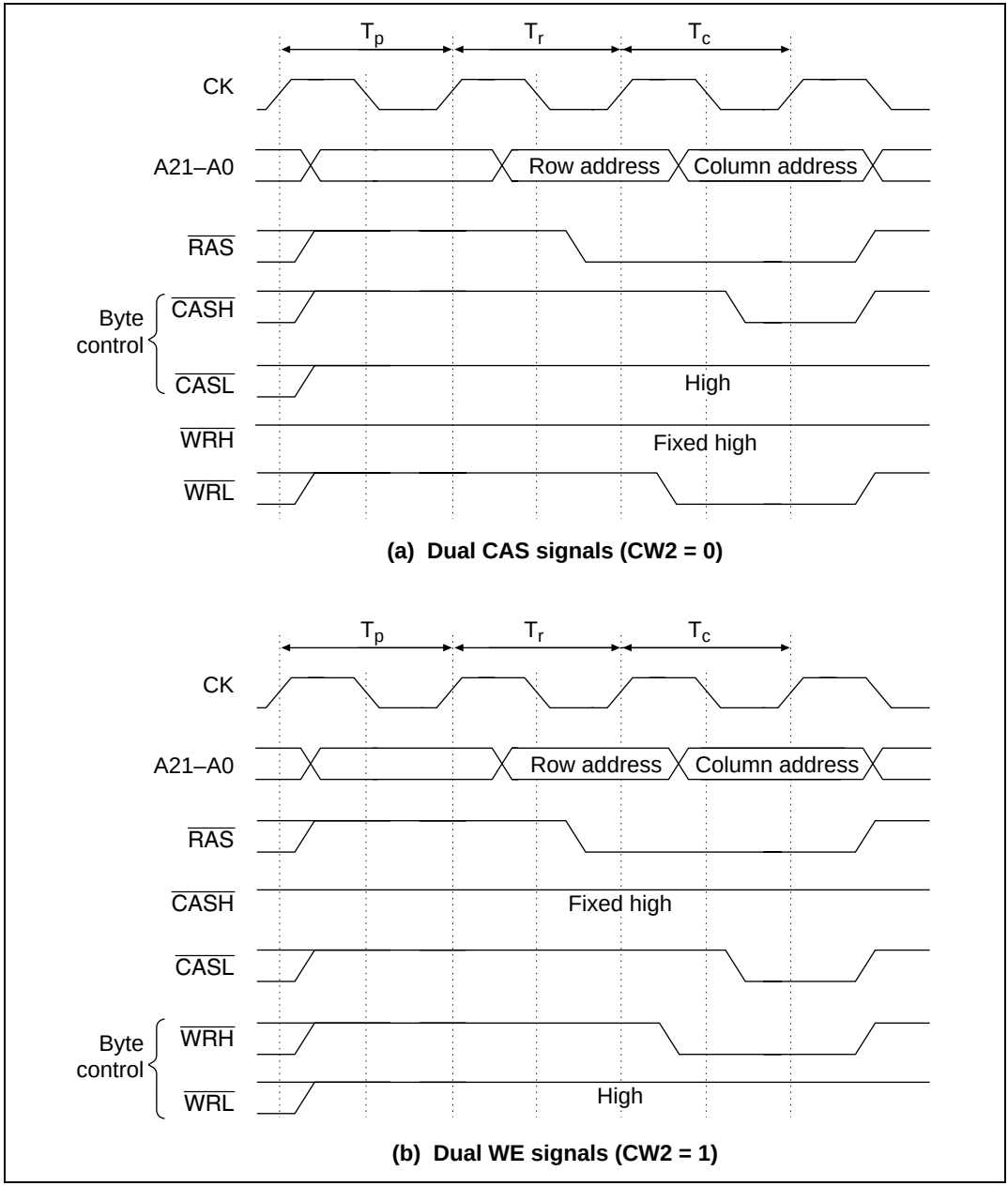


Figure 8.21 Byte Access Control Timing for DRAM Access (Upper Byte Write Cycle, Short Pitch)

8.5.5 DRAM Burst Mode

In addition to the normal mode of DRAM access, in which row addresses are output at every access and data then accessed (full access), the DRAM also has a high-speed page mode for use when continuously accessing the same row. The high speed page mode enables fast access of data simply by changing the column address after the row address is output (burst mode). Select between full access and burst operation by setting the burst enable bit (BE) in DCR. When the BE bit is set to 1, burst operation is performed when the row address matches the previous DRAM access row address. Figure 8.22 shows a comparison between full access and burst operation.

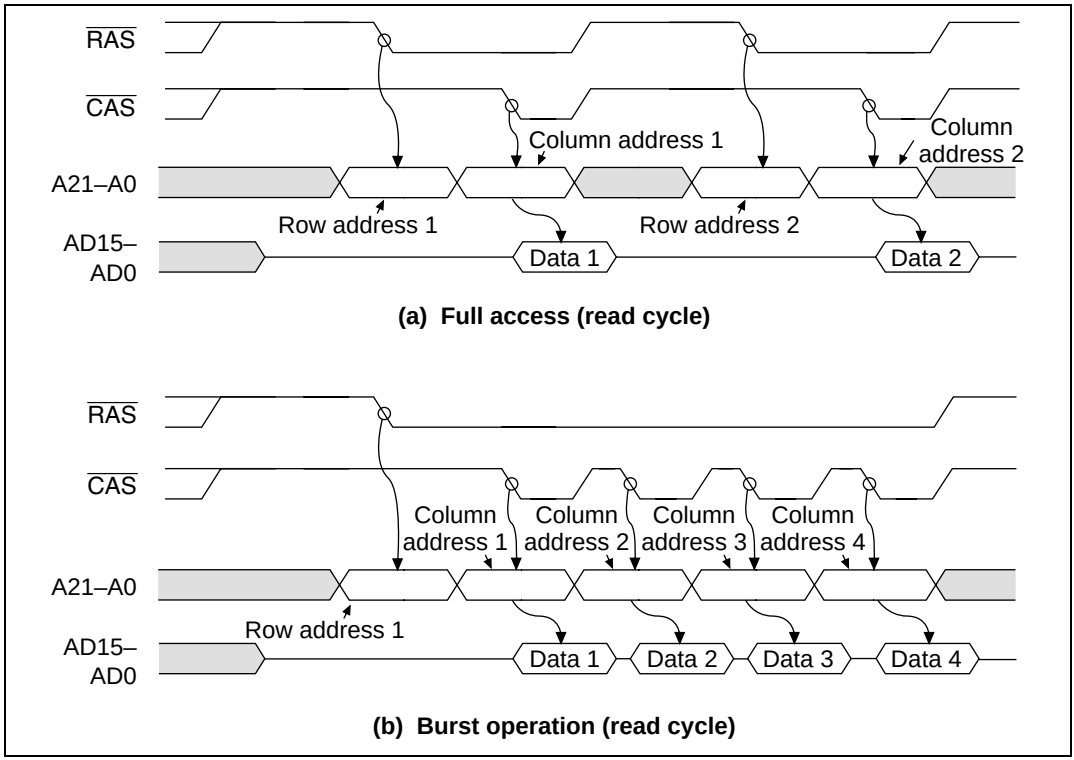


Figure 8.22 Full Access and Burst Operation

Short pitch high-speed page mode or long pitch high-speed page mode burst transfers can be selected independently for DRAM read/write cycles even when burst operation is selected by using the bits corresponding to area 1 in WCR1 and WCR2 (RW1, WW1, DRW1, DWW1). RAS down mode or RAS up mode can be selected by setting the RAS down bit (RASD) in DCR when there is an access outside the DRAM space during burst operation.

Short-Pitch, High-Speed Page Mode and Long-Pitch High-Speed Page Mode: When burst operation is selected by setting the BE bit to 1 in DCR, short pitch high-speed page mode or long pitch high-speed page mode can be selected by setting the RW1, WW1, DRW1, and DWW1 bits in WCR1 and WCR2.

- Short-pitch, high-speed page mode: When the RW1, WW1, DRW1, and DWW1 bits in WCR1 and WCR2 are cleared to 0, and the corresponding DRAM access cycle is continuing, the $\overline{\text{CAS}}$ signal and column address output cycles continue as long as the row addresses continue to match. The column address output cycle is performed in 1 state and the $\overline{\text{WAIT}}$ signal is not sampled. Figure 8.23 shows the read cycle timing for short-pitch, high-speed page mode.

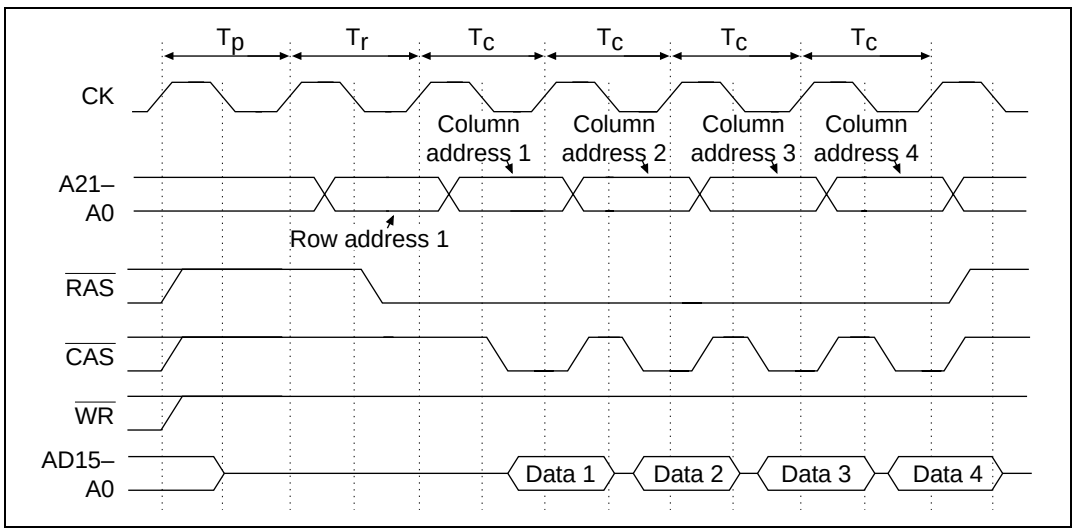
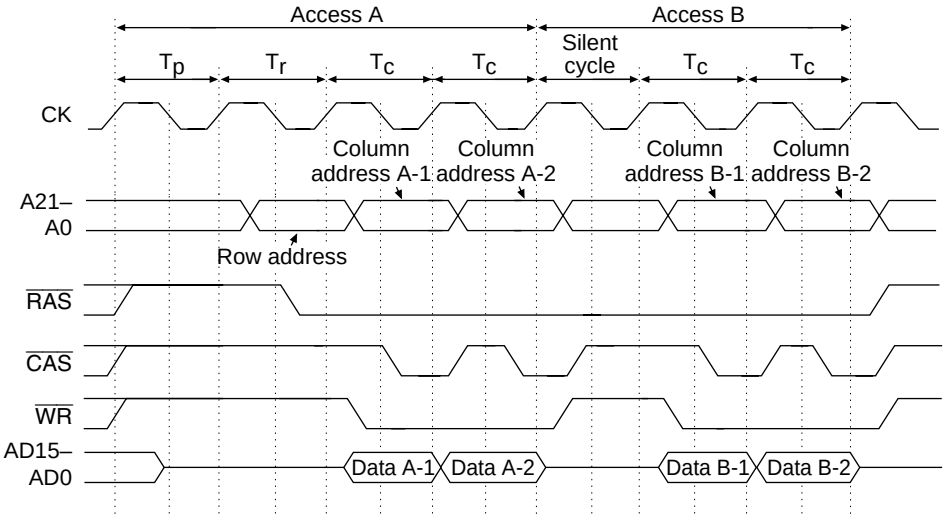


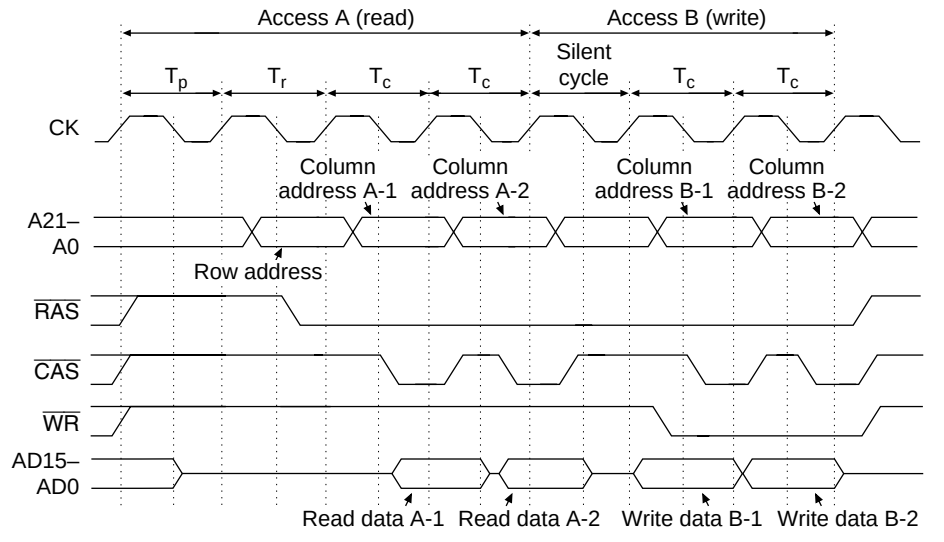
Figure 8.23 Short-Pitch, High-Speed Page Mode (Read Cycle)

When the write cycle continues for the same row address in short-pitch, high-speed page mode, an open cycle (silent cycle) is produced for 1 cycle only. This timing is shown in figure 8.24. Likewise, when a write cycle continues after the read cycle for the same row address, a silent cycle is produced for 1 cycle. This timing is shown in figure 8.25. Note also that when DRAM is written to in short-pitch, high-speed page mode when using DMAC single address mode, a silent cycle is inserted in each transfer. The details of timing are discussed in sections 20.1.3 (3) and 20.2.3 (3), Bus Timing.



Note: Accesses A and B are examples of 32-bit data accesses in their respective 16-bit bus width spaces.

Figure 8.24 Short-Pitch, High-Speed Page Mode (Write Cycle)



Note: Accesses A and B are examples of 32-bit data accesses in their respective 16-bit bus width spaces.

Figure 8.25 Short-Pitch, High-Speed Page Mode (Read and Write Cycles Continuing with Same Row Address)

The high-level duty of the $\overline{CAS}$ signal can be selected in short-pitch, high-speed page mode using the CAS duty bit (CDTY) in DCR. When the CDTY bit is cleared to 0, the high-level duty is 50% of the T_C state; when CDTY is set to 1, it is 35% of the T_C state.

- Long-pitch, high-speed page mode: When the RW1, WW1, DRW1, and DWW1 bits in WCR1 and WCR2 are set to 1, and the corresponding DRAM access cycle is continuing, the $\overline{CAS}$ signal and column address output cycles (2 states) continue as long as the row addresses continue to match. When the $\overline{WAIT}$ signal is detected at the low level, the second cycle of the column address output cycle is repeated as the wait state. Figure 8.26 shows the timing for long-pitch, high-speed page mode. See sections 20.1.3 (3) and 20.2.3 (3), Bus Timing, for more information about the timing.

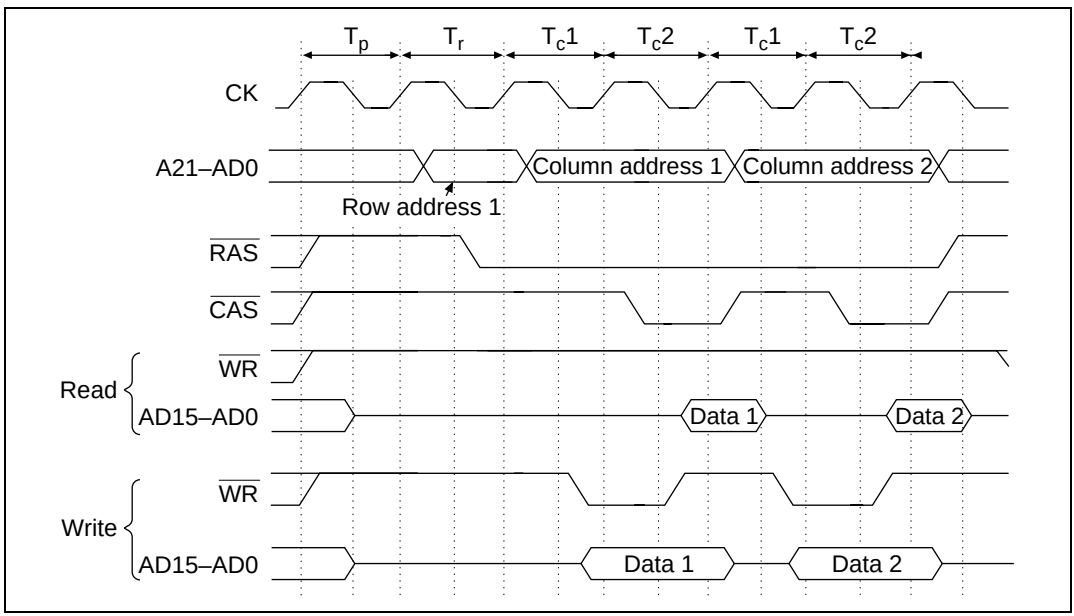


Figure 8.26 Long-Pitch, High-Speed Page Mode (Read/Write Cycle)

RAS Down Mode and RAS Up Mode: Sometimes access to another area can occur between accesses to the DRAM even though burst operation has been selected. Keeping the $\overline{RAS}$ signal low while this other access is occurring allows burst operation to continue the next time the same row of the DRAM is accessed. The RASD bit in DCR selects RAS down mode when set to 1 and RAS up mode when cleared to 0. In both RAS down mode and RAS up mode, burst operation is continued while the same row address continues to be accessed, even if the bus master is changed.

- RAS down mode: When the RASD bit in DCR is set to 1, the DRAM access pauses and the $\overline{RAS}$ signal is held low throughout the access of the other space while waiting for the next

access to the DRAM area. When the row address for the next DRAM access is the same as the previous DRAM access, burst operation continues. Figure 8.27 shows the timing of RAS down mode when external memory space is accessed during burst operation.

The $\overline{RAS}$ signal can be held low in the DRAM for a limited time; the $\overline{RAS}$ signal must be returned to high within the specified limits even when RAS down mode is selected since the critical low level period is set. In this chip, even when RAS down mode is selected, the $\overline{RAS}$ signal automatically reverts to high when the DRAM is refreshed, so the BSC's refresh control function can be employed to set a CAS-before-RAS refresh that will keep operation within specifications. See section 8.5.6, Refresh Control, for details.

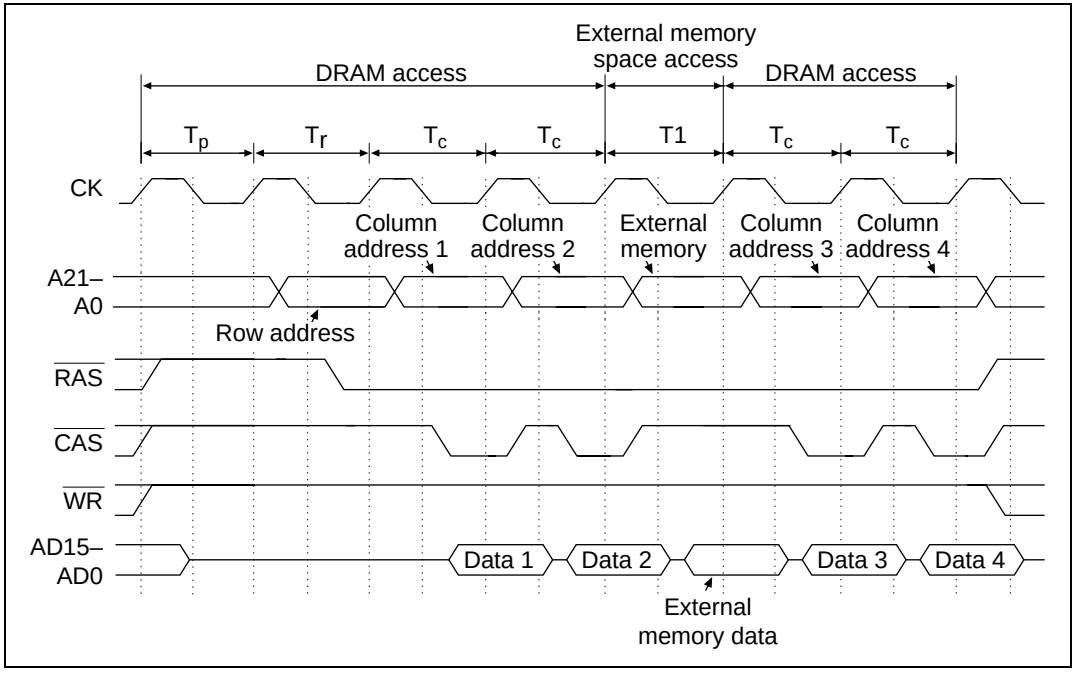


Figure 8.27 RAS Down Mode

- RAS up mode: When the RASD bit is cleared to 0, the $\overline{RAS}$ signal reverts to high whenever a DRAM access pauses for access to another space. Burst operation continues only while DRAM access is continuous. Figure 8.28 shows the timing when an external memory space access occurs during burst operation in RAS up mode.

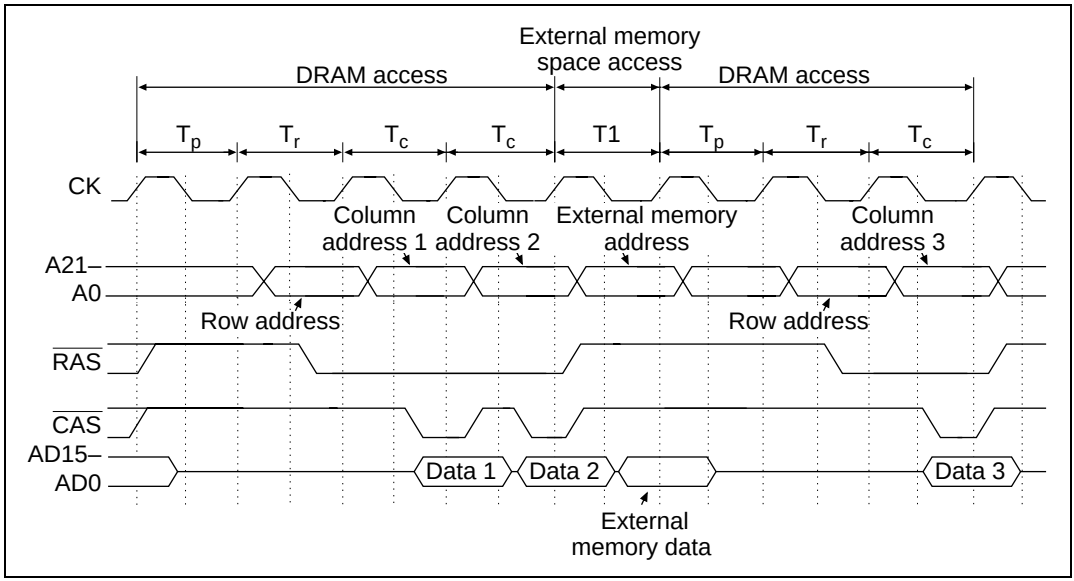


Figure 8.28 RAS Up Mode

8.5.6 Refresh Control

The BSC has a function for controlling DRAM refreshing. By setting the refresh mode bit (RMODE) in the refresh control register (RCR), either CAS-before-RAS refresh (CBR) or self-refresh can be selected. When no refresh is performed, the refresh timer counter (RTCNT) can be used as an 8-bit interval timer.

CAS-Before-RAS Refresh (CBR): A refresh is performed at an interval determined by the input clock selected with clock select bits 2–0 (CKS2–CKS0) in the refresh timer control/status register (RTCSR) and the value set in the refresh time constant register (RTCOR). Set the values of RTCOR and CKS2–CKS0 so they satisfy the refresh interval specifications of the DRAM being used.

To perform a CBR refresh, clear the RMODE bit in RCR to 0 and then set the refresh control bit (RFSHE) bit to 1. Also write the required values to RTCNT and RTCOR. When the clock is subsequently selected with the CKS2–CKS0 bits in RTCSR, RTCNT will begin to increment from its current value. The RTCNT value is constantly compared with the RTCOR value and a CBR

refresh is performed when they match. RTCNT is simultaneously cleared to H'00 and incrementing begins again.

When the clock is selected with the CKS2–CKS0 bits, RTCNT immediately begins to increment from its current value. This means that when the RTCOR cycle is set after the CKS2–CKS0 bits are set, the RTCNT count may already be higher than the RTCOR cycle. When this occurs, the RTCNT will overflow once (from H'FF to H'00) and incrementing will start again. Since the CBR refresh will not be performed until the RTCNT again matches the RTCOR value, the initial refresh interval will be rather long. It is thus advisable to set the RTCOR cycle prior to setting the CKS2–CKS0 bits and start it incrementing. When CBR refresh control is being performed after use as an 8-bit interval timer, the RTCNT count value may be in excess of the refresh cycle. For this reason, clear RTCNT by writing H'00 before starting refresh control to assure a correct refresh interval.

When the RW1 bit in WCR1 is set to 1 and the read cycle is set to long pitch, the number of wait states selected by the RLW1 and RLW0 bits in RCR will be inserted into the CBR refresh cycle, regardless of the status of the $\overline{\text{WAIT}}$ signal. Figure 8.29 shows RTCNT operation and figure 8.30 shows the timing of the CBR refresh. For details on timing, see sections 20.1.3 (3) and 20.2.3 (3), Bus Timing.

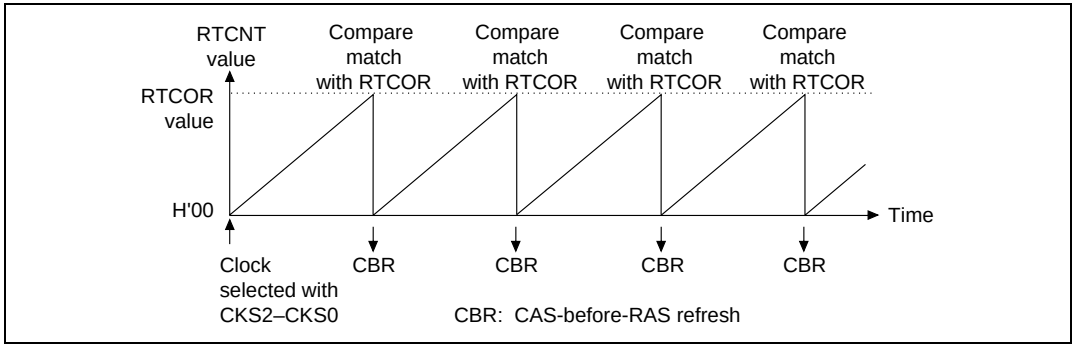


Figure 8.29 Refresh Timer Counter (RTCNT) Operation

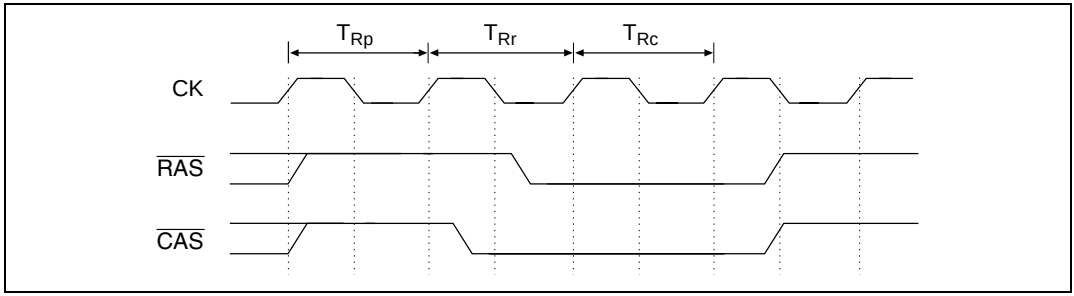


Figure 8.30 Output Timing for CAS-Before-RAS Refresh Signal

Self-Refresh Mode: Some DRAMs have a self-refresh mode (battery back-up mode). This is a type of a standby mode in which the refresh timing and refresh addresses are generated inside the DRAM chip. When the RFSHE and RMODE bits in RCR are both set to 1, the DRAM will enter self-refresh mode when the $\overline{CAS}$ and $\overline{RAS}$ signals are output as shown in figure 8.31. See sections 20.1.3 (3) and 20.2.3 (3), Bus Timing, for details. DRAM self-refresh mode is cleared when the RMODE bit in RCR is cleared to 0 (figure 8.31). The RFSHE bit should be left at 1 when this is done. Some DRAM vendors recommend that after exiting self-refresh mode, all row addresses should be refreshed again. This can be done using the BSC's CBR refresh function to set all row addresses for refresh in software.

To access a DRAM area while in self-refresh mode, first clear the RMODE bit to 0 and exit self-refresh mode.

The chip can be kept in the self-refresh state and shifted to standby mode by setting it to self-refresh mode, setting the standby bit (SBY) in the standby control register (SBYCR) to 1, and then executing a SLEEP instruction.

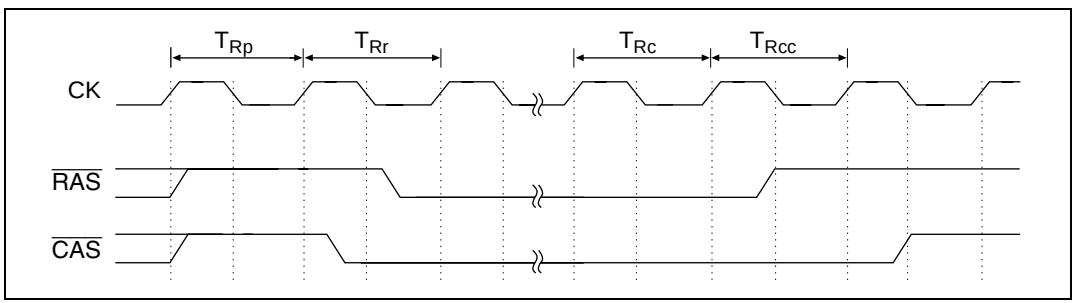


Figure 8.31 Output Timing for Self-Refresh Signal

Refresh Requests and Bus Cycle Requests: When a CAS-before-RAS refresh or self-refresh is requested during bus cycle execution, parallel execution is sometimes possible. Table 8.11 summarizes the operation when refresh and bus cycles are in contention.

Table 8.11 Refresh and Bus Cycle Contention

	Type of Bus Cycle				
	External Space Access				
	External Memory Space, Multiplexed I/O Space		DRAM Space		On-Chip ROM, On-Chip RAM, On-Chip Supporting Module Access
Type of Refresh	Read Cycle	Write Cycle	Read Cycle	Write Cycle	
CAS-before-RAS refresh	Yes	No	No	No	Yes
Self-refresh	Yes	Yes	No	No	Yes

Yes: Can be executed in parallel

No: Cannot be executed in parallel

When parallel execution is possible, the $\overline{RAS}$ and $\overline{CAS}$ signals are output simultaneously during bus cycle execution and the refresh is executed. When parallel execution is not possible, the refresh occurs after the bus cycle has ended.

Using RTCNT as an 8-Bit Interval Timer: When not performing refresh control, RTCNT can be used as an 8-bit interval timer. Simply set the RFSHE bit in RCR to 0. To produce a compare match interrupt (CMI), set the compare match interrupt enable bit (CMIE) to 1 and set the interrupt generation timing in RTCOR. When the input clock is selected with the CKS2–CKS0 bits in RTCSR, RTCNT starts incrementing as an 8-bit interval timer. Its value is constantly compared with RTCOR, and when a match occurs, the CMF bit in RTCSR is set to 1 and a CMI interrupt is produced. RTCNT is cleared to H'00.

When the clock is selected with the CKS2–CKS0 bits, RTCNT starts incrementing immediately. This means that when the RTCOR cycle is set after the CKS2–CKS0 bits are set, the RTCNT count may already be higher than the RTCOR cycle. When this occurs, the RTCNT will overflow once (H'FF goes to H'00) and the count up will start again. No interrupt will be generated until the RTCNT again matches the RTCOR value. It is thus advisable to set the RTCOR cycle prior to setting the CKS2–CKS0 bits. After its use as an 8-bit interval timer, the RTCNT count value may be in excess of the set cycle. For this reason, write H'00 to the RTCNT to clear it before starting to use it again with new settings. RTCNT can then be restarted and an interrupt obtained after the correct interval.

8.6 Address/Data Multiplexed I/O Space Access

The BSC is equipped with a function that multiplexes address and data input/output on pins AD15–AD0 in area 6. This allows the SH microprocessor to be directly connected to peripheral chips that require address/data multiplexing.

8.6.1 Basic Timing

When the multiplexed I/O enable bit (IOE) in BCR is set to 1, the area 6 space with address bit A27 as 0 (H'6000000–H'6FFFFFF) becomes an address/data multiplexed I/O space that, when accessed, multiplexes addresses and data. When the A14 address bit is 0, the bus width is 8 bits and address output and data input/output are performed on the AD7–AD0 pins. When the A14 address bit is 1, the bus width is 16 bits and address output and data input/output are performed on the AD15–AD0 pins. In the address/data multiplexed I/O space, access is controlled with the $\overline{AH}$, $\overline{RD}$, and $\overline{WR}$ signals. Accesses in the address/data multiplexed I/O space are performed in 4 states, regardless of the WCR settings. Figure 8.32 shows the timing when the address/data multiplexed I/O space is accessed.

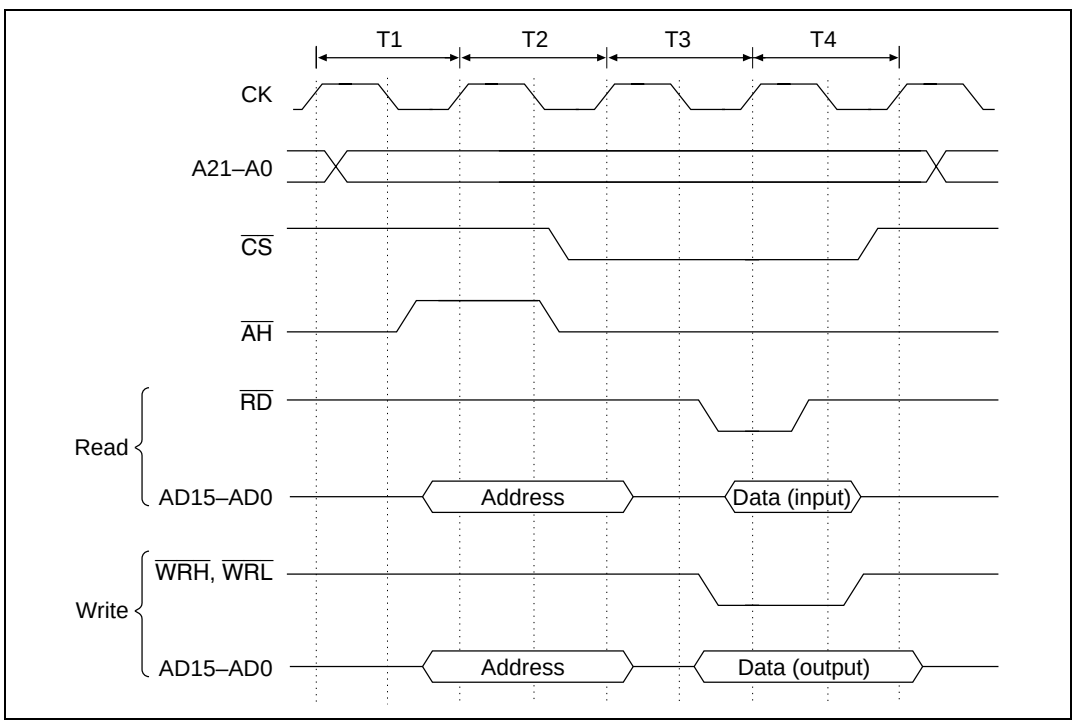


Figure 8.32 Access Timing For Address/Data Multiplexed I/O Space

A high-level duty of 35% or 50% can be selected for the $\overline{RD}$ signal using the RD duty bit (RDDTY) in BCR. When RDDTY is 1, the high-level duty is 35% of the T3 or T_W state, lengthening the access time for external devices.

8.6.2 Wait State Control

When the address/data multiplexed I/O space is accessed, the $\overline{WAIT}$ pin input signal is sampled and a wait state inserted whenever a low level is detected, regardless of the WCR setting. Figure 8.33 shows an example in which a $\overline{WAIT}$ signal causes one wait state to be inserted.

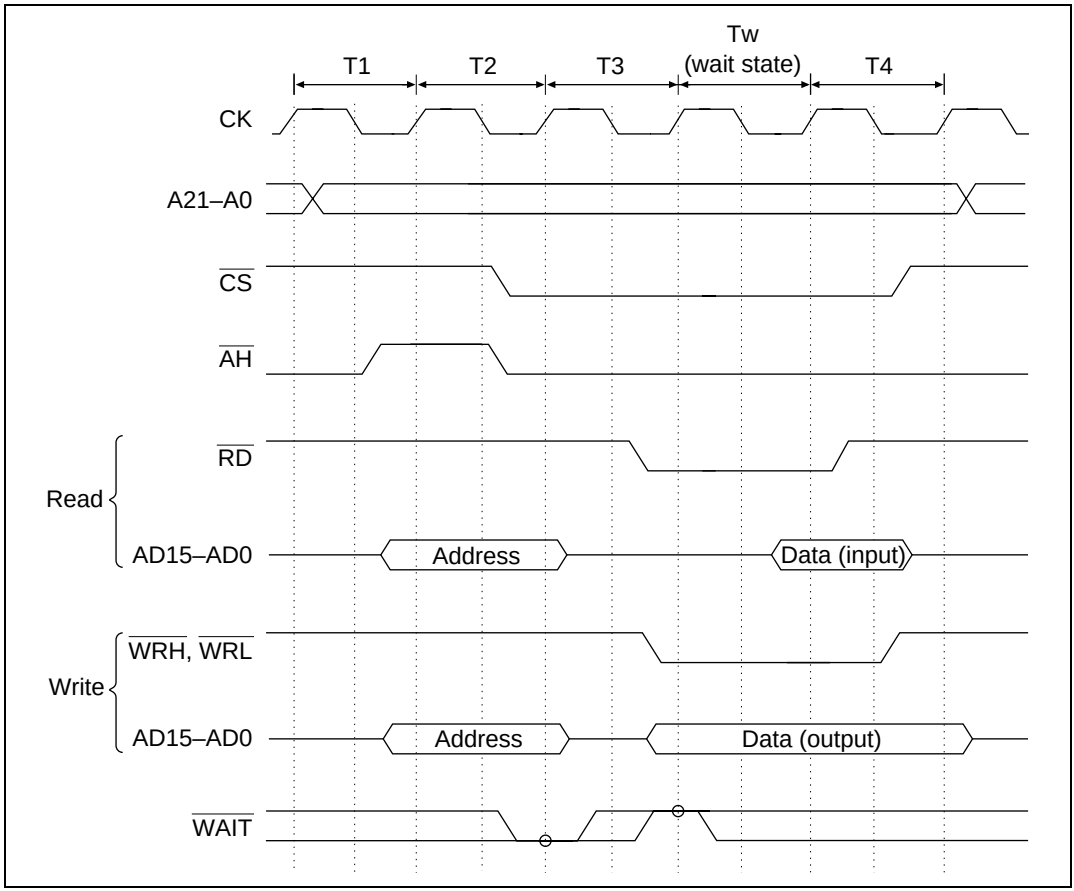


Figure 8.33 Wait State Timing For Address/Data Multiplexed I/O Space Access

8.6.3 Byte Access Control

The byte access control signals when the address/data multiplexed I/O space is being accessed are of two types ($\overline{WRH}$, $\overline{WRL}$, A0, or $\overline{WR}$, $\overline{HBS}$, $\overline{LBS}$), just as for byte access control of external memory space access. These types can be selected using the BAS bit in BCR. See section 8.4.3, Byte Access Control, for details.

8.7 Parity Check and Generation

The BSC can check and generate parity for data input and output to or from the DRAM space of area 1 and the external memory space of area 2.

To check and generate parity, select the space (DRAM space only, or DRAM space and area 2) for which parity is to be checked and generated using the parity check enable bits (PCHK1 and PCHK0) in the parity control register, and select odd or even parity with the parity polarity bit (PEO).

When data is input from the space selected with the PCHK1 and PCHK0 bits, the BSC checks the PEO bit to see if the polarity of the DPH pin input (upper byte parity data) is accurate for the AD15–AD8 pin input (upper byte data) or if the DPL pin input (lower byte parity data) is accurate for the AD7–AD0 pin input (lower byte data). If the check indicates that either the upper or lower byte parity is incorrect, a parity error interrupt is produced (PEI).

When outputting data to the space selected with the PCHK1 and PCHK0 bits, the BSC outputs parity data output of the polarity set in the PEO bit from the DPH pin for the AD15–AD8 pin output (upper byte data) or from the DPL pin for the AD7–AD0 pin input (lower byte data) using the same timing as the data output.

The BSC is also able to force parity output for use in testing the system's parity error check function. When the parity force output bit (PFRC) in PCR is set to 1, a high level is forcibly output from the DPH and DPL pins when data is output to the space selected with the PCHK1 and PCHK0 bits.

8.8 Warp Mode

In warp mode, an external write cycle or DMA single address mode transfer cycle and an internal access cycle (read/write to on-chip memory or on-chip supporting modules) operate independently and in parallel. Warp mode is entered by setting the warp mode bit (WARP) in BCR to 1. This allows the chip to be operated at high speed.

When, in warp mode, an external write cycle or DMA single address mode transfer cycle continues for at least 2 states and there is an internal access, only the external write cycle will be performed in the initial state. The external write cycle and internal access cycle will be performed in parallel from the next state on, without waiting for the end of the external write cycle. Figure 8.34 shows the timing when an access to an on-chip supporting module and an external write cycle are performed in parallel.

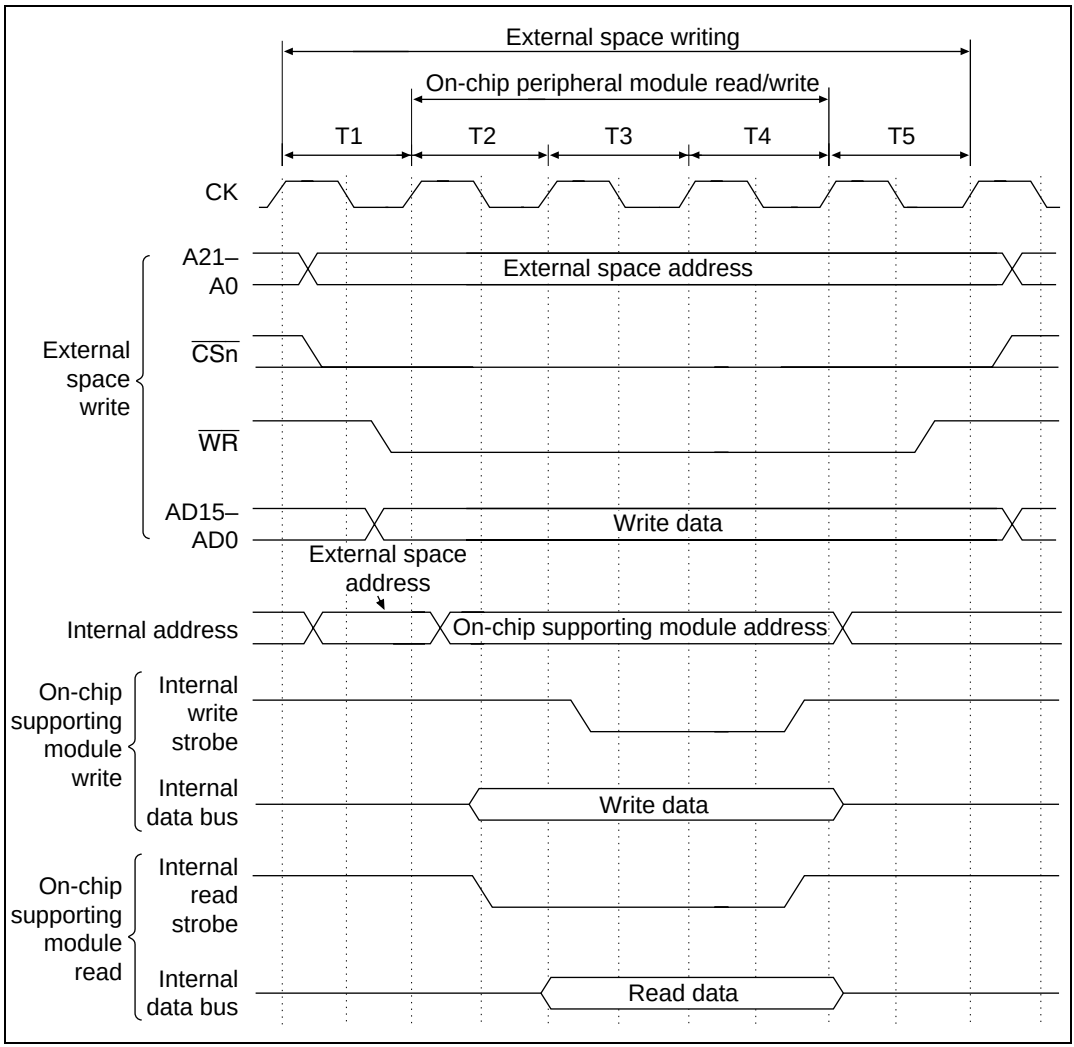


Figure 8.34 Warp Mode Timing (Access to On-Chip Supporting Module and External Write Cycle)

8.9 Wait State Control

The WCR1–WCR3 registers of the BSC can be set to control sampling of the $\overline{\text{WAIT}}$ signal when accessing various areas, and the number of bus cycle states. Table 8.12 shows the number of bus cycle states when accessing various areas.

Table 8.12 Bus Cycle States when Accessing Address Spaces

	CPU Read Cycle, DMAC Dual Mode Read Cycle, DMAC Single Mode Memory Read/Write Cycle	
Address Space	**Corresponding Bits in WCR1 and WCR2 = 0**	**Corresponding Bits in WCR1 and WCR2 = 1**
External memory (areas 1, 3–5, 7)	1 state fixed; $\overline{\text{WAIT}}$ signal ignored	2 states + wait states from $\overline{\text{WAIT}}$ signal
External memory (Areas 0, 2, 6; long wait avail-able)	1 state + long wait state*, $\overline{\text{WAIT}}$ signal ignored	1 state + long wait state* + wait states from $\overline{\text{WAIT}}$ signal
DRAM space (area 1)	Column address cycle: 1 state, $\overline{\text{WAIT}}$ signal ignored (short pitch)	Column address cycle: 2 states + wait states from $\overline{\text{WAIT}}$ signal (long pitch)
Multiplexed I/O space (area 6)	4 states + wait states from $\overline{\text{WAIT}}$ signal	
On-chip supporting module space (area 5)	3 states fixed, $\overline{\text{WAIT}}$ signal ignored	
On-chip ROM (area 0)	1 state fixed, $\overline{\text{WAIT}}$ signal ignored	
On-chip RAM (area 7)	1 state fixed, $\overline{\text{WAIT}}$ signal ignored	

	CPU Write Cycle, DMAC Dual Mode Memory Write Cycle (WW1 of WCR1)	
Address Space	**WW1 of WCR1=0**	**WW1 of WCR1=1**
External memory (area 1)	Setting prohibited	2 states + wait state from $\overline{\text{WAIT}}$ signal
External memory (areas 3–5, 7)	2 states + wait states from $\overline{\text{WAIT}}$ signal	
External memory (Areas 0, 2, 6; long wait available)	1 state + long wait state* + wait states from $\overline{\text{WAIT}}$ signal	
DRAM space (area 1)	Column address cycle: 1 state, $\overline{\text{WAIT}}$ signal ignored (short pitch)	Column address cycle: 2 states + wait states from $\overline{\text{WAIT}}$ signal (long pitch)
Multiplexed I/O space (area 6)	4 states + wait states from $\overline{\text{WAIT}}$ signal	
On-chip peripheral module space (area 5)	3 states fixed, $\overline{\text{WAIT}}$ signal ignored	
On-chip ROM (area 0)	1 state fixed, $\overline{\text{WAIT}}$ signal ignored	
On-chip RAM (area 7)	1 state fixed, $\overline{\text{WAIT}}$ signal ignored	

Note: * The number of long wait states (1 to 4) is set in WCR3.

For details on bus cycles when external spaces are accessed, see section 8.4, Accessing External Memory Space, section 8.5, DRAM Interface Operation, and section 8.6, Address/Data Multiplexed I/O Space Access.

Accesses to on-chip spaces are as follows: On-chip supporting module spaces (area 5 when address bit A27 is 1) are always 3-state access spaces, regardless of WCR, with no $\overline{\text{WAIT}}$ signal sampling. Accesses to on-chip ROM (area 0 when MD2–MD0 are 010) and on-chip RAM (area 7 when address bit A27 is 0) are always performed in 1 state, regardless of WCR, with no $\overline{\text{WAIT}}$ signal sampling.

If the bus timing specifications (t_{WTS} and t_{WTH}) are not observed when the $\overline{\text{WAIT}}$ signal is input in external space access, this will simply mean that $\overline{\text{WAIT}}$ signal assertion and negation will not be detected, but will not result in misoperation. Note, however, that the inability to detect $\overline{\text{WAIT}}$ signal assertion may result in a problem with memory access due to insertion of an insufficient number of waits.

8.10 Bus Arbitration

The SuperH microcomputer can release the bus to external devices when they request the bus. It has two internal bus masters, the CPU and the DMAC. Priorities for releasing the bus for these two are as follows.

Bus request from external device > refresh > DMAC > CPU

Thus, an external device has priority when it generates a bus request, even when the DMAC is carrying out a burst transfer.

Note that when a refresh request is generated while the bus is released to an external device, $\overline{\text{BACK}}$ goes high and the bus can be acquired to perform refreshing upon receipt of a $\overline{\text{BREQ}}$ = high response from the external device. Input all bus requests from external devices to the $\overline{\text{BREQ}}$ pin. The signal indicating that the bus has been released is output from the $\overline{\text{BACK}}$ pin. Figure 8.35 illustrates the bus release procedure.

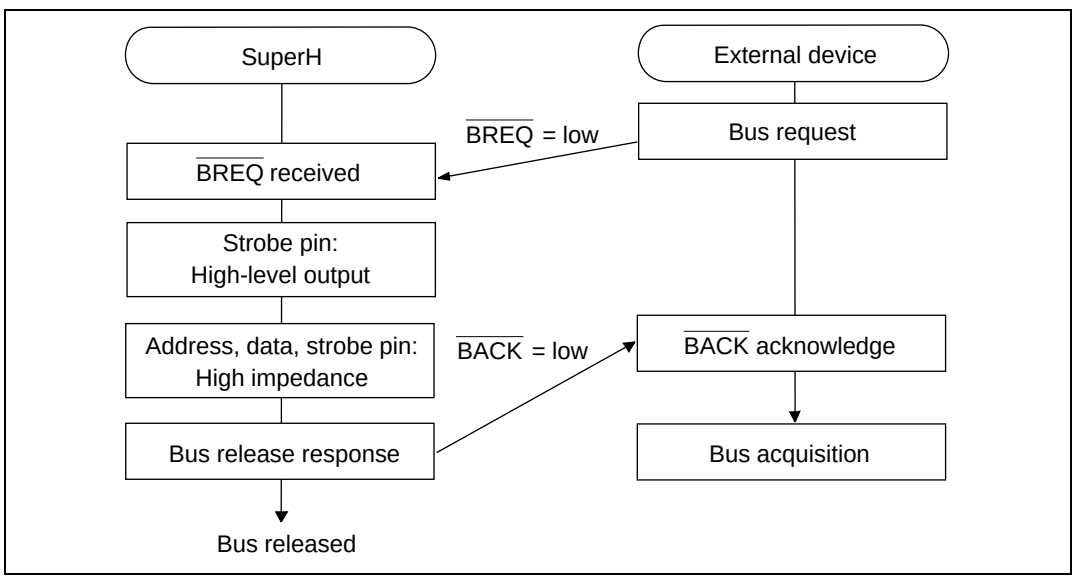


Figure 8.35 Bus Release Procedure

8.10.1 Operation of Bus Arbitration

If there is conflict between bus arbitration and refreshing, the operation is as follows.

1. If DRAM refreshing is requested in this chip when the bus is released and $\overline{\text{BACK}}$ is low, $\overline{\text{BACK}}$ goes high and the occurrence of the refresh request can be indicated externally. At this time, the external device may generate a bus cycle when $\overline{\text{BREQ}}$ is low even if $\overline{\text{BACK}}$ is high. Therefore, the bus remains released to the external device. Then, when $\overline{\text{BREQ}}$ goes high, this chip acquires bus ownership, and executes a refresh and the bus cycle of the CPU or DMAC. After the external device acquires bus ownership and $\overline{\text{BACK}}$ is low, a refresh is requested when $\overline{\text{BACK}}$ goes high even if $\overline{\text{BREQ}}$ input is low. Therefore, drive $\overline{\text{BREQ}}$ high immediately to release the bus for this chip to hold DRAM data (see figure 8.36).
2. When $\overline{\text{BREQ}}$ changes from high to low and an internal refresh is requested at the timing of bus release by this chip, $\overline{\text{BACK}}$ may remain high. The bus is released to the external device since $\overline{\text{BREQ}}$ input is low. This operation is based on the above specification (1). To hold DRAM data, drive $\overline{\text{BREQ}}$ high and release the bus to this chip immediately when the external device detects that $\overline{\text{BACK}}$ does not change to low during a fixed time (see figure 8.37). When a refresh request is generated and $\overline{\text{BACK}}$ returns to high, as shown in figure 8.37, a momentary narrow pulse-shaped spike may be output where $\overline{\text{BACK}}$ was originally supposed to go low.

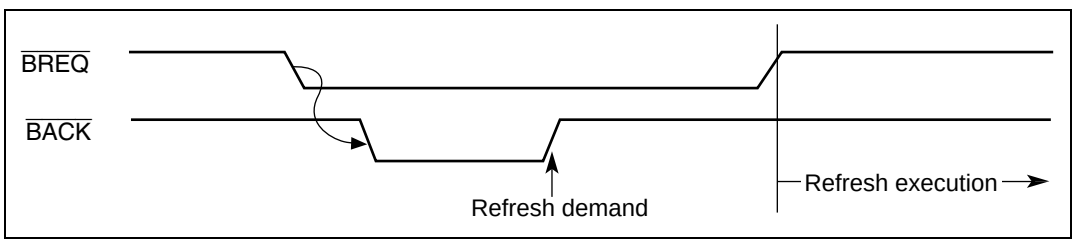


Figure 8.36 $\overline{\text{BACK}}$ Operation in Response to Refresh Demand (1)

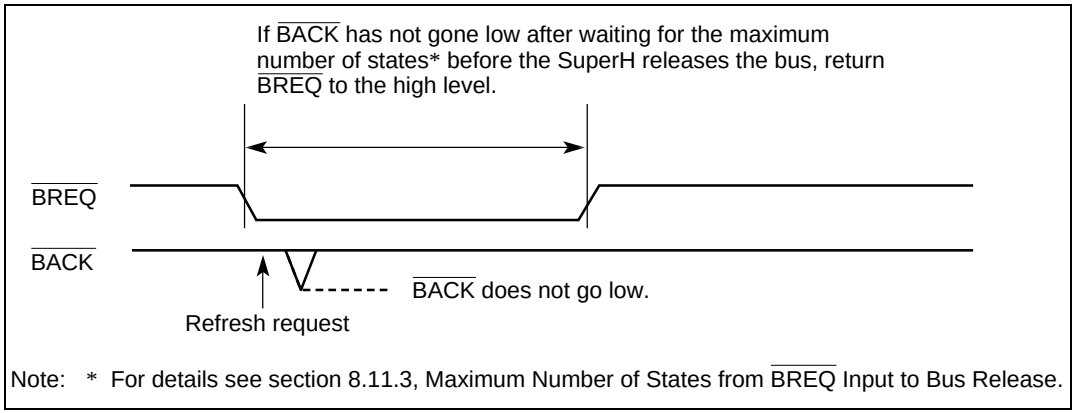


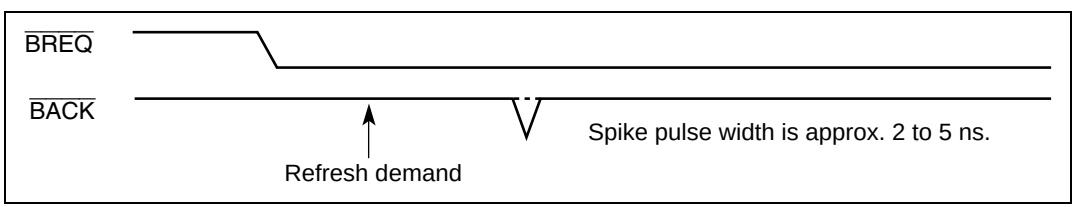
Figure 8.37 BACK Operation in Response to Refresh Request (2)

3. If a refresh request is generated during DMA transfer in burst mode, the DMA transfer is halted and a refresh is executed.

8.10.2 BACK Operation

1. BACK operation

   When an internal refresh is requested during an attempt to assert the BACK signal and BACK is not asserted but remains high, a momentary narrow pulse-shaped spike may be output, as shown below.



2. Preventing spikes in the BACK signal

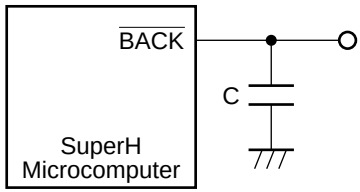
   The following measures should be taken to prevent spikes in the BACK signal:

   a. When BREQ is input to release the bus, make sure that a conflict with a refresh operation does not occur. Stop the refresh operation or operate the refresh timer counter (RTCNT) or the refresh time constant register (RTCOR) of the bus controller (BSC) to shift the refresh timing.

   b. A spike in the BACK signal has a narrow pulse width of approximately 2 to 5 ns, which can be eliminated by using a capacitor as shown in the figure below.

For example, adding a capacitance of 220 pF can raise the minimum voltage of the spike above 2.0 V.

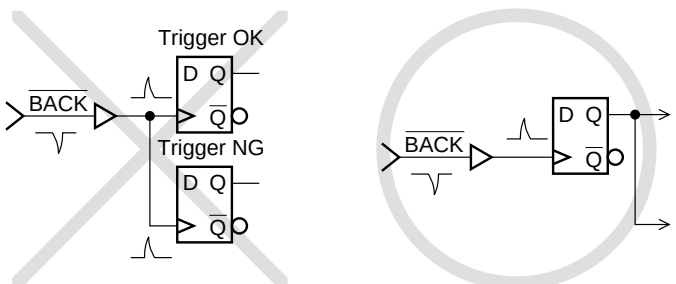
Note that delay of the $\overline{\text{BACK}}$ signal increases in units of approximately 0.1 ns/pF. (When a capacitance of 220 pF is added, the delay increases by approximately 22 ns.)



Circuit with capacitor for eliminating spikes

c. Latching the $\overline{\text{BACK}}$ signal by using a flip-flop or triggering the flip-flop may or may not be successful due to the narrow pulse width of the spike. Implement a circuit configuration which will cause no problems when latching $\overline{\text{BACK}}$ or using $\overline{\text{BACK}}$ as a trigger signal.

When splitting the $\overline{\text{BACK}}$ signal into two signals and latching each of them using a flip-flop or triggering the flip-flop, the flip-flop may operate for one signal but not for the other. To capture the $\overline{\text{BACK}}$ signal using a flip-flop, receive the $\overline{\text{BACK}}$ signal using a single flip-flop then distribute the signal (see figure below).



8.11 Usage Notes

8.11.1 Usage Notes on Manual Reset

Condition: When DRAM (long-pitch mode) is used and a manual reset is performed.

The low width of $\overline{RAS}$ output may be shorter than usual in a reset (2.5 tcyc → 1.5 tcyc), preventing the specified value (t_{RAS}) of DRAM from being satisfied.

Corresponding DRAM conditions: Long-pitch/normal mode
Long-pitch/high-speed page mode

There are no problems regarding operations except for the above conditions.

There are the following four cases (figures 8.38 to 8.41) for the output states of DRAM control signals ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WR}$) corresponding to $\overline{RES}$ latch timing. Actual output levels are shown by solid lines (not by dashed lines).

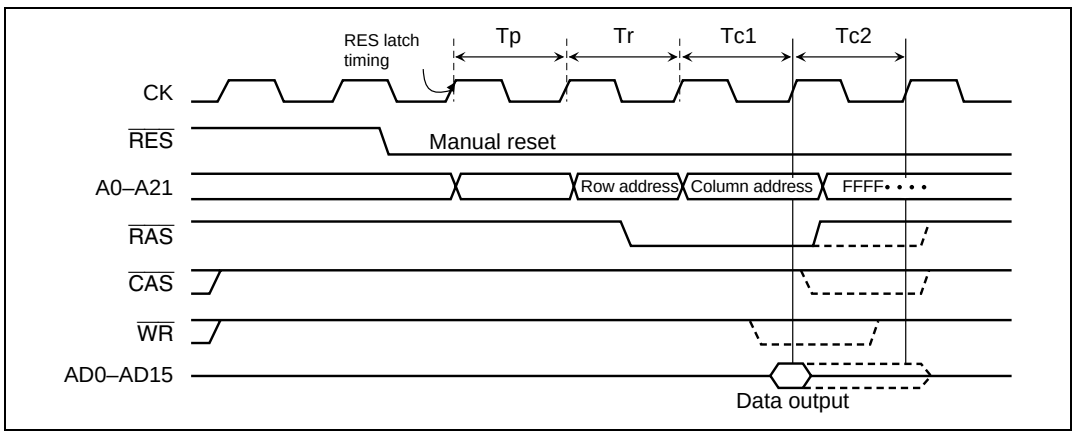


Figure 8.38 Long-Pitch Mode Write (1)

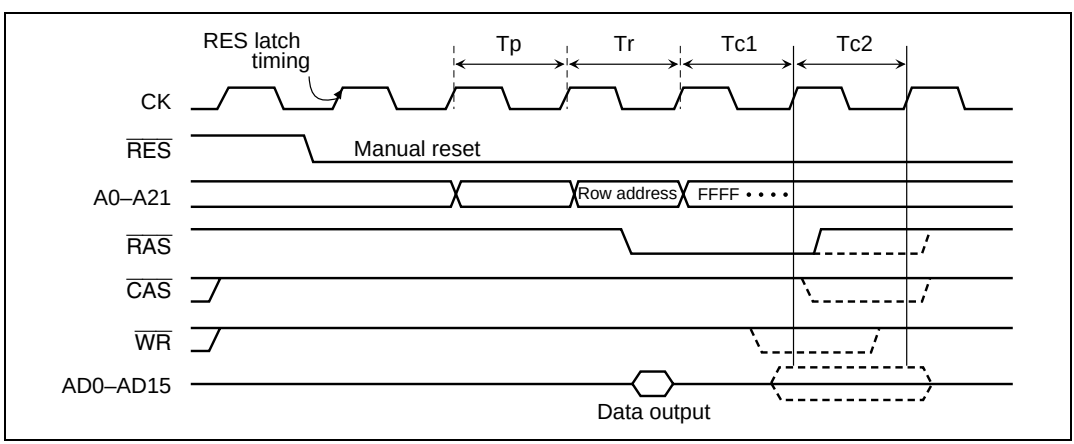


Figure 8.39 Long-Pitch Mode Write (2)

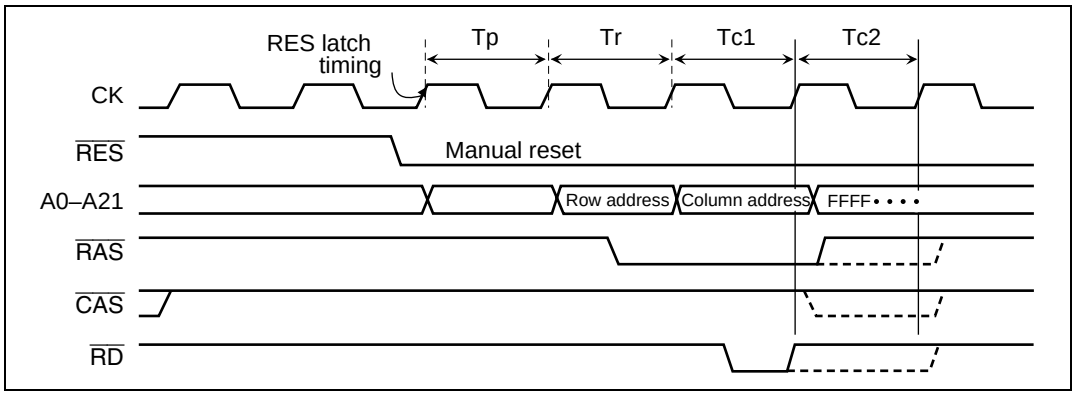


Figure 8.40 Long-Pitch Mode Read (1)

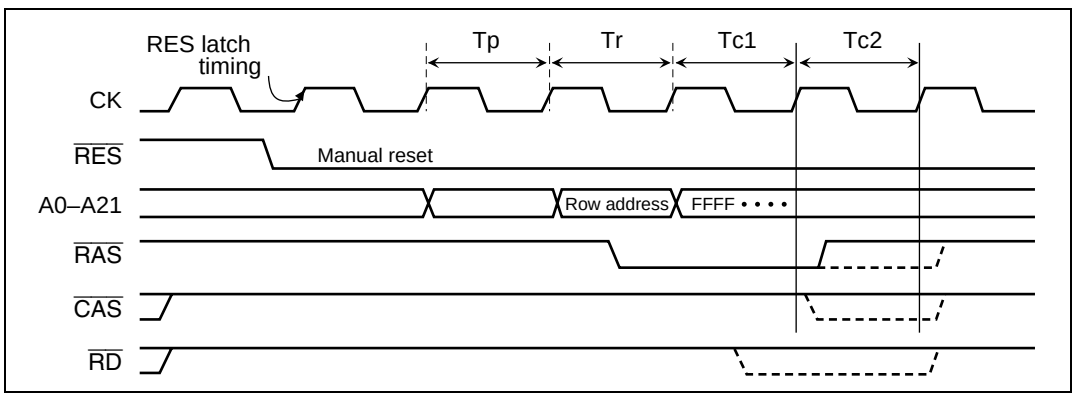


Figure 8.41 Long-Pitch Mode Read (2)

For the signal output shown by solid lines, DRAM data may not be held. Therefore, when DRAM data must be held after a reset, take one of the measures described below.

1. When resetting manually, use the watchdog timer (WDT) reset function.
2. Even if the low width of $\overline{RAS}$ becomes as short as 1.5 tcyc as shown above, use with a frequency that satisfies the DRAM standard (t_{RAS}).
3. Even if the low width of $\overline{RAS}$ is 1.5 tcyc, use an external circuit so that a $\overline{RAS}$ signal with a low width of 2.5 tcyc is input in the DRAM (if the low width of $\overline{RAS}$ is higher than 2.5 tcyc, operate so that the current waveform is input in the DRAM).

These measures are not required when DRAM data is initialized or loaded again after a manual reset.

8.11.2 Usage Notes on Parity Data Pins DPH and DPL

The following specifies the setup time, t_{DS}, of parity data DPH and DPL with respect to the fall of the $\overline{CAS}$ signal when parity data DPH and DPL are written to DRAM in long-pitch mode (early write).

Table 8.13 Setup Time of Parity Data DPH and DPL

Item	Symbol	Min
Data setup time with respect to $\overline{CAS}$ (for only DPH and DPL in long-pitch mode)	t_{DS}	-5ns

Therefore, when writing parity data DPH and DPL to the DRAM in long-pitch mode, delay the $\overline{WRH}$ and $\overline{WRL}$ signals of this chip and used delayed writing. Normal data is also delay-written, but this is not a problem.

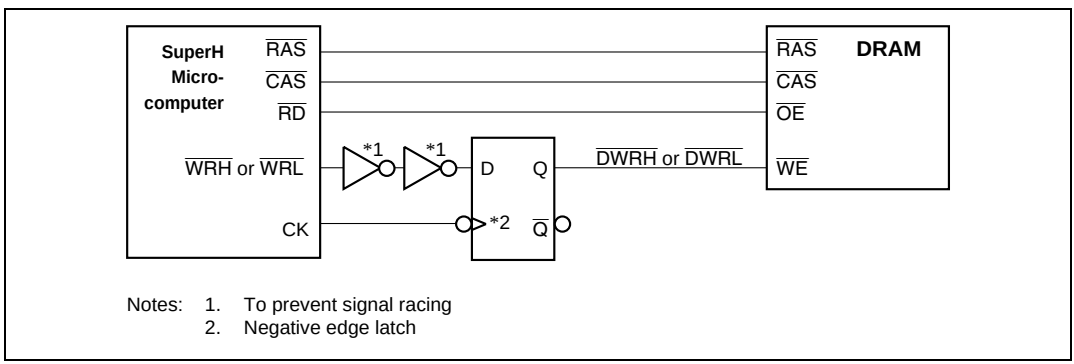


Figure 8.42 Delayed-Write Control Circuit

8.11.3 Maximum Number of States from $\overline{BREQ}$ Input to Bus Release

The maximum number of states from $\overline{BREQ}$ input to bus release is:

Maximum number of states for which bus is not released + approx. 4.5 states

Note: Breakdown of approx. 4.5 states:

1.5 states:	Until BACK output after end of bus cycle
1 state (min.):	t_{BACD1}
1 state (max.):	t_{BRQS}
1 state:	Sampling in 1 state before end of bus cycle

$\overline{BREQ}$ is sampled one state before the bus cycle. If $\overline{BREQ}$ is input without satisfying t_{BRQS}, the bus is released after executing cycle B following the end of bus cycle A, as shown in figure 8.43.

The maximum number of states from $\overline{\text{BREQ}}$ input to bus release are used when B is a cycle comprising the maximum number of states for which the bus is not released; the number of states is the maximum number of states for which bus is not released + approx. 4.5 states.

The maximum number of states for which the bus is not released requires careful investigation.

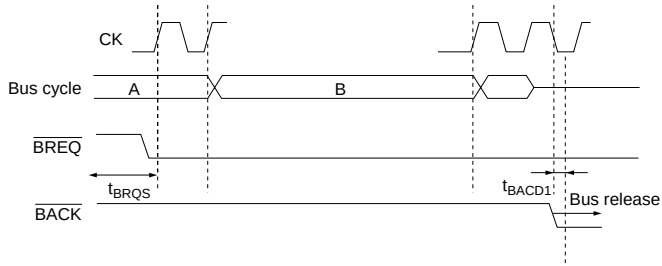


Figure 8.43 When $\overline{\text{BREQ}}$ is Input without Satisfying t_{BRQS}

1. Cycles in which bus is not released
   a. One bus cycle

      The bus is never released during one bus cycle. For example, in the case of a longword read (or write) in 8-bit ordinary space, one bus cycle consists of 4 memory accesses to 8-bit ordinary space, as shown in figure 8.44. The bus is not released between these accesses. Assuming one memory access to require 2 states, the bus is not released for a period of 8 states.

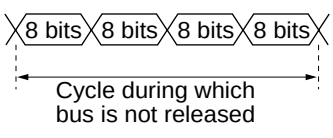


Figure 8.44 One Bus Cycle

   b. TAS instruction read cycle and write cycle

      The bus is never released during a TAS instruction read cycle and write cycle (figure 8.45). The TAS instruction read cycle and write cycle should be regarded as one bus cycle during which the bus is not released.

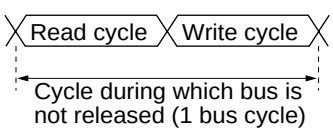


Figure 8.45 TAS Instruction Read Cycle and Write Cycle

c. Refresh cycle + bus cycle

The bus is never released during a refresh cycle and the following bus cycle ((a) or (b) above)) (figure 8.46).

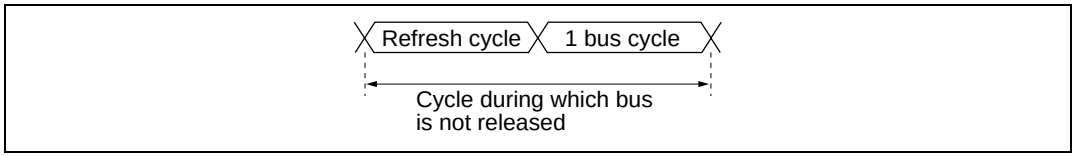


Figure 8.46 Refresh Cycle and Following Bus Cycle

2. Bus release procedure

The bus release procedure is shown in figure 8.47. Figure 8.47 shows the case where $\overline{\text{BREQ}}$ is input one state before the break between bus cycles so that tBRQS is satisfied. In the SH7032 and SH7034, the bus is released after the bus cycle in which $\overline{\text{BREQ}}$ is input (if $\overline{\text{BREQ}}$ is input between bus cycles, after the bus cycle starting next).

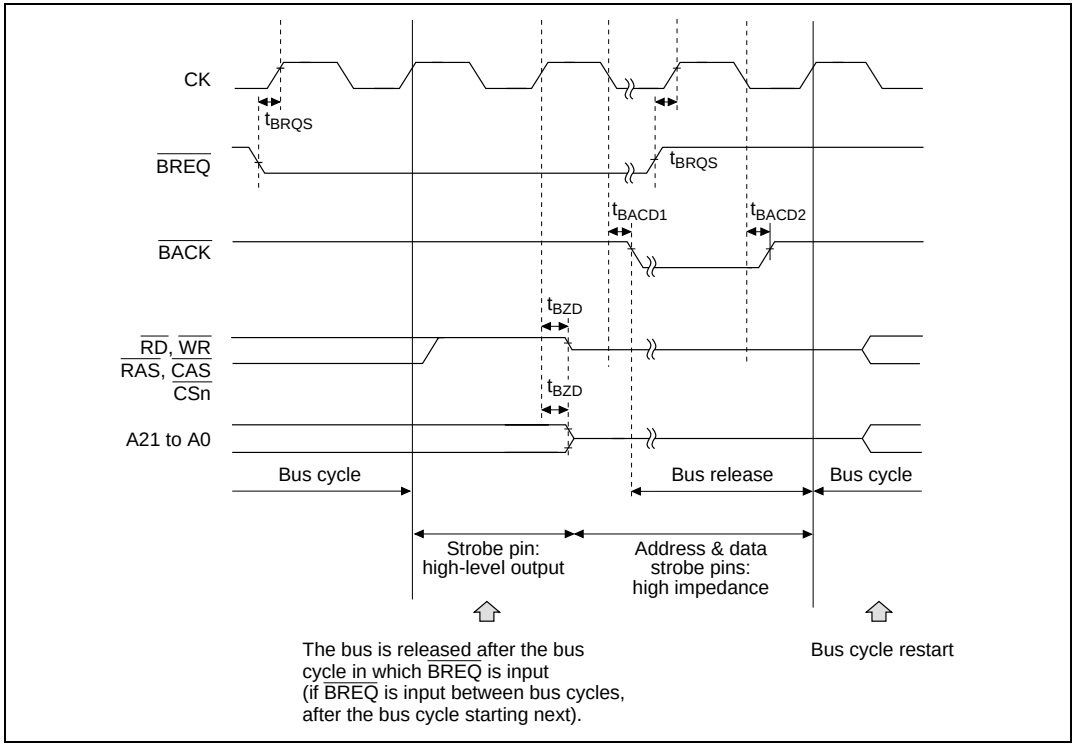


Figure 8.47 Bus Release Procedure

Section 9 Direct Memory Access Controller (DMAC)

9.1 Overview

The SuperH microcomputer chip includes a four-channel direct memory access controller (DMAC). The DMAC can be used in place of the CPU to perform high speed transfers between external devices that have DACK (transfer request acknowledge signal), external memory, memory-mapped external devices, on-chip memory, and on-chip supporting modules (excluding the DMAC itself). Using the DMAC reduces the burden on the CPU and increases overall operating efficiency.

9.1.1 Features

The DMAC has the following features.

- Four channels
- Four Gbytes of address space in the architecture
- Byte or word selectable as data transfer unit
- 65536 transfers (maximum)
- Single address mode transfers (channels 0 and 1): Either the transfer source or transfer destination (peripheral device) is accessed by a DACK signal (selectable) while the other is accessed by address. One transfer unit of data is transferred in each bus cycle.

  Device combinations for which transfer is possible:

  — External device with DACK and memory-mapped external device (including external memories)

  — External device with DACK and memory-mapped external memory
- Dual address mode transfer (channels 0–3): Both the transfer source and transfer destination are accessed by address. One transfer unit of data is transferred in 2 bus cycles.

  Device combinations for which transfer is possible:

  — Two external memories

  — External memory and memory-mapped external device

  — Two memory-mapped devices

  — External memory and on-chip memory

  — Memory-mapped external device and on-chip supporting module (excluding the DMAC)

  — External memory and on-chip memory

  — Memory-mapped external device and on-chip supporting module (excluding the DMAC)

  — Two on-chip memories

— On-chip memory and on-chip supporting module (excluding the DMAC)
— Two on-chip supporting modules (excluding the DMAC)

- Transfer requests
  — External request (From $\overline{\text{DREQ}}$ pins (channels 0 and 1 only). $\overline{\text{DREQ}}$ can be detected either by edge or by level)
  — Requests from on-chip supporting modules (serial communication interface (SCI), A/D converter (A/D), and 16-bit integrated timer pulse unit (ITU))
  — Auto-request (the transfer request is generated automatically within the DMAC)
- Selectable bus modes: Cycle-steal mode or burst mode
- Selectable channel priority levels: Fixed, round-robin, or external-pin round-robin modes
- CPU can be asked for interrupt when data transfer ends
- Maximum transfer rate
  — 20 M words/s (320 MB/s)
  For 5 V and 20 MHz
  Bus mode: Burst mode
  Transmission size: Word

9.1.2 Block Diagram

Figure 9.1 shows a block diagram of the DMAC.

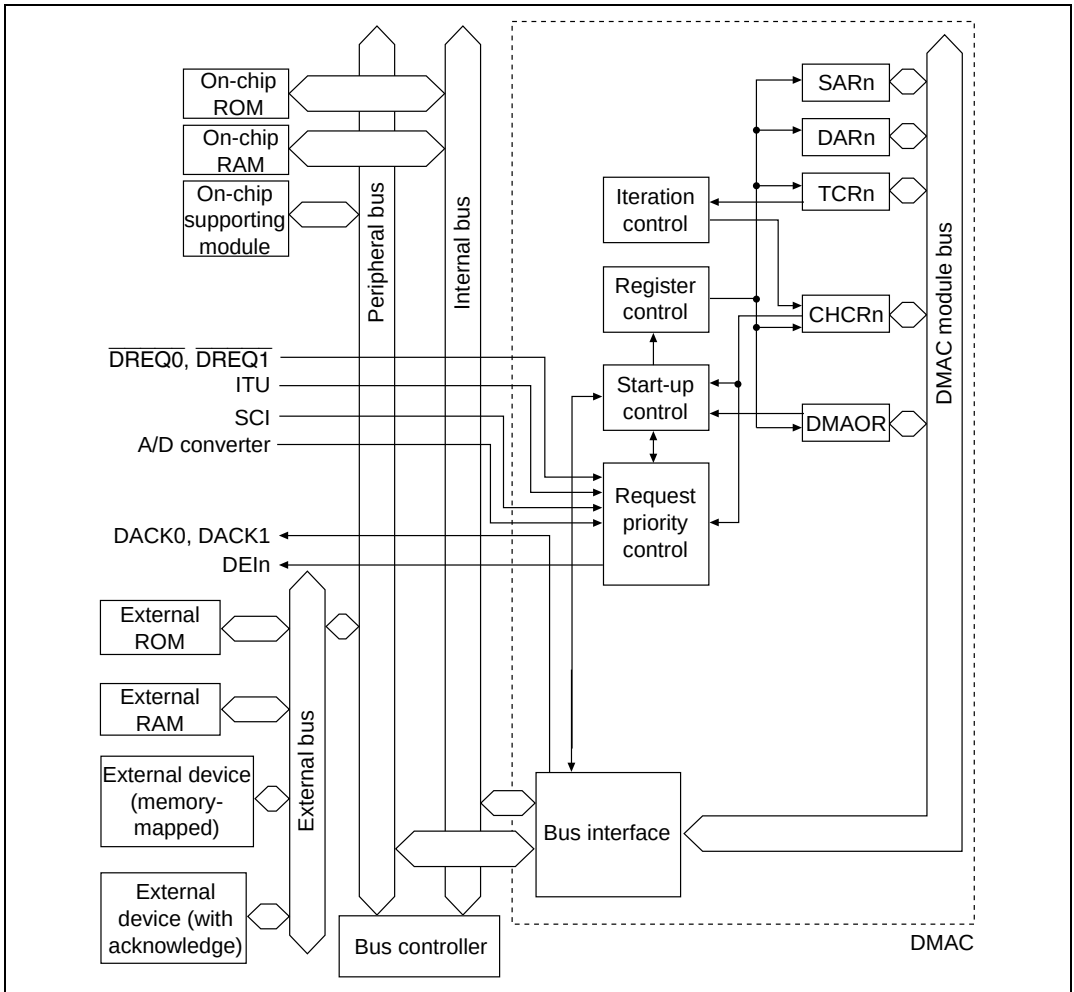


Figure 9.1 Block Diagram of DMAC

9.1.3 Pin Configuration

Table 9.1 shows the DMAC pins.

Table 9.1 Pin Configuration

Channel	Name	Symbol	I/O	Function
0	DMA transfer request	$\overline{\text{DREQ0}}$	I	DMA transfer request input from external device to channel 0
	DMA transfer request acknowledge	DACK0	O	DMA transfer request acknowledge output from channel 0 to external device
1	DMA transfer request	$\overline{\text{DREQ1}}$	I	DMA transfer request input from external device to channel 1
	DMA transfer request acknowledge	DACK1	O	DMA transfer request acknowledge output from channel 1 to external device

9.1.4 Register Configuration

Table 9.2 summarizes the DMAC registers. The DMAC has a total of 17 registers. Each channel has four control registers. One other control register is shared by all channels.

Table 9.2 DMAC Registers

Channel	Name	Abbreviation	R/W	Initial Value	Address*4	Access Size
0	DMA source address register 0	SAR0*3	R/W	Undefined	H'5FFFF40	16, 32
	DMA destination address register 0	DAR0*3	R/W	Undefined	H'5FFFF44	16, 32
	DMA transfer count register 0	TCR0*3	R/W	Undefined	H'5FFFF4A	16, 32
	DMA channel control register 0	CHCR0	R/(W)*1	H'0000	H'5FFFF4E	8, 16, 32
1	DMA source address register 1	SAR1*3	R/W	Undefined	H'5FFFF50	16, 32
	DMA destination address register 1	DAR1*3	R/W	Undefined	H'5FFFF54	16, 32
	DMA transfer count register 1	TCR1*3	R/W	Undefined	H'5FFFF5A	16, 32
	DMA channel control register 1	CHCR1	R/(W)*1	H'0000	H'5FFFF5E	8, 16, 32
2	DMA source address register 2	SAR2*3	R/W	Undefined	H'5FFFF60	16, 32
	DMA destination address register 2	DAR2*3	R/W	Undefined	H'5FFFF64	16, 32
	DMA transfer count register 2	TCR2*3	R/W	Undefined	H'5FFFF6A	16, 32
	DMA channel control register 2	CHCR2	R/(W)*1	H'0000	H'5FFFF6E	8, 16, 32
3	DMA source address register 3	SAR3*3	R/W	Undefined	H'5FFFF70	16, 32
	DMA destination address register 3	DAR3*3	R/W	Undefined	H'5FFFF74	16, 32
	DMA transfer count register 3	TCR3*3	R/W	Undefined	H'5FFFF7A	16, 32
	DMA channel control register 3	CHCR3	R/(W)*1	H'0000	H'5FFFF7E	8, 16, 32
Shared	DMA operation register	DMAOR	R/(W)*2	H'0000	H'5FFFF48	8, 16, 32

Notes:
1. Only 0 can be written in bit 1 of CHCR0–CHCR3, to clear flags.
2. Only 0 can be written in bits 1 and 2 of DMAOR, to clear flags.
3. Access SAR0–SAR3, DAR0–DAR3, and TCR0–TCR3 by longword or word. If byte access is used when writing, the value of the register contents will be undefined; if used when reading, the value read will be undefined.
4. Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.

9.2 Register Descriptions

9.2.1 DMA Source Address Registers 0–3 (SAR0–SAR3)

DMA source address registers 0–3 (SAR0–SAR3) are 32-bit read/write registers that specify the source address of a DMA transfer. During a DMA transfer, these registers indicate the next source address (in single-address mode, SAR is ignored in transfers from external devices with DACK to memory-mapped external devices or external memory).

The initial value after a reset or in standby mode is undefined.

Bit	31	30	29	28	27	26	25	24
Initial value	—	—	—	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	…	0
				…	
Initial value	—	—	—	…	—
Read/Write	R/W	R/W	R/W	…	R/W

9.2.2 DMA Destination Address Registers 0–3 (DAR0–DAR3)

DMA destination address registers 0–3 (DAR0–DAR3) are 32-bit read/write registers that specify the destination address of a DMA transfer. During a DMA transfer, these registers indicate the next destination address (in single-address mode, DAR is ignored in transfers from memory-mapped external devices or external memory to external devices with DACK). The initial value after a reset or in standby mode is undefined.

Bit	31	30	29	28	27	26	25	24
Initial value	—	—	—	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	…	0
				…	
Initial value	—	—	—	…	—
Read/Write	R/W	R/W	R/W	…	R/W

9.2.3 DMA Transfer Count Registers 0–3 (TCR0–TCR3)

DMA transfer count registers 0–3 (TCR0–TCR3) are 16-bit read/write registers that specify the DMA transfer count (bytes or words). The number of transfers is 1 when the setting is H'0001, 65535 when the setting is H'FFFF, and 65536 (the maximum) when H'0000 is set. During a DMA transfer, these registers indicate the remaining transfer count. The initial value after a reset or in standby mode is undefined.

Bit	15	14	13	12	11	10	9	8
Initial value	—	—	—	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	—	—	—	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.2.4 DMA Channel Control Registers 0–3 (CHCR0–CHCR3)

DMA channel control registers 0–3 (CHCR0–CHCR3) are 16-bit read/write registers that control the DMA transfer mode. They also indicate the DMA transfer status. They are initialized to H'0000 by a reset and in standby mode.

Bit	15	14	13	12	11	10	9	8
	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	AM	AL	DS	TM	TS	IE	TE	DE
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*2	R/(W)*2	R/(W)*2	R/W	R/W	R/W	R/(W)*1	R/W

Notes: 1. Only 0 can be written, to clear the flag.
2. Writing is valid only for CHCR0 and CHCR1.

Bits 15 and 14—Destination Address Mode Bits 1 and 0 (DM1 and DM0): DM1 and DM0 select whether the DMA destination address is incremented, decremented, or left fixed (in the single address mode, DM1 and DM0 are ignored when transfers are made from memory-mapped external devices or external memory to external devices with DACK). DM1 and DM0 are initialized to 00 by a reset and in standby mode.

Bit 15: DM1	Bit 14: DM0	Description
0	0	Fixed destination address (Initial value)
0	1	Destination address is incremented (+1 or +2 depending on whether the transfer size is word or byte)
1	0	Destination address is decremented (–1 or –2 depending on whether the transfer size is word or byte)
1	1	Reserved (illegal setting)

Bits 13 and 12—source address mode bits 1, 0 (SM1 and SM0): SM1 and SM0 select whether the DMA source address is incremented, decremented, or left fixed (in the single address mode, SM1 and SM0 are ignored when transfers are made from external devices with DACK to memory-mapped external devices or external memory). SM1 and SM0 are initialized to 00 by resets or in standby mode.

Bit 13: SM1	Bit 12: SM0	Description
0	0	Fixed source address (Initial value)
0	1	Source address is incremented (+1 or +2 depending on if the transfer size is word or byte)
1	0	Source address is decremented (–1 or –2 depending on if the transfer size is word or byte)
1	1	Reserved (illegal setting)

Bits 11–8—Resource Select Bits 3–0 (RS3–RS0): RS3–RS0 specify which transfer requests will be sent to the DMAC. Do not change the transfer request source unless the DMA enable bit (DE) is 0. The RS3–RS0 bits are initialized to 0000 by a reset and in standby mode.

Bit 11: RS3	Bit 10: RS2	Bit 9: RS1	Bit 8: RS0	Description
0	0	0	0	$\overline{\text{DREQ}}$ (External request*[1], dual address mode) (Initial value)
0	0	0	1	Reserved (illegal setting)
0	0	1	0	$\overline{\text{DREQ}}$ (External request*[1], single address mode*[2])
0	0	1	1	$\overline{\text{DREQ}}$ (External request*[1], single address mode*[3])
0	1	0	0	RXI0 (On-chip serial communication interface 0 receive data full interrupt transfer request)*[4]
0	1	0	1	TXI0 (On-chip serial communication interface 0 transmit data empty interrupt transfer request)*[4]
0	1	1	0	RXI1 (On-chip serial communication interface 1 receive data full interrupt transfer request)*[4]
0	1	1	1	TXI1 (On-chip serial communication interface 1 transmit data empty interrupt transfer request)*[4]
1	0	0	0	IMIA0 (On-chip ITU0 input capture/compare match A interrupt transfer request)*[4]
1	0	0	1	IMIA1 (On-chip ITU1 input capture/compare match A interrupt transfer request)*[4]
1	0	1	0	IMIA2 (On-chip ITU2 input capture/compare match A interrupt transfer request)*[4]
1	0	1	1	IMIA3 (On-chip ITU3 input capture/compare match A interrupt transfer request)*[4]
1	1	0	0	Auto-request (Transfer requests automatically generated within DMAC)*[4]
1	1	0	1	ADI (A/D conversion end interrupt request of on-chip A/D converter)*[4]
1	1	1	0	Reserved (illegal setting)
1	1	1	1	Reserved (illegal setting)

SCI0, SCI1: Serial communication interface channels 0 and 1

ITU0–ITU3: Channels 0–3 of the 16-bit integrated timer pulse unit

Notes: 1. These bits are valid only in channels 0 and 1. None of these request sources can be selected in channels 2 and 3.

2. Transfer from memory-mapped external device or external memory to external device with DACK.

3. Transfer from external device with DACK to memory-mapped external device or external memory.

4. Dual address mode.

Bit 7—Acknowledge Mode Bit (AM): In dual address mode, AM selects whether the DACK signal is output during the data read cycle or write cycle. This bit is valid only in channels 0 and 1. The AM bit is initialized to 0 by a reset and in standby mode. The AM bit is not valid in single address mode.

Bit 7: AM	Description	
0	DACK is output in read cycle	(Initial value)
1	DACK is output in write cycle	

Bit 6—Acknowledge Level Bit (AL): AL selects active-high or active-low for the DACK signal. This bit is valid only in channels 0 and 1. The AL bit is initialized to 0 by a reset and in standby mode.

Bit 6: AL	Description	
0	DACK is active-high	(Initial value)
1	DACK is active-low	

Bit 5—$\overline{\text{DREQ}}$ Select Bit (DS): DS selects the $\overline{\text{DREQ}}$ input detection method used. This bit is valid only in channels 0 and 1. The DS bit is initialized to 0 by a reset and in standby mode.

Bit 5: DS	Description	
0	$\overline{\text{DREQ}}$ detected by low level	(Initial value)
1	$\overline{\text{DREQ}}$ detected by falling edge	

Bit 4—Transfer Bus Mode Bit (TM): TM selects the bus mode for DMA transfers. The TM bit is initialized to 0 by a reset and in standby mode. When the source of the transfer request is an on-chip supporting module, see table 9.4, Selecting On-Chip Peripheral Module Request Modes with the RS Bits.

Bit 4: TM	Description	
0	Cycle-steal mode	(Initial value)
1	Burst mode	

Bit 3—Transfer Size Bit (TS): TS selects the transfer unit size. If the on-chip supporting module that is the source or destination of the transfer can only be accessed in bytes, byte must be selected with this bit. The TS bit is initialized to 0 by a resets and in standby mode.

Bit 3: TS	Description	
0	Byte (8 bits)	(Initial value)
1	Word (16 bits)	

Bit 2—Interrupt Enable Bit (IE): IE determines whether or not to request a CPU interrupt at the end of a DMA transfer. When the IE bit is set to 1, an interrupt (DEI) request is sent to the CPU when the TE bit is set. The IE bit is initialized to 0 by a reset and in standby mode.

Bit 2: IE	Description	
0	Interrupt request disabled	(Initial value)
1	Interrupt request enabled	

Bit 1—Transfer End Flag Bit (TE): TE indicates that the transfer has ended. When a DMA transfer ends normally and the value in the DMA transfer count register (TCR) becomes 0, the TE bit is set to 1. This flag is not set if the transfer ends because of an NMI interrupt or address error, or because the DE bit or the DME bit in the DMA operation register (DMAOR) was cleared. To clear the TE bit, read 1 from it and then write 0.

When this flag is set, setting the DE bit to 1 does not enable a DMA transfer. The TE bit is initialized to 0 by a reset and in standby mode.

Bit 1: TE	Description	
0	DMA has not ended or was aborted To clear TE, the CPU must read TE after it has been set to 1, then write a 0 in this bit	(Initial value)
1	DMA has ended normally	

Bit 0—DMA Enable Bit (DE): DE enables or disables DMA transfers. In auto-request mode, the transfer starts when this bit or the DME bit in DMAOR is set to 1. The TE bit and the NMIF and AE bits in DMAOR must be all cleared to 0. In external request mode or on-chip supporting module request mode, the transfer begins when the DMA transfer request is received from a device or on-chip supporting module, provided this bit and the DME bit are set to 1. As with auto request mode, the TE bit and the NMIF and AE bits must be all cleared to 0. The transfer can be stopped by clearing this bit to 0.

The DE bit is initialized to 0 by a reset and in standby mode.

Bit 0: DE	Description	
0	DMA transfer disabled	(Initial value)
1	DMA transfer enabled	

9.2.5 DMA Operation Register (DMAOR)

The DMA operation register (DMAOR) is a 16-bit read/write register that controls the DMA transfer mode. It also indicates the DMA transfer status. It is initialized to H'0000 by a reset and in standby mode.

Bit	15	14	13	12	11	10	9	8
	——	—	—	—	—	—	PR1	PR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	AE	NMIF	DME
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R/(W)*	R/(W)*	R/W

Note: * Write only 0 to clear the flag.

Bits 15–10—Reserved: These bits are always read as 0. The write value should always be 0.

Bits 9 and 8—Priority Mode Bits 1 and 0 (PR1 and PR0): PR1 and PR0 select the priority level between channels when there are simultaneous transfer requests for multiple channels.

Bit 9: PR1	Bit 8: PR0	Description
0	0	Fixed priority order (Ch. 0 > Ch. 3 > Ch. 2 > Ch. 1) (Initial value)
0	1	Fixed priority order (Ch. 1 > Ch. 3 > Ch. 2 > Ch. 0)
1	0	Round-robin mode priority order (the priority order immediately after a reset is Ch. 0 > Ch. 3 > Ch. 2 > Ch. 1)
1	1	External-pin round-robin mode priority order (the priority order immediately after a reset is Ch. 3 > Ch. 2 > Ch. 1 > Ch. 0)

Bits 7–3—Reserved: These bits are always read as 0. The write value should always be 0.

Bit 2—Address Error Flag Bit (AE): AE indicates that an address error has occurred in the DMAC. When this flag is set to 1, the channel cannot be enabled even if the DE bit in the DMA channel control register (CHCR) and the DME bit are set to 1. To clear the AE bit, read 1 from it and then write 0. It is initialized to 0 by a reset and in standby mode.

Bit 2: AE	Description	
0	No DMAC address error	(Initial value)
	To clear the AE bit, read 1 from it and then write 0	
1	Address error by DMAC	

Bit 1—NMI Flag Bit (NMIF): NMIF indicates that an NMI interrupt has occurred. When this flag is set to 1, the channel cannot be enabled even if the DE bit in CHCR and the DME bit are set to 1. To clear the NMIF bit, read 1 from it and then write 0. It is initialized to 0 by a reset and in standby mode.

Bit 1: NMIF	Description	
0	No NMI interrupt	(Initial value)
	To clear the NMIF bit, read 1 from it and then write 0	
1	NMI has occurred	

Bit 0—DMA Master Enable Bit (DME): DME enables or disables DMA transfers on all channels. A channel becomes enabled for a DMA transfer when the DE bit in each DMA's CHCR and the DME bit are set to 1. For this to be effective, however, the TE bit of each CHCR and the NMIF and AE bits must all be 0. When the DME bit is cleared, all channel DMA transfers are aborted.

Bit 0: DME	Description	
0	DMA transfers disabled on all channels	(Initial value)
1	DMA transfers enabled on all channels	

9.3 Operation

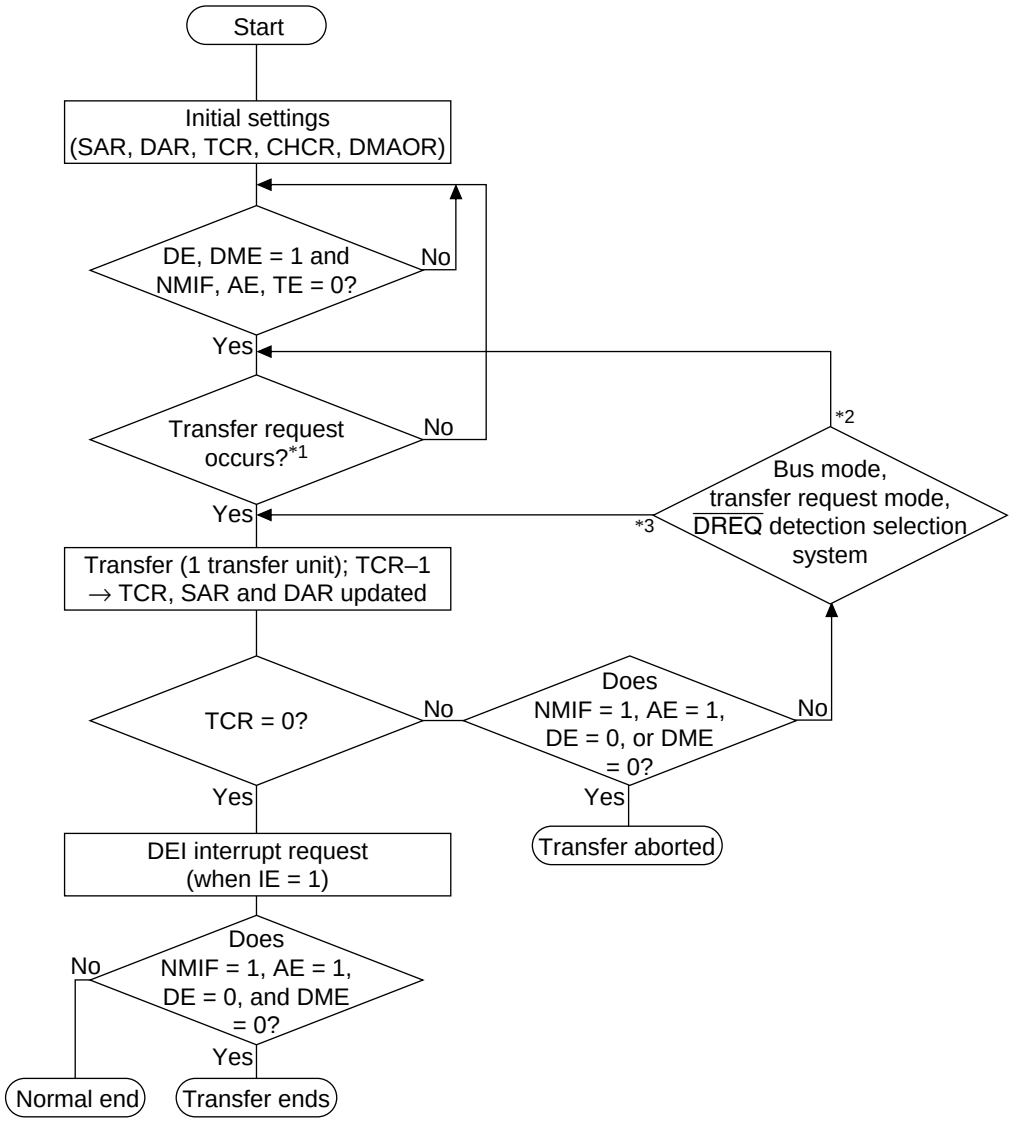
When there is a DMA transfer request, the DMAC starts the transfer according to the predetermined channel priority order; when the transfer end conditions are satisfied, it ends the transfer. Transfers can be requested in three modes: auto-request, external request, and on-chip module request. Transfer can be in either single address mode or dual address mode. The bus mode can be either burst or cycle steal.

9.3.1 DMA Transfer Flow

After the DMA source address registers (SAR), DMA destination address registers (DAR), DMA transfer count registers (TCR), DMA channel control registers (CHCR), and DMA operation register (DMAOR) are set, the DMAC transfers data according to the following procedure:

1. Checks to see if transfer is enabled (DE = 1, DME = 1, TE = 0, NMIF = 0, AE = 0).
2. When a transfer request arrives and transfer is enabled, the DMAC transfers one transfer unit of data. (For an auto-request, the transfer begins automatically when the DE bit and DME bit are set to 1. The TCR value will be decremented by 1.) The actual transfer flows vary by address mode and bus mode.
3. When the specified number of transfer have been completed (when TCR reaches 0), the transfer ends normally. If the IE bit in CHCR is set to 1 at this time, a DEI interrupt is sent to the CPU.
4. When an address error occurs in the DMAC or an NMI interrupt is generated, the transfer is aborted. Transfers are also aborted when the DE bit in CHCR or the DME bit in DMAOR changes to 0.

Figure 9.2 shows a flowchart of this procedure.



Notes: 1. In auto-request mode, transfer begins when NMIF, AE, and TE are all 0 and the DE and DME bits are set to 1.
2. $\overline{\text{DREQ}}$ = level detection in burst mode (external request), or cycle steal mode.
3. $\overline{\text{DREQ}}$ = edge detection in burst mode (external request), or auto request mode in burst mode.

Figure 9.2 DMA Transfer Flowchart

9.3.2 DMA Transfer Requests

DMA transfer requests are basically generated in either the data transfer source or destination, but they can also be generated by devices and on-chip supporting modules that are neither the source nor the destination. Transfers can be requested in three modes: auto-request, external request, and on-chip module request. The request mode is selected with the RS3–RS0 bits in the DMA channel control registers 0–3 (CHCR0–CHCR3).

Auto-Request Mode: When there is no transfer request signal from an external source, as in a memory-to-memory transfer or a transfer between memory and an on-chip supporting module unable to request a transfer, the auto-request mode allows the DMAC to automatically generate a transfer request signal internally. When the DE bits in CHCR0–CHCR3 and the DME bit in DMAOR are set to 1, the transfer begins (so long as the TE bits in CHCR0–CHCR3 and the NMIF and AE bits in DMAOR are all 0).

External Request Mode: In this mode a transfer is performed in response to a request signal ($\overline{\text{DREQ}}$) of an external device. Choose one of the modes shown in table 9.3 according to the application system. When this mode is selected, if DMA transfer is enabled (DE = 1, DME = 1, TE = 0, NMIF = 0, AE = 0), a transfer is performed upon a request at the $\overline{\text{DREQ}}$ input. Choose to detect $\overline{\text{DREQ}}$ by either the falling edge or low level of the signal input with the DS bit in CHCR0–CHCR3 (DS = 0 specifies level detection, DS = 1 specifies edge detection). The source of the transfer request does not have to be the data transfer source or destination.

Table 9.3 Selecting External Request Modes with the RS Bits

RS3	RS2	RS1	RS0	Address Mode	Source	Destination
0	0	0	0	Dual address mode	Any*	Any*
0	0	1	0	Single address mode	External memory or memory-mapped external device	External device with DACK
0	0	1	1	Single address mode	External device with DACK	External memory or memory-mapped external device

Note: * External memory, memory-mapped external device, on-chip memory, on-chip supporting module (excluding DMAC)

On-Chip Module Request: In this mode a transfer is performed in response to a transfer request signal (interrupt request signal) of an on-chip module. The transfer request signals include the receive data full interrupt (RXI) of the serial communication interface (SCI), the transmit data empty interrupt (TXI) of the SCI, the input capture A/compare match A interrupt request (IMIA) of the 16-bit integrated pulse timer (ITU), and the A/D conversion end interrupt (ADI) of the A/D

converter (table 9.4). When this mode is selected, if DMA transfer is enabled (DE = 1, DME = 1, TE = 0, NMIF = 0, AE = 0), a transfer is performed upon input of a transfer request signal. The source of the transfer request does not have to be the data transfer source or destination. When RXI is set as the transfer request, however, the transfer source must be the SCI's receive data register (RDR). Likewise, when TXI is set as the transfer request, the transfer source must be the SCI's transmit data register (TDR). If the transfer request is from the A/D converter, the data transfer source must be an A/D converter register.

Table 9.4 Selecting On-Chip Peripheral Module Request Modes with the RS Bits

RS 3	RS 2	RS 1	RS 0	DMA Transfer Request Source	DMA Transfer Request Signal	Source	Desti-nation	Bus Mode
0	1	0	0	SCI0 receiver	RXI0 (SCI0 receive data full interrupt transfer request)	RDR0	Any*	Cycle steal
0	1	0	1	SCI0 transmitter	TXI0 (SCI0 transmit data empty interrupt transfer request)	Any	TDR0	Cycle steal
0	1	1	0	SCI1 receiver	RXI1 (SCI1 receive data full interrupt transfer request)	RDR1	Any*	Cycle steal
0	1	1	1	SCI1 transmitter	TXI1 (SCI1 transmit data empty interrupt transfer request)	Any*	TDR1	Cycle steal
1	0	0	0	ITU0	IMIA0 (ITU0 input capture A/ compare match A)	Any*	Any*	Burst/Cycl e steal
1	0	0	1	ITU1	IMIA1 (ITU1 input capture A/ compare match A)	Any*	Any*	Burst/Cycl e steal
1	0	1	0	ITU2	IMIA2 (ITU2 input capture A/ compare match A)	Any*	Any*	Burst/Cycl e steal
1	0	1	1	ITU3	IMIA3 (ITU3 input capture A/ compare match A)	Any*	Any*	Burst/Cycl e steal
1	1	0	1	A/D converter	ADI (A/D conversion end interrupt)	ADDR	Any	Burst/Cycl e steal

SCI0, SCI1: Serial communication interface channels 0 and 1

ITU0-ITU3: Channels 0–3 of the 16-bit integrated timer pulse unit

RDR0, RDR1: Receive data registers 0, 1 of SCI

TDR0, TDR1: Transmit data registers 0, 1 of SCI

ADDR: A/D data register of A/D converter

Note: * External memory, memory-mapped external device, on-chip memory, on-chip supporting module (excluding DMAC)

When outputting transfer requests from on-chip supporting modules, the appropriate interrupt enable bits must be set to output the interrupt signals. Note that transfer request signals from on-chip supporting modules (interrupt request signals) are sent not just to the DMAC but to the CPU as well. When an on-chip supporting module is specified as the transfer request source, set the priority level values in the interrupt priority level registers (IPRC–IPRE) of the interrupt controller (INTC) at or below the levels set in the I3–I0 bits of the CPU's status register (SR) so that the CPU does not acknowledge the interrupt request signal.

The DMA transfer request signals in table 9.4 are automatically withdrawn when the corresponding DMA transfer is performed. If cycle steal mode is being used, the DMA transfer request (interrupt request) will be cleared at the first transfer; if burst mode is being used, it will be cleared at the last transfer.

9.3.3 Channel Priority

When the DMAC receives simultaneous transfer requests on two or more channels, it selects a channel according to a predetermined priority order. The three modes (fixed mode, round-robin mode, and external-pin round-robin mode) are selected by priority bits PR1 and PR0 in the DMA operation register.

Fixed Mode: In this mode, the priority levels among the channels remain fixed. When the PR1 and PR0 bits are set to 00, the priority order, high to low, is Ch. 0 > Ch. 3 > Ch. 2 > Ch. 1. When the PR1 and PR0 bits are set to 01, the priority order, high to low, is Ch. 1 > Ch. 3 > Ch. 2 > Ch. 0.

Round-Robin Mode: Each time one word or byte is transferred on one channel, the priority order is rotated. The channel on which the transfer just finished rotates to the bottom of the priority order. When necessary, the priority order of channels other than the one that just finished the transfer can also be shifted to keep the relationship between the channels from changing (figure 9.3). The priority order immediately after a reset is channel 0 > channel 3 > channel 2 > channel 1.

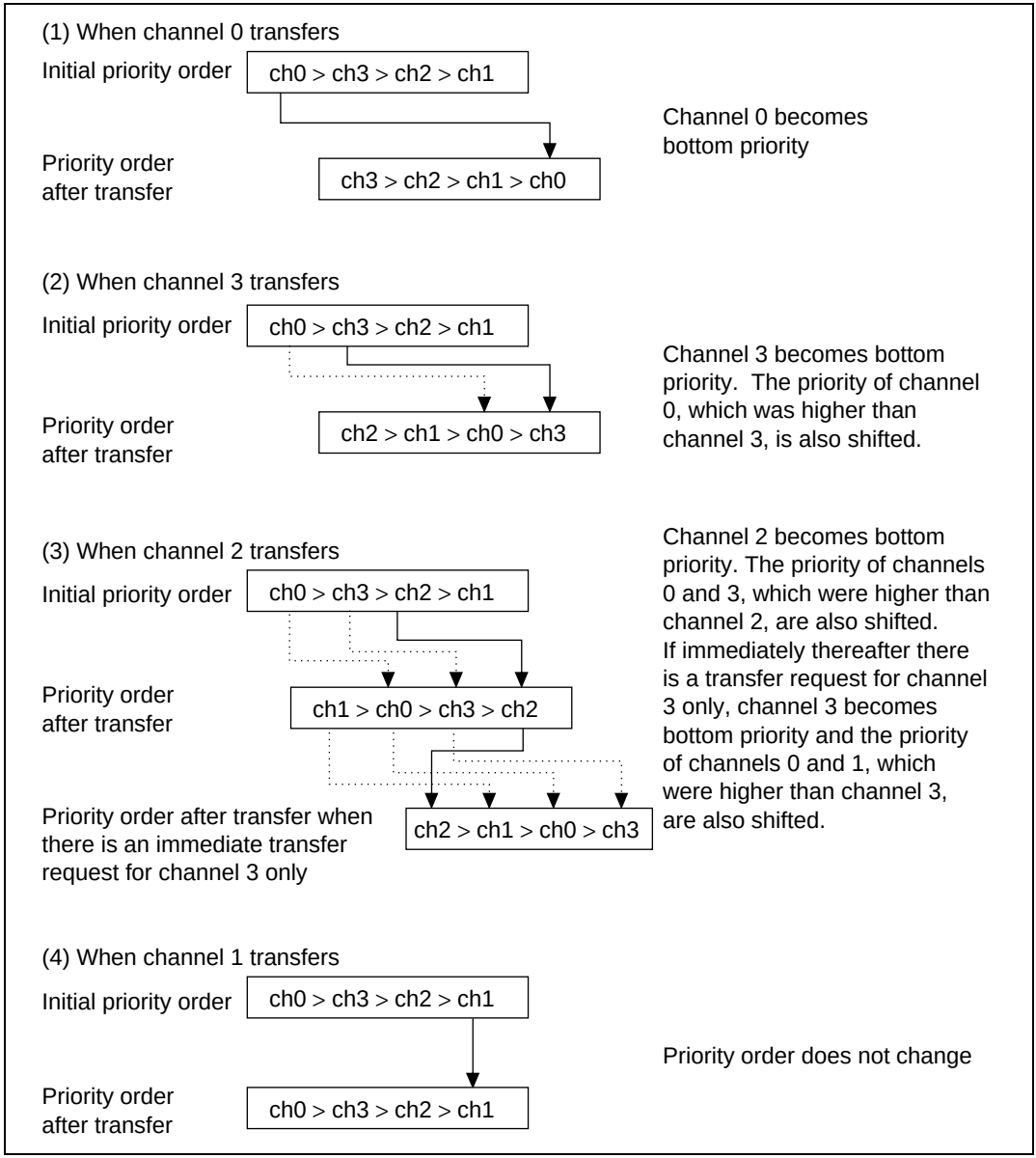


Figure 9.3 Round-Robin Mode

Figure 9.4 shows how the priority order changes when channel 0 and channel 1 transfers are requested simultaneously and a channel 3 transfer is requested during the channel 0 transfer. The DMAC operates as follows:

1. Transfer requests are generated simultaneously for channels 1 and 0.
2. Channel 0 has a higher priority, so the channel 0 transfer begins first (channel 1 waits for transfer).
3. A channel 3 transfer request occurs during the channel 0 transfer (channels 1 and 3 are both waiting)
4. When the channel 0 transfer ends, channel 0 becomes the lowest priority.
5. At this point, channel 3 has a higher priority than channel 1, so the channel 3 transfer begins (channel 1 waits for transfer).
6. When the channel 3 transfer ends, channel 3 becomes the lowest priority.
7. The channel 1 transfer begins.
8. When the channel 1 transfer ends, channels 1 and 2 shift downward in priority so that channel 1 becomes the lowest priority.

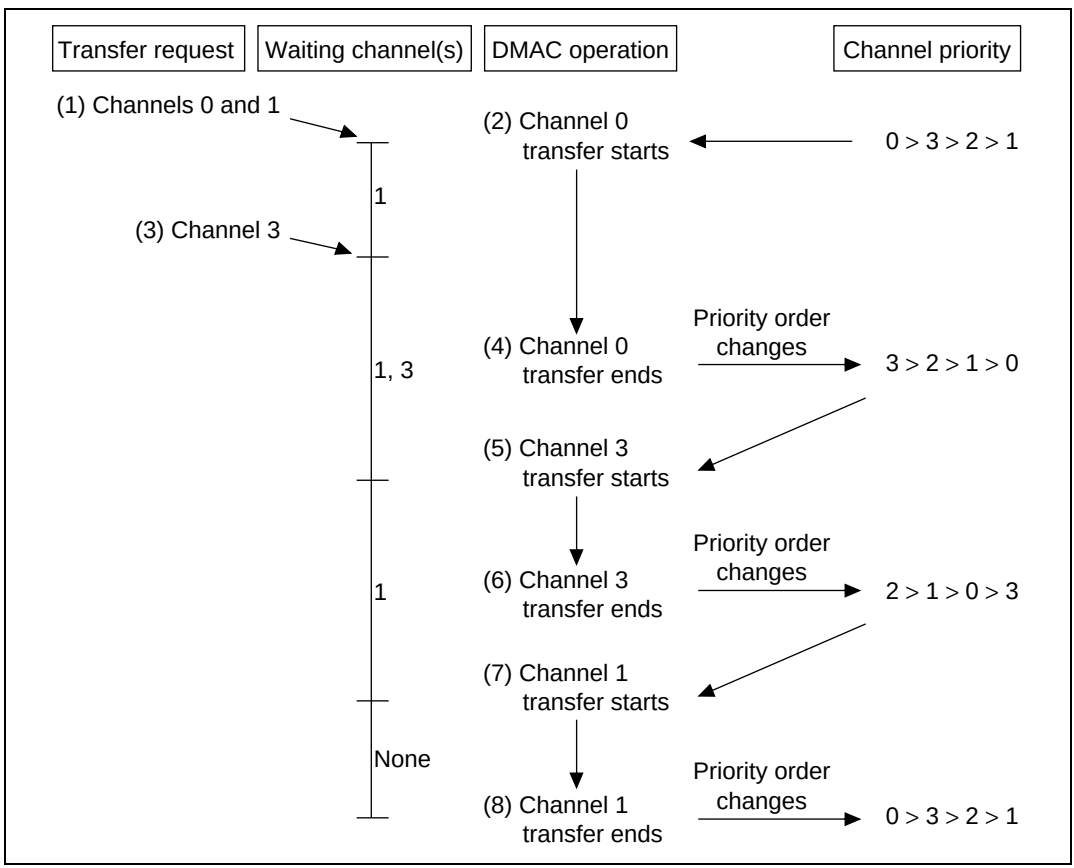


Figure 9.4 Changes in Channel Priority in Round-Robin Mode

External-Pin Round-Robin Mode: External-pin round-robin mode switches the priority levels of channel 0 and channel 1, which are the channels that can receive transfer requests from external pins $\overline{\text{DREQ0}}$ and $\overline{\text{DREQ1}}$. The priority levels are changed after each (byte or word) transfer on channel 0 or channel 1 is completed. The channel which just finished the transfer rotates to the bottom of the priority order. The priority levels of channels 2 and 3 do not change. The initial priority order after a reset is channel 3 > channel 2 > channel 1 > channel 0.

Figure 9.5 shows how the priority order changes when channel 0 and channel 1 transfers are requested simultaneously and a channel 0 transfer is requested again after both channels finish their transfers. The DMAC operates as follows:

1. Transfer requests are generated simultaneously for channels 1 and 0.
2. Channel 1 has a higher priority, so the channel 1 transfer begins first (channel 0 waits for transfer).
3. When the channel 1 transfer ends, channel 1 becomes the lowest priority.
4. The channel 0 transfer begins.
5. When the channel 0 transfer ends, channel 0 becomes the lowest priority.
6. A channel 0 transfer request occurs again.
7. The channel 0 transfer begins.
8. When the channel 0 transfer ends, the priority order does not change, because channel 0 is already the lowest priority.

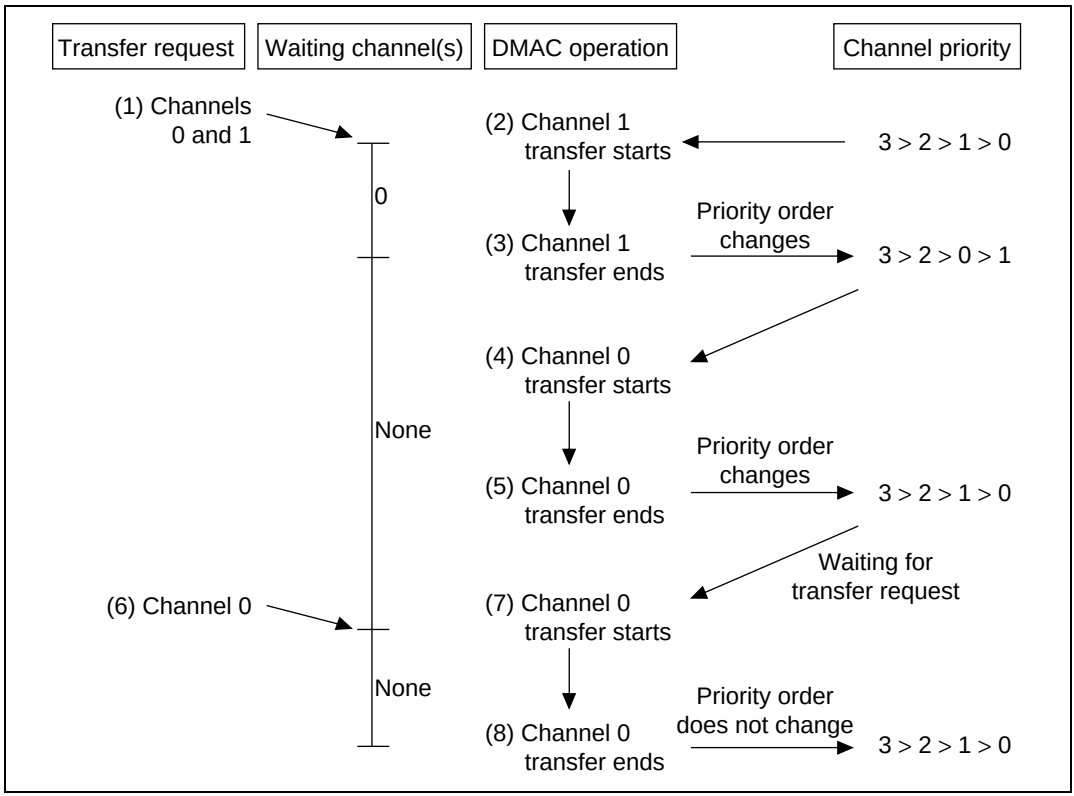


Figure 9.5 Example of Changes in Priority in External-Pin Round-Robin Mode

9.3.4 DMA Transfer Types

The DMAC supports the transfers shown in table 9.5. It can operate in single address mode or dual address mode, which are defined by how many bus cycles the DMAC takes to access the transfer source and transfer destination. The actual transfer operation timing varies with the bus mode. The DMAC has two bus modes: cycle-steal mode and burst mode.

Table 9.5 Supported DMA Transfers

	Destination				
Source	**External Device with DACK**	**External Memory**	**Memory-Mapped External Device**	**On-Chip Memory**	**On-Chip Supporting Module**
External device with DACK	Not available	Single	Single	Not available	Not available
External memory	Single	Dual	Dual	Dual	Dual
Memory-mapped external device	Single	Dual	Dual	Dual	Dual
On-chip memory	Not available	Dual	Dual	Dual	Dual
On-chip supporting module	Not available	Dual	Dual	Dual	Dual

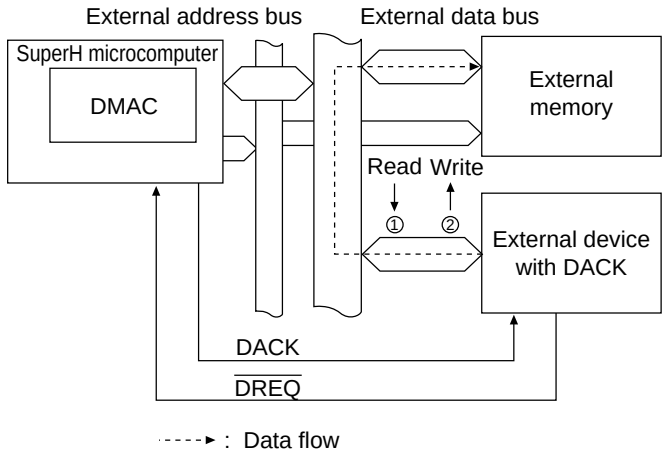
Single: Single address mode

Dual: Dual address mode

Address Modes:

- Single Address Mode

  In single address mode, both the transfer source and destination are external; one (selectable) is accessed by a DACK signal while the other is accessed by an address. In this mode, the DMAC performs the DMA transfer in 1 bus cycle by simultaneously outputting a transfer request acknowledge DACK signal to one external device to access it while outputting an address to the other end of the transfer. Figure 9.6 shows an example of a transfer between an external memory and an external device with DACK in which the external device outputs data to the data bus while that data is written in external memory in the same bus cycle.



Note: The read/write direction is decided by the RS3-RS0 bits in the CHCRn registers. If RS3-RS0 = 0010, the direction is as shown in case 1 (circled number above); if RS3-RS0 = 0011, the direction is as shown in case 2. In the Electrical Characteristics section, DACK output (read) indicates case 1, and DACK output (write) indicates case 2.

Figure 9.6 Data Flow in Single Address Mode

Two types of transfers are possible in single address mode: 1) transfers between external devices with DACK and memory-mapped external devices, and 2) transfers between external devices with DACK and external memory. The only transfer request for either of these is the external request ($\overline{\text{DREQ}}$). Figure 9.7 shows the DMA transfer timing for single address mode.

The DACK output when a transfer occurs from an external device with DACK to a memory-mapped external device is the write waveform. The DACK output when a transfer occurs from a memory-mapped external device to an external device with DACK is the read waveform. The settings of the acknowledge mode (AM) bits in the channel control registers (CHCR0, CHCR1) have no effect.

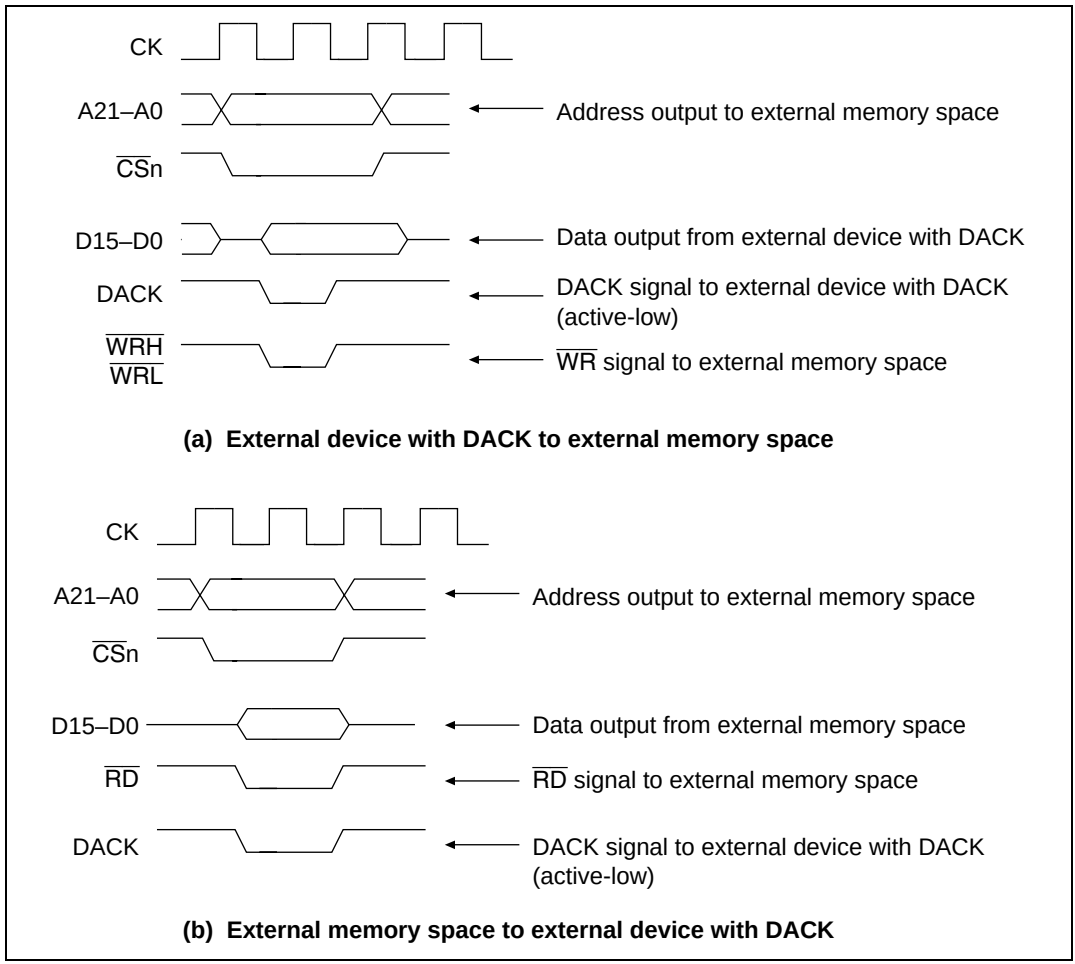


Figure 9.7 Examples of DMA Transfer Timing in Single Address Mode

- Dual Address Mode

  In dual address mode, both the transfer source and destination are accessed (selectable) by an address. The source and destination can be located externally or internally. The source is accessed in the read cycle and the destination in the write cycle, so the transfer is performed in two separate bus cycles. The transfer data is temporarily stored in the DMAC. Figure 9.8 shows an example of a transfer between two external memories in which data is read from one memory in the read cycle and written to the other memory in the following write cycle.

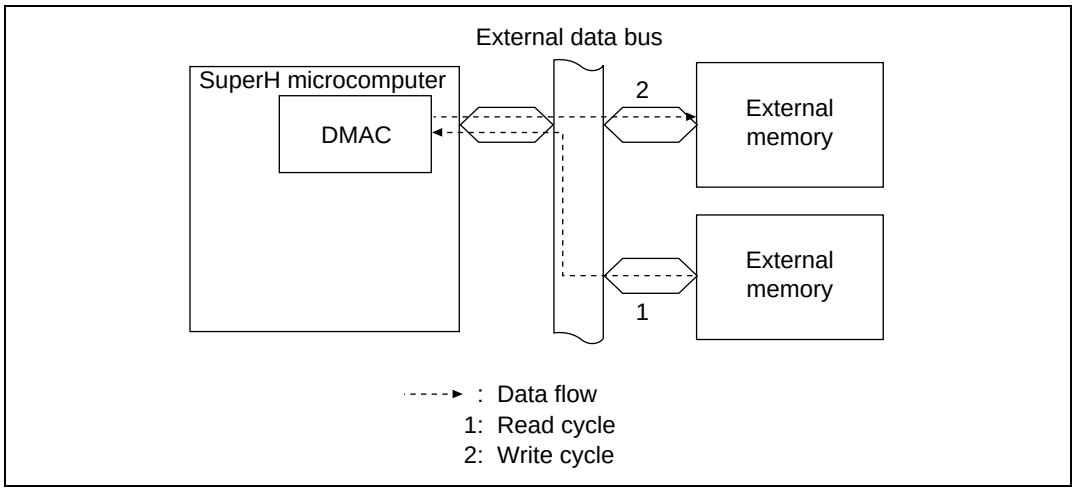


Figure 9.8 Data Flow in Dual Address Mode

In dual address mode transfers, external memory, memory-mapped external devices, on-chip memory and on-chip supporting modules can be mixed without restriction. Specifically, this enables the following transfer types:

1. Between external memory and a external memory
2. Between external memory and a memory-mapped external device
3. Between a memory-mapped external devices
4. Between external memory and on-chip memory
5. Between external memory and an on-chip supporting module (excluding the DMAC)
6. Between memory-mapped external device and on-chip memory
7. Between memory-mapped external device and an on-chip supporting module (excluding the DMAC)
8. On-chip memory to on-chip memory
9. Between on-chip memory and an on-chip supporting module (excluding the DMAC)
10. Between on-chip supporting modules (excluding the DMAC)

Transfer requests can be auto requests, external requests, or on-chip supporting module requests. When the transfer request source is either the SCI or A/D converter, however, either the data destination or source must be the SCI or A/D converter (table 9.4). In dual address mode, DACK is output in read or write cycles other than for internal memory and external supporting modules. CHCR controls the cycle in which DACK is output.

Figure 9.9 shows the DMA transfer timing in dual address mode.

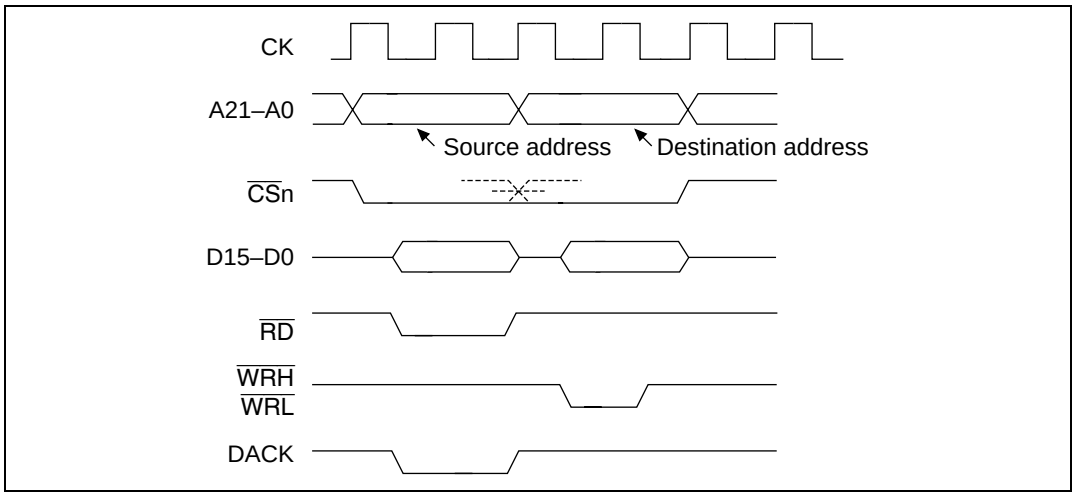


Figure 9.9 DMA Transfer Timing in Dual Address Mode (External Memory Space to External Memory Space Transfer with DACK Output in Read Cycle)

Bus Modes: There are two bus modes: cycle-steal and burst. Select the mode with the TM bits in CHCR0–CHCR3.

- Cycle-Steal Mode

  In cycle-steal mode, the bus is given to another bus master after a one-transfer-unit (word or byte) DMA transfer. When another transfer request occurs, the bus is obtained from the other bus master and a transfer is performed for one transfer unit. When that transfer ends, the bus is passed to the other bus master. This is repeated until the transfer end conditions are satisfied.

  Cycle-steal mode can be used with all categories of transfer destination, transfer source and transfer request. Figure 9.10 shows an example of DMA transfer timing in cycle-steal mode.

  Transfer conditions shown in the figure are:

  — Dual address mode

  — DREQ level detection

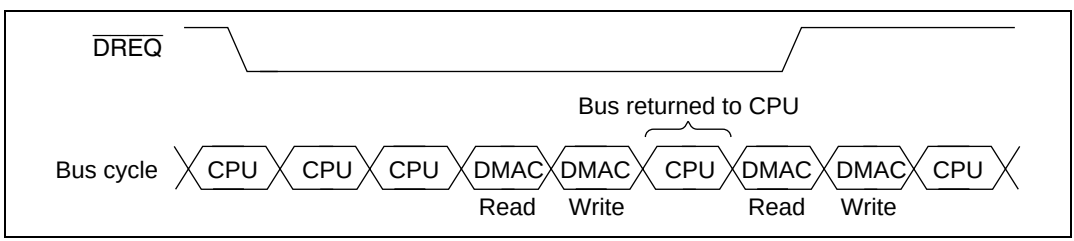


Figure 9.10 Transfer Example in Cycle-Steal Mode (Dual Address Mode, DREQ Level Detection)

- Burst Mode

  Once the bus is obtained, the transfer is performed continuously until the transfer end condition is satisfied. In external request mode with low-level detection at the $\overline{\text{DREQ}}$ pin, however, when the $\overline{\text{DREQ}}$ pin is driven high, the bus passes to the other bus master after the bus cycle of the DMAC that currently has an acknowledged request ends, even if the transfer end conditions have not been satisfied.

  Burst mode cannot be used when the serial communication interface (SCI) is the transfer request source. Figure 9.11 shows an example of DMA transfer timing in burst mode. The transfer conditions shown in the figure are:

  — Single address mode

  — $\overline{\text{DREQ}}$ level detection

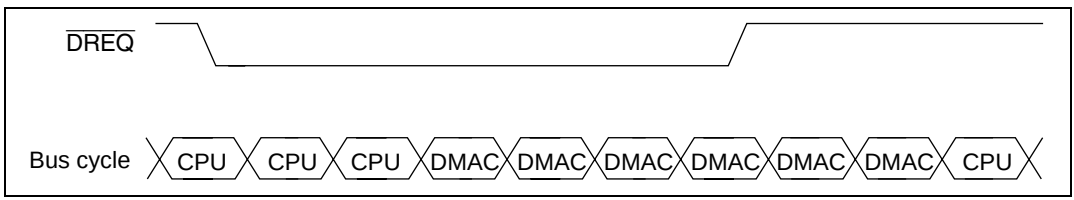


Figure 9.11 Transfer Example in Burst Mode (Single Address Mode, $\overline{\text{DREQ}}$ Level Detection)

Relationship between Request Modes and Bus Modes by DMA Transfer Category: Table 9.6 shows the relationship between request modes and bus modes by DMA transfer category.

Table 9.6 Relationship of Request Modes and Bus Modes by DMA Transfer Category

Address Mode	Transfer Category	Request Mode	Bus Mode	Transfer Size (bits)	Usable Channels
Single	External device with DACK and external memory	External	B/C	8/16	0,1
	External device with DACK and memory-mapped external device	External	B/C	8/16	0, 1
Dual	External memory and external memory	All*1	B/C	8/16	0–3*5
	External memory and memory-mapped external device	All*1	B/C	8/16	0–3*5
	Memory-mapped external device and memory-mapped external device	All*1	B/C	8/16	0–3*5
	External memory and on-chip memory	All*1	B/C	8/16	0–3*5
	External memory and on-chip supporting module	All*2	B/C*3	8/16*4	0–3*5
	Memory-mapped external device and on-chip memory	All*1	B/C	8/16	0–3*5
	Memory-mapped external device and on-chip supporting module	All*2	B/C*3	8/16*4	0–3*5
	On-chip memory and on-chip memory	All*1	B/C	8/16	0–3*5
	On-chip memory and on-chip supporting module	All*2	B/C*3	8/16*4	0–3*5
	On-chip supporting module and on-chip supporting module	All*2	B/C*3	8/16*4	0–3*5

B: Burst, C: Cycle steal

Notes: 1. External requests, auto requests and on-chip supporting module requests are all available. For on-chip supporting module requests, however, SCI and A/D converter cannot be specified as the transfer request source.

2. External requests, auto requests and on-chip supporting module requests are all available. When the SCI or A/D converter is also the transfer request source, however, the transfer destination or transfer source must be the SCI or A/D converter, respectively.

3. If the transfer request source is the SCI, cycle-steal only.

4. The access size permitted when the transfer destination or source is an on-chip supporting module register.

5. If the transfer request is an external request, channels 0 and 1 only.

Bus Mode and Channel Priority Order: When a given channel (1) is transferring in burst mode and there is a transfer request to a channel (2) with a higher priority, the transfer of the channel with higher priority (2) will begin immediately. When channel 2 is also operating in burst mode, the channel 1 transfer will continue when the channel 2 transfer has completely finished. When channel 2 is in cycle-steal mode, channel 1 will begin operating again after channel 2 completes the transfer of one transfer unit, but the bus will then switch between the two in the order channel 1, channel 2, channel 1, channel 2. Since channel 1 is in burst mode, it will not give the bus to the CPU. This example is illustrated in figure 9.12.

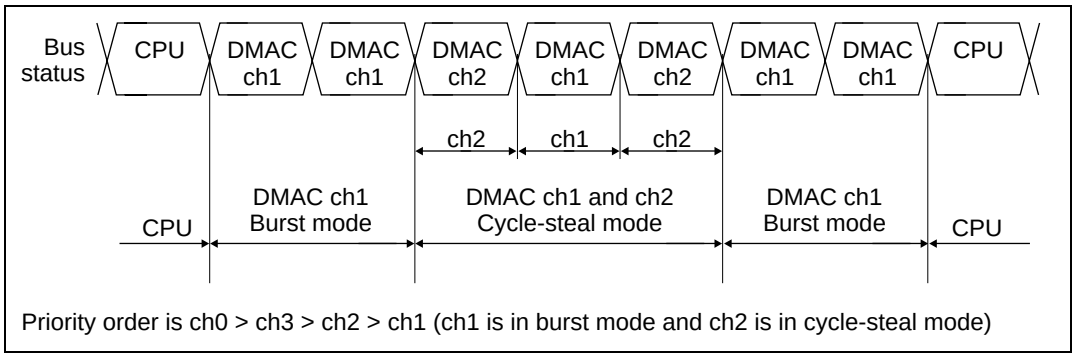


Figure 9.12 Bus Handling when Multiple Channels are Operating

9.3.5 Number of Bus Cycle States and $\overline{\text{DREQ}}$ Pin Sample Timing

Number of States in Bus Cycle: The number of states in the bus cycle when the DMAC is the bus master is controlled by the bus state controller just as it is when the CPU is the bus master. The bus cycle in dual address mode is controlled by wait state control register 1 (WCR1) while the single address mode bus cycle is controlled by wait state control register 2 (WCR2). For details, see section 8.9, Wait State Control.

$\overline{\text{DREQ}}$ Pin Sampling Timing: Normally, when $\overline{\text{DREQ}}$ input is detected immediately prior to the rise edge of the clock pulse (CK) in external request mode, a DMAC bus cycle will be generated and the DMA transfer performed two states later at the earliest. The sampling timing after $\overline{\text{DREQ}}$ input detection differs by bus mode, address mode, and method of $\overline{\text{DREQ}}$ input detection.

- $\overline{\text{DREQ}}$ pin sampling timing in cycle-steal mode

  In cycle-steal mode, the sampling timing is the same regardless of whether $\overline{\text{DREQ}}$ is detected by edge or level. With edge detection, however, once the signal is sampled it will not be sampled again until the next edge detection. Once $\overline{\text{DREQ}}$ input is detected, the next sampling is not performed until the first state, among those DMAC bus cycles thereby produced, in which a DACK signal is output (including the detection state itself). The next sampling occurs immediately prior to the rising edge of the clock pulse (CK) of the third state after the bus cycle previous to the bus cycle in which the DACK signal is output.

  Figures 9.13 to 9.22 show the sampling timing of the $\overline{\text{DREQ}}$ pin in cycle-steal mode for each bus cycle. When no $\overline{\text{DREQ}}$ input is detected at the sampling after the aforementioned $\overline{\text{DREQ}}$ detection, the next sampling occurs in the next state in which a DACK signal is output. If no $\overline{\text{DREQ}}$ input is detected at this time, sampling occurs at every subsequent state.

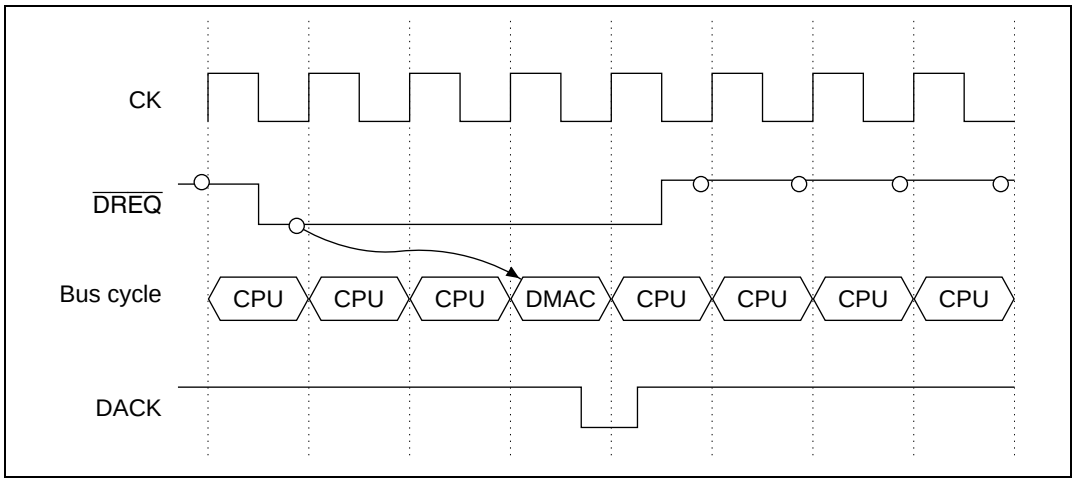
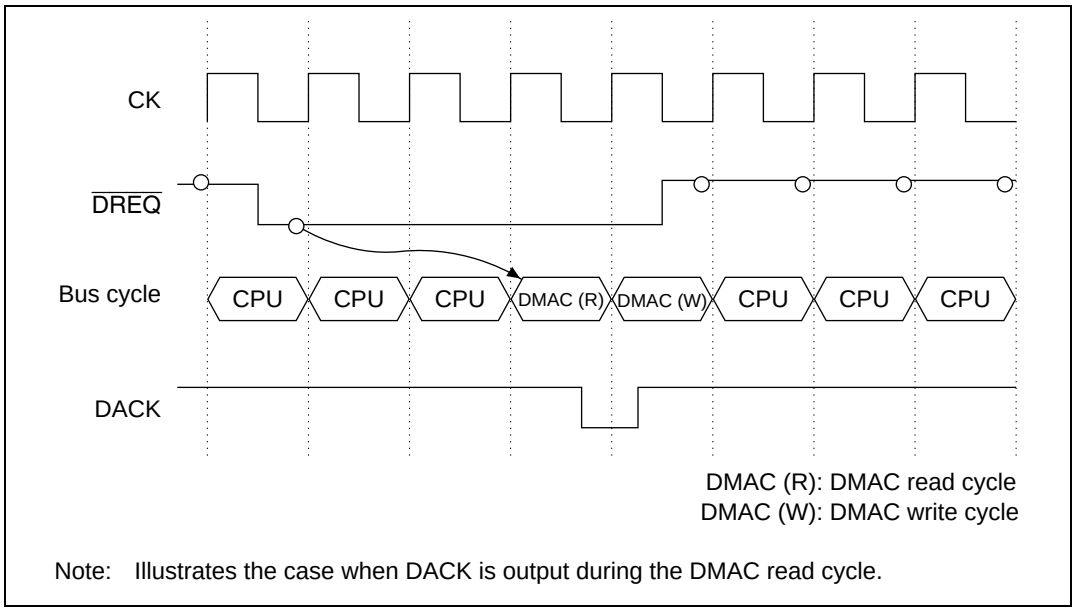


Figure 9.13 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Single Address Mode, Bus Cycle = 1 State)



Note: Illustrates the case when DACK is output during the DMAC read cycle.

Figure 9.14 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Dual Address Mode, Bus Cycle = 1 State)

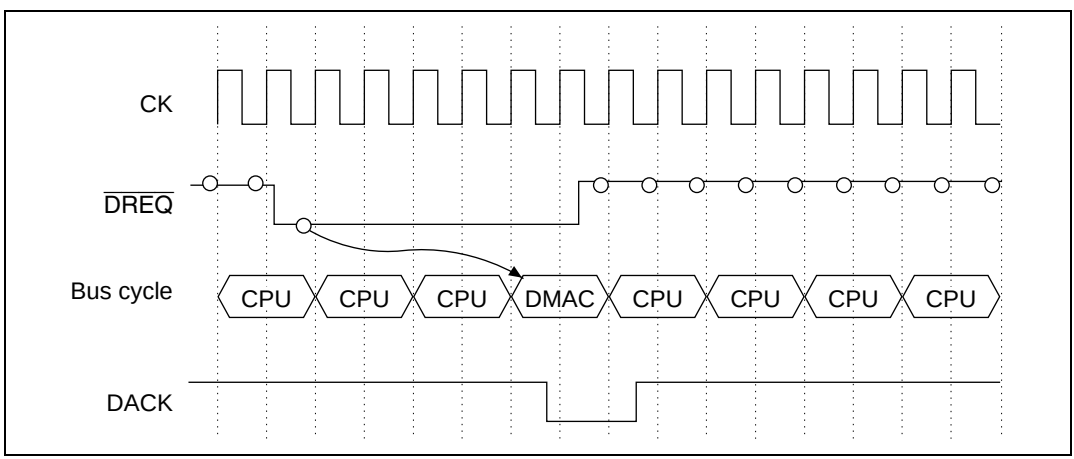
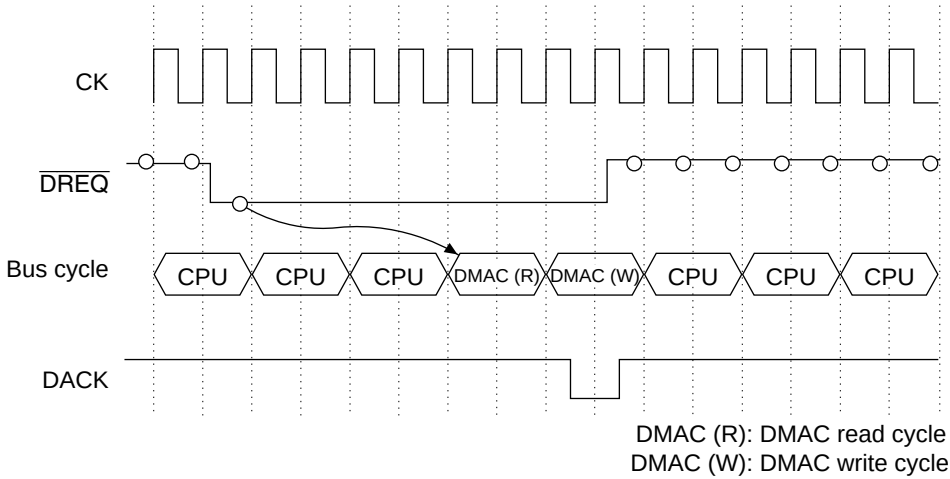
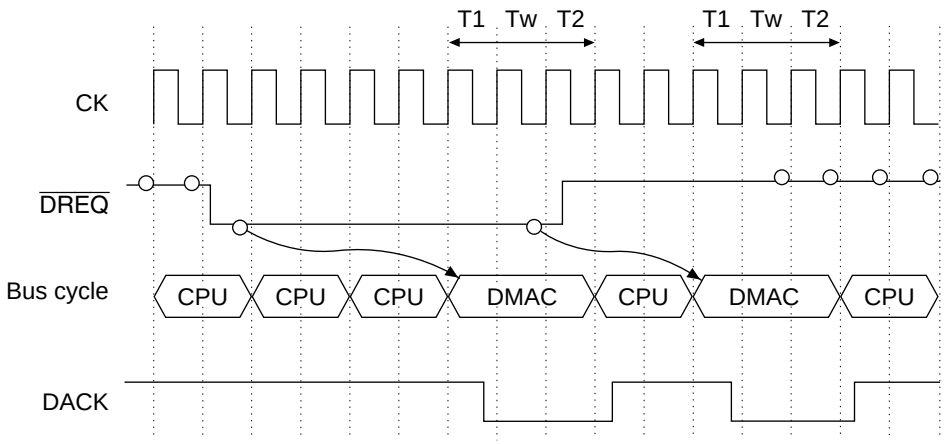


Figure 9.15 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Single Address Mode, Bus Cycle = 2 States)



Note: Illustrates the case when DACK is output during the DMAC write cycle.

Figure 9.16 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Dual Address Mode, Bus Cycle = 2 States)



Note: When $\overline{\text{DREQ}}$ is negated at the third state of the DMAC cycle, the next DMA transfer will be executed because the sampling is performed at the second state of the DMAC cycle.

Figure 9.17 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Single Address Mode, Bus Cycle = 2 States + 1 Wait State)

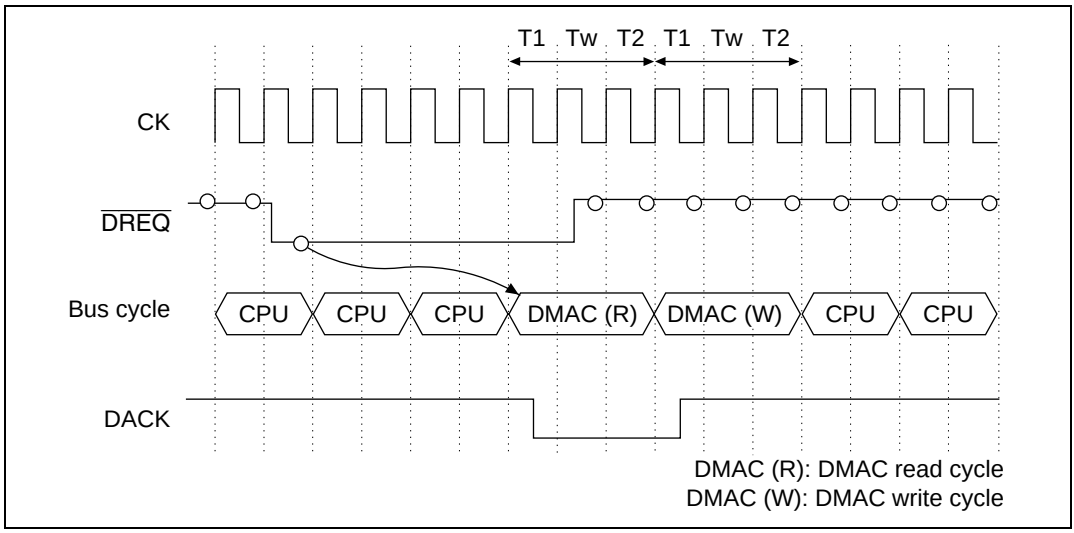
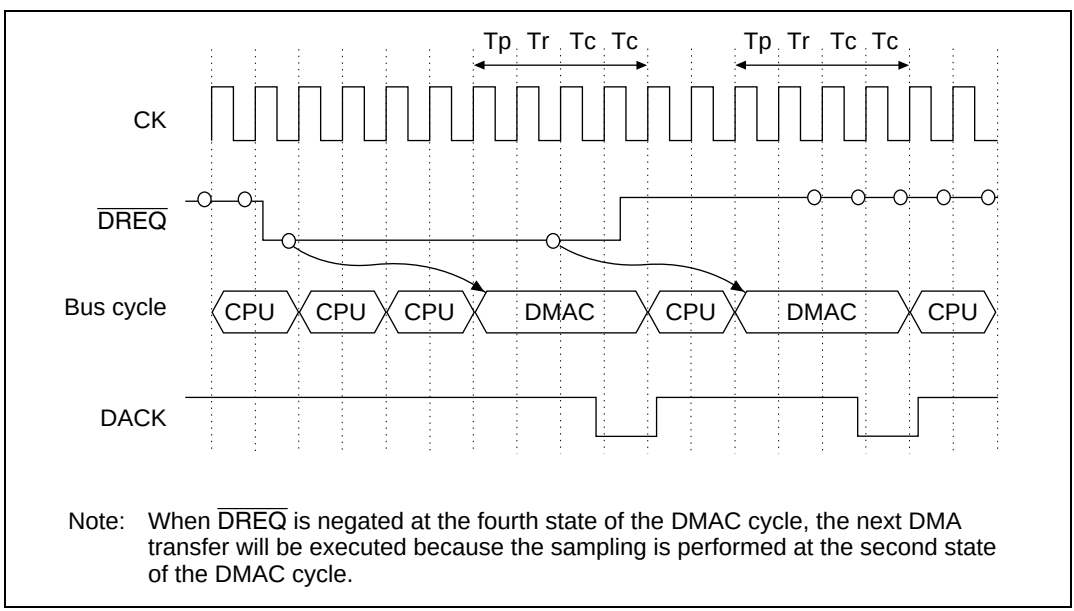
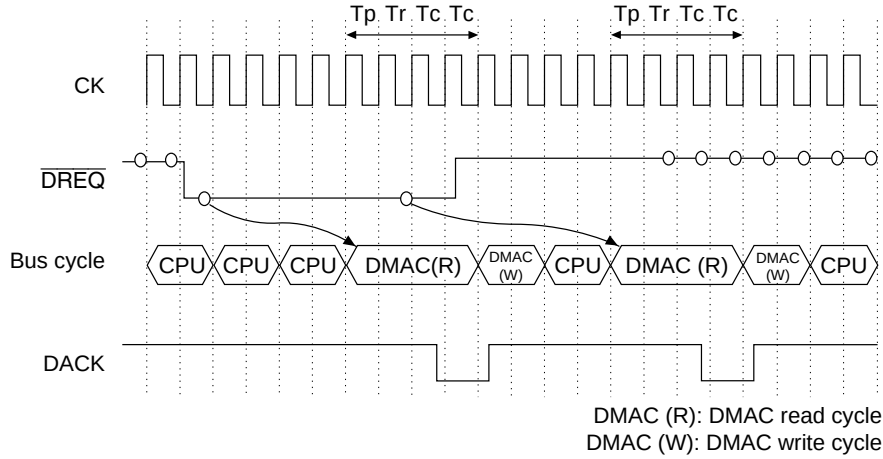


Figure 9.18 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Dual Address Mode, Bus Cycle = 2 States + 1 Wait State)



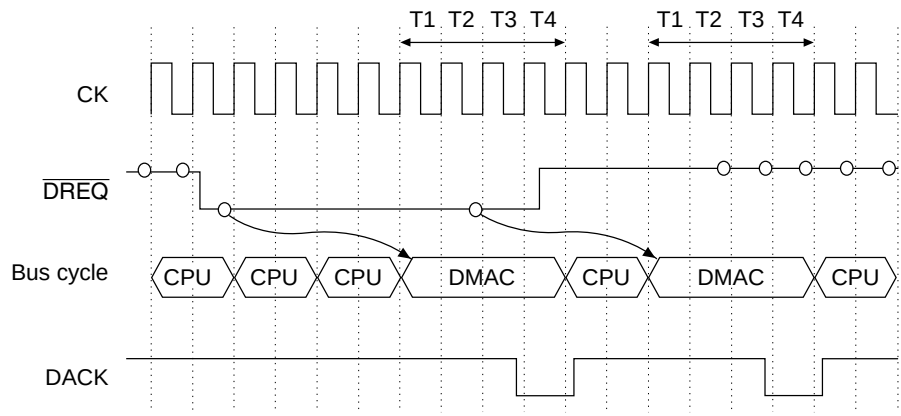
Note: When $\overline{\text{DREQ}}$ is negated at the fourth state of the DMAC cycle, the next DMA transfer will be executed because the sampling is performed at the second state of the DMAC cycle.

Figure 9.19 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Single Address Mode, Bus Cycle = DRAM Bus Cycle (Long Pitch Normal Mode))



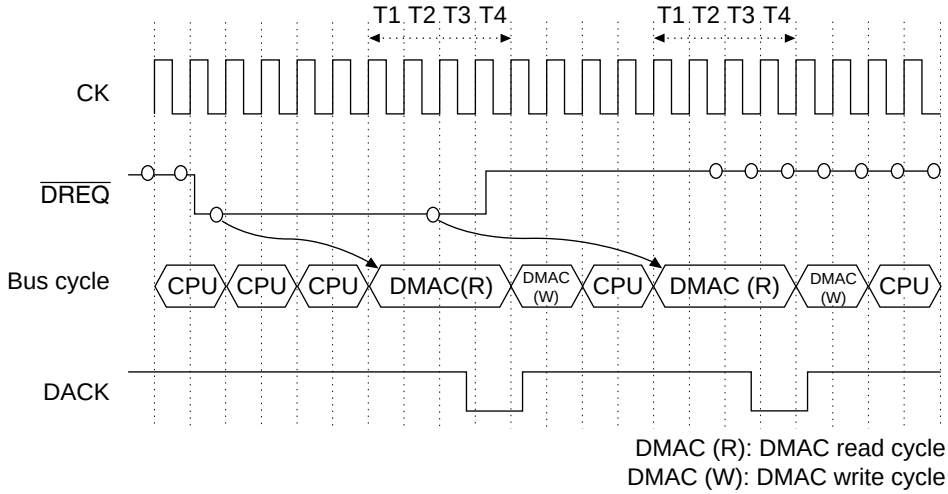
Note: When $\overline{\text{DREQ}}$ is negated at the fourth state of the DMAC cycle, the next DMA transfer will be executed because the sampling is performed at the second state of the DMAC cycle.

Figure 9.20 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Dual Address Mode, Bus Cycle = DRAM Bus Cycle (Long Pitch Normal Mode))



Note: When $\overline{\text{DREQ}}$ is negated at the fourth state of the DMAC cycle, the next DMA transfer will be executed because the sampling is performed at the second state of the DMAC cycle.

Figure 9.21 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Single Address Mode, Bus Cycle = Address/Data Multiplex I/O Bus Cycle)



Note: When $\overline{\text{DREQ}}$ is negated at the fourth state of the DMAC cycle, the next DMA transfer will be executed because the sampling is performed at the second state of the DMAC cycle.

Figure 9.22 $\overline{\text{DREQ}}$ Sampling Timing in Cycle-Steal Mode (Output with $\overline{\text{DREQ}}$ Level Detection and DACK Active-Low) (Dual Address Mode, Bus Cycle = Address/Data Multiplex I/O Bus Cycle)

- $\overline{\text{DREQ}}$ pin sampling timing in burst mode

  In burst mode, the sampling timing differs depending on whether $\overline{\text{DREQ}}$ is detected by edge or level.

  When $\overline{\text{DREQ}}$ input is being detected by edge, once the falling edge of the $\overline{\text{DREQ}}$ signal is detected, the DMA transfer continues until the transfer end conditions are satisfied, regardless of the status of the $\overline{\text{DREQ}}$ pin. No sampling happens during this time. After the transfer ends, sampling occurs every state until the TE bit of CHCR is cleared.

  When $\overline{\text{DREQ}}$ input is being detected by level, once the $\overline{\text{DREQ}}$ input is detected, subsequent sampling is performed at the end of every CPU or DMAC bus cycle in single address mode. In dual address mode, subsequent sampling is performed at the start of every DMAC read cycle. In both single address mode and dual address mode, if no $\overline{\text{DREQ}}$ input is detected at this time, subsequent sampling occurs at every state.

  Figures 9.23 and 9.24 show the $\overline{\text{DREQ}}$ pin sampling timing in burst mode when $\overline{\text{DREQ}}$ input is detected by low level.

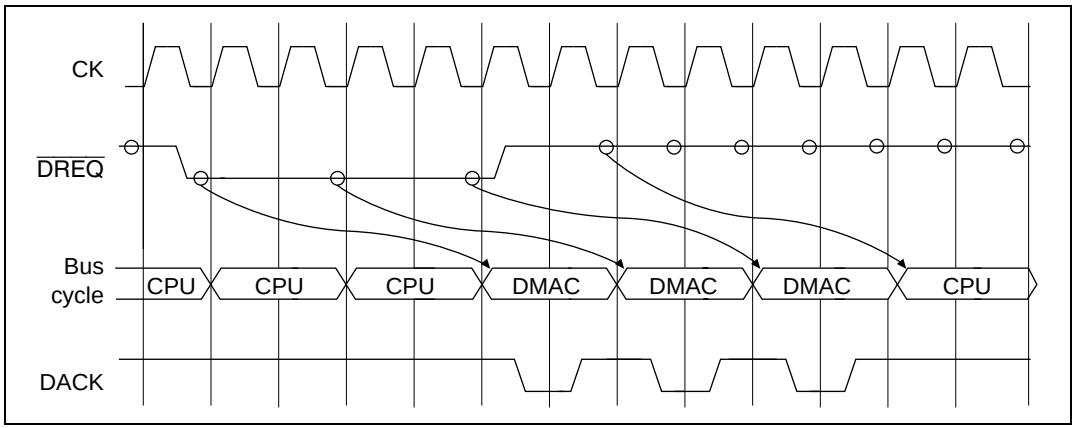


Figure 9.23 $\overline{\text{DREQ}}$ Pin Sampling Timing in Burst Mode (Single Address $\overline{\text{DREQ}}$ Level Detection, DACK Active-Low, 1 Bus Cycle = 2 States)

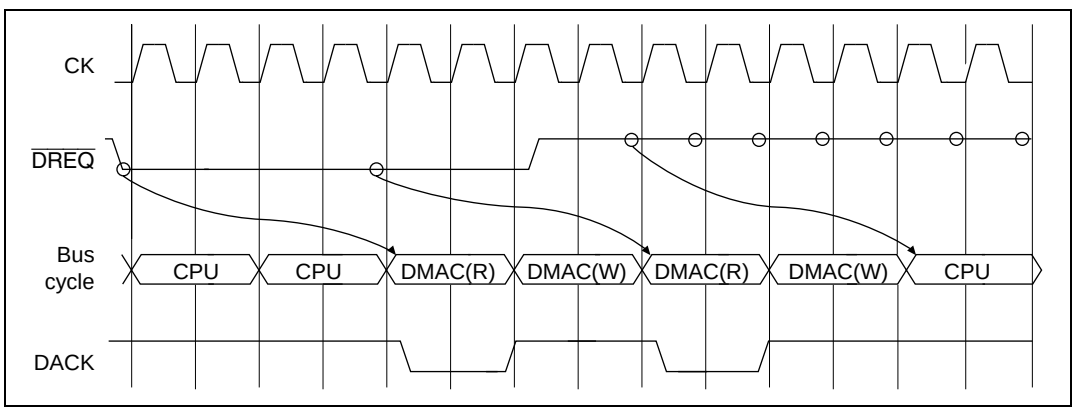


Figure 9.24 $\overline{\text{DREQ}}$ Pin Sampling Timing in Burst Mode (Dual Address $\overline{\text{DREQ}}$ Level Detection, DACK Active-Low, DACK Output in Read Cycle, 1 Bus Cycle = 2 States)

9.3.6 DMA Transfer Ending Conditions

The DMA transfer ending conditions differ for individual channel ending and ending on all channels together.

Individual Channel Ending Conditions: There are two ending conditions. A transfer ends when the value of the channel's DMA transfer count register (TCR) is 0, or when the DE bit in the channel's CHCR is cleared to 0.

- When TCR is 0: When the TCR value becomes 0 and the corresponding channel's DMA transfer ends, the transfer end flag bit (TE) is set in CHCR. If the IE (interrupt enable) bit has been set, a DMAC interrupt (DEI) request is sent to the CPU.
- When DE in CHCR is 0: Software can halt a DMA transfer by clearing the DE bit in the channel's CHCR. The TE bit is not set when this happens.

Conditions for Ending All Channels Simultaneously: Transfers on all channels end when 1) the NMIF (NMI flag) bit or AE (address error flag) bit is set to 1 in DMAOR, or 2) when the DME bit in DMAOR is cleared to 0.

- Transfers ending when the NMIF or AE bit is set to 1 in DMAOR: When an NMI interrupt or DMAC address error occurs, the NMIF or AE bit is set to 1 in DMAOR and all channels stop their transfers. SAR, DAR, and TCR are all updated by the transfer immediately preceding the halt. The TE bit is not set. To resume transfer after NMI interrupt exception handling or address error exception handling, clear the appropriate flag bit to 0. When a channel's DE bit is then set to 1, the transfer on that channel will restart. To avoid restarting transfer on a particular channel, keep its DE bit cleared to 0. In dual address mode, DMA transfer will be halted after the completion of the write cycle that follows the initial read cycle in which the address error occurs. SAR, DAR, and TCR are updated by the final transfer.
- Transfers ending when DME is cleared to 0 in DMAOR: Clearing the DME bit to 0 in DMAOR forcibly aborts transfer on all channels at the end of the current cycle. The TE bit is not set.

9.4 Examples of Use

9.4.1 DMA Transfer between On-Chip RAM and Memory-Mapped External Device

In the following example, data is transferred from on-chip RAM to a memory-mapped external device with an input capture A/compare match A interrupt (IMIA0) from channel 0 of the 16-bit integrated timer pulse unit (ITU) as the transfer request signal. The transfer is performed by DMAC channel 3. Table 9.7 shows the transfer conditions and register values.

Table 9.7 Transfer Conditions and Register Settings for Transfer Between On-Chip RAM and Memory-Mapped External Device

Transfer Conditions	Register	Setting
Transfer source: on-chip RAM	SAR3	H'FFFFE00
Transfer destination: memory-mapped external device	DAR3	Destination address
Number of transfers: 8	TCR3	H'0008
Transfer destination address: fixed	CHCR3	H'1805
Transfer source address: incremented		
Transfer request source (transfer request signal): ITU channel 0 (IMIA0)		
Bus mode: cycle-steal		
Transfer unit: byte		
DEI interrupt request generated at end of transfer (channel 3 enabled for transfer)		
Channel priority order: fixed (0 > 3 > 2 > 1) (all channels enabled for transfer)	DMAOR	H'0001

9.4.2 Example of DMA Transfer between On-Chip SCI and External Memory

In this example, receive data of on-chip serial communication interface (SCI) channel 0 is transferred to external memory using DMAC channel 3. Table 9.8 shows the transfer conditions and register settings.

Table 9.8 Transfer Conditions and Register Settings for Transfer between On-Chip SCI and External Memory

Transfer Conditions	Register	Setting
Transfer source: RDR0 of on-chip SCI0	SAR3	H'FFFFEC5
Transfer destination: external memory	DAR3	Destination address
Number of transfers: 64	TCR3	H'0040
Transfer destination address: incremented	CHCR3	H'4405
Transfer source address: fixed		
Transfer request source (transfer request signal): SCI0 (RXI0)		
Bus mode: cycle-steal		
Transfer unit: byte		
DEI interrupt request generated at end of transfer (channel 3 enabled for transfer)		
Channel priority order: fixed (0 > 3 > 2 > 1) (all channels enabled for transfer)	DMAOR	H'0001

9.4.3 Example of DMA Transfer Between On-Chip A/D Converter and External Memory

In this example, the results of an A/D conversion by the on-chip A/D converter are transferred to external memory using DMAC channel 3. Input from channel 0 (AN0) is A/D-converted using scan mode. Table 9.9 shows the transfer conditions and register settings.

Table 9.9 Transfer Conditions and Register Settings for Transfer Between On-Chip A/D Converter and External Memory

Transfer Conditions	Register	Setting
Transfer source: ADDRA of on-chip A/D converter	SAR3	H'FFFFEE0 (ADDRAH register address)
Transfer destination: external memory	DAR3	Destination address
Number of transfers: 16	TCR3	H'0010
Transfer destination address: incremented	CHCR3	H'4D0D
Transfer source address: fixed		
Transfer request source (transfer request signal): A/D converter (ADI)		
Bus mode: cycle-steal		
Transfer unit: word		
DEI interrupt request generated at end of transfer (channel 3 enabled for transfer)		
Channel priority order: fixed (0 > 3 > 2 > 1) (all channels enabled for transfer)	DMAOR	H'0001

9.5 Usage Notes

1. All registers other than the DMA operation register (DMAOR) and DMA channel control registers 0–3 (CHCR0–CHCR3) should be accessed in word or longword units.
2. Before rewriting the RS0–RS3 bits in CHCR0–CHCR3, first clear the DE bit to 0 (when rewriting CHCR with a byte access, be sure to set the DE bit to 0 in advance).
3. Even when an NMI interrupt is input when the DMAC is not operating, the NMIF bit in DMAOR will be set.
4. Interrupt during DMAC transfer

   When an interrupt occurs during DMAC transfer, the following operation takes place.

   a. When an NMI interrupt is input, the DMAC stops operation and returns the bus to the CPU. The CPU then executes the interrupt handling.

   b. When an interrupt other than an NMI occurs

      - When the DMAC is in burst mode

        The DMAC does not return the bus to the CPU in burst mode. Therefore, even when an interrupt is requested in DMAC operation, the CPU cannot acquire the bus with, the result that interrupt handling is not executed. When the DMAC completes the transfer and the CPU acquires the bus, the CPU executes interrupt handling if the interrupt requested during DMAC transfer is not cleared.*

        Note: * Clear conditions for an interrupt request:

        —When an interrupt is requested from an on-chip supporting module, and the interrupt source flag is cleared

        —When an interrupt is requested by $\overline{\text{IRQ}}$ (edge detection), and the CPU begins interrupt handling for the $\overline{\text{IRQ}}$ request source

        —When an interrupt is requested by $\overline{\text{IRQ}}$ (level detection), and the $\overline{\text{IRQ}}$ interrupt request signal returns to the high level

      - When the DMAC is in cycle-steal mode

        The DMAC returns the bus to the CPU every time the DMAC completes a transfer unit in cycle-steal mode. Therefore, the CPU executes the requested interrupt handling when it acquires the bus.

5. The CPU and DMAC leave the bus released and the operation of the chip is stopped when the following conditions are satisfied
   - The warp bit (WARP) in the bus control register (BCR) of the bus controller (BSC) is set
   - The DMAC is in cycle-steal transfer mode
   - The CPU accesses (reads/writes) the on-chip I/O space

   Remedy: Clear the warp bit in BCR to 0 to set normal mode.

6. Notes on use of the SLEEP instruction
   a. Operation contents

      When a DMAC bus cycle is entered immediately after executing a SLEEP instruction, there are cases when DMA transfer is not carried out correctly.

   b. Remedy
      - Stop operation (for example, by clearing the DMA enable bit (DE) in the DMA channel control register (CHCRn)) before entering sleep mode.
      - To use the DMAC when in sleep mode, first exit sleep mode by means of an interrupt.

   In cases when the CPU is not carrying out any other processing but is waiting for the DMAC to end its transfer during DMAC operation, do not use the SLEEP instruction, but use the transfer end flag bit (TE) in the channel DMA control register and a polling software loop.
7. Sampling of $\overline{\text{DREQ}}$

   If $\overline{\text{DREQ}}$ is set to level detection in DMA cycle-steal mode, sampling of $\overline{\text{DREQ}}$ may take place before DACK is output. Note that some system configurations involve unnecessary DMA transfers.

   Operation:

   As shown in Figure 9.25, sampling of $\overline{\text{DREQ}}$ is carried out immediately before the rising edge of the third-state clock (CK) after completion of the bus cycle preceding the DMA bus cycle where DACK is output.

   If DACK is output after the third state of the DMA bus cycle, sampling of $\overline{\text{DREQ}}$ must be carried out before DACK is output.

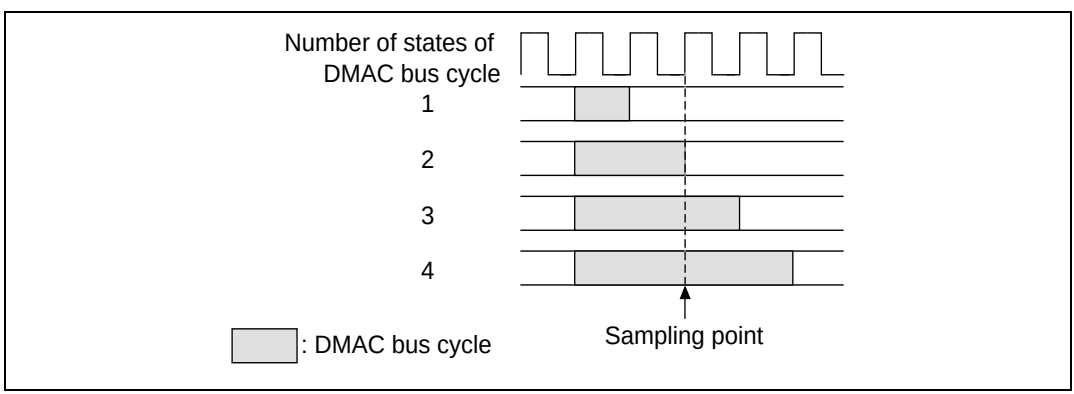


Figure 9.25 $\overline{\text{DREQ}}$ Sampling Points

Especially, if, as shown in figure 9.26, the DMA bus cycle is a full access to DRAM or if a refresh request is generated, sampling of $\overline{\text{DREQ}}$ takes place before DACK is output as mentioned above. This phenomenon is found when one of the following transfers is made with $\overline{\text{DREQ}}$ set to level detection in DMA cycle-steal mode, in a system which employs DRAM (refresh enabled).

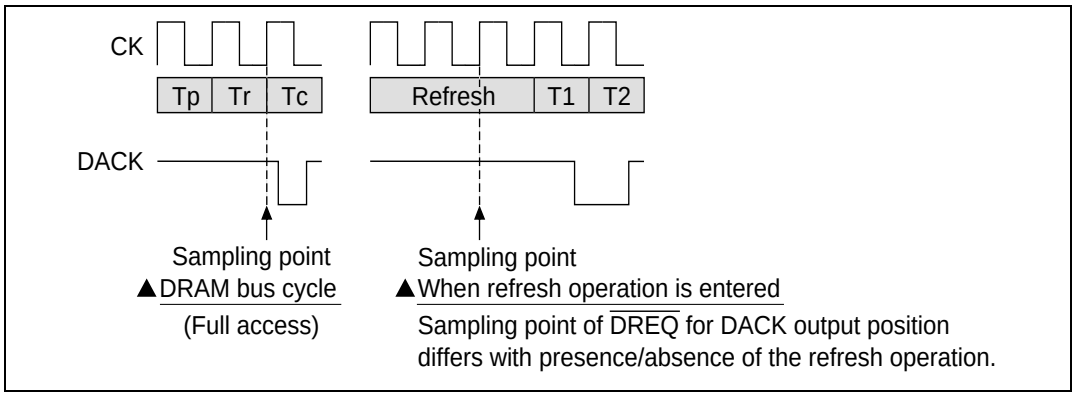


Figure 9.26 Example of $\overline{\text{DREQ}}$ Sampling before Output of DACK

- Transfer from a device with DACK to memory in single address mode (not restricted to DRAM)
- Transfer from DRAM to a device with DACK in single address mode
- Output at DACK write in dual address mode
- Output at DACK read in dual address mode and DMA transfer using DRAM as the source

Remedy:

To prevent unnecessary DMA transfers, configure the system so that $\overline{\text{DREQ}}$ is edge-detected and the edge corresponding to the next transfer request occurs after DACK output.

8. When the following operations are performed in the order shown when the pin to which $\overline{\text{DREQ}}$ input is assigned is designated as a general input pin by the pin function controller (PFC) and inputs a low-level signal, the $\overline{\text{DREQ}}$ falling edge is detected, and a DMA transfer request accepted, immediately after the setting in (b) is performed:
   a. A channel control register (CHCRn) setting is made so that an interrupt is detected at the falling edge of $\overline{\text{DREQ}}$.
   b. The function of the pin to which $\overline{\text{DREQ}}$ input is assigned is switched from general input to $\overline{\text{DREQ}}$ input by a pin function controller (PFC) setting.

   Therefore, when switching the pin function from general input pin to $\overline{\text{DREQ}}$ input, the pin function controller (PFC) setting should be changed to $\overline{\text{DREQ}}$ input while the pin to which $\overline{\text{DREQ}}$ input is assigned is high.

Section 10 16-Bit Integrated Timer Pulse Unit (ITU)

10.1 Overview

The SuperH microcomputer has an on-chip 16-bit integrated timer pulse unit (ITU) with five 16-bit timer channels.

10.1.1 Features

ITU features are listed below:

- Can process a maximum of twelve different pulse outputs and ten different pulse inputs.
- Has ten general registers (GR), two per channel, that can be set to function independently as output compare or input capture registers.
- Selection of eight counter input clock sources for all channels
  - Internal clock: ϕ, $\phi/2$, $\phi/4$, $\phi/8$,
  - External clock: TCLKA, TCLKB, TCLKC, TCLKD
- All channels can be set for the following operating modes:
  - Compare match waveform output: 0 output/1 output/selectable toggle output (0 output/1 output for channel 2)
  - Input capture function: Selectable rising edge, falling edge, or both rising and falling edges
  - Counter clearing function: Counters can be cleared by a compare match or input capture.
  - Synchronizing mode: Two or more timer counters (TCNT) can be written to simultaneously. Two or more timer counters can be simultaneously cleared by a compare match or input capture. Counter synchronization functions enable synchronized input/output.
  - PWM mode: PWM output can be provided with any duty cycle. When combined with the counter synchronizing function, enables up to five-phase PWM output.
- Channel 2 can be set to phase counting mode: Two-phase encoder output can be counted automatically.
- Channels 3 and 4 can be set in the following modes:
  - Reset-synchronized PWM mode: By combining channels 3 and 4, 3-phase PWM output is possible with positive and negative waveforms .
  - Complementary PWM mode: By combining channels 3 and 4, 3-phase PWM output is possible with non-overlapping positive and negative waveforms.
- Buffer operation: Input capture registers can be double-buffered. Output compare registers can be updated automatically.

- High-speed access via internal 16-bit bus: The TCNT, GR, and buffer register (BR) 16-bit registers can be accessed at high speed via a 16-bit bus.
- Fifteen interrupt sources: Ten compare match/input capture interrupts (2 sources per channel) and five overflow interrupts are vectored independently for a total of 15 sources.
- Can activate DMAC: The compare match/input capture interrupts of channels 0–3 can start the DMAC (one for each of four channels).
- Output trigger can be generated for the programmable timing pattern controller (TPC): The compare match/input capture signals of channel 0–3 can be used as output triggers for the TPC.

Table 10.1 summarizes the ITU functions.

Table 10.1 ITU Functions

Item		Channel 0	Channel 1	Channel 2	Channel 3	Channel 4
Counter clocks		Internal: φ, φ/2, φ/4, φ/8 External: Independently selectable from TCLKA, TCLKB, TCLKC, and TCLKD				
General registers (output compare/ input capture dual registers)		GRA0, GRB0	GRA1, GRB1	GRA2, GRB2	GRA3, GRB3	GRA4, GRB4
Buffer registers		No	No	No	BRA3, BRB3	BRA4, BRB4
Input/output pins		TIOCA0, TIOCB0	TIOCA1, TIOCB1	TIOCA2, TIOCB2	TIOCA3, TIOCB3	TIOCA4, TIOCB4
Output pins		No	No	No	No	TOCXA4, TOCXB4
Counter clear function (compare match or input capture)		GRA0/GRB0	GRA1/GRB1	GRA2/GRB2	GRA3/GRB3	GRA4/GRB4
Compare match output	0	Yes	Yes	Yes	Yes	Yes
	1	Yes	Yes	Yes	Yes	Yes
	Toggle output	Yes	Yes	No	Yes	Yes
Input capture function		Yes	Yes	Yes	Yes	Yes
Synchronization		Yes	Yes	Yes	Yes	Yes
PWM mode		Yes	Yes	Yes	Yes	Yes
Reset-synchronized PWM mode		No	No	No	Yes	Yes
Complementary PWM mode		No	No	No	Yes	Yes
Phase counting mode		No	No	Yes	No	No
Buffer operation		No	No	No	Yes	Yes
DMAC activation		GRA0 compare match or input capture	GRA1 compare match or input capture	GRA2 compare match or input capture	GRA3 compare match or input capture	No
Interrupt sources (three)		• Compare match/input capture A0 • Compare match/input capture B0 • Overflow	• Compare match/input capture A1 • Compare match/input capture B1 • Overflow	• Compare match/input capture A2 • Compare match/input capture B2 • Overflow	• Compare match/input capture A3 • Compare match/input capture B3 • Overflow	• Compare match/input capture A4 • Compare match/input capture B4 • Overflow

10.1.2 Block Diagram

ITU Block Diagram (Overall Diagram): Figure 10.1 shows a block diagram of the ITU.

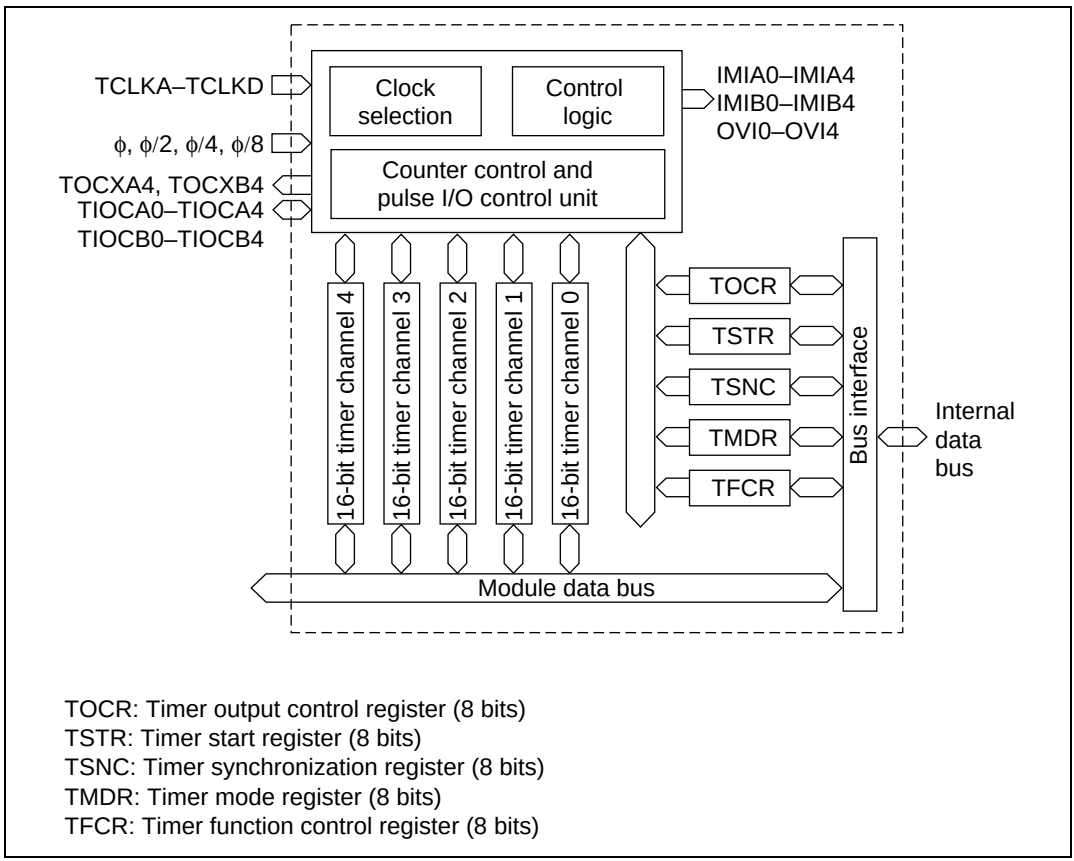
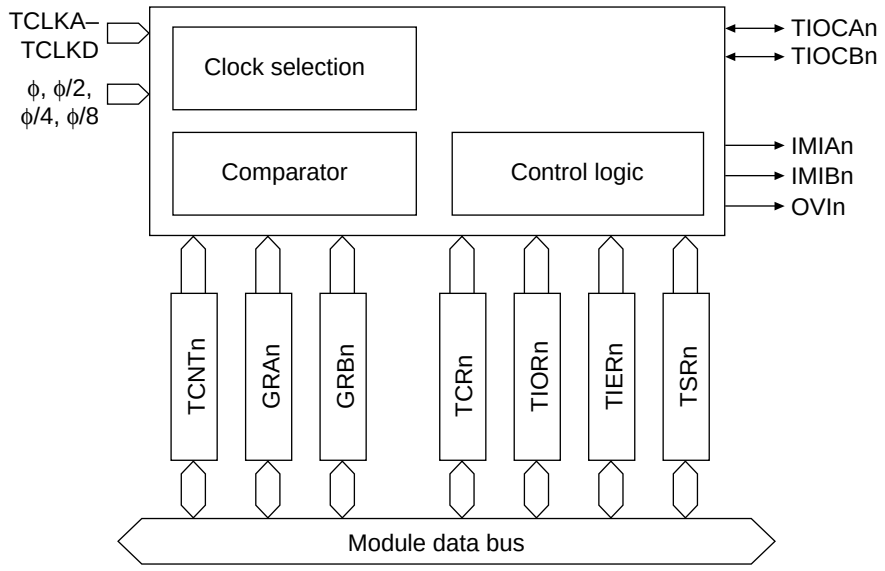


Figure 10.1 Block Diagram of ITU

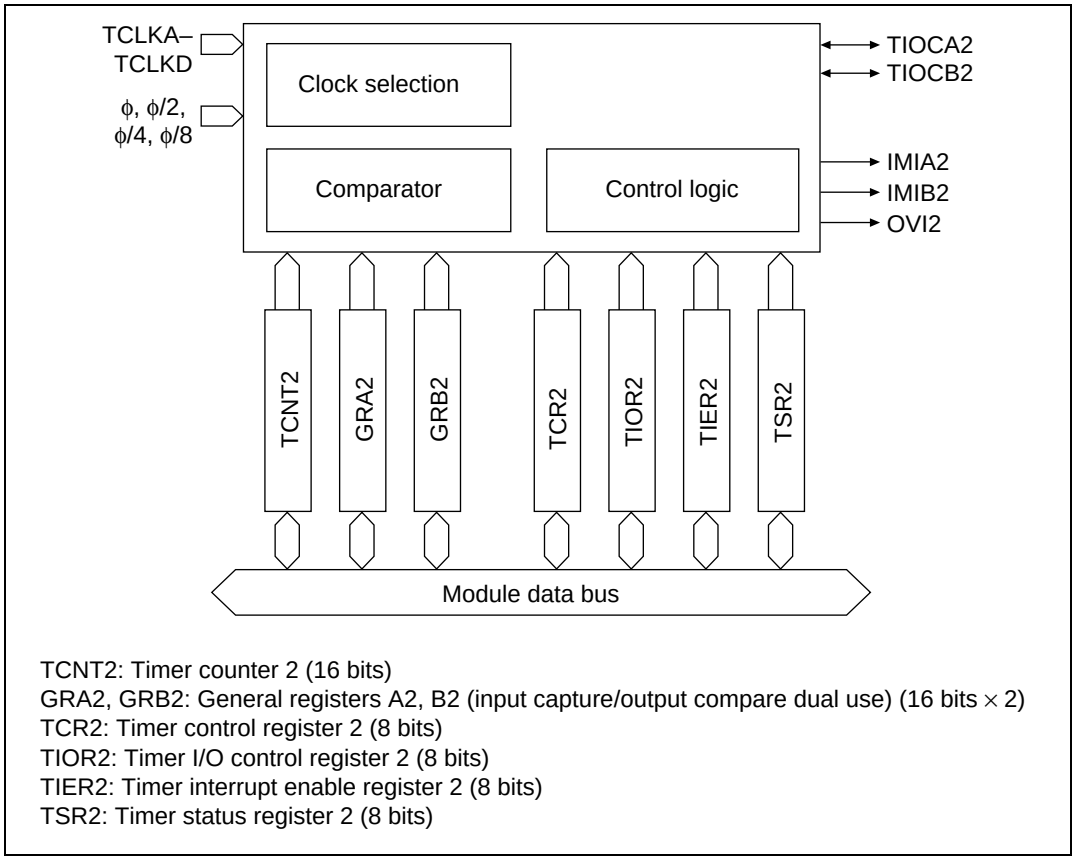
Block Diagram of Channels 0 and 1: ITU channels 0 and 1 have the same function. Figure 10.2 shows a block diagram of channels 0 and 1.



TCNTn: Timer counter n (16 bits)
GRAn, GRBn: General registers An, Bn (input capture/output compare dual use) (16 bits × 2)
TCRn: Timer control register n (8 bits)
TIORn: Timer I/O control register n (8 bits)
TIERn: Timer interrupt enable register n (8 bits)
TSRn: Timer status register n (8 bits)
(n = 0 or 1)

Figure 10.2 Block Diagram of Channels 0 and 1 (One Channel Shown)

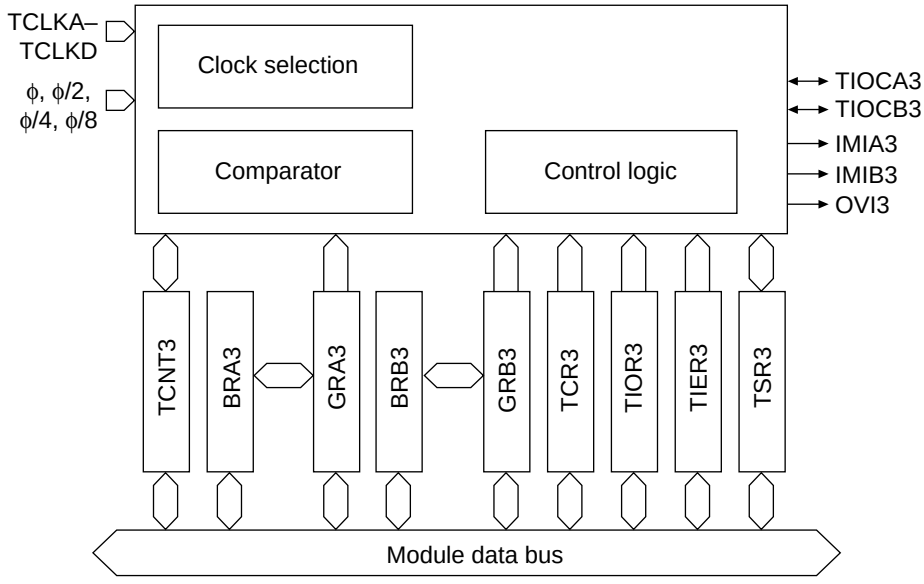
Block Diagram of Channel 2: Figure 10.3 shows a block diagram of channel 2. Channel 2 is capable of 0 output/1 output only.



TCNT2: Timer counter 2 (16 bits)
GRA2, GRB2: General registers A2, B2 (input capture/output compare dual use) (16 bits × 2)
TCR2: Timer control register 2 (8 bits)
TIOR2: Timer I/O control register 2 (8 bits)
TIER2: Timer interrupt enable register 2 (8 bits)
TSR2: Timer status register 2 (8 bits)

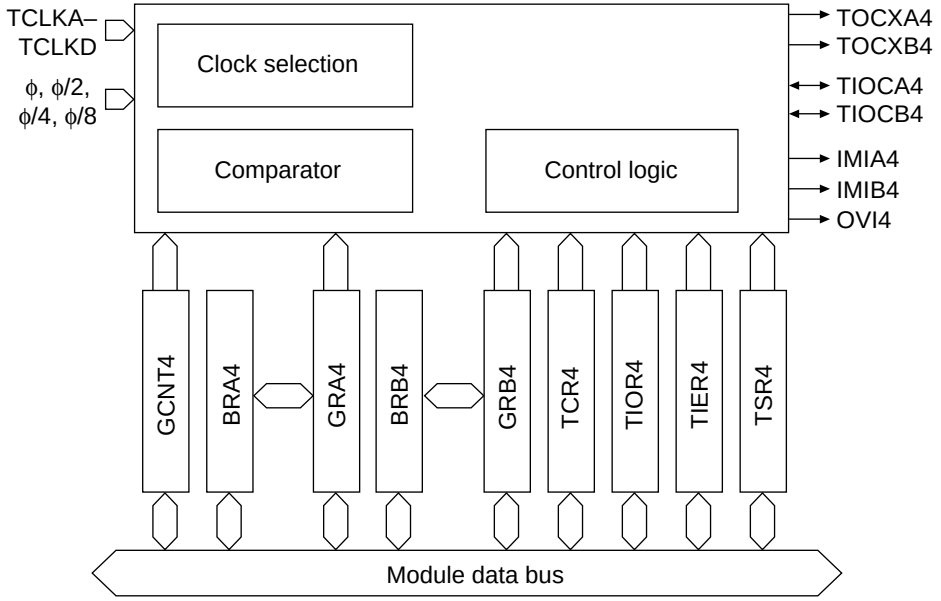
Figure 10.3 Block Diagram of Channel 2

Block Diagrams of Channels 3 and 4: Figure 10.4 shows a block diagram of channel 3; figure 10.5 shows a block diagram of channel 4.



TCNT3: Timer counter 3 (16 bits)
GRA3, GRB3: General registers A3, B3 (input capture/output compare dual use) (16 bits × 2)
BRA3, BRB3: Buffer registers A3, B3 (input capture/output compare dual use) (16 bits × 2)
TCR3: Timer control register 3 (8 bits)
TIOR3: Timer I/O control register 3 (8 bits)
TIER3: Timer interrupt enable register 3 (8 bits)
TSR3: Timer status register 3 (8 bits)

Figure 10.4 Block Diagram of Channel 3



TCNT4: Timer counter 4 (16 bits)
GRA4, GRB4: General registers A4, B4 (input capture/output compare dual use) (16 bits × 2)
BRA4, BRB4: Buffer registers A4, B4 (input capture/output compare dual use) (16 bits × 2)
TCR4: Timer control register 4 (8 bits)
TIOR4: Timer I/O control register 4 (8 bits)
TIER4: Timer interrupt enable register 4 (8 bits)
TSR4: Timer status register 4 (8 bits)

Figure 10.5 Block Diagram of Channel 4

10.1.3 Input/Output Pins

Table 10.2 summarizes the ITU pins. External pin functions should be set with the pin function controller to match to the ITU setting. See section 15, Pin Function Controller, for details. ITU pins need to be set using the pin function controller (PFC) after the chip is set to ITU mode.

Table 10.2 Pin Configuration

Channel	Name	Pin Name	I/O	Function
Shared	Clock input A	TCLKA	I	External clock A input pin (A-phase input pin in phase counting mode)
	Clock input B	TCLKB	I	External clock B input pin (B-phase input pin in phase counting mode)
	Clock input C	TCLKC	I	External clock C input pin
	Clock input D	TCLKD	I	External clock D input pin
0	Input capture/output compare A0	TIOCA0	I/O	GRA0 output compare/GRA0 input capture/PWM output pin (in PWM mode)
	Input capture/output compare B0	TIOCB0	I/O	GRB0 output compare/GRB0 input capture
1	Input capture/output compare A1	TIOCA1	I/O	GRA1 output compare/GRA1 input capture/PWM output pin (in PWM mode)
	Input capture/output compare B1	TIOCB1	I/O	GRB1 output compare/GRB1 input capture
2	Input capture/output compare A2	TIOCA2	I/O	GRA2 output compare/GRA2 input capture/PWM output pin (in PWM mode)
	Input capture/output compare B2	TIOCB2	I/O	GRB2 output compare/GRB2 input capture
3	Input capture/output compare A3	TIOCA3	I/O	GRA3 output compare/GRA3 input capture/PWM output pin (in PWM mode, complementary PWM mode, or reset-synchronized PWM mode)
	Input capture/output compare B3	TIOCB3	I/O	GRB3 output compare/GRB3 input capture/PWM output pin (in complementary PWM mode or reset-synchronized PWM mode)
4	Input capture/output compare A4	TIOCA4	I/O	GRA4 output compare/GRA4 input capture/PWM output pin (in PWM mode, complementary PWM mode or reset-synchronized PWM mode)
	Input capture/output compare B4	TIOCB4	I/O	GRB4 output compare/GRB4 input capture/PWM output pin (in complementary PWM mode or reset-synchronized PWM mode)
	Output compare XA4	TOCXA4	O	PWM output pin (in complementary PWM mode or reset-synchronized PWM mode)
	Output compare XB4	TOCXB4	O	PWM output pin (in complementary PWM mode or reset-synchronized PWM mode)

10.1.4 Register Configuration

Table 10.3 summarizes the ITU register configuration.

Table 10.3 Register Configuration

Channel	Name	Abbreviation	R/W	Initial Value	Address*1	Access Size
Shared	Timer start register	TSTR	R/W	H'E0/H'60	H'5FFFF00	8
	Timer synchro register	TSNC	R/W	H'E0/H'60	H'5FFFF01	8
	Timer mode register	TMDR	R/W	H'80/H'00	H'5FFFF02	8
	Timer function control register	TFCR	R/W	H'C0/H'40	H'5FFFF03	8
	Timer output control register	TOCR	R/W	H'FF/H'7F	H'5FFFF31	8
0	Timer control register 0	TCR0	R/W	H'80/H'00	H'5FFFF04	8
	Timer I/O control register 0	TIOR0	R/W	H'88/H'08	H'5FFFF05	8
	Timer interrupt enable register 0	TIER0	R/W	H'F8/H'78	H'5FFFF06	8
	Timer status register 0	TSR0	R/(W)*2	H'F8/H'78	H'5FFFF07	8
	Timer counter 0	TCNT0	R/W	H'00	H'5FFFF08	8, 16, 32
					H'5FFFF09	8, 16, 32
	General register A0	GRA0	R/W	H'FF	H'5FFFF0A	8, 16, 32
					H'5FFFF0B	8, 16, 32
	General register B0	GRB0	R/W	H'FF	H'5FFFF0C	8, 16
					H'5FFFF0D	8, 16
1	Timer control register 1	TCR1	R/W	H'80/H'00	H'5FFFF0E	8
	Timer I/O control register 1	TIOR1	R/W	H'88/H'08	H'5FFFF0F	8
	Timer interrupt enable register 1	TIER1	R/W	H'F8/H'78	H'5FFFF10	8
	Timer status register 1	TSR1	R/(W)*2	H'F8/H'78	H'5FFFF11	8
	Timer counter 1	TCNT1	R/W	H'00	H'5FFFF12	8, 16
					H'5FFFF13	8, 16
	General register A1	GRA1	R/W	H'FF	H'5FFFF14	8, 16, 32
					H'5FFFF15	8, 16, 32
	General register B1	GRB1	R/W	H'FF	H'5FFFF16	8, 16, 32
					H'5FFFF17	8, 16, 32

Channel	Name	Abbrevi-ation	R/W	Initial Value	Address*1	Access Size
2	Timer control register 2	TCR2	R/W	H'80/H'00	H'5FFFF18	8
	Timer I/O control register 2	TIOR2	R/W	H'88/H'08	H'5FFFF19	8
	Timer interrupt enable register 2	TIER2	R/W	H'F8/H'78	H'5FFFF1A	8
	Timer status register 2	TSR2	R/(W)*2	H'F8/H'78	H'5FFFF1B	8
	Timer counter 2	TCNT2	R/W	H'00	H'5FFFF1C	8, 16, 32
					H'5FFFF1D	8, 16, 32
	General register A2	GRA2	R/W	H'FF	H'5FFFF1E	8, 16, 32
					H'5FFFF1F	8, 16, 32
	General register B2	GRB2	R/W	H'FF	H'5FFFF20	8, 16
					H'5FFFF21	8, 16
3	Timer control register 3	TCR3	R/W	H'80/H'00	H'5FFFF22	8
	Timer I/O control register 3	TIOR3	R/W	H'88/H'08	H'5FFFF23	8
	Timer interrupt enable register 3	TIER3	R/W	H'F8/H'78	H'5FFFF24	8
	Timer status register 3	TSR3	R/(W)*2	H'F8/H'78	H'5FFFF25	8
	Timer counter 3	TCNT3	R/W	H'00	H'5FFFF26	8, 16
					H'5FFFF27	8, 16
	General register A3	GRA3	R/W	H'FF	H'5FFFF28	8, 16, 32
					H'5FFFF29	8, 16, 32
	General register B3	GRB3	R/W	H'FF	H'5FFFF2A	8, 16, 32
					H'5FFFF2B	8, 16, 32
	Buffer register A3	BRA3	R/W	H'FF	H'5FFFF2C	8, 16, 32
					H'5FFFF2D	8, 16, 32
	Buffer register B3	BRB3	R/W	H'FF	H'5FFFF2E	8, 16, 32
					H'5FFFF2F	8, 16, 32
4	Timer control register 4	TCR4	R/W	H'80/H'00	H'5FFFF32	8
	Timer I/O control register 4	TIOR4	R/W	H'88/H'08	H'5FFFF33	8
	Timer interrupt enable register 4	TIER4	R/W	H'F8/H'78	H'5FFFF34	8
	Timer status register 4	TSR4	R/(W)*2	H'F8/H'78	H'5FFFF35	8
	Timer counter 4	TCNT4	R/W	H'00	H'5FFFF36	8, 16
					H'5FFFF37	8, 16
	General register A4	GRA4	R/W	H'FF	H'5FFFF38	8, 16, 32
					H'5FFFF39	8, 16, 32

Channel	Name	Abbreviation	R/W	Initial Value	Address*1	Access Size
4	General register B4	GRB4	R/W	H'FF	H'5FFFF3A	8, 16, 32
					H'5FFFF3B	8, 16, 32
	Buffer register A4	BRA4	R/W	H'FF	H'5FFFF3C	8, 16, 32
					H'5FFFF3D	8, 16, 32
	Buffer register B4	BRB4	R/W	H'FF	H'5FFFF3E	8, 16, 32
					H'5FFFF3F	8, 16, 32

Notes: 1. Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.
2. Only 0 can be written to clear flags.

10.2 ITU Register Descriptions

10.2.1 Timer Start Register (TSTR)

The timer start register (TSTR) is an eight-bit read/write register that starts and stops the timer counters (TCNT) of channels 0–4. TSTR is initialized to H'E0 or H'60 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	—	—	—	STR4	STR3	STR2	STR1	STR0
Initial value	*	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Note: * Undefined

Bits 7–5—Reserved: Cannot be modified. Bit 7 is read as undefined. Bits 6 and 5 are always read as 1. The write value to bit 7 should be 0 or 1, and the write value to bits 6 and 5 should always be 1.

Bit 4—Count Start 4 (STR4): STR4 starts and stops TCNT4.

Bit 4: STR4	Description	
0	TCNT4 is halted	(Initial value)
1	TCNT4 is counting	

Bit 3—Count Start 3 (STR3): STR3 starts and stops TCNT3.

Bit 3: STR3	Description	
0	TCNT3 is halted	(Initial value)
1	TCNT3 is counting	

Bit 2—Count Start 2 (STR2): STR2 starts and stops TCNT2.

Bit 2: STR2	Description	
0	TCNT2 is halted	(Initial value)
1	TCNT2 is counting	

Bit 1—Count Start 1 (STR1): STR1 starts and stops TCNT1.

Bit 1: STR1	Description	
0	TCNT1 is halted	(Initial value)
1	TCNT1 is counting	

Bit 0—Count Start 0 (STR0): STR0 starts and stops TCNT0.

Bit 0: STR0	Description	
0	TCNT0 is halted	(Initial value)
1	TCNT0 is counting	

10.2.2 Timer Synchro Register (TSNC)

The timer synchro register (TSNC) is an eight-bit read/write register that selects timer synchronizing modes for channels 0–4. Channels for which 1 is set in the corresponding bit will be synchronized. TSNC is initialized to H'E0 or H'60 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	—	—	—	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
Initial value	*	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Note: * Undefined

Bits 7–5 Reserved: Bit 7 is read as undefined. Bits 6 and 5 are always read as 1. The write value to bit 7 should be 0 or 1, and the write value to bits 6 and 5 should always be 1.

Bit 4—Timer Synchro 4 (SYNC4): SYNC4 selects synchronizing mode for channel 4.

Bit 4: SYNC4	Description
0	The timer counter for channel 4 (TCNT4) operates independently (Preset/clear of TCNT4 is independent of other channels) (Initial value)
1	Channel 4 operates synchronously. Synchronized preset/clear of TNCT4 enabled.

Bit 3—Timer Synchro 3 (SYNC3): SYNC3 selects synchronizing mode for channel 3.

Bit 3: SYNC3	Description
0	The timer counter for channel 3 (TCNT3) operates independently (Preset/clear of TCNT3 is independent of other channels) (Initial value)
1	Channel 3 operates synchronously. Synchronized preset/clear of TNCT3 enabled.

Bit 2—Timer Synchro 2 (SYNC2): SYNC2 selects synchronizing mode for channel 2.

Bit 2: SYNC2	Description
0	The timer counter for channel 2 (TCNT2) operates independently (Preset/clear of TCNT2 is independent of other channels) (Initial value)
1	Channel 2 operates synchronously. Synchronized preset/clear of TNCT2 enabled.

Bit 1—Timer Synchro 1 (SYNC1): SYNC1 selects synchronizing mode for channel 1.

Bit 1: SYNC1	Description
0	The timer counter for channel 1 (TCNT1) operates independently (Preset/clear of TCNT1 is independent of other channels) (Initial value)
1	Channel 1 operates synchronously. Synchronized preset/clear of TNCT1 enabled.

Bit 0—Timer Synchro 0 (SYNC0): SYNC0 selects synchronizing mode for channel 0.

Bit 0: SYNC0	Description
0	The timer counter for channel 0 (TCNT0) operates independently (Preset/clear of TCNT0 is independent of other channels) (Initial value)
1	Channel 0 operates synchronously. Synchronized preset/clear of TNCT0 enabled.

10.2.3 Timer Mode Register (TMDR)

The timer mode register (TMDR) is an eight-bit read/write register that selects PWM mode for channels 0–4, sets phase counting mode for channel 2, and sets the conditions for the overflow flag (OVF). TMDR is initialized to H'80 or H'00 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	—	MDF	FDIR	PWM4	PWM3	PWM2	PWM1	PWM0
Initial value	*	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Undefined

Bit 7—Reserved: Bit 7 is read as undefined. The write value should be 0 or 1.

Bit 6—Phase Counting Mode (MDF): MDF selects phase counting mode for channel 2.

Bit 6: MDF	Description
0	Channel 2 operates normally (Initial value)
1	Channel 2 operates in phase counting mode

When the MDF bit is set to 1 to select phase counting mode, the timer counter (TCNT2) becomes an up/down-counter and the TCLKA and TCLKB pins become count clock input pins. TCNT2 counts on both the rising and falling edges of TCLKA and TCLKB, with increment/decrement chosen as follows:

Count Direction	Decrement				Increment			
TCLKA pin	Rising	High	Falling	Low	Rising	High	Falling	Low
TCLKB pin	Low	Rising	High	Falling	High	Falling	Low	Rising

In phase counting mode, selections for external clock edge made with the CKEG1 and CKEG0 bits in timer control register 2 (TCR2) and the counter clock selection made in the TPSC2–TPSC0 bits are ignored. The phase counting mode described above takes priority. Settings for counter clear conditions in the CCLR1 and CCLR0 bits in TCR2 and settings for timer I/O control register 2 (TIOR2), timer interrupt enable register (TIER2), and timer status register 2 (TSR2) compare match/input capture functions and interrupts, however, are valid even in phase counting mode.

Bit 5—Flag Direction (FDIR): FDIR selects the setting condition for the overflow flag (OVF) in timer status register 2 (TSR2). This bit is valid no matter which mode channel 2 is operating in.

Bit 5: FDIR	Description	
0	OVF of TSR2 is set to 1 when TCNT2 overflows or underflows	(Initial value)
1	OVF of TSR2 is set to 1 when TCNT2 overflows	

Bit 4—PWM Mode 4 (PWM4): PWM4 selects PWM mode for channel 4. When the PWM4 bit is set to 1 and PWM mode is entered, the TIOCA4 pin becomes a PWM output pin. 1 is output on a compare match of general register A4 (GRA4); 0 is output on a compare match of general register B4 (GRB4). When complementary PWM mode or reset-synchronized PWM mode is set by the CMD1 and CMD0 bits in the timer function control register (TFCR), the setting of this bit is ignored in favor of the settings of CMD1 and CMD0.

Bit 4: PWM4	Description	
0	Channel 4 operates normally	(Initial value)
1	Channel 4 operates in PWM mode	

Bit 3—PWM Mode 3 (PWM3): PWM3 selects the PWM mode for channel 3. When the PWM3 bit is set to 1 and PWM mode is entered, the TIOCA3 pin becomes a PWM output pin. 1 is output on a compare match of general register A3 (GRA3); 0 is output on a compare match of general register B3 (GRB3). When complementary PWM mode or reset-synchronized PWM mode is set by the CMD1 and CMD0 bits in the timer function control register (TFCR), the setting of this bit is ignored in favor of the settings of CMD1 and CMD0.

Bit 3: PWM3	Description	
0	Channel 3 operates normally	(Initial value)
1	Channel 3 operates in PWM mode	

Bit 2—PWM Mode 2 (PWM2): PWM2 selects the PWM mode for channel 2. When the PWM2 bit is set to 1 and PWM mode is entered, the TIOCA2 pin becomes a PWM output pin. 1 is output

on a compare match of general register A2 (GRA2); 0 is output on a compare match of general register B2 (GRB2).

Bit 2: PWM2	Description	
0	Channel 2 operates normally	(Initial value)
1	Channel 2 operates in PWM mode	

Bit 1—PWM Mode 1 (PWM1): PWM1 selects the PWM mode for channel 1. When the PWM1 bit is set to 1 and PWM mode is entered, the TIOCA1 pin becomes a PWM output pin. 1 is output on a compare match of general register A1 (GRA1); 0 is output on a compare match of general register B1 (GRB1).

Bit 1: PWM1	Description	
0	Channel 1 operates normally	(Initial value)
1	Channel 1 operates in PWM mode	

Bit 0—PWM Mode 0 (PWM0): PWM0 selects the PWM mode for channel 0. When the PWM0 bit is set to 1 and PWM mode is entered, the TIOCA0 pin becomes a PWM output pin. 1 is output on a compare match of general register A0 (GRA0); 0 is output on a compare match of general register B0 (GRB0).

Bit 0: PWM0	Description	
0	Channel 0 operates normally	(Initial value)
1	Channel 0 operates in PWM mode	

10.2.4 Timer Function Control Register (TFCR)

The timer function control register (TFCR) is an 8-bit read/write register that selects complementary PWM/reset-synchronized PWM for channels 3 and 4 and sets the buffer operation. TFCR is initialized to H'C0 or H'40 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	—	—	CMD1	CMD0	BFB4	BFA4	BFB3	BFA3
Initial value	*	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Undefined

Bits 7 and 6—Reserved: Bit 7 is read as undefined. Bit 6 is always read as 1. The write value to bit 7 should be 0 or 1. The write value to bit 6 should always be 1.

Bits 5 and 4—Combination Mode 1 and 0 (CMD1 and CMD0): CMD1 and CMD0 select complementary PWM mode or reset-synchronized mode for channels 3 and 4. Set the complementary PWM/reset-synchronized PWM mode while the timer counter (TCNT) being used is off. When these bits are used to set complementary PWM/reset-synchronized PWM mode, they take priority over the PWM4 and PWM3 bits in TMDR. While the complementary PWM/reset-synchronized PWM mode settings and the SYNC4 and SYNC3 bit settings of the timer synchro register (TSNC) are valid simultaneously, when complementary PWM mode is set, channels 3 and 4 should not be set to operate simultaneously (the SYNC 4 and SYNC 3 bits in TSNC should not both be set to 1).

Bit 5: CMD1	Bit 4: CMD0	Description	
0	0	Channels 3 and 4 operate normally	(Initial value)
	1	Channels 3 and 4 operate normally	
1	0	Channels 3 and 4 operate together in complementary PWM mode	
	1	Channels 3 and 4 operate together in reset-synchronized PWM mode	

Bit 3—Buffer Mode B4 (BFB4): BFB4 selects buffer mode for GRB4 and BRB4 in channel 4.

Bit 3: BFB4	Description	
0	GRB4 operates normally in channel 4	(Initial value)
1	GRB4 and BRB4 operate in buffer mode in channel 4	

Bit 2—Buffer Mode A4 (BFA4): BFA4 selects buffer mode for GRA4 and BRA4 in channel 4.

Bit 2: BFA4	Description	
0	GRA4 operates normally in channel 4	(Initial value)
1	GRA4 and BRA4 operate in buffer mode in channel 4	

Bit 1—Buffer Mode B3 (BFB3): BFB3 selects buffer mode for GRB3 and BRB3 in channel 3.

Bit 1: BFB3	Description	
0	GRB3 operates normally in channel 3	(Initial value)
1	GRB3 and BRB3 operate in buffer mode in channel 3	

Bit 0—Buffer Mode A3 (BFA3): BFA3 selects buffer mode for GRA3 and BRA3 in channel 3.

Bit 0: BFA3	Description	
0	GRA3 operates normally in channel 3	(Initial value)
1	GRA3 and BRA3 operate in buffer mode in channel 3	

10.2.5 Timer Output Control Register (TOCR)

The timer output control register (TOCR) is an eight-bit read/write register that inverts the output level in complementary PWM mode/reset-synchronized PWM mode. Setting bits OLS3 and OLS4 is valid only in complementary PWM mode and reset-synchronized PWM mode. In other output situations, these bits are ignored. TOCR is initialized to H'FF or H'7F by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	OLS4	OLS3
Initial value	*	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	R/W	R/W

Note: * Undefined

Bits 7–2—Reserved: Bit 7 is read as undefined. Bits 6–2 are always read as 1. The write value to bit 7 should be 0 or 1. The write value to bits 6–2 should always be 1.

Bit 1—Output Level Select 4 (OLS4): OLS4 selects the output level for complementary PWM mode or reset-synchronized PWM mode.

Bit 1: OLS4	Description	
0	TIOCA3, TIOCA4, and TIOCB4 are inverted and output	
1	TIOCA3, TIOCA4, and TIOCB4 are output directly	(Initial value)

Bit 0—Output Level Select 3 (OLS3): OLS3 selects the output level for complementary PWM mode or reset-synchronized PWM mode.

Bit 0: OLS3	Description	
0	TIOCB3, TOCXA4, and TOCXB4 are inverted and output	
1	TIOCB3, TOCXA4, and TOCXB4 are output directly	(Initial value)

10.2.6 Timer Counters (TCNT)

The ITU has five 16-bit timer counters (TCNT), one for each channel.

Each TCNT is a 16-bit read/write counter that counts by input from a clock source. The clock source is selected by timer prescaler bits 2–0 (TPSC2–TPSC0) in the timer control register (TCR).

TCNT0 and TCNT 1 are strictly up-counters. Up/down-counting occurs for TCNT2 when phase counting mode is selected, or for TCNT3 and TCNT 4 when complementary PWM mode is selected. In other modes, they are up-counters.

TCNT can be cleared to H'0000 by compare match with the corresponding general register A or B (GRA, GRB) or input capture to GRA or GRB (counter clear function).

When TCNT overflows (changes from H'FFFF to H'0000), the overflow flag (OVF) in the timer status register (TSR) is set to 1. The OVF of the corresponding channel TSR is also set to 1 when TCNT underflows (changes from H'0000 to H'FFFF).

TCNT is connected to the CPU by a 16-bit bus, so it can be written or read by either word access or byte access. TCNT is initialized to H'0000 by a reset and in standby mode.

Table 10.4 Timer Counters (TCNT)

Channel	Abbreviation	Function
0	TCNT0	Increment counter
1	TCNT1	
2	TCNT2	Phase counting mode: Increment/decrement All others: Increment
3	TCNT3	Complementary PWM mode: Increment/decrement All others: Increment
4	TCNT4	

Bit	15	14	13	12	11	10	9	8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

10.2.7 General Registers A and B (GRA and GRB)

Each of the five ITU channels has two 16-bit general registers (GR) for a total of ten registers.

Each GR is a 16-bit read/write register that can function as either an output compare register or an input capture register. The function is selected by settings in the timer I/O control register (TIOR).

When a general register (GRA/GRB) is used as an output compare register, its value is constantly compared with the timer counter (TCNT) value. When the two values match (compare match), the IMFA/IMFB bit is set to 1 in the timer status register (TSR). If compare match output is selected in TIOR, a specified value is output at the output compare pin.

When a general register is used as an input capture register, an external input capture signal is detected and the TCNT value is stored. The IMFA/IMFB bit in the corresponding TSR is set to 1 at the same time. The valid edge or edges of the input capture signal are selected in TIOR. The TIOR setting is ignored when set for PWM mode, complementary PWM mode, or reset-synchronized PWM mode.

General registers are connected to the CPU by a 16-bit bus, so general registers can be written or read by either word access or byte access. General registers are initialized as output compare registers (no pin output) by a reset and in standby mode. The initial value is H'FFFF.

Table 10.5 General Registers A and B (GRA and GRB)

Channel	Abbreviation	Function
0	GRA0, GRB0	Output compare/input capture dual register
1	GRA1, GRB1	
2	GRA2, GRB2	
3	GRA3, GRB3	Output compare/input capture dual register. Can also be set for buffer
4	GRA4, GRB4	operation in combination with the buffer registers (BRA, BRB)

Bit	15	14	13	12	11	10	9	8
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

10.2.8 Buffer Registers A and B (BRA, BRB)

Each buffer register is a 16-bit read/write register that is used in buffer mode. The ITU has four buffer registers, two each for channels 3 and 4. Buffer operation can be set independently by the timer function control register (TFCR) bits BFB4, BFA4, BFB3, and BFB3. The buffer registers are paired with the general registers and their function changes automatically to match the function of corresponding general register.

The buffer registers are connected to the CPU by a 16-bit bus, so they can be written or read by either word or byte access. Buffer registers are initialized to H'FFFF by a reset and in standby mode.

Table 10.6 Buffer Registers A and B (BRA, BRB)

Channel	Abbreviation	Function
3	BRA3, BRB3	When used for buffer operation: When the corresponding GRA and GRB are output compare registers, the buffer registers function as output compare buffer registers that can automatically transfer the BRA and BRB values to GRA and GRB upon a compare match. When the corresponding GRA and GRB are input capture registers, the buffer registers function as input capture buffer registers that can automatically transfer the values stored until an input capture in the GRA and GRB to the BRA and BRB.
4	BRA4, BRB4	

Bit	15	14	13	12	11	10	9	8
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

10.2.9 Timer Control Register (TCR)

The ITU has five 8-bit timer control registers (TCR), one for each channel.

TCR is an 8-bit read/write register that selects the timer counter clock, the edges of the external clock source, and the counter clear source. TCR is initialized to H'80 or H'00 by a reset and in standby mode.

Table 10.7 Timer Control Register (TCR)

Channel	Abbreviation	Function
0	TCR0	TCR controls the TCNTs. The TCRs have the same functions on all channels. When channel 2 is set for phase counting mode, setting the CKEG1, CKEG2, and TPSC2–TPSC0 bits will have no effect.
1	TCR1	
2	TCR2	
3	TCR3	
4	TCR4	

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	*	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Undefined

Bit 7—Reserved: Bit 7 is read as undefined. The write value should be 0 or 1.

Bits 6 and 5—Counter Clear 1 and 0 (CCLR1 and CCLR0): CCLR1 and CCLR0 select the counter clear source.

Bit 6: CCLR1	Bit 5: CCLR0	Description	
0	0	TCNT is not cleared	(Initial value)
	1	TCNT is cleared by general register A (GRA) compare match or input capture*1	
1	0	TCNT is cleared by general register B (GRB) compare match or input capture*1	
	1	Synchronizing clear: TCNT is cleared in synchronization with clear of other timer counters operating in sync*2	

Notes: 1. When GR is functioning as an output compare register, TCNT is cleared upon a compare match. When functioning as an input capture register, TCNT is cleared upon input capture.
2. The timer synchro register (TSNC) sets the synchronization.

Bits 4 and 3—External Clock Edge 1/0 (CKEG1 and CKEG0): CKEG1 and CKEG0 select external clock input edge. When channel 2 is set for phase counting mode, settings of the CKEG1 and CKEG0 bits in TCR are ignored and the phase counting mode operation takes priority.

Bit 4: CKEG1	Bit 3: CKEG0	Description	
0	0	Count rising edges	(Initial value)
	1	Count falling edges	
1	—	Count both rising and falling edges	

Bits 2–0—Timer Prescaler 2–0 (TPS2–TPS0): TPS2–TPS0 select the counter clock source. When TPSC2 = 0 and an internal clock source is selected, the timer counts only falling edges. When TPSC2 = 1 and an external clock is selected, the count edge is as set by CKEG1 and CKEG0. When phase counting mode is selected for channel 2 (the MDF bit in the timer mode register is 1), the settings of TPSC2–TPSC0 in TCR2 are ignored and the phase counting operation takes priority.

Bit 2: TPSC2	Bit 1: TPSC1	Bit 0: TPSC0	Counter Clock (and Cycle when ϕ = 10 MHz)
0	0	0	Internal clock ϕ (Initial value)
		1	Internal clock ϕ/2
	1	0	Internal clock ϕ/4
		1	Internal clock ϕ/8
1	0	0	External clock A (TCLKA)
		1	External clock B (TCLKB)
	1	0	External clock C (TCLKC)
		1	External clock D (TCLKD)

10.2.10 Timer I/O Control Register (TIOR)

The timer I/O control register (TIOR) is an eight-bit read/write register that selects the output compare or input capture function for general registers GRA and GRB. It also selects the function of the TIOCA and TIOCB pins. If output compare is selected, TIOR also selects the output settings. If input capture is selected, TIOR also selects the input capture edge. TIOR is initialized to H'88 or H'08 by a reset and in standby mode. Each ITU channel has one TIOR.

Table 10.8 Timer I/O Control Register (TIOR)

Channel	Abbreviation	Function
0	TIOR0	TIOR controls the GRs. Some functions vary during PWM. When channels 3 and 4 are set for complementary PWM mode/reset-synchronized PWM mode, TIOR3 and TIOR4 settings are not valid.
1	TIOR1	
2	TIOR2	
3	TIOR3	
4	TIOR4	

Bit	7	6	5	4	3	2	1	0
	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
Initial value	*	0	0	0	1	0	0	0
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Note: * Undefined

Bit 7—Reserved: Bit 7 is read as undefined. The write value should be 0 or 1.

Bits 6–4—I/O Control B2–B0 (IOB2–IOB0): IOB2–IOB0 selects the GRB function.

Bit 6: IOB2	Bit 5: IOB1	Bit 4: IOB0	GRB Function	
0	0	0	GRB is an output compare register	Compare match with pin output disabled (Initial value)
		1		0 output at GRB compare match*[1]
	1	0		1 output at GRB compare match*[1]
		1		Output toggles at GRB compare match (1 output for channel 2 only)*[1] *[2]
1	0	0	GRB is an input capture register	GRB captures rising edge of input
		1		GRB captures falling edge of input
	1	0		GRB captures both edges of input
		1		

Notes: 1. After reset, the value output is 0 until the first compare match occurs.
2. Channel 2 has no compare-match driven toggle output function. If it is set for toggle, 1 is automatically selected as the output.

Bit 3—Reserved: Bit 3 always is read as 1. The write value should always be 1.

Bits 2–0—I/O Control A2–A0 (IOA2–IOA0): IOA2–IOA0 select the GRB function.

Bit 2: IOA2	Bit 1: IOA1	Bit 0: IOA0	GRA Function	
0	0	0	GRA is an output compare register	Compare match with pin output disabled (Initial value)
		1		0 output at GRA compare match*1
	1	0		1 output at GRA compare match*1
		1		Output toggles at GRA compare match (1 output for channel 2 only)*1 *2
1	0	0	GRA is an input capture register	GRA captures rising edge of input
		1		GRA captures falling edge of input
	1	0		GRA captures both edges of input
		1		

Notes: 1. After reset, the value output is 0 until the first compare match occurs.
2. Channel 2 has no compare-match driven toggle output function. If it is set for toggle, 1 is automatically selected as the output.

10.2.11 Timer Status Register (TSR)

The timer status register (TSR) is an eight-bit read/write register containing flags that indicate timer counter (TCNT) overflow/underflow and general register (GRA/GRB) compare match or input capture. These flags are interrupt sources. If the interrupt is enabled by the corresponding bit in the timer interrupt enable register (TIER), an interrupt request is sent to the CPU. TSR is initialized to H'F8 or H'78 by a reset and in standby mode. Each ITU channel has one TSR.

Table 10.9 Timer Status Register (TSR)

Channel	Abbreviation	Function
0	TSR0	TSR indicates input capture, compare match and overflow status.
1	TSR1	
2	TSR2	
3	TSR3	
4	TSR4	

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	OVF	IMFB	IMFA
Initial value	*1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	R/(W)*2	R/(W)*2	R/(W)*2

Notes: 1. Undefined
2. Only 0 can be written, to clear the flag.

Bits 7–3—Reserved: Bit 7 is read as undefined. Bits 6–3 are always read as 1. The write value to bit 7 should be 0 or 1. The write value to bits 6–3 should always be 1.

Bit 2—Overflow Flag (OVF): OVF indicates that a TCNT overflow/underflow has occurred.

Bit 2: OVF	Description
0	Clearing condition: Read OVF when OVF = 1, then write 0 in OVF (Initial value)
1	Setting condition: TCNT overflow from H'FFFF to H'0000 or underflow from H'0000 to H'FFFF

Note: A TCNT underflow occurs when the TCNT up/down-counter is functioning. It may occur in the following cases: (1) When channel 2 is set to phase counting mode (MDF bit in TMDR is 1), or (2) when channel 3 and 4 are set to complementary PWM mode (CMD1 bit in TFCR is 1 and CMD0 bit is 0).

Bit 1—Input Capture/Compare Match B (IMFB): IMFB indicates a GRB compare match or input capture.

Bit 1: IMFB	Description
0	Clearing condition: Read IMFB when IMFB = 1, then write 0 in IMFB (Initial value)
1	Setting conditions: • GRB is functioning as an output compare register and TCNT = GRB • GRB is functioning as an input capture register and the value of TCNT is transferred to GRB by an input capture signal

Bit 0—Input Capture/Compare Match A (IMFA): IMFA indicates a GRA compare match or input capture.

Bit 0: IMFA	Description
0	Clearing condition: Read IMFA when IMFA = 1, then write 0 in IMFA (Initial value) DMAC is activated by an IMIA interrupt (only channels 0–3)
1	Setting conditions: • GRA is functioning as an output compare register and TCNT = GRA • GRA is functioning as an input capture register and the value of TCNT is transferred to GRA by an input capture signal

10.2.12 Timer Interrupt Enable Register (TIER)

The timer status interrupt enable register (TIER) is an eight-bit read/write register that controls enabling/disabling of overflow interrupt requests and general register compare match/input capture interrupt requests. TIER is initialized to H'F8 or H'78 by a reset and in standby mode. Each ITU channel has one TIER.

Table 10.10 Timer Interrupt Enable Register (TIER)

Channel	Abbreviation	Function
0	TIER0	TIER controls interrupt enabling/disabling
1	TIER1	
2	TIER2	
3	TIER3	
4	TIER4	

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	OVIE	IMIEB	IMIEA
Initial value	*	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	R/W	R/W	R/W

Note: * Undefined

Bits 7–3—Reserved: Bit 7 is read as undefined. Bits 6–3 are always read as 1. The write value to bit 7 should be 0 or 1. The write value to bits 6–3 should always be 1.

Bit 2—Overflow Interrupt Enable (OVIE): When the TSR overflow flag (OVF) is set to 1, OVIE enables or disables interrupt requests from OVF.

Bit 2: OVIE	Description	
0	Disables interrupt requests by OVF	(Initial value)
1	Enables interrupt requests from OVF	

Bit 1—Input Capture/Compare Match Interrupt Enable B (IMIEB): When the IMFB bit in TSR is set to 1, IMIEB enables or disables interrupt requests by IMFB.

Bit 1: IMIEB	Description	
0	Disables interrupt requests by IMFB (IMIB)	(Initial value)
1	Enables interrupt requests by IMFB (IMIB)	

Bit 0—Input Capture/Compare Match Interrupt Enable A (IMIEA): When the IMFA bit in TSR is set to 1, IMIEA enables or disables interrupt requests by IMFA.

Bit 0: IMIEA	Description	
0	Disables interrupt requests by IMFA (IMIA)	(Initial value)
1	Enables interrupt requests by IMFA (IMIA)	

10.3 CPU Interface

10.3.1 16-Bit Accessible Registers

The timer counters (TCNT), general registers A and B (GRA, GRB), and buffer registers A and B (BRA, BRB) are 16-bit registers. The SH CPU can access these registers a word at a time using a 16-bit data bus. Byte access is also possible. Read and write operations performed on TCNT in word units are shown in figures 10.6 and 10.7. Byte-unit read and write operations on TCNTH and TCNTL are shown in figures 10.8 to 10.11.

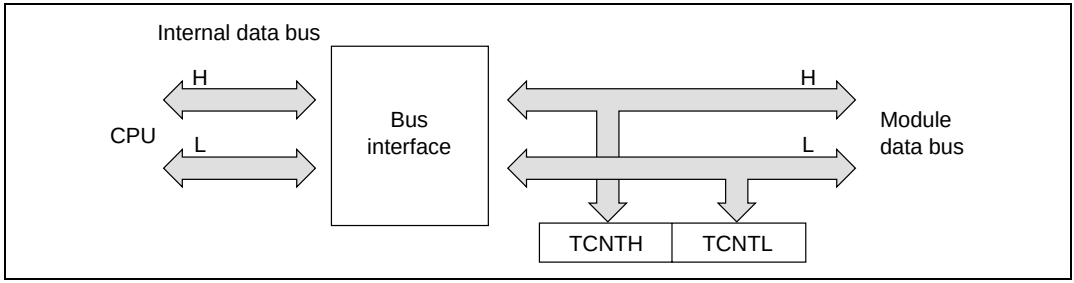


Figure 10.6 TCNT Access (CPU to TCNT (Word))

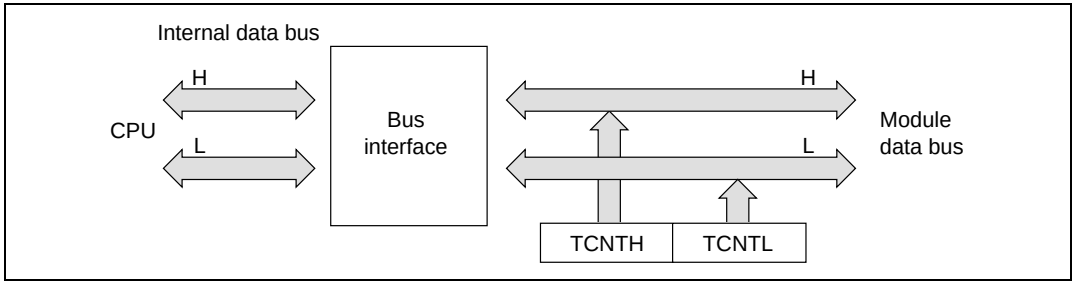


Figure 10.7 TCNT Access (TCNT to CPU (Word))

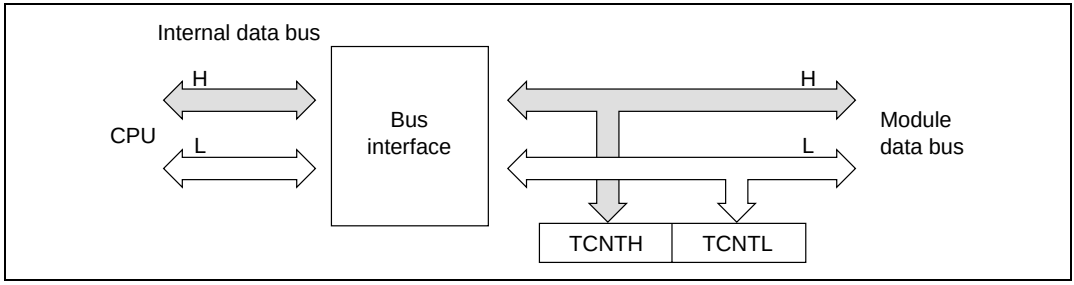


Figure 10.8 TCNT Access (CPU to TCNT (Upper Byte))

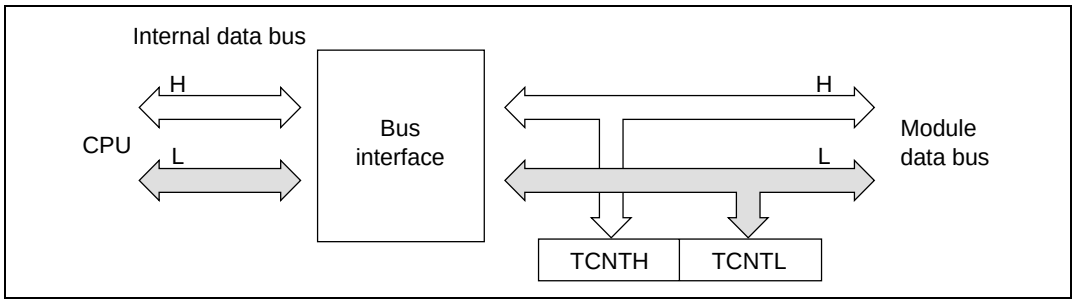


Figure 10.9 TCNT Access (CPU to TCNT (Lower Byte))

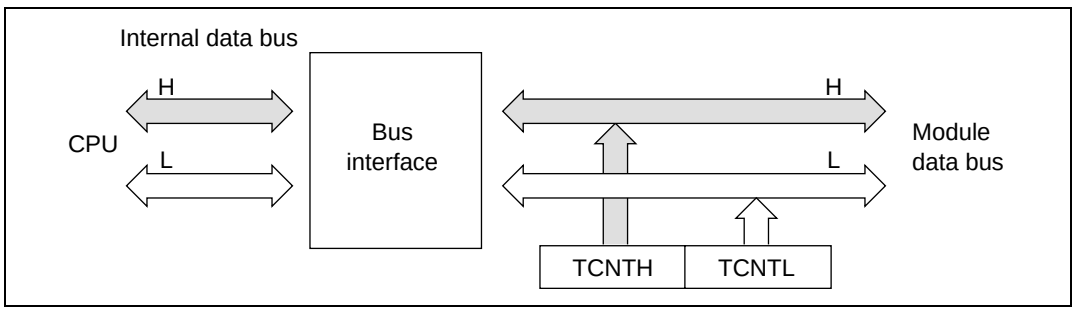


Figure 10.10 TCNT Access (TCNT to CPU (Upper Byte))

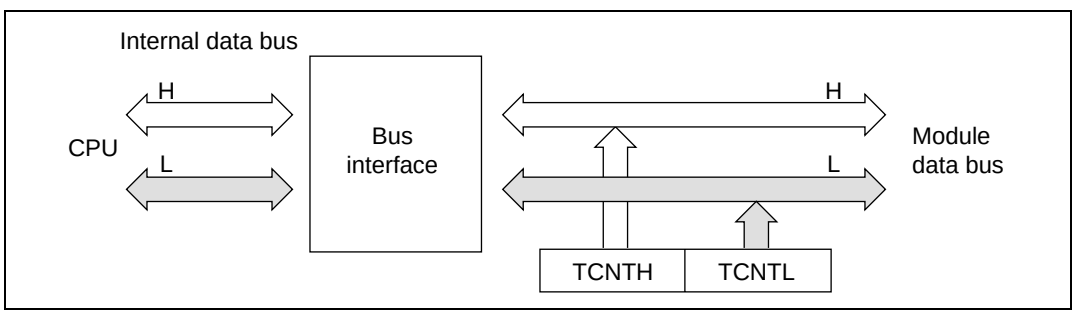


Figure 10.11 TCNT Access (TCNT to CPU (Lower Byte))

10.3.2 8-Bit Accessible Registers

All registers other than the TCNT register, general registers, and buffer registers are 8-bit registers. These are connected to the CPU by an 8-bit data bus. Figures 10.12 and 10.13 illustrate reading and writing in byte units with the timer control register (TCR). These registers must be accessed by byte access.

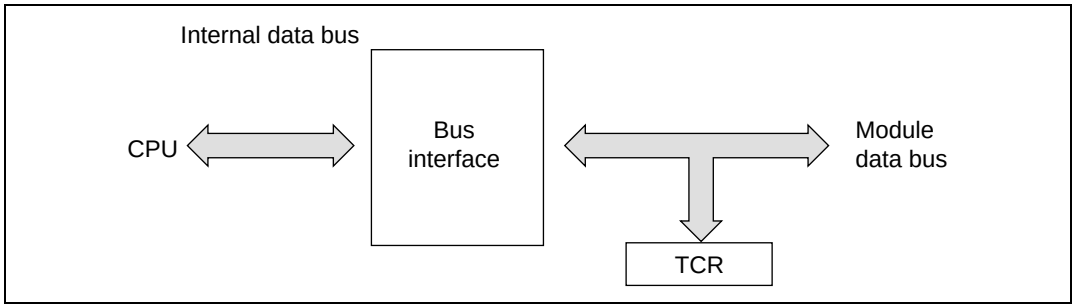


Figure 10.12 TCR Access (CPU to TCR)

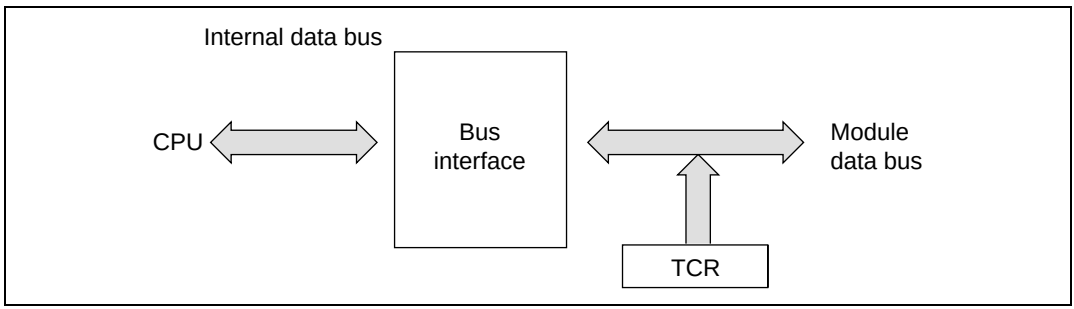


Figure 10.13 TCR Access (TCR to CPU)

10.4 Operation

10.4.1 Overview

The operation modes are described below.

Ordinary Operation: Each channel has a timer counter (TCNT) and general register (GR). The TCNT is an up-counter and can also operate as a free-running counter, periodic counter, or external event counter. General registers A and B (GRA and GRB) can be used as output compare registers or input capture registers.

Synchronized Operation: The TCNT of a channel set for synchronized operation perform synchronized presetting. When any TCNT of a channel operating in the synchronized mode is rewritten, the TCNTs in other channels are simultaneously rewritten as well. The CCLR1 and CCLR0 bits of the timer control register of multiple channels set for synchronous operation can be set to clear the TCNTs simultaneously.

PWM Mode: In PWM mode, a PWM waveform is output from the TIOCA pin. Output becomes 1 upon compare match A and 0 upon compare match B. GRA and GRB can be set so that the PWM waveform output has a duty cycle between 0% and 100%. When set for PWM mode, the GRA and GRB automatically become output compare registers.

Reset-Synchronized PWM Mode: Three pairs of positive and negative PWM waveforms can be obtained using channels 3 and 4 (the three phases of the PWM waveform share a transition point on one side). When set for reset-synchronized PWM mode, GRA3, GRB3, GRA4, and GRB4 automatically become output compare registers. The TIOCA3, TIOCB3, TIOCA4, TOCXA4, TIOCB4, and TOCXB4 pins also become PWM output pins and TCNT3 becomes an up-counter. TCNT4 functions independently (although GRA and GRB are isolated from TCNT4).

Complementary PWM Mode: Three pairs of complementary positive and negative PWM waveforms whose positive and negative phases do not overlap can be obtained using channels 3 and 4. When set for complementary PWM mode, GRA3, GRB3, GRA4, and GRB4 automatically become output compare registers. The TIOCA3, TIOCB3, TIOCA4, TOCXA4, TIOCB4, and TOCXB4 pins also become PWM output pins while TCNT3 and TCNT4 become up-counters.

Phase Counting Mode: In phase counting mode, the phase differential between two clocks input from the TCLKA and TCLKB pins is detected and the TCNT2 operates as an up/down-counter. In phase counting mode, the TCLKA and TCLKB pins become clock inputs and TCNT2 functions as an up/down-counter.

Buffer Mode:

- When GR is an output compare register: The BR value of each channel is transferred to GR when a compare match occurs.
- When GR is an input capture register: The TCNT value is transferred to GR when an input capture occurs and simultaneously the value previously stored in GR is transferred to BR.
- Complementary PWM mode: When TCNT3 and TCNT4 change count directions, the BR value is transferred to GR.
- Reset-synchronized PWM mode: The BR value is transferred to GR upon a GRA3 compare match.

10.4.2 Basic Functions

Counter Operation: When a start bit (STR0–STR4) in the timer start register (TSTR) is set to 1, the corresponding timer counter (TCNT) starts counting. There are two counting modes: a free-running mode and a periodic mode.

- Procedure for selecting counting mode (figure 10.14):
  1. Set bits TPSC2–TPSC0 in TCR to select the counter clock source. If an external clock source is selected, set bits CKEG1 and CKEG0 in TCR to select the desired edge of the external clock signal.
  2. To operate as a periodic counter, set CCLR1 and CCLR0 in TCR to select whether to clear TCNT at GRA compare match or GRB compare match.
  3. Set GRA or GRB selected in step 2 as an output compare register using the timer I/O control register (TIOR).
  4. Write the desired cycle value in GRA or GRB selected in step 1.
  5. Set the STR bit in TSTR to 1 to start counting.

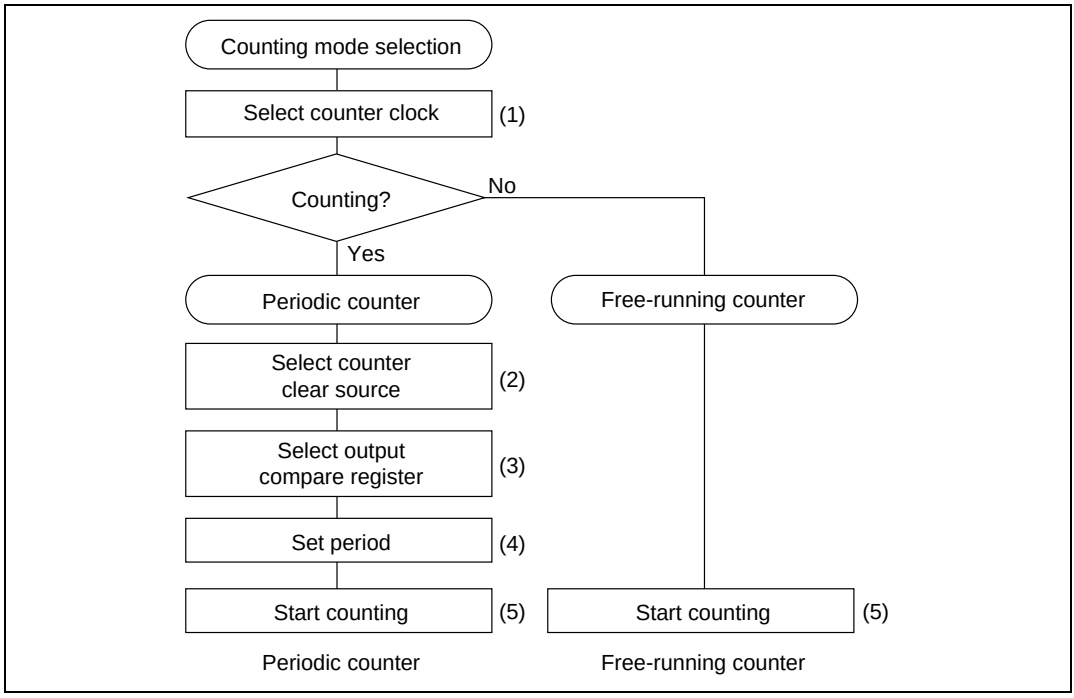


Figure 10.14 Procedure for Selecting the Counting Mode

- Free-running count and periodic count

  A reset of the counters for channels 0–4 leaves them all in free-running mode. When a corresponding bit in TSTR is set to 1, the corresponding timer counter operates as a free-running counter and begins to increment. When the count wraps around from H'FFFF to H'0000, the overflow flag (OVF) in the timer status register (TSR) is set to 1. If the OVIE bit in the timer's corresponding interrupt enable register (TIER) is set to 1, an interrupt request will be sent to the CPU. After TCNT overflows, counting continues from H'0000. Figure 10.15 shows an example of free-running counting.

  Periodic counter operation is obtained for a given channel's TCNT by selecting compare match as a TCNT clear source. (Set GRA or GRB for period setting to output compare register and select counter clear upon compare match using the CCLR1 and CCLR0 bits in the timer control register (TCR).) After setting, TCNT begins incrementing as a periodic counter when the corresponding bit in TSTR is set to 1. When the count matches GRA or GRB, the IMFA/IMFB bit in TSR is set to 1 and the counter is automatically cleared to H'0000. If the IMIEA/IMIEB bit of the corresponding TIER is set to 1 at this point, an interrupt request will be sent to the CPU. After the compare match, TCNT continues counting from H'0000. Figure 10.16 shows an example of periodic counting.

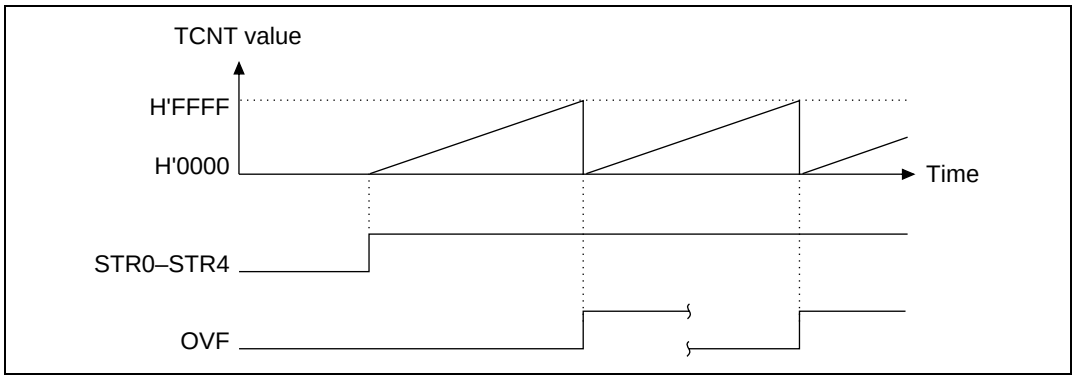


Figure 10.15 Free-Running Counter Operation

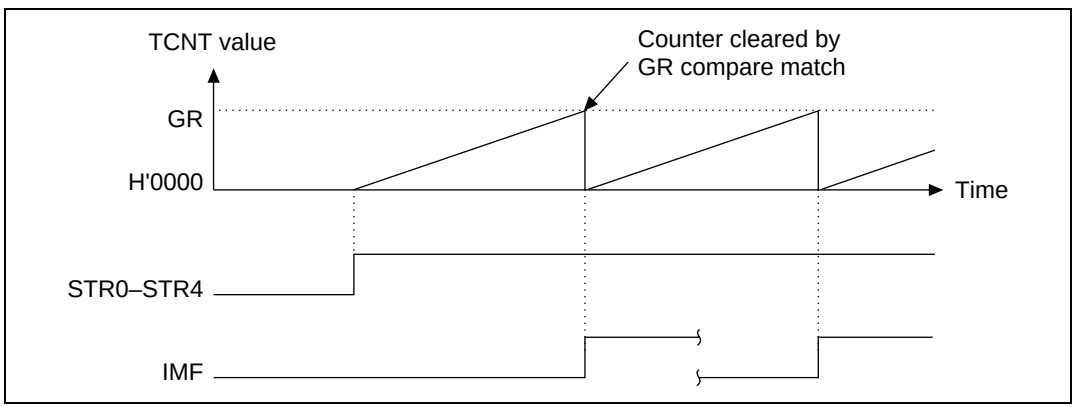


Figure 10.16 Periodic Counter Operation

- TCNT counter timing

  Internal clock source: Bits TPSC2–TPSC0 in TCR select the system clock (CK) or one of three internal clock sources (φ/2, φ/4, φ/8) obtained by prescaling the system clock. Figure 10.17 shows the timing.

  External clock source: The external clock input pin (TCLKA–TCLKD) source is selected by bits TPSC2–TPSC0 in TCR and its valid edges are selected with the CKEG1 and CKEG0 bits in TCR. The rising edge, falling edge, or both edges can be selected. The pulse width of the external clock signal must be at least 1.5 system clocks when a single edge is selected and at least 2.5 system clocks when both edges are selected. Shorter pulses will not be counted correctly. Figure 10.18 shows the timing when both edges are detected.

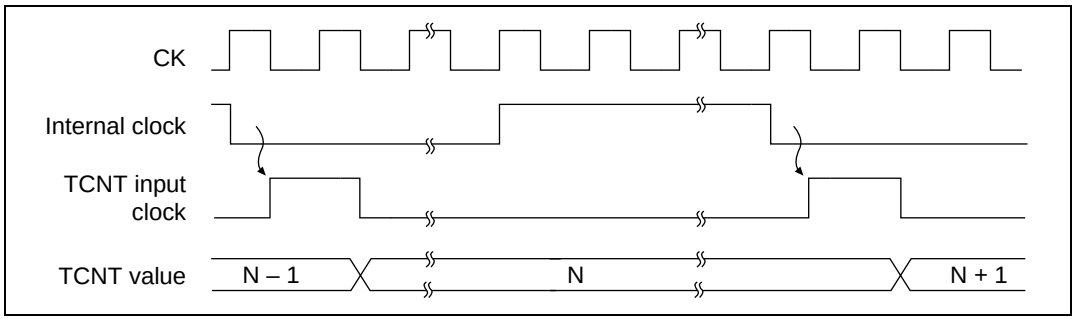


Figure 10.17 Count Timing for Internal Clock Sources

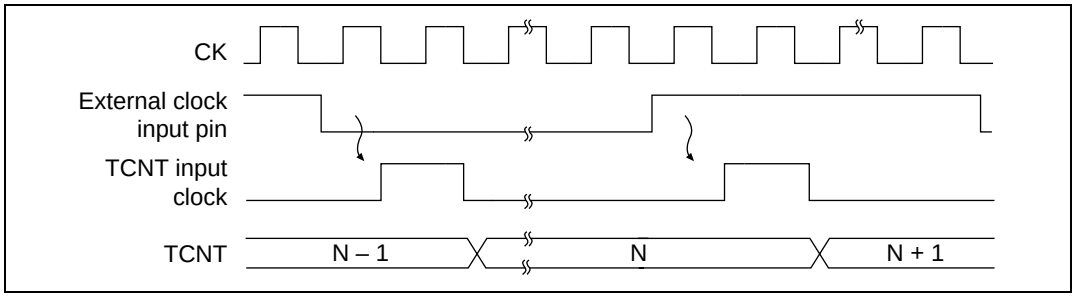


Figure 10.18 Count Timing for External Clock Sources (Both-Edge Detection)

Compare-Match Waveform Output Function: For ITU channels 0, 1, 3, and 4, the output from the corresponding TIOCA and TIOCB pins upon compare matches A and B can be in three modes: 0-level output, 1-level output, or toggle. Toggle output cannot be selected for channel 2.

- Procedure for selecting the waveform output mode (figure 10.19):
  1. Set TIOR to select 0 output, 1 output, or toggle output for compare match output. The compare match output pin will output 0 until the first compare match occurs.
  2. Set a value in GRA or GRB to select the compare match timing.
  3. Set the STR bit in TSTR to 1 to start counting.

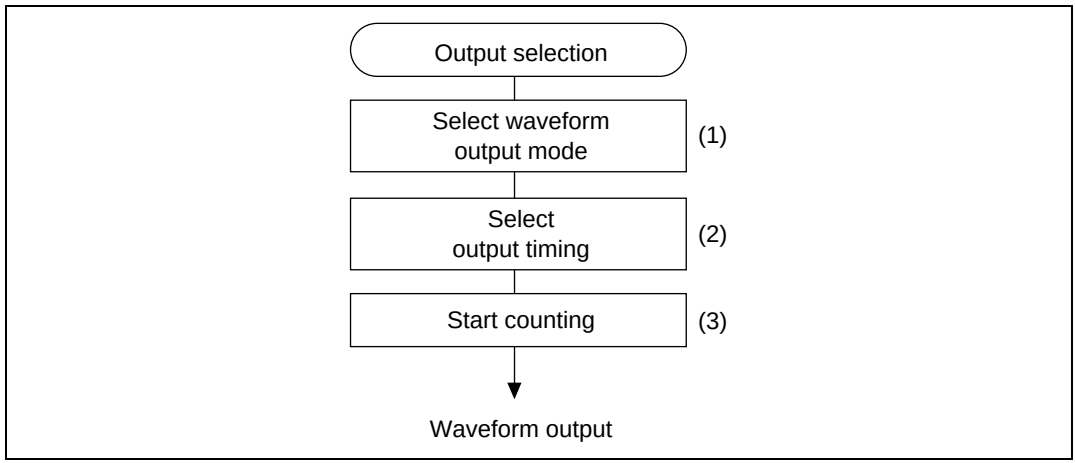


Figure 10.19 Procedure for Selecting Compare Match Waveform Output Mode

- Waveform output operation

  Figure 10.20 illustrates 0 output/1 output. In the example, TCNT is a free-running counter, 0 is output upon compare match A, and 1 is output upon compare match B. When the pin level matches the set level, the pin level does not change.

  Figure 10.21 shows an example of toggle output. In the figure, TCNT operates as a periodic counter cleared by GRB compare match with toggle output at both compare match A and compare match B.

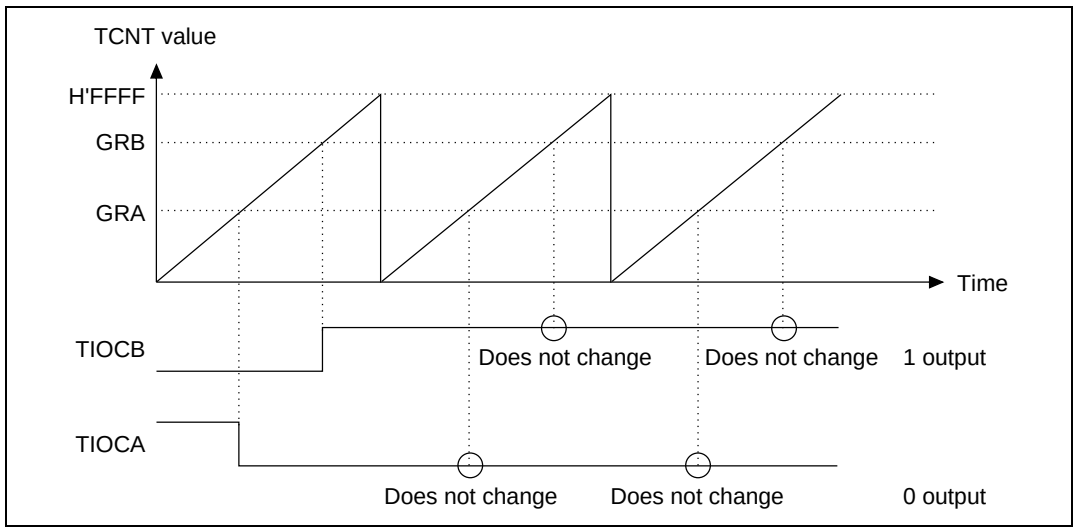


Figure 10.20 Example of 0 Output/1 Output

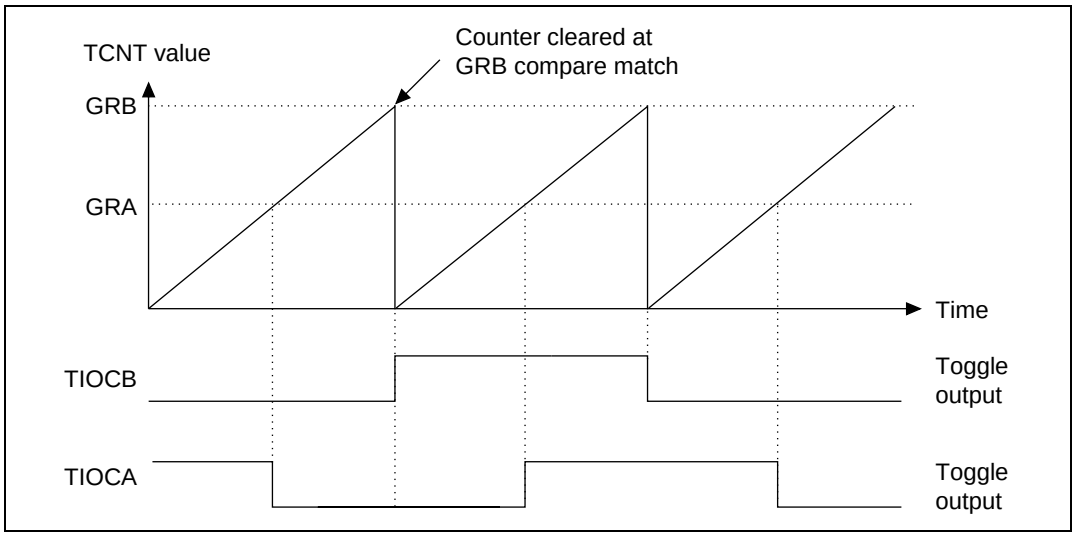


Figure 10.21 Example of Toggle Output

- Compare match output timing

  The compare match signal is generated in the last state in which TCNT and the general register match (when TCNT changes from the matching value to the next value). When a compare match signal is generated, the output value set in TIOR is output to the output compare pin (TIOCA, TIOCB). Accordingly, when TCNT matches a general register, the compare match signal is not generated until the next counter clock pulse. Figure 10.22 shows the output timing of the compare match signal.

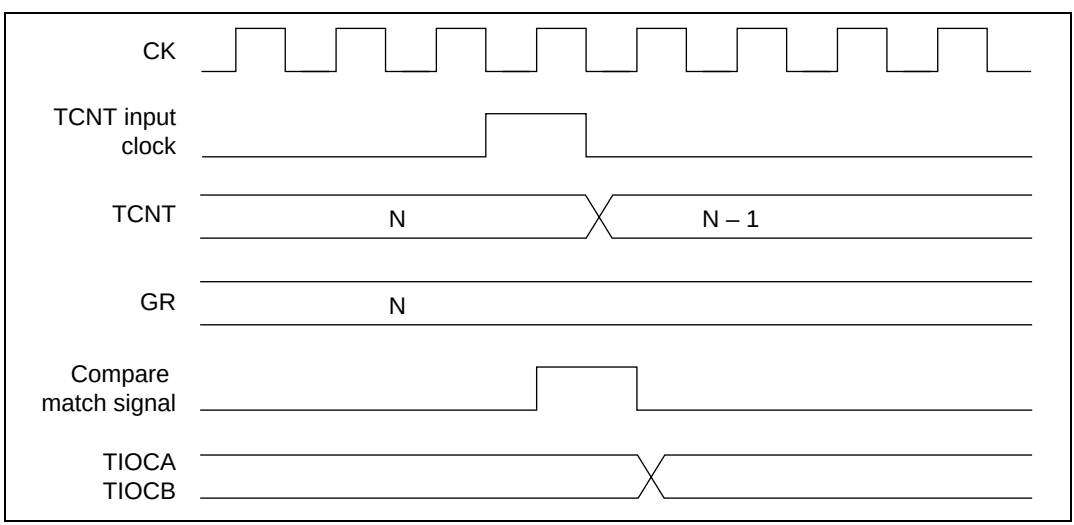


Figure 10.22 Compare Match Signal Output Timing

Input Capture Mode: In input capture mode, the counter value is captured into a general register when the input edge is detected at an input capture/output compare pin (TIOCA, TIOCB).

Detection can take place on the rising edge, falling edge, or both edges. The pulse width and cycle can be measured by using the input capture function.

- Procedure for selecting input capture mode (figure 10.23)
  1. Set TIOR to select the input capture function of GR and select the rising edge, falling edge, or both edges as the input edge of the input capture signal. Put the corresponding port into input-capture mode using the pin function controller before setting TIOR.
  2. Set the STR bit in TSTR to 1 to start the TCNT count.

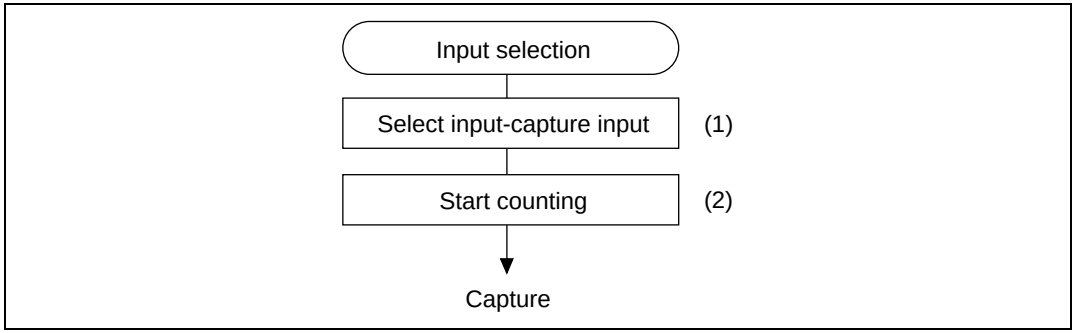


Figure 10.23 Procedure for Selecting Input Capture Mode

- Input capture operation

  Figure 10.24 illustrates input capture. The falling edge of TIOCB and both edges of TIOCA are selected as input capture edges. In the example, TCNT is set to clear at GRB input capture.

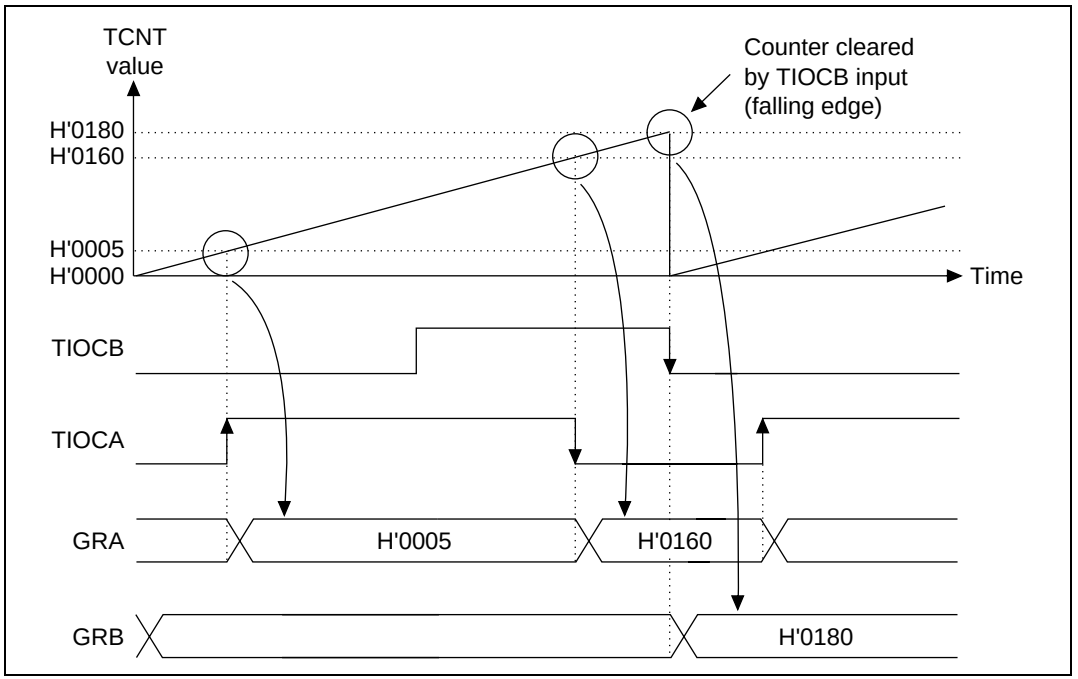


Figure 10.24 Input Capture Operation

- Input capture timing

  Input capture on the rising edge, falling edge, or both edges can be selected by settings in TIOR. Figure 10.25 shows the timing when the rising edge is selected. The pulse width of the input capture signal must be at least 1.5 system clocks for single-edge capture, and 2.5 system clocks for capture of both edges.

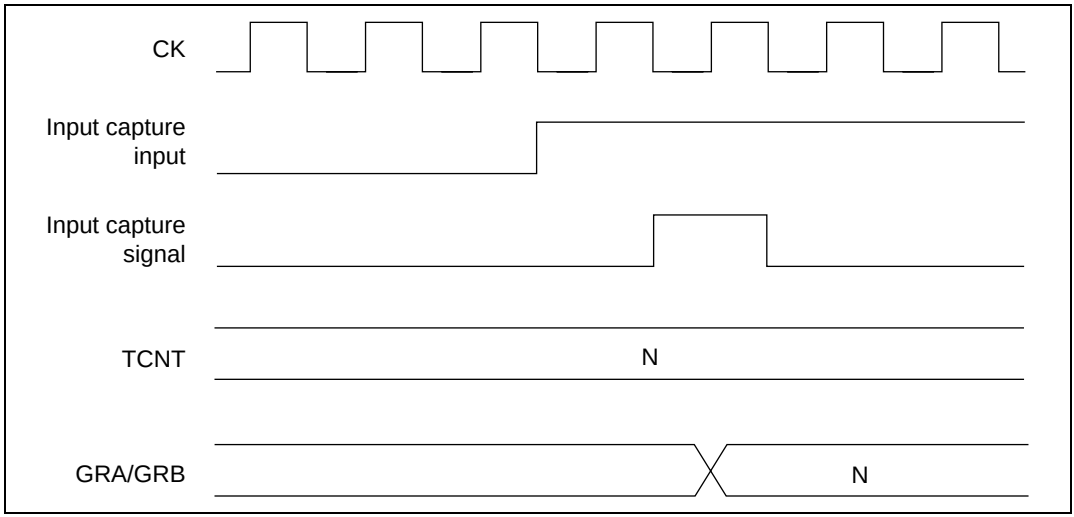


Figure 10.25 Input Capture Signal Timing

10.4.3 Synchronizing Mode

In synchronizing mode, two or more timer counters can be rewritten simultaneously (synchronized preset). Multiple timer counters can also be cleared simultaneously using TCR settings (synchronized clear). Synchronizing mode enables the general registers to be incremented with a single time base. All five channels can be set for synchronous operation.

Procedure for Selecting Synchronizing Mode (figure 10.26):

1. Set 1 in the SYNC bit of the timer synchro register (TSNC) to use the channels in the synchronizing mode.
2. When a value is written in TCNT in any of the synchronized channels, the same value is simultaneously written in TCNT in the other channels.
3. Set the counter to clear with compare match/input capture using bits CCLR1 and CCLR0 in TCR.
4. Set the counter clear source to synchronized clear using the CCLR1 and CCLR0 bits.
5. Set the STR bits in TSTR to 1 to start the TCNT count.

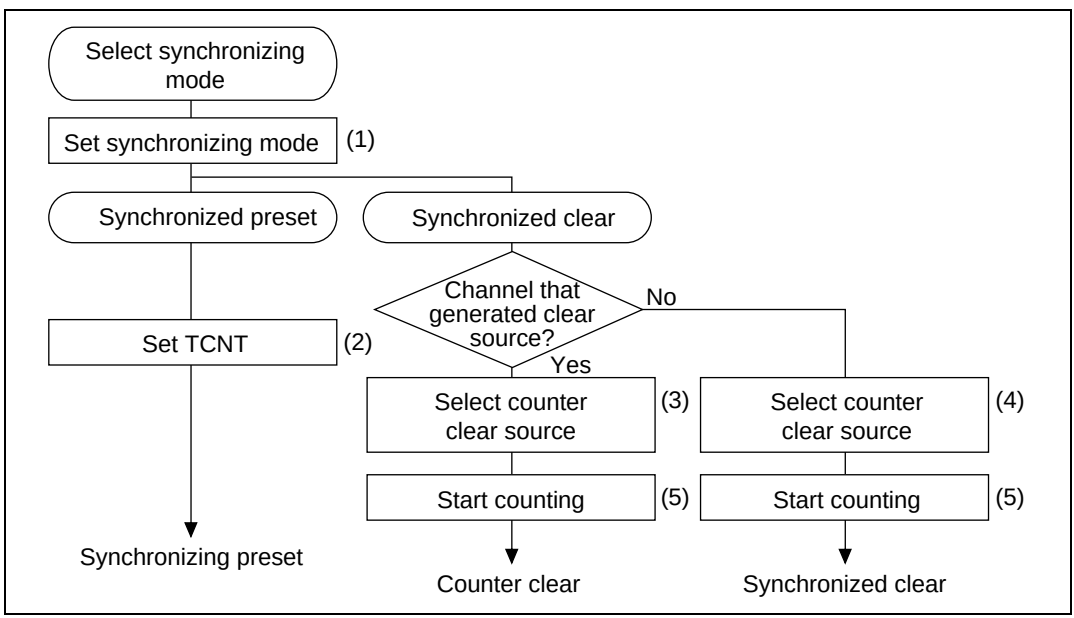


Figure 10.26 Procedure for Selecting Synchronizing Mode

Synchronized Operation: Figure 10.27 shows an example of synchronized operation. Channels 0, 1, and 2 are set to synchronized operation and PWM output. Channel 0 is set for a counter clear upon compare match with GRB0. Channels 1 and 2 are set for counter clears by synchronizing clears. Accordingly, their timers are sync preset, then sync cleared by a GRB0 compare match, and then a three-phase PWM waveform is output from the TIOCA0, TIOCA1, and TIOCA2 pins. See section 10.4.4, PWM Mode, for details on PWM mode.

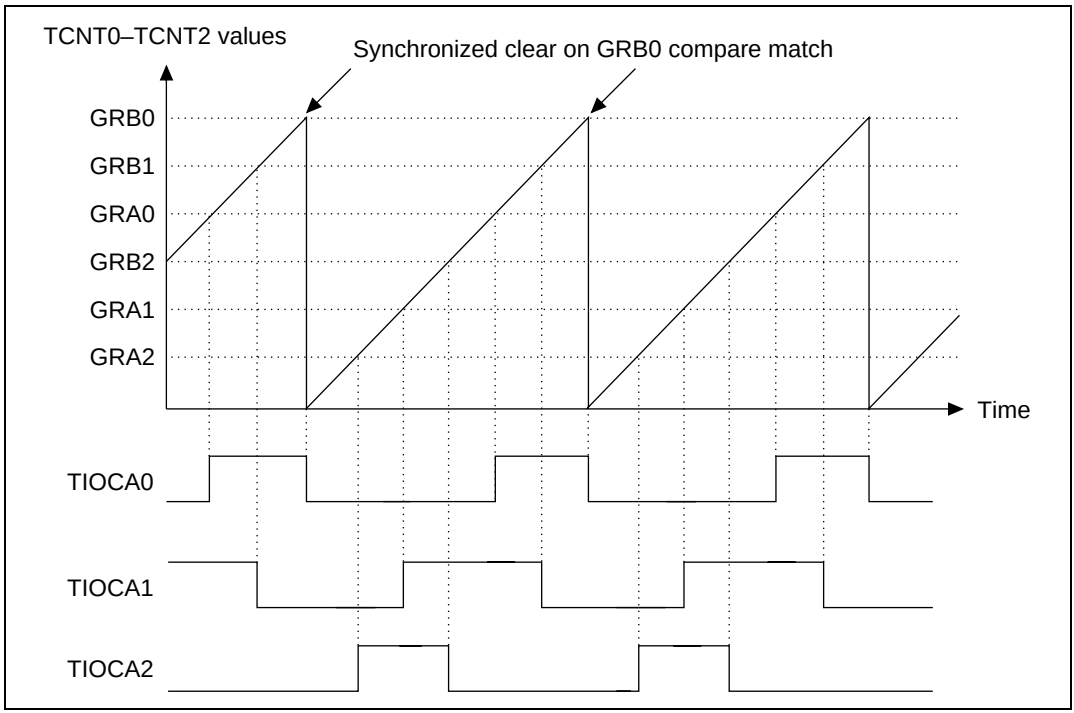


Figure 10.27 Example of Synchronized Operation

10.4.4 PWM Mode

PWM mode is controlled using both GRA and GRB in pairs. The PWM waveform is output from the TIOCA output pin. The PWM waveform's 1 output timing is set in GRA and the 0 output timing is set in GRB. A PWM waveform with a duty cycle between 0% and 100% can be output from the TIOCA pin by selecting either compare match GRA or GRB as the counter clear source for the timer counter. All five channels can be set to PWM mode.

Table 10.11 lists the combinations of PWM output pins and registers. Note that when GRA and GRB are set to the same value, the output will not change even if a compare match occurs.

Table 10.11 Combinations of PWM Output Pins and Registers

Channel	Output Pin	1 Output	0 Output
0	TIOCA0	GRA0	GRB0
1	TIOCA1	GRA1	GRB1
2	TIOCA2	GRA2	GRB2
3	TIOCA3	GRA3	GRB3
4	TIOCA4	GRA4	GRB4

Procedure for Selecting PWM Mode (Figure 10.28):

1. Set bits TPSC2–TPSC0 in TCR to select the counter clock source. If an external clock source is selected, set bits CKEG1 and CKEG0 in TCR to select the desired edge of the external clock signal.
2. Set CCLR1 and CCLR0 in TCR to select the counter clear source.
3. Set the time at which the PWM waveform should go to 1 in GRA.
4. Set the time at which the PWM waveform should go to 0 in GRB.
5. Set the PWM bit in TMDR to select PWM mode. When PWM mode is selected, regardless of the contents of TIOR, GRA and GRB become output compare registers specifying the times at which the PWM waveform goes high and low. TIOCA becomes a PWM output pin. TIOCB functions according to the setting of bits IOB1 and IOB0 in TIOR.
6. Set the STR bit in TSTR to start the TCNT count.

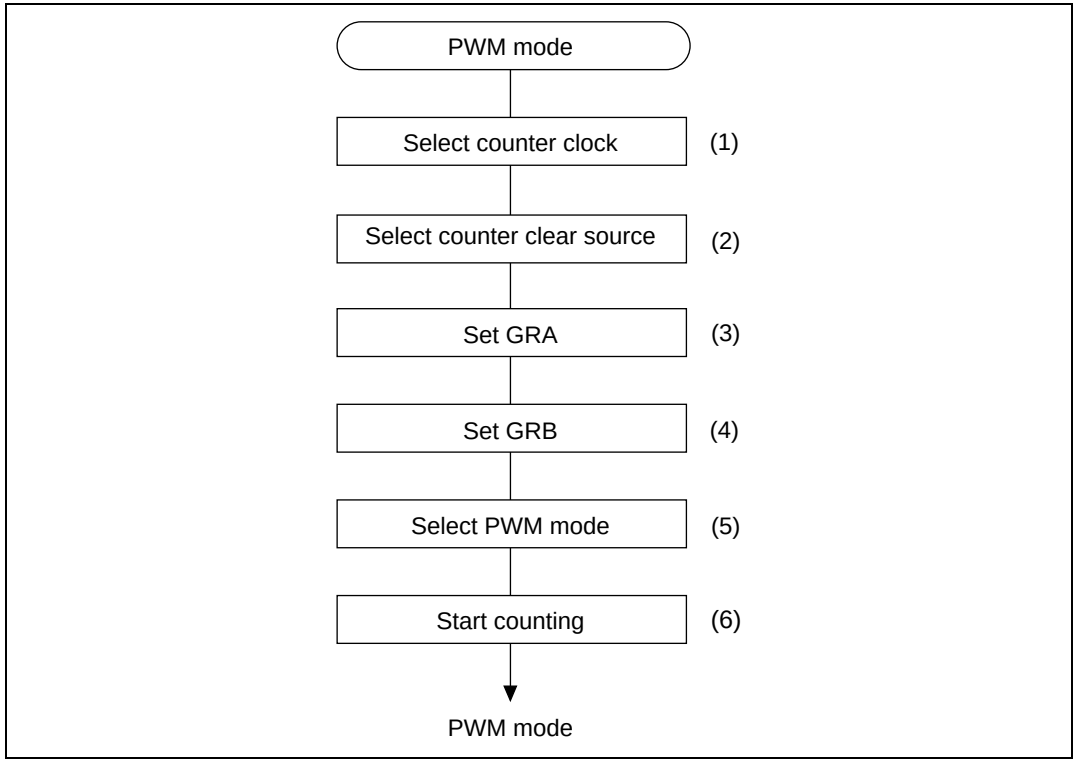
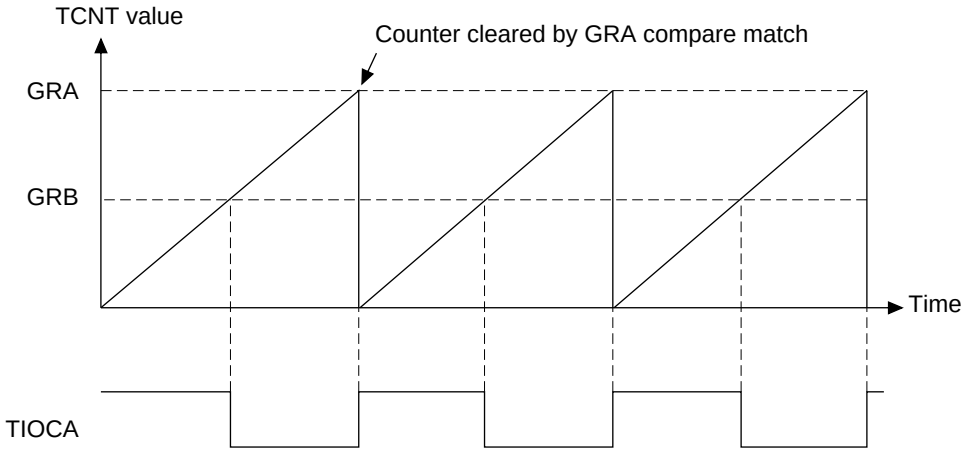


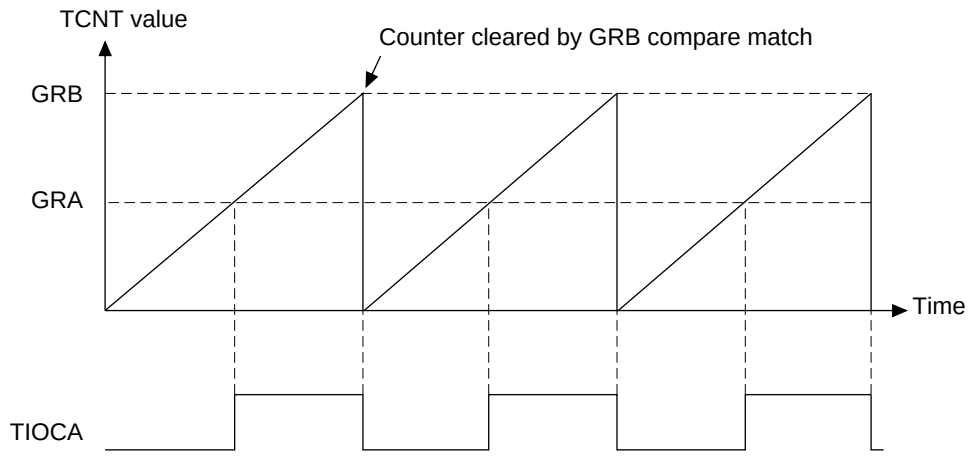
Figure 10.28 Procedure for Selecting PWM Mode

PWM Mode Operation: Figure 10.29 illustrates PWM mode operation. When PWM mode is set, the TIOCA pin becomes the output pin. Output is 1 when TCNT matches GRA, and 0 when TCNT matches GRB. TCNT can be cleared by compare match with either GRA or GRB. This can be used in both free-running and synchronized operation.

Figure 10.30 shows examples of PWM waveforms output with 0% and 100% duty cycles. A 0% duty waveform can be obtained by setting the counter clear source to GRB and then setting GRA to a larger value than GRB. A 100% duty waveform can be obtained by setting the counter clear source to GRA and then setting GRB to a larger value than GRA.

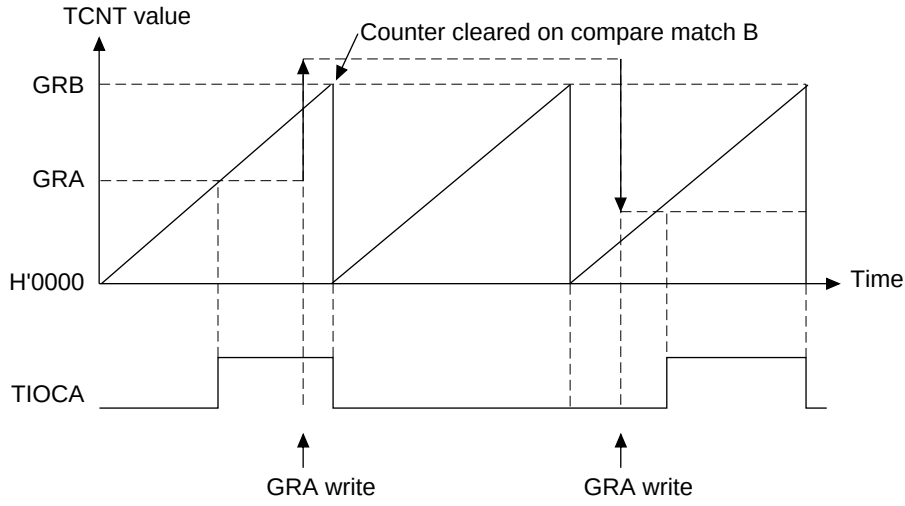


a. Counter cleared by GRA

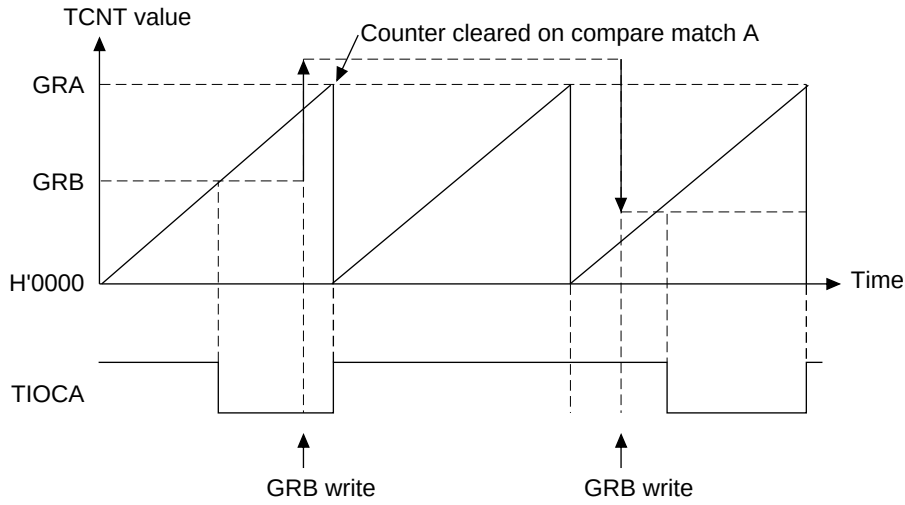


b. Counter cleared by GRB

Figure 10.29 PWM Mode Operation Example 1



a. 0% duty



b. 100% duty

Figure 10.30 PWM Mode Operation Example 2

10.4.5 Reset-Synchronized PWM Mode

In reset-synchronized PWM mode, three pairs of complementary positive and negative PWM waveforms that share a common wave turning point can be obtained using channels 3 and 4. When set for reset-synchronized PWM mode, the TIOCA3, TIOCB3, TIOCA4, TOCXA4, TIOCB4, and TOCXB4 pins become PWM output pins and TCNT3 becomes an up-counter. Table 10.12 shows the PWM output pins used and table 10.13 shows the settings of the registers used.

Table 10.12 Output Pins for Reset-Synchronized PWM Mode

Channel	Output Pin	Description
3	TIOCA3	PWM output 1
	TIOCB3	PWM output 1' (negative-phase waveform of PWM output 1)
4	TIOCA4	PWM output 2
	TOCXA4	PWM output 2' (negative-phase waveform of PWM output 2)
	TIOCB4	PWM output 3
	TOCXB4	PWM output 3' (negative-phase waveform of PWM output 3)

Table 10.13 Register Settings for Reset-Synchronized PWM Mode

Register	Setting
TCNT3	Initial setting of H'0000
TCNT4	Not used (functions independently)
GRA3	Sets count cycle for TCNT3
GRB3	Sets the turning point for PWM waveform output by the TIOCA3 and TIOCB3 pins
GRA4	Sets the turning point for PWM waveform output by the TIOCA4 and TOCXA4 pins
GRB4	Sets the turning point for PWM waveform output by the TIOCB4 and TOCXB4 pins

Procedure for Selecting Reset-Synchronized PWM Mode (figure 10.31):

1. Clear the STR3 bit in TSTR to halt TCNT3. Reset-synchronized PWM mode must be set while TCNT3 is halted.
2. Set bits TPSC2-TPSC0 in TCR to select the counter clock source for channel 3. If an external clock source is selected, select the external clock edge with bits CKEG1 and CKEG0 in TCR.
3. Set bits CCLR1 and CCLR0 in TCR3 to select GRA3 as a counter clear source.
4. Set bits CMD1 and CMD0 in TFCR to select reset-synchronized PWM mode. TIOCA3, TIOCB3, TIOCA4, TIOCB4, TOCXA4, and TOCXB4 become PWM output pins.
5. Reset TCNT3 (to H'0000). TCNT4 need not be set.

6. GRA3 is the waveform period register. Set the waveform period value in GRA3. Set the transition times of the PWM output waveforms in GRB3, GRA4, and GRB4. Set times within the compare match range of TCNT3.

   $X \leq GRA3$ (X: set value)

7. Set the PFC for the external pin to be used.
8. Set the STR3 bit in TSTR to 1 to start the TCNT3 count.

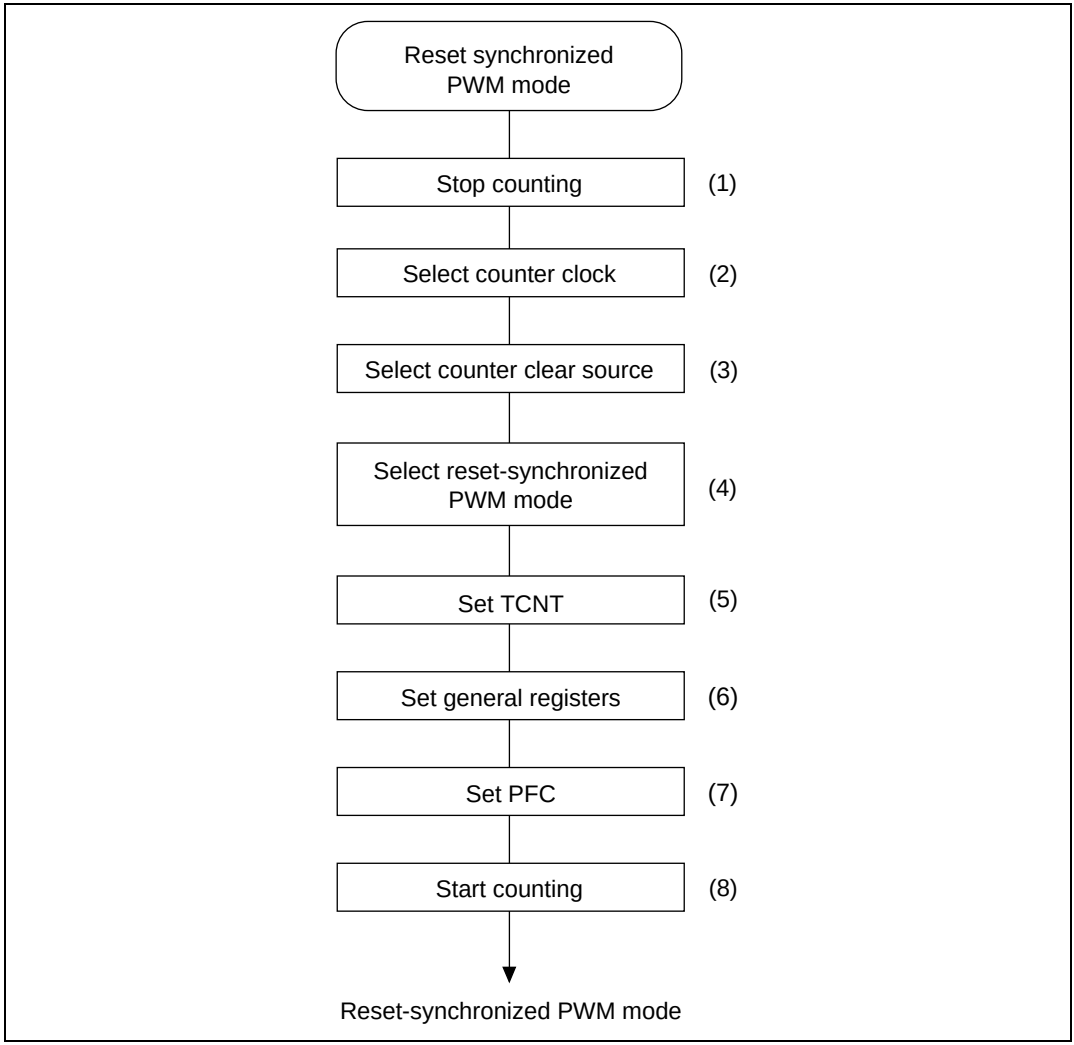


Figure 10.31 Procedure for Selecting Reset-Synchronized PWM Mode

Reset-Synchronized PWM Mode Operation: Figure 10.32 shows an example of operation in reset-synchronized PWM mode. TCNT3 operates as an up-counter that is cleared to H'0000 at compare match with GRA3. TCNT4 runs independently and is isolated from GRA4 and GRB4. The PWM waveform outputs toggle at each compare match (GRB3, GRA3, and GRB4 with TCNT3) and when the counter is cleared.

See section 10.4.8, Buffer Mode, for details on simultaneously setting reset-synchronized PWM mode and buffer operation.

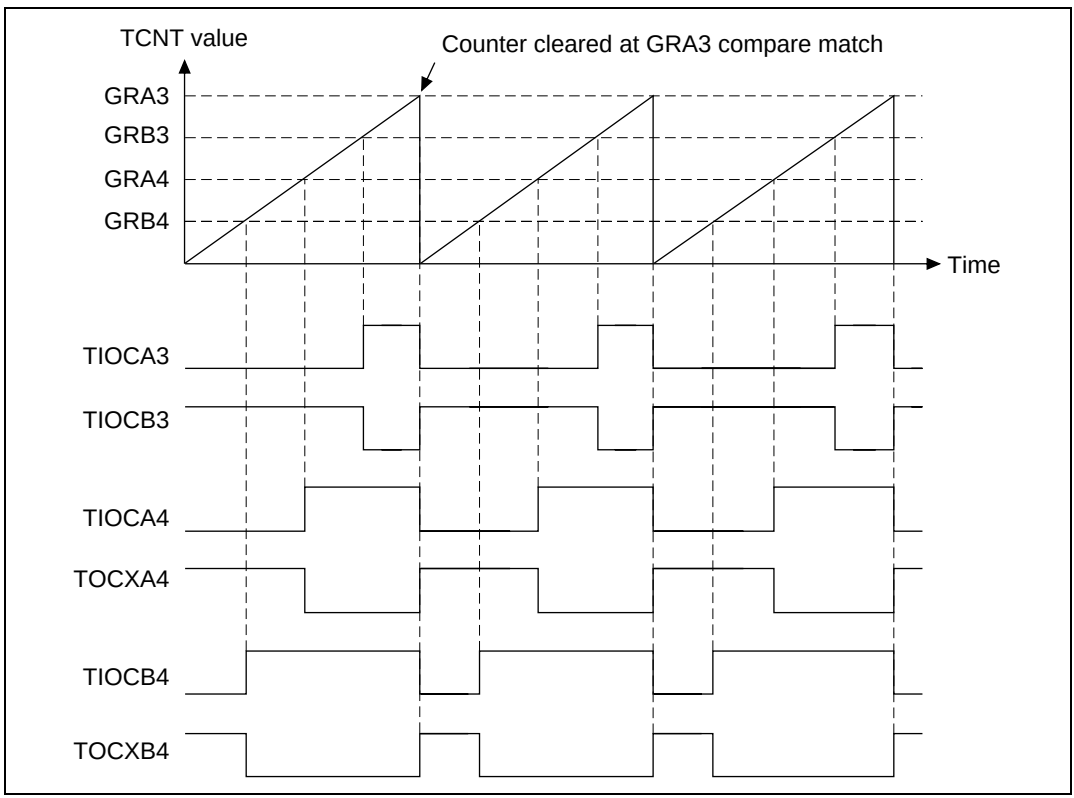


Figure 10.32 Reset-Synchronized PWM Mode Operation Example 1

10.4.6 Complementary PWM Mode

In complementary PWM mode, three pairs of complementary, non-overlapping, positive and negative PWM waveforms can be obtained using channels 3 and 4. In complementary PWM mode, the TIOCA3, TIOCB3, TIOCA4, TOCXA4, TIOCB4, and TOCXB4 pins become PWM output pins and TCNT3 and TCNT4 become up-counters. Table 10.14 shows the PWM output pins used and table 10.15 shows the settings of the registers used.

Table 10.14 Output Pins for Complementary PWM Mode

Channel	Output Pin	Description
3	TIOCA3	PWM output 1
	TIOCB3	PWM output 1' (non-overlapping negative-phase waveform of PWM output 1)
4	TIOCA4	PWM output 2
	TOCXA4	PWM output 2' (non-overlapping negative-phase waveform of PWM output 2)
	TIOCB4	PWM output 3
	TOCXB4	PWM output 3' (non-overlapping negative-phase waveform of PWM output 3)

Table 10.15 Register Settings for Complementary PWM Mode

Register	Setting
TCNT3	Initial setting of non-overlap cycle (difference with TCNT4)
TCNT4	Initial setting of H'0000
GRA3	Sets upper limit of TCNT3–1
GRB3	Sets the turning point for PWM waveform output by the TIOCA3 and TIOCB3 pins
GRA4	Sets the turning point for PWM waveform output by the TIOCA4 and TOCXA4 pins
GRB4	Sets the turning point for PWM waveform output by the TIOCB4 and TOCXB4 pins

Procedure for Selecting Complementary PWM Mode (Figure 10.33):

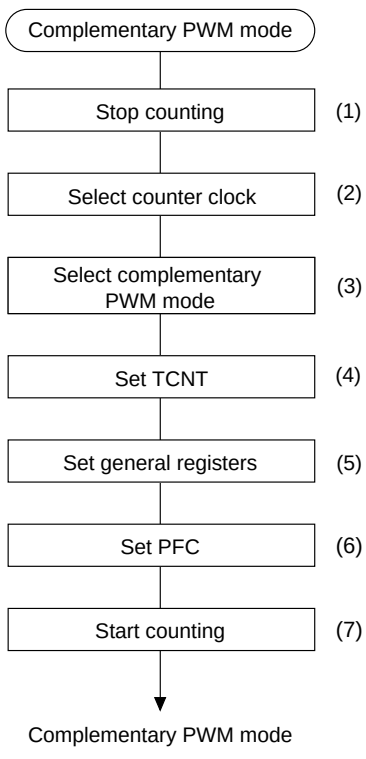
1. Clear the STR3 and STR4 bits in TSTR to halt the timer counters. Complementary PWM mode must be set while TCNT3 and TCNT4 are halted.
2. Set bits TPSC2–TPSC0 in TCR to select the same counter clock source for channels 3 and 4. If an external clock source is selected, select the external clock edge with bits CKEG1 and CKEG0 in TCR. Do not select any counter clear source with bits CCLR1 and CCLR0 in TCR.

3. Set bits CMD1 and CMD0 in TMDB to select complementary PWM mode. TIOCA3, TIOCB3, TIOCA4, TIOCB4, TOCXA4, and TOCXB4 become PWM pins.
4. Reset TCNT4 (to H'0000). Set the non-overlap offset in TCNT3. Do not set TCNT3 and TCNT4 to the same value.
5. GRA3 is the waveform period register. Set the upper limit of TCNT3–1*. Set the transition times of the PWM output waveforms in GRB3, GRA4, and GRB4. Set times within the compare match range of TCNT3 and TCNT4.

   $T \leq X$

   (X: initial setting of GRB3, GRA4, and GRB4; T: initial setting of TCNT3)

   Note: * GRA3 = [cycle count/2] + [count of non-overlaps] - 2cyc=[upper limit of TCNT3]-1
6. Set the PFC for the external pin to be used.
7. Set the STR3 and STR4 bits in TSTR to 1 to start the TCNT3 and TCNT4 counts.



Note: To re-establish complementary PWM mode after it has been aborted, start settings from step 1.

Figure 10.33 Procedure for Selecting Complementary PWM Mode

Complementary PWM Mode Operation: Figure 10.34 shows an example of operation in complementary PWM mode. TCNT3 and TCNT4 operate as up/down-counters, counting down from compare match of TCNT3 and GRA3 and counting up when TCNT4 underflows. PWM waveforms are output by repeated compare matches with GRB3, GRA4, and GRB4 in the sequence TCNT3, TCNT4, TCNT4, TCNT3 (in this mode, TCNT3 starts out at a higher value than TCNT4).

Figure 10.35 shows examples of PWM waveforms with 0% and 100% duty cycles (in one phase) in complementary PWM mode. In this example, the pin output changes upon GRB3 compare match, so duty cycles of 0% and 100% can be obtained by setting GRB3 to a value larger than GRA3. Combining buffer operation with the above operation makes it easy to change the duty while operating. See section 10.4.8, Buffer Mode, for details.

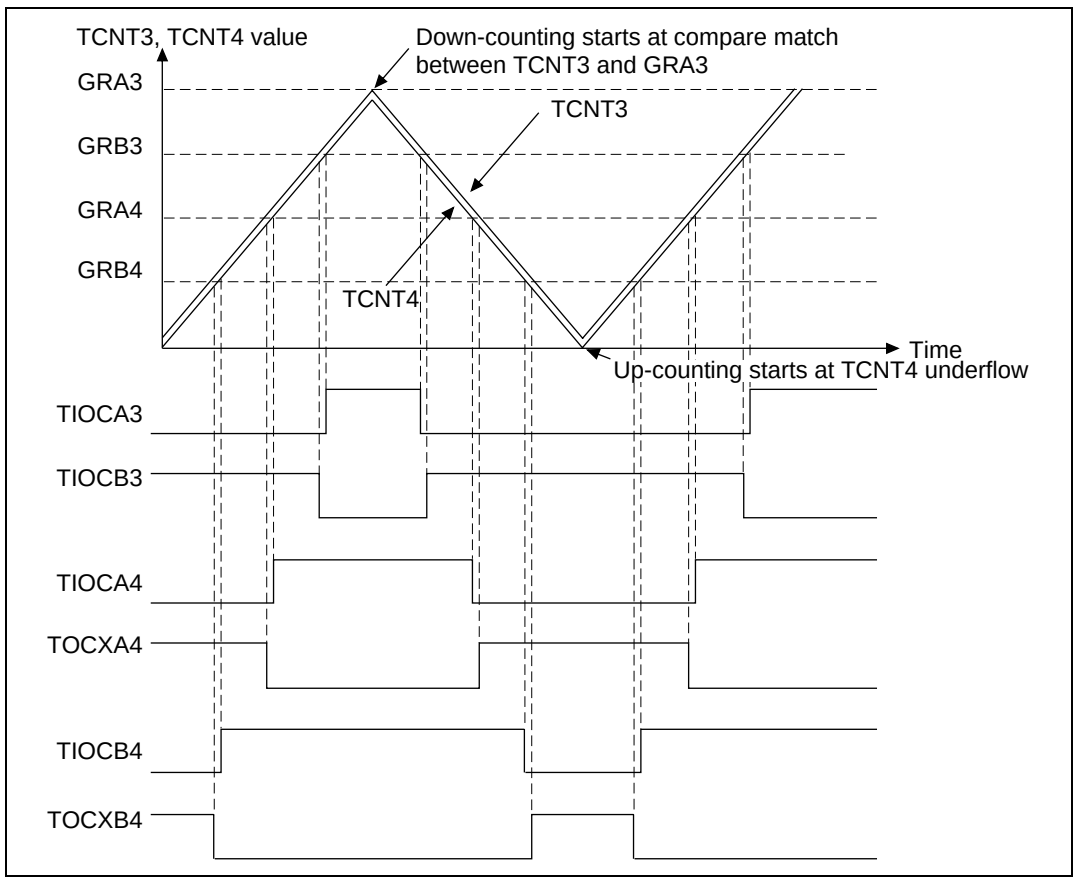


Figure 10.34 Complementary PWM Mode Operation Example 1

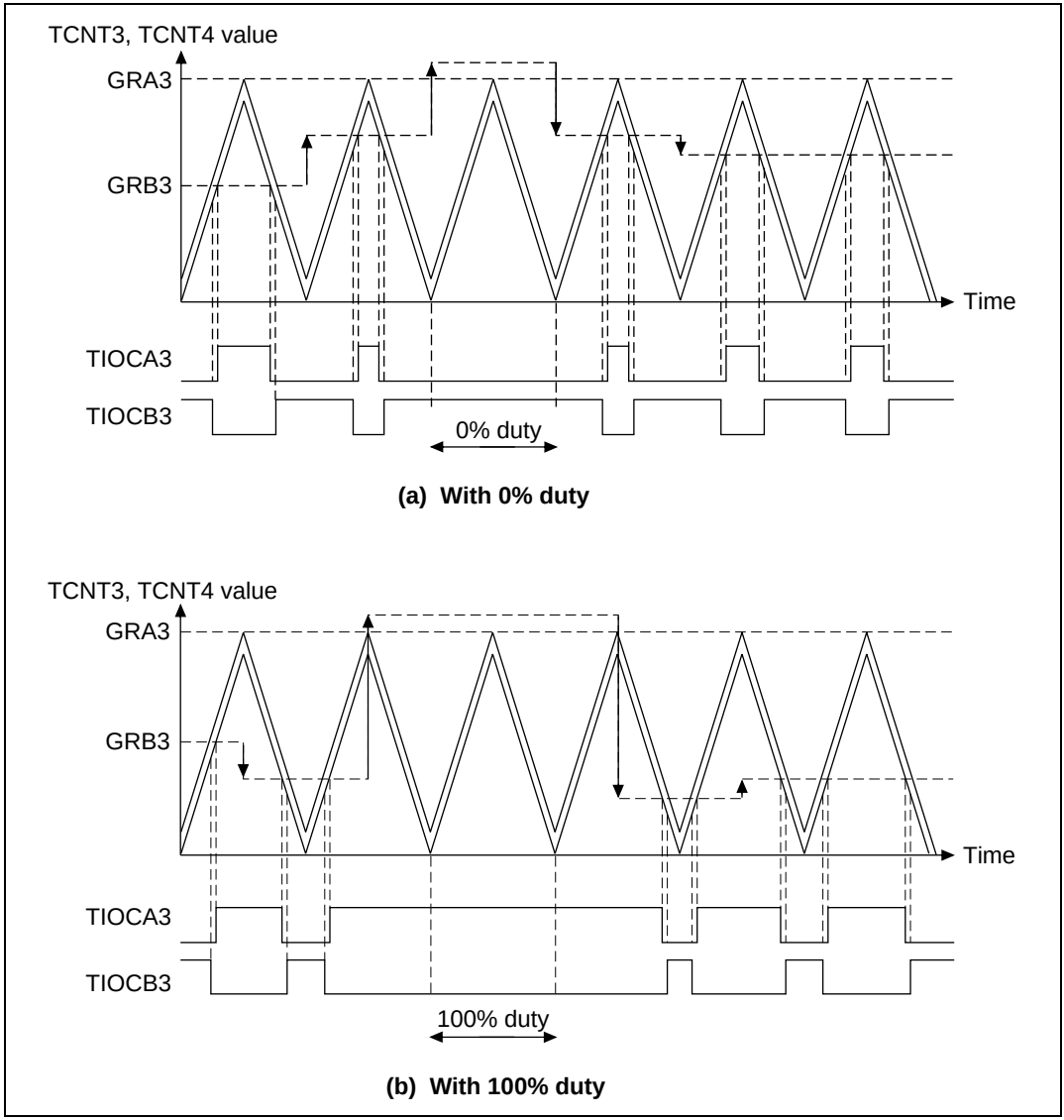


Figure 10.35 Complementary PWM Mode Operation Example 2

At the point where the up-count/down-count changes in complementary PWM mode, TCNT3 and TCNT4 will overshoot and undershoot, respectively. When this occurs, the setting conditions for the IMFA bit of channel 3 and the overflow flag (OVF) of channel 4 are different from usual. Transfer conditions for the buffer also differ. The timing is as shown in figures 10.36 and 10.37.

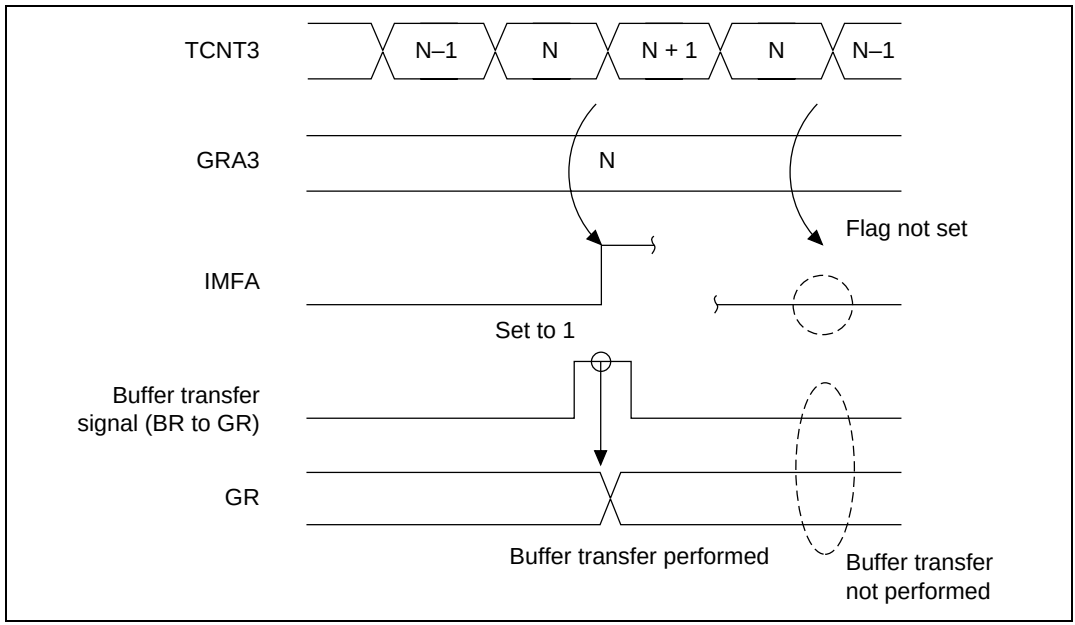


Figure 10.36 Overshoot Timing

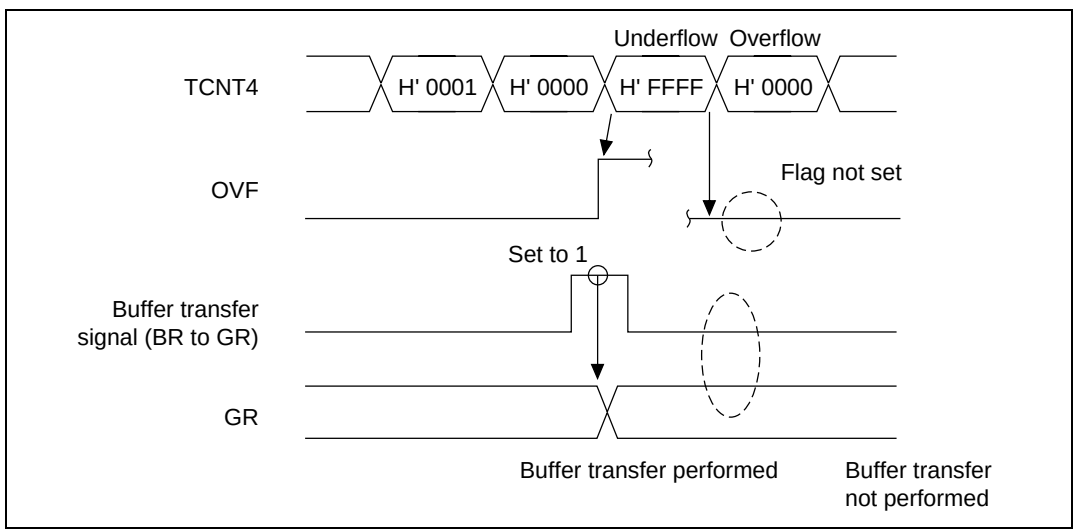


Figure 10.37 Undershoot Timing

The IMFA bit of channel 3 is set to 1 for increment pulses and the OVF bit of channel 4 is set to 1 for underflows only. The buffer register (BR) set for the buffer operation is transferred to GR upon compare match A3 (when incrementing) or TCNT4 underflow.

GR Setting in Complementary PWM Mode: Note the following when setting the general registers in complementary PWM mode and when making changes during operation.

- Initial values: Settings from H'0000 to T–1 (T: TCNT3 initial setting) are prohibited. After counting starts, this setting is allowed from the point when the first A3 compare match occurs.
- Methods of changing settings: Use buffer operation. Writing directly to general registers may result in incorrect waveform output.
- When changing settings: See figure 10.38.

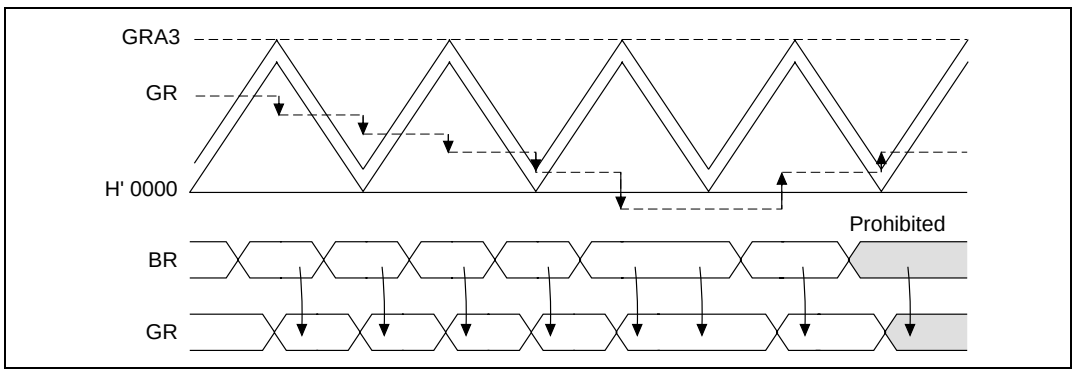


Figure 10.38 Example of Changing GR Settings with Buffer Operation (1)

Buffer Transfers when Changing from Increment to Decrement: When the contents of GR are in the range GRA3 – T + 1 to GRA3, do not transfer a value outside this range. When the contents of GR are outside this range, do not a transfer a value within it. Figure 10.39 illustrates a point for caution regarding changing of GR settings with buffer operation.

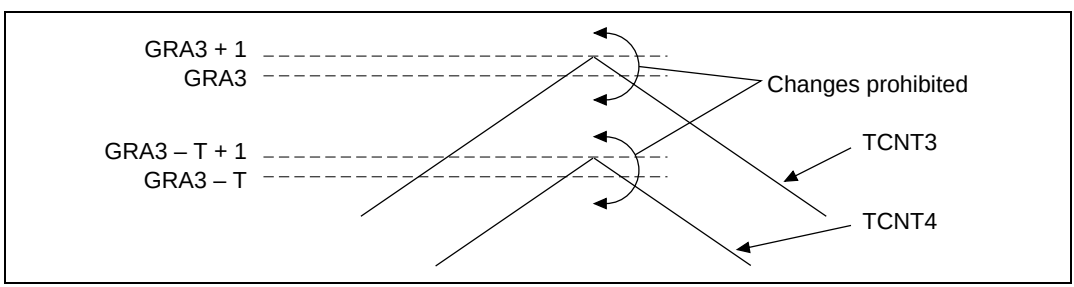


Figure 10.39 Caution on Changing GR Settings with Buffer Operation (1)

Buffer Transfers when Changing from Decrement to Increment: When the contents of GR are in the range H'0000 to T–1, do not transfer a value outside this range. When the contents of GR are outside this range, do not transfer a value within it. Figure 10.40 illustrates this point for caution regarding changing of GR settings with buffer operation

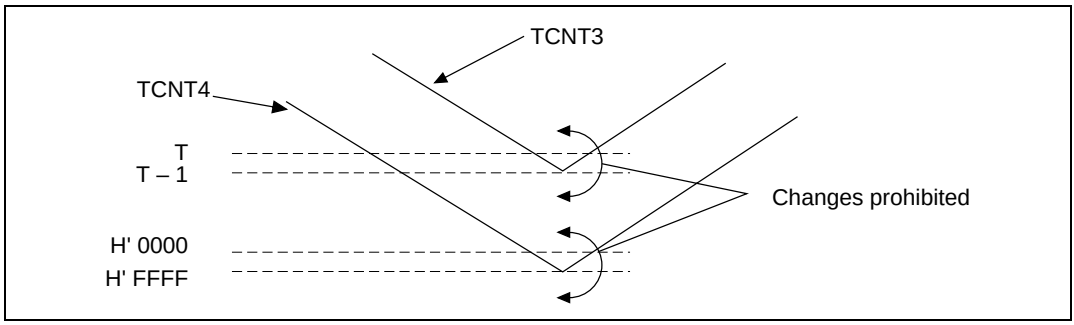


Figure 10.40 Caution on Changing GR Settings with Buffer Operation (2)

When GR Settings are Outside the Count Range (H'0000–GRA3): Waveforms with a duty cycle of 0% and 100% can be output by setting GR outside the count area. Be sure to make the direction of the count (increment/decrement) when writing a setting from outside the count area into the buffer register (BR) the same as the count direction when writing the setting that returns to within the count area in BR.

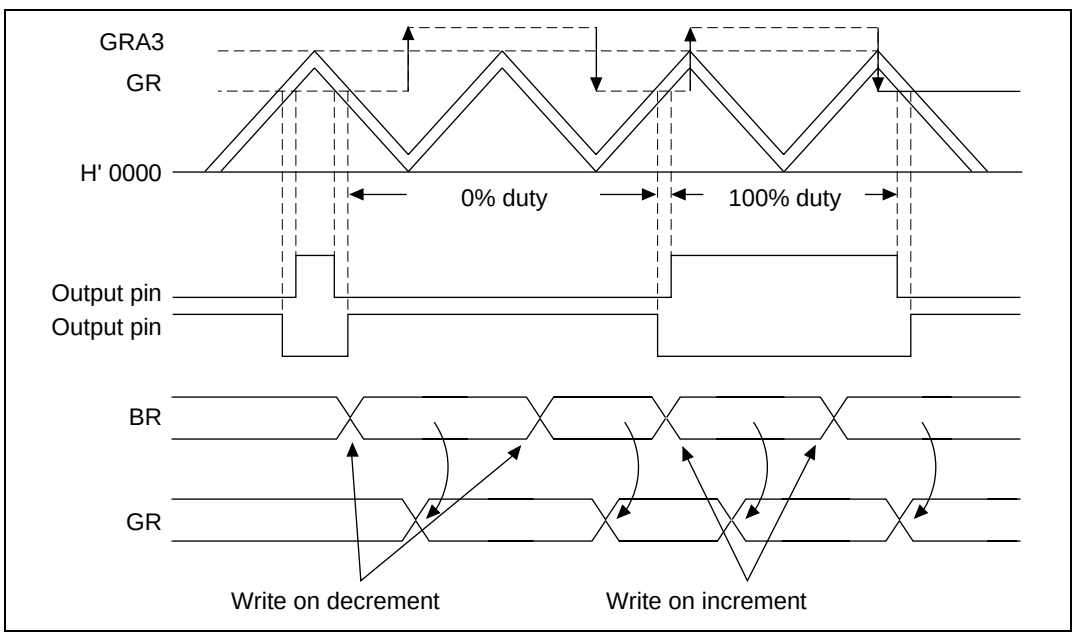


Figure 10.41 Example of Changing GR Settings with Buffer Operation (2)

The above settings are made by detecting the occurrence of a GRA3 compare match or underflow of TCNT4 and then writing to BR. They can also be accomplished by starting the DMAC with a GRA3 compare match.

10.4.7 Phase Counting Mode

Phase counting mode detects the phase differential of two external clock inputs (TCLKA and TCLKB) and increments or decrements TCNT2. When phase counting mode is set, the TCLKA and TCLKB pins become external clock input pins, regardless of the settings of the TPSC2–TPSC0 bits in TCR2 or the CKEG1 and CKEG0 bits. TCNT2 also becomes an up/down-counter.

Since the TCR2 CCLR1/CCLR0 bits, TIOR2, TIER2, TSR2, GRA2, and GRB2 are all enabled, input capture and compare match functions and interrupt sources can be used. Phase counting is available only for channel 2.

Procedure for Selecting Phase Counting Mode: Figure 10.42 shows the procedure for selecting phase counting mode.

1. Set the MDF bit in the timer mode register (TMDR) to 1 to select phase counting mode.
2. Select the flag set conditions using the FDIR bit in TMDR.
3. Set the STR2 bit in the timer start register (TSTR) to 1 to start the count.

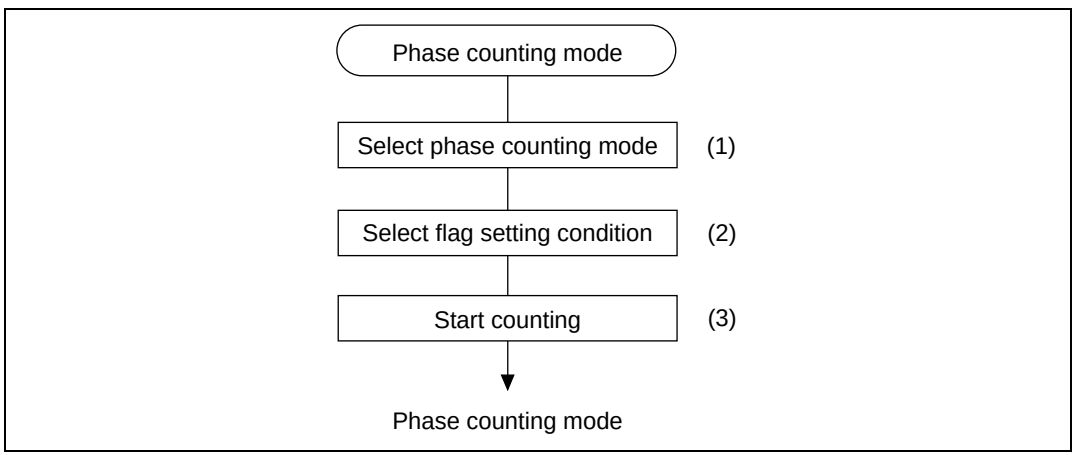


Figure 10.42 Procedure for Selecting Phase Counting Mode

Phase Counting Operation: Figure 10.43 shows an example of phase counting mode operation. Table 10.16 lists the up-counting and down-counting conditions for TCNT2. The ITU counts on both rising and falling edges of TCLKA and TCLKB. The phase differential and overlap of TCLKA and TCLKB must be 1.5 cycles or more and the pulse width must be 2.5 cycles or more.

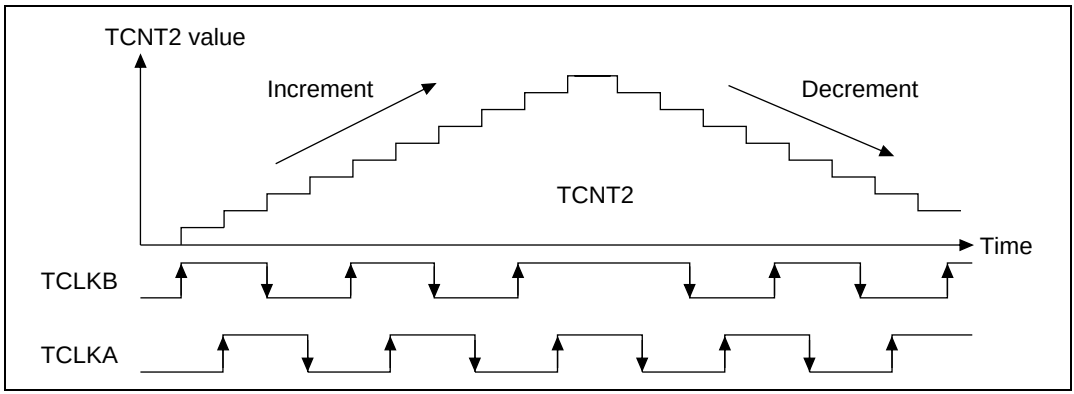


Figure 10.43 Phase Counting Mode Operation

Table 10.16 Up/Down-Counting Conditions

Counting Direction	Increment				Decrement			
TCLKB	Rising	High	Falling	Low	Rising	High	Falling	Low
TCLKA	Low	Rising	High	Falling	High	Falling	Low	Rising

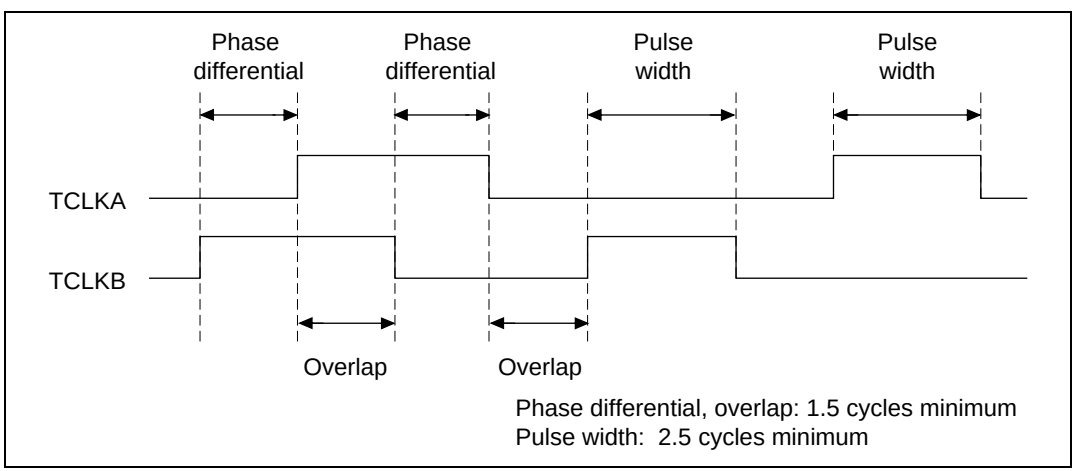


Figure 10.44 Phase Differentials, Overlap, and Pulse Width in Phase Counting Mode

10.4.8 Buffer Mode

In buffer mode, the buffer operation functions differ depending on whether the general registers are set to output compare or input capture, reset-synchronized PWM mode, or complementary PWM mode. Buffer mode is a function of channels 3 and 4 only. Buffer operations set this way function as follows.

GR is an Output Compare Register: The value of the buffer register of a channel is transferred to GR when a compare match occurs in the channel. This is illustrated in figure 10.45.

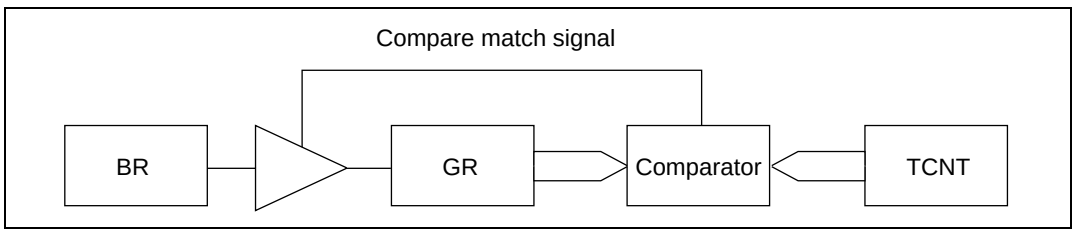


Figure 10.45 Compare Match Buffer Operation

GR is an Input Capture Register: TCNT values are transferred to GR when input capture occurs and the value previously stored in GR is transferred to BR. This operation is illustrated in figure 10.46.

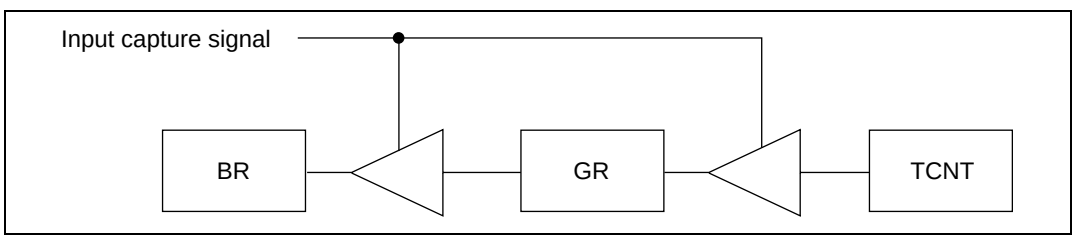


Figure 10.46 Input Capture Buffer Operation

Complementary PWM Mode: When the count direction of TCNT3 and TCNT4 changes, the BR value is transferred to GR. The following timing is employed for this transfer:

- When there is a TCNT3/GRA3 compare-match
- When there is a TCNT4 underflows

Reset-Synchronized PWM Mode: The BR value is transferred to GR upon a GRA3 compare match.

Procedure for Selecting Buffer Mode (Figure 10.47):

1. Set TIOR to select the output compare or input capture function of GR.
2. Set bits BFA3, BFB3 and BFB4 in TFCR to select buffer mode for GR.
3. Set the STR bit in TSTR to 1 to start the TCNT count.

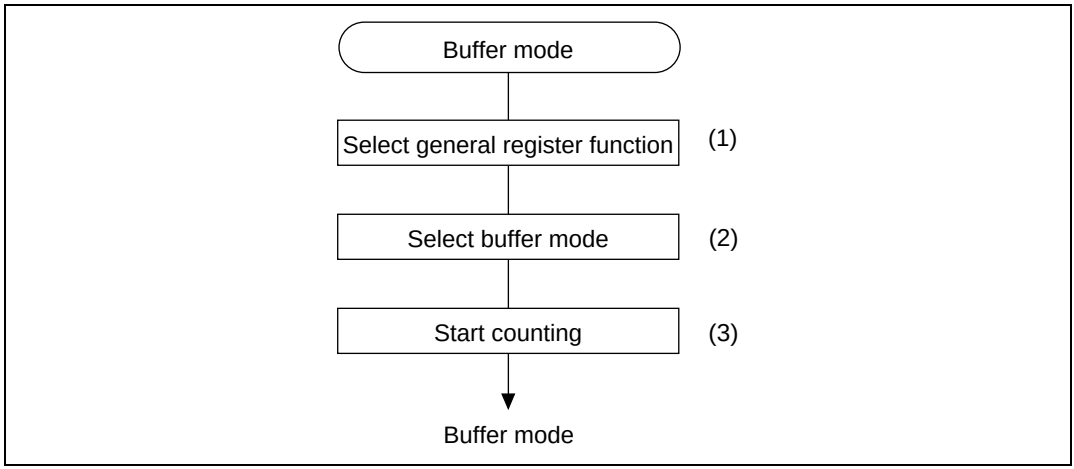


Figure 10.47 Procedure for Selecting Buffer Mode

Buffer Mode Operation: Figure 10.48 shows an example of an operation in buffer mode with GRA set as an output compare register and GRA and buffer register A (BRA) set for buffer operation. TCNT operates as a periodic counter that is cleared by a GRB compare match. TIOCA and TIOCB are set to toggle at compare matches A and B. Since buffer mode is selected, when TIOCA toggles at compare match A, the BRA value is simultaneously transferred to GRA. This operation is repeated at every compare match A. The transfer timing is shown in figure 10.49.

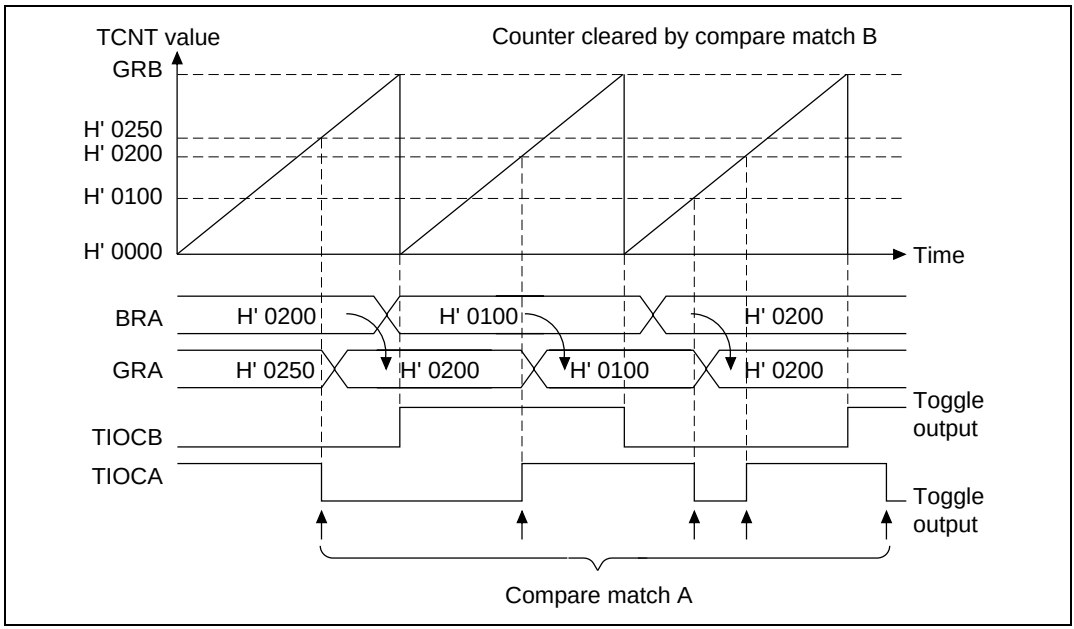


Figure 10.48 Buffer Mode Operation Example 1 (Output Compare Register)

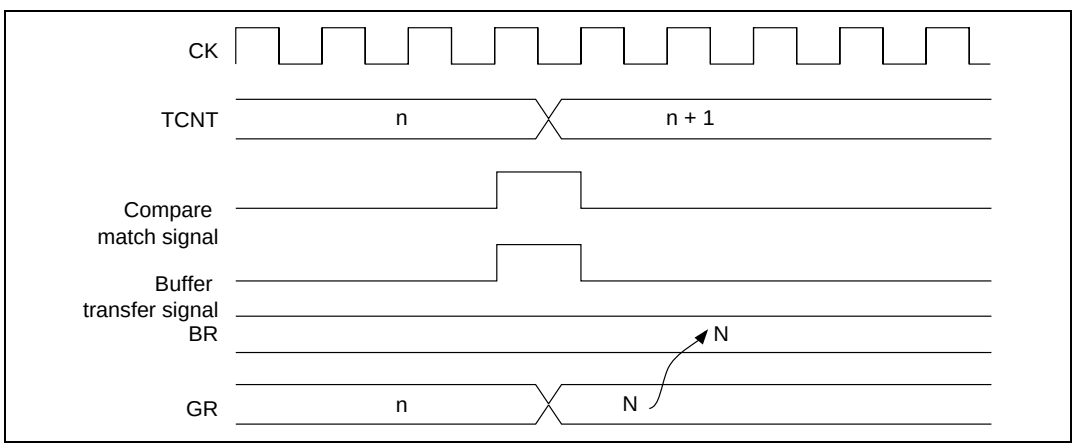


Figure 10.49 Compare Match Timing Example for Buffer Operation

Figure 10.50 shows an example of input capture operation in buffer mode between GRA and BRA with GRA as an input capture register. TCNT is cleared by input capture B. The falling edge is selected as the input capture edge at TIOCB. Both edges are selected as input capture edges at TIOCA. When the TCNT value is stored in GRA by input capture A, the previous GRA value is transferred to BRA. The timing is shown in figure 10.51.

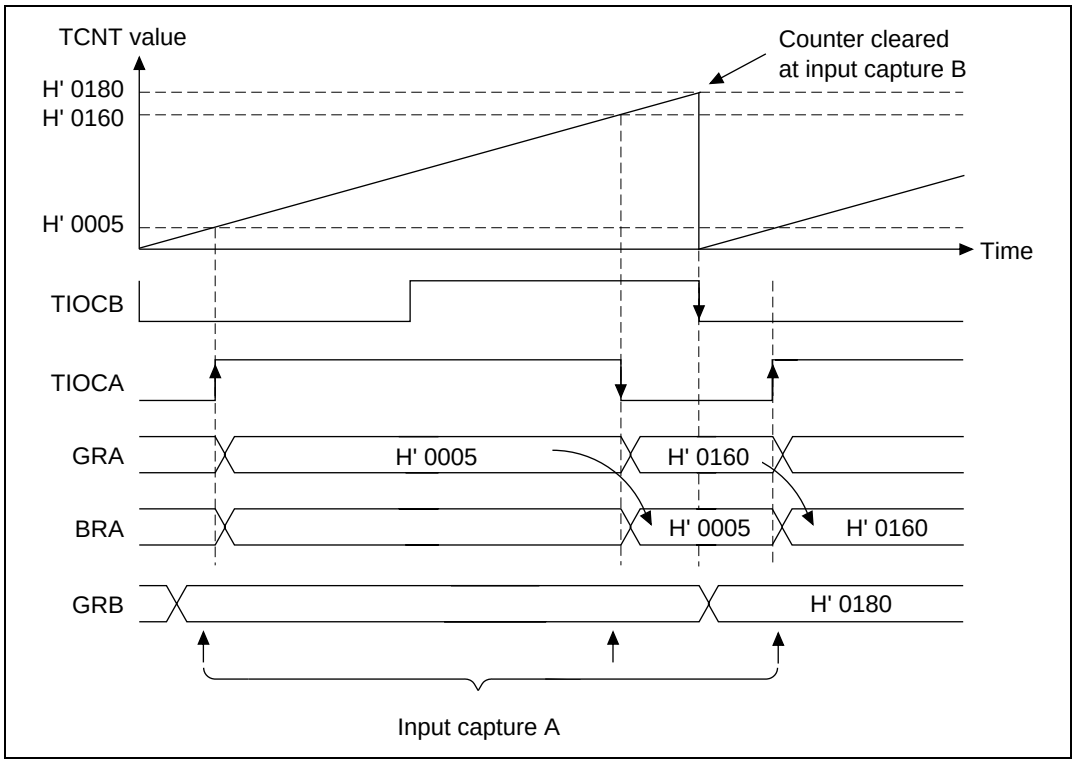


Figure 10.50 Buffer Mode Operation Example 2 (Input Capture Register)

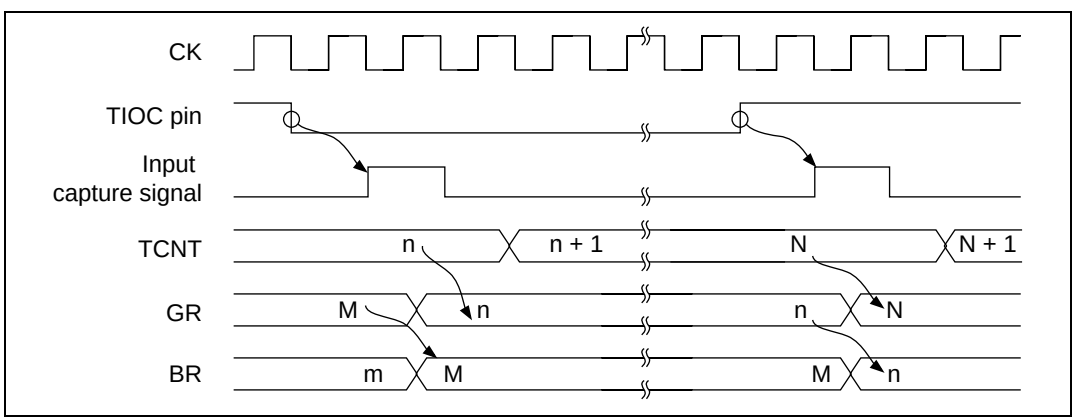


Figure 10.51 Input Capture Timing Example for Buffer Operation

An example of buffer operation in complementary PWM mode between GRB3 and BRB3 is shown in figure 10.52. By making GRB3 larger than GRA3 using buffer operation, a PWM waveform with a duty cycle of 0% is generated. The transfer from BRB to GRB occurs upon TCNT3 and GRA compare match and TCNT4 underflow.

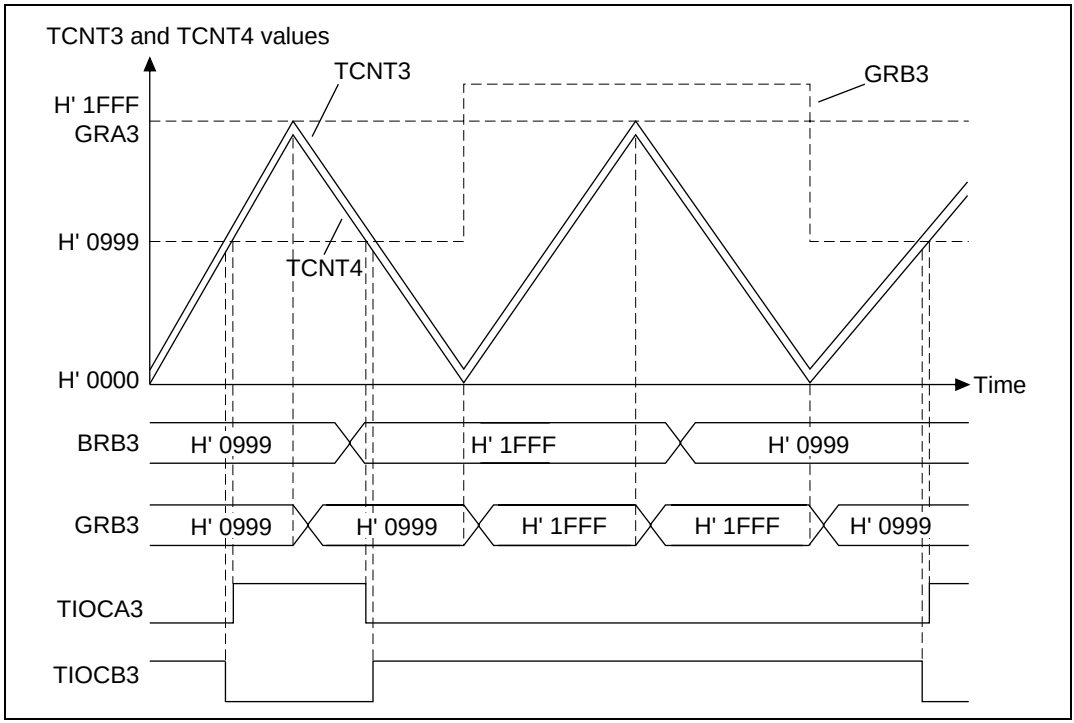


Figure 10.52 Buffer Mode Operation Example 3 (Complementary PWM Mode)

10.4.9 ITU Output Timing

ITU outputs in channels 3 and 4 can be inverted with TOCR.

Output Inversion Timing with TOCR: Output levels can be inverted by inverting the output level select bits (OLS4 and OLS3) in TOCR in complementary PWM mode and reset-synchronized PWM mode. Figure 10.53 illustrates the timing.

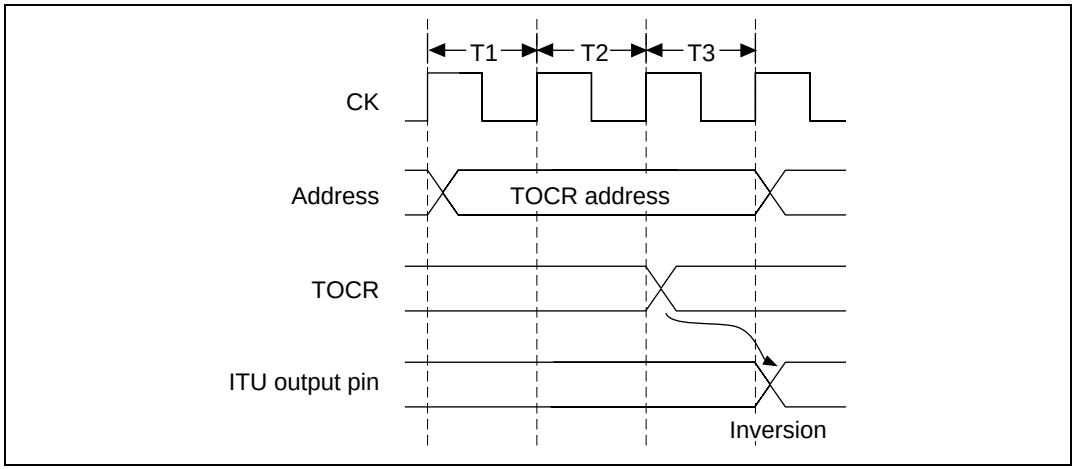


Figure 10.53 Example of Inverting ITU Output Levels by Writing to TOCR

10.5 Interrupts

The ITU has two interrupt sources: input capture/compare match and overflow.

10.5.1 Timing of Setting Status Flags

Timing for Setting IMFA and IMFB in a Compare Match: The IMF bits in TSR are set to 1 by a compare match signal generated when TCNT matches a general register. The compare match signal is generated in the last state in which the values match (when TCNT is updated from the matching count to the next count). Therefore, when TCNT matches GRA or GRB, the compare match signal is not generated until the next timer clock input. Figure 10.54 shows the timing of setting the IMF bits.

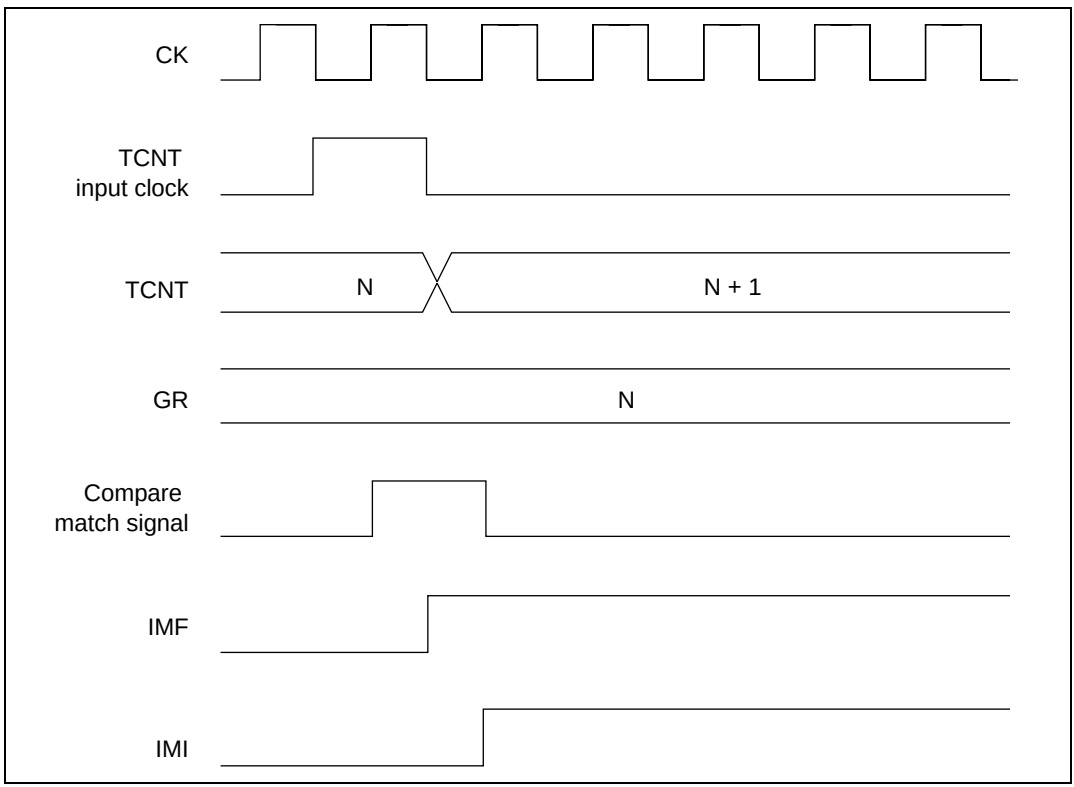


Figure 10.54 Timing of Setting Compare Match Flags (IMFA, IMFB)

Timing of Setting IMFA, IMFB for Input Capture: IMFA and IMFB are set to 1 by an input capture signal. At this time, the TCNT contents are transferred to GR. Figure 10.55 shows the timing.

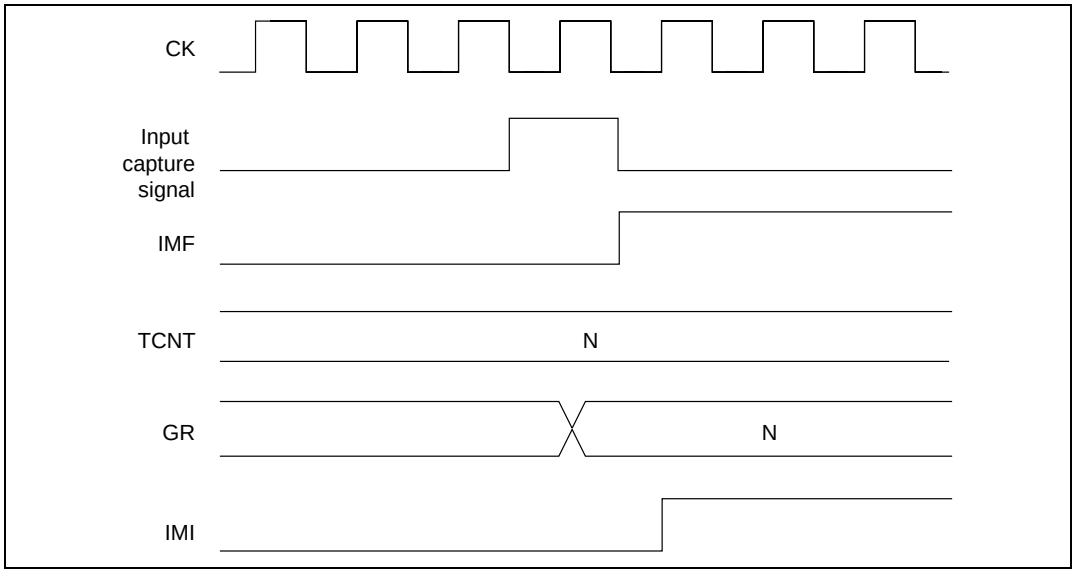


Figure 10.55 Timing of Setting IMFA and IMFB for Input Capture

Timing of Setting Overflow Flag (OVF): OVF is set to 1 when TCNT overflows from H'FFFF to H'0000 or underflows from H'0000 to H'FFFF. Figure 10.56 shows the timing.

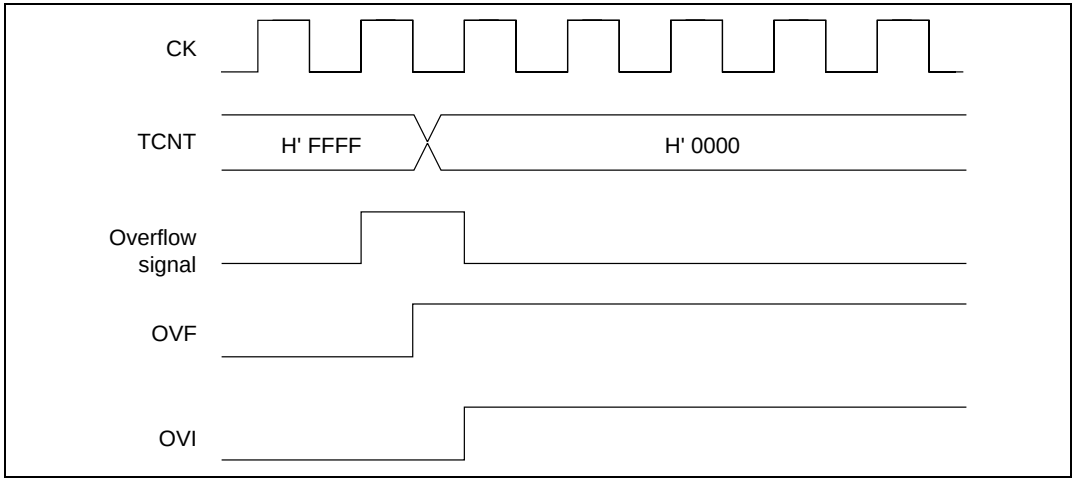


Figure 10.56 Timing of Setting OVF

10.5.2 Status Flag Clear Timing

The status flags are cleared by being read by the CPU when set to 1, then being written with 0. This timing is shown in figure 10.57.

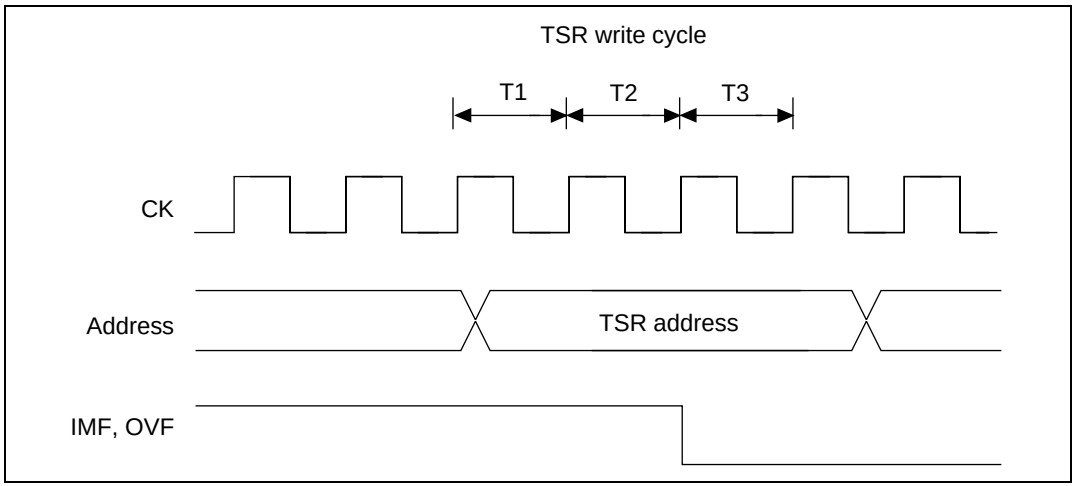


Figure 10.57 Timing of Status Flag Clearing

10.5.3 Interrupt Sources and DMAC Activation

The ITU has compare match/input capture A interrupts, compare match/input capture B interrupts and overflow interrupts for each channel. Each of the fifteen of these three types of interrupts are allocated their own independently vectored addresses. When the interrupt's interrupt request flag is set to 1 and the interrupt enable bit is set to 1, the interrupt is requested.

The channel priority order can be changed with the interrupt controller. For more information, see section 5, Interrupt Controller (INTC). The compare match/input capture A interrupts of channels 0–3 can start the DMAC to transfer data. Table 10.17 lists the interrupt sources.

Table 10.17 ITU Interrupt Sources

Channel	Interrupt Source	Description	DMAC Activation	Priority Order*
0	IMIA0	Compare match or input capture A0	Yes	High
	IMIB0	Compare match or input capture B0	No	↑
	OVI0	Overflow 0	No	
1	IMIA1	Compare match or input capture A1	Yes	
	IMIB1	Compare match or input capture B1	No	
	OVI1	Overflow 1	No	
2	IMIA2	Compare match or input capture A2	Yes	
	IMIB2	Compare match or input capture B2	No	
	OVI2	Overflow 2	No	
3	IMIA3	Compare match or input capture A3	Yes	
	IMIB3	Compare match or input capture B3	No	
	OVI3	Overflow 3	No	
4	IMIA4	Compare match or input capture A4	No	
	IMIB4	Compare match or input capture B4	No	↓
	OVI4	Overflow 4	No	Low

Note: * Indicates the initial status following a reset. The ranking of channels can be altered using the interrupt controller.

10.6 Notes and Precautions

This section describes contention and other matters requiring special attention during ITU operation.

10.6.1 Contention between TCNT Write and Clear

If a counter clear signal occurs in the T3 state of a TCNT write cycle, clearing the counter takes priority and the write is not performed. The timing is shown in figure 10.58.

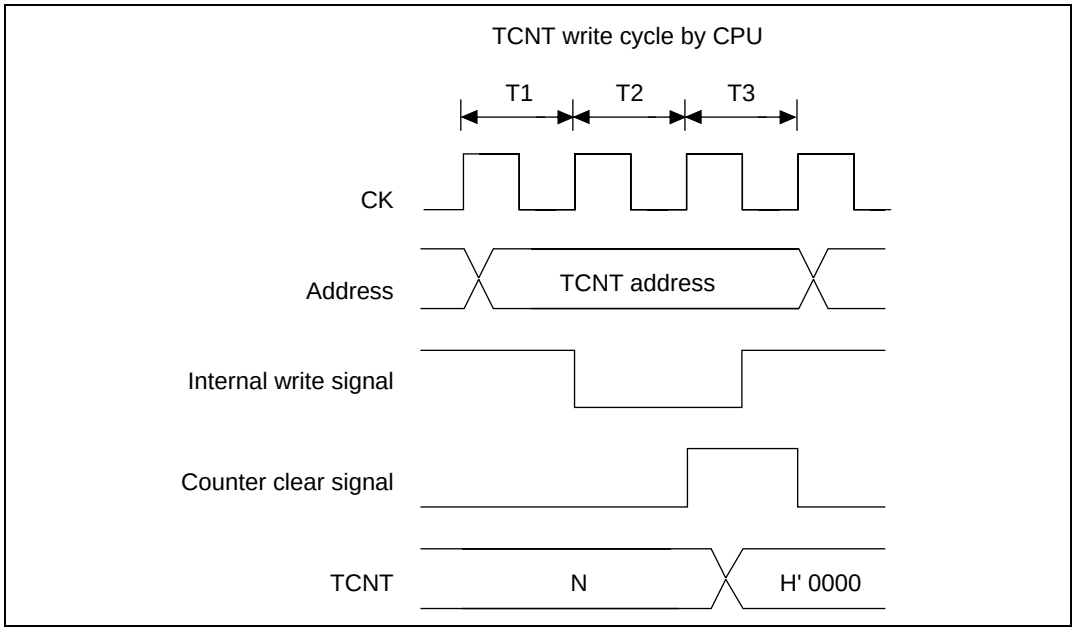


Figure 10.58 Contention between TCNT Write and Clear

10.6.2 Contention between TCNT Word Write and Increment

If an increment pulse occurs in the T3 state of a TCNT word write cycle, writing takes priority and TCNT is not incremented. The timing is shown in figure 10.59.

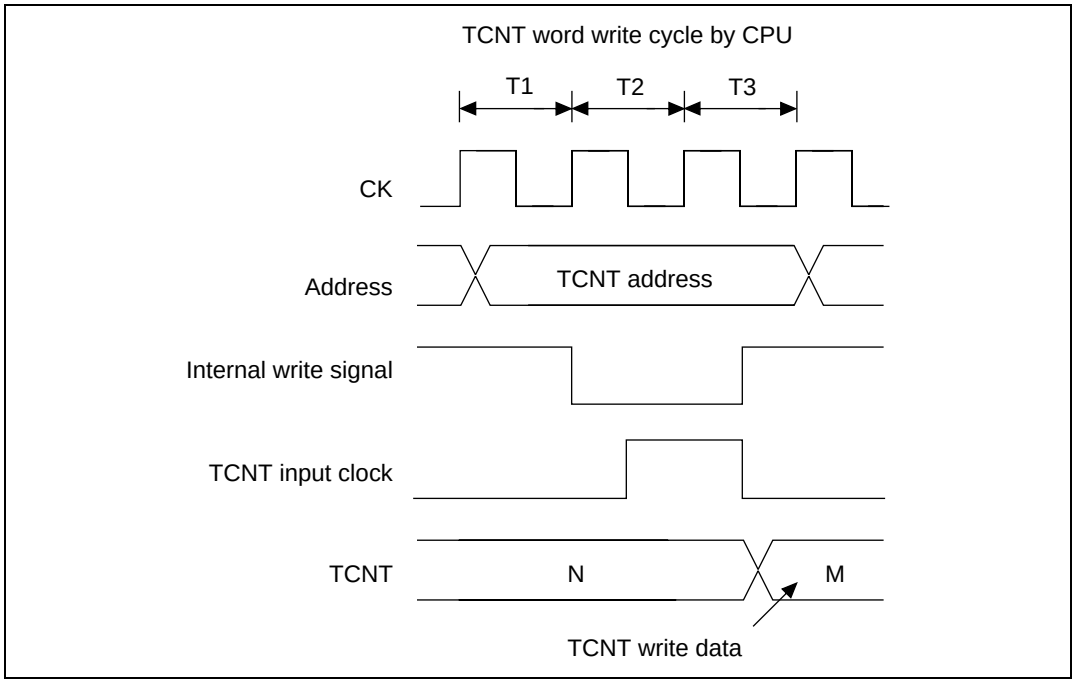


Figure 10.59 Contention between TCNT Word Write and Increment

10.6.3 Contention between TCNT Byte Write and Increment

If an increment pulse occurs in the T2 state or T3 state of a TCNT byte write cycle, counter writing takes priority and the byte data on the side that was previously written is not incremented. The TCNT byte data that was not written is also not incremented and retains its previous value. The timing is shown in figure 10.60 (which shows an increment during state T2 of a byte write cycle to TCNTH).

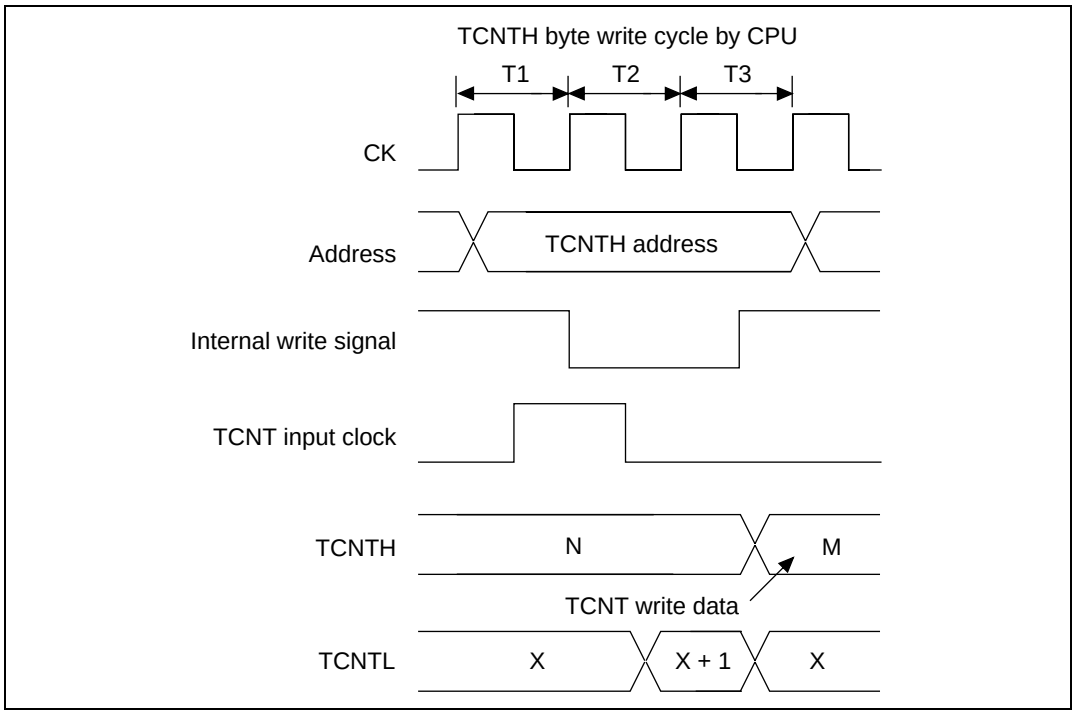


Figure 10.60 Contention between TCNT Byte Write and Increment

10.6.4 Contention between GR Write and Compare Match

If a compare match occurs in the T3 state of a general register (GR) write cycle, writing takes priority and the compare match signal is inhibited. The timing is shown in figure 10.61.

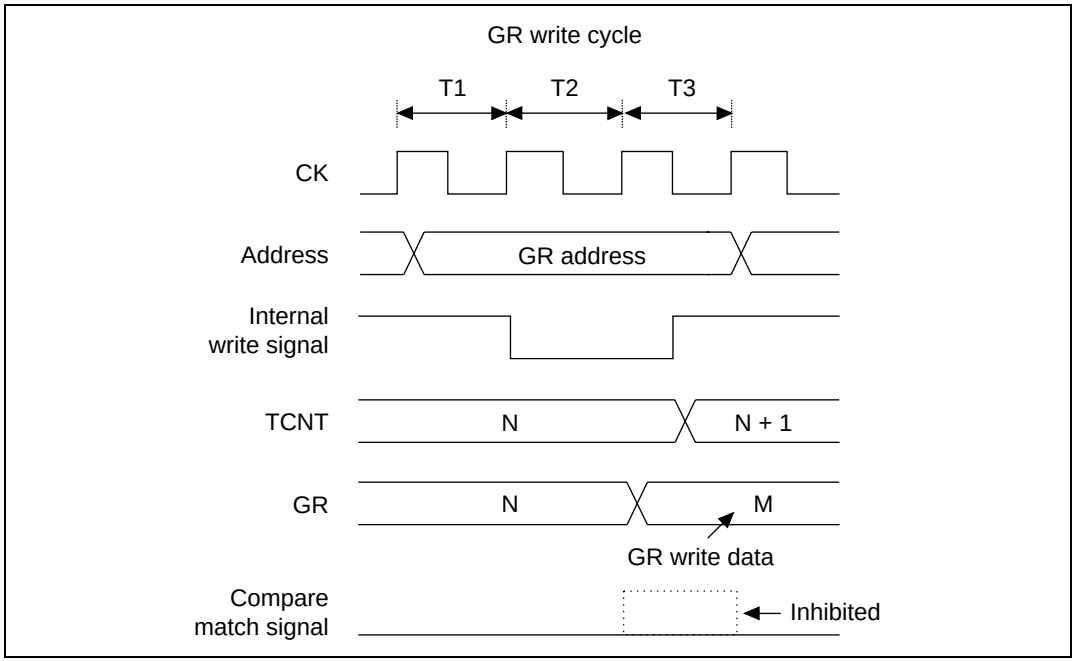


Figure 10.61 Contention between General Register Write and Compare Match

10.6.5 Contention between TCNT Write and Overflow/Underflow

If an overflow occurs in the T3 state of a TCNT write cycle, writing takes priority over counter incrementing. OVF is set to 1. The same applies to underflows. The timing is shown in figure 10.62.

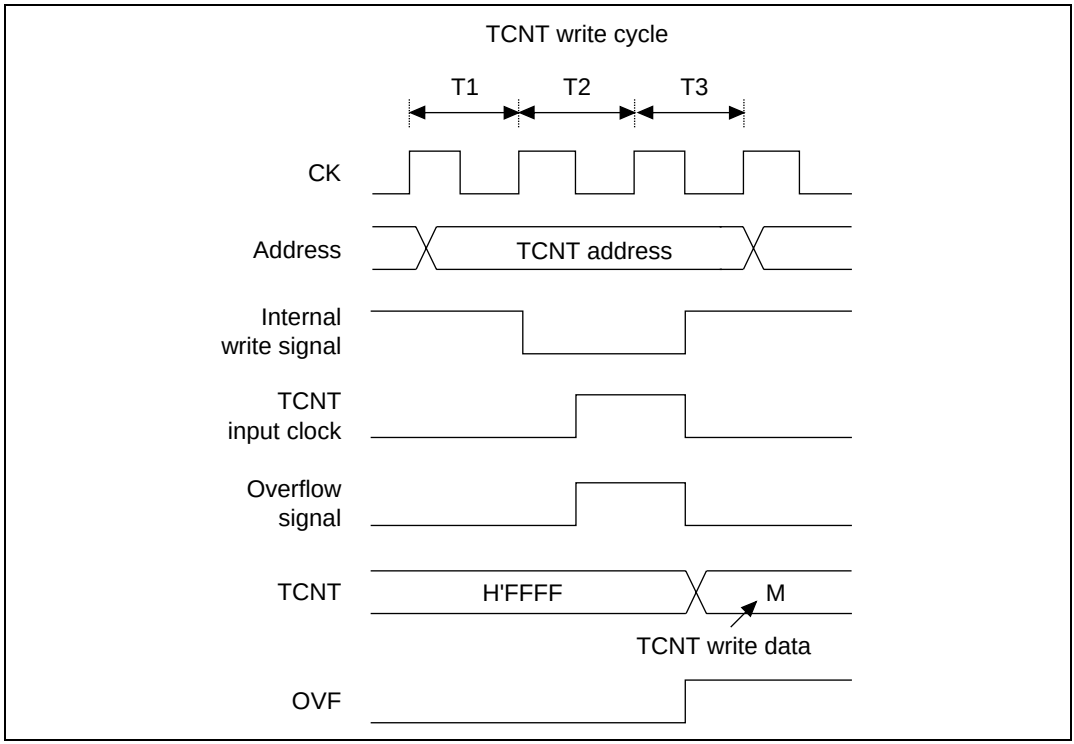


Figure 10.62 Contention between TCNT Write and Overflow

10.6.6 Contention between General Register Read and Input Capture

If an input capture signal is generated during the T3 state of a general register read cycle, the value before input capture is read. The timing is shown in figure 10.63.

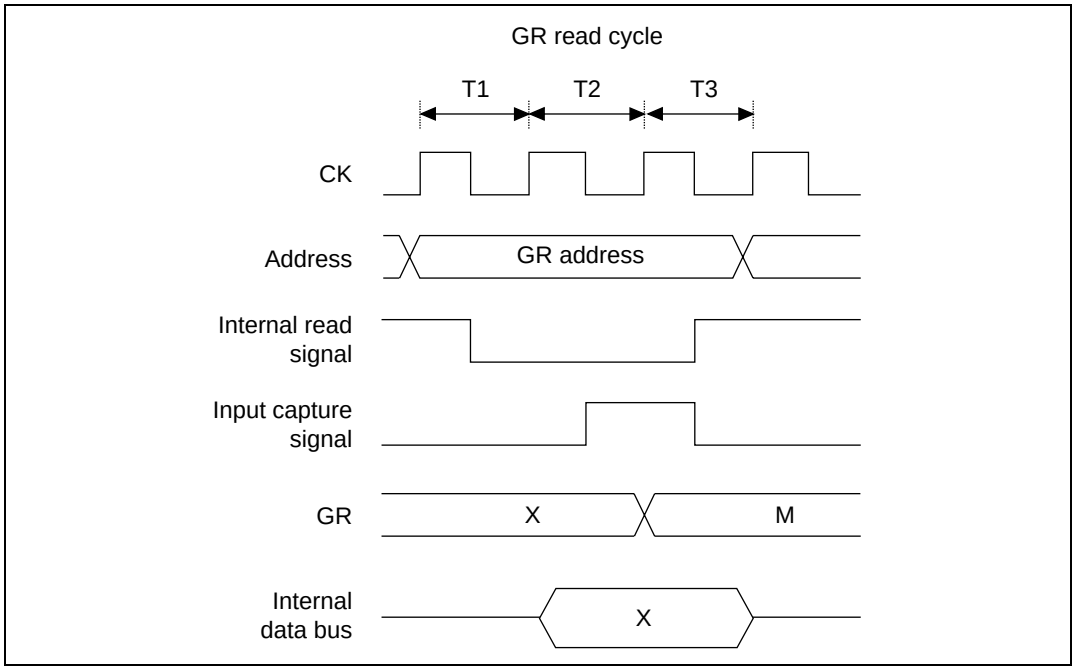


Figure 10.63 Contention between General Register Read and Input Capture

10.6.7 Contention Between Counter Clearing by Input Capture and Counter Increment

If an input capture signal and counter increment signal occur simultaneously, the counter is cleared by the input capture signal. The counter is not incremented by the increment signal. The TCNT value before the counter is cleared is transferred to the general register. The timing is shown in figure 10.64.

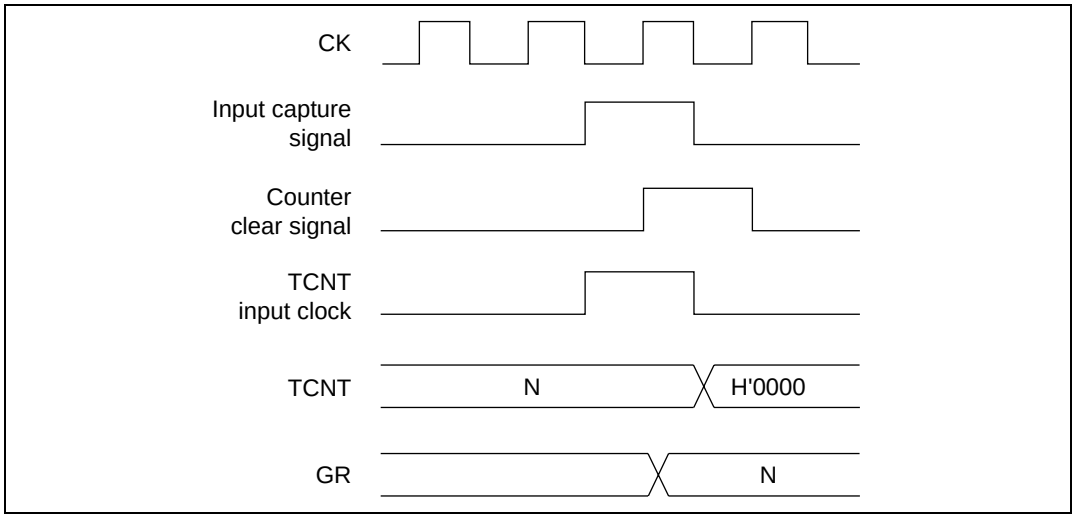


Figure 10.64 Contention between Counter Clearing by Input Capture and Counter Increment

10.6.8 Contention between General Register Write and Input Capture

If an input capture signal is generated during the T3 state of a general register write cycle, the input capture transfer takes priority and the write to GR is not performed. The timing is shown in figure 10.65.

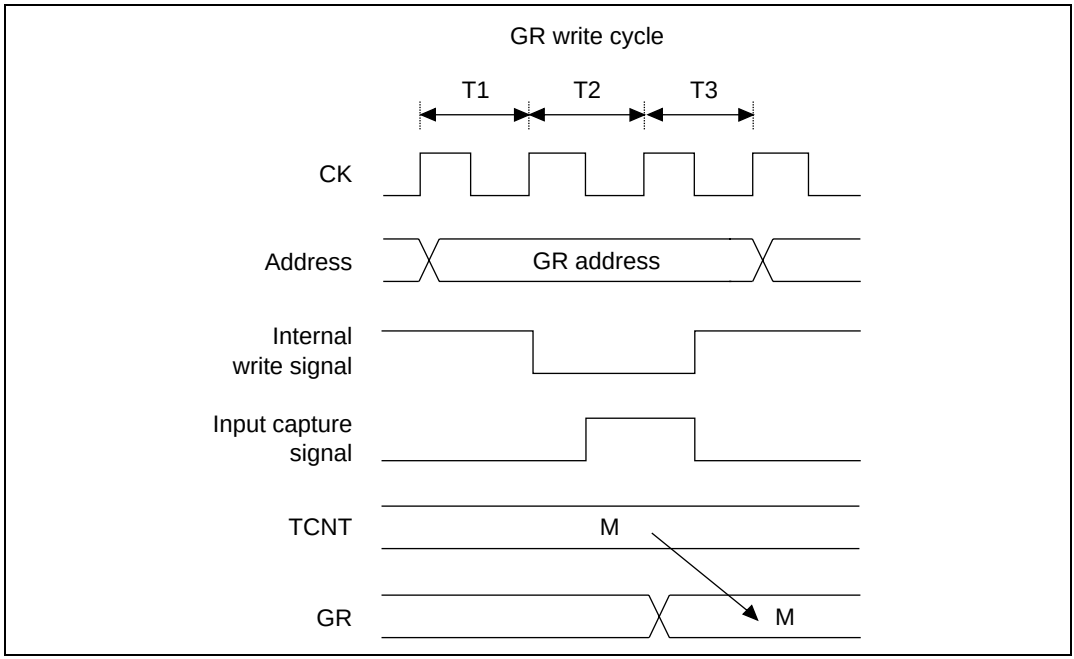


Figure 10.65 Contention between General Register Write and Input Capture

10.6.9 Note on Waveform Cycle Setting

When a counter is cleared by compare match, the counter is cleared in the last state in which the TCNT value matches the GR value (when TCNT is updated from the matching count to the next count). The actual counter frequency is therefore given by the following formula:

$f = \phi/(N + 1)$
(f: counter frequency; ϕ: operating frequency; N: value set in GR)

10.6.10 Contention between BR Write and Input Capture

When a buffer register (BR) is being used as an input capture register and an input capture signal is generated in the T3 state of the write cycle, the buffer operation takes priority over the BR write. The timing is shown in figure 10.66.

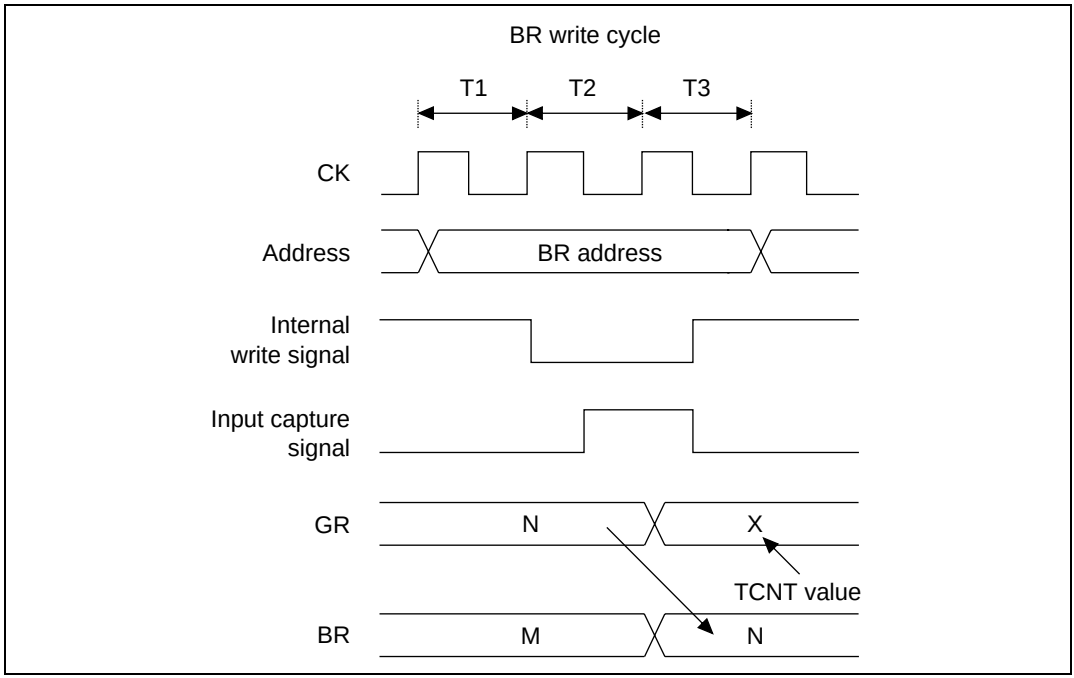


Figure 10.66 Contention between BR Write and Input Capture

10.6.11 Note on Writing in Synchronizing Mode

After synchronizing mode is selected, if TCNT is written by byte access, all 16 bits of all synchronized counters assume the same value as the counter that was addressed.

Example: Figures 10.67 and 10.68 show byte write and word write when channels 2 and 3 are synchronized

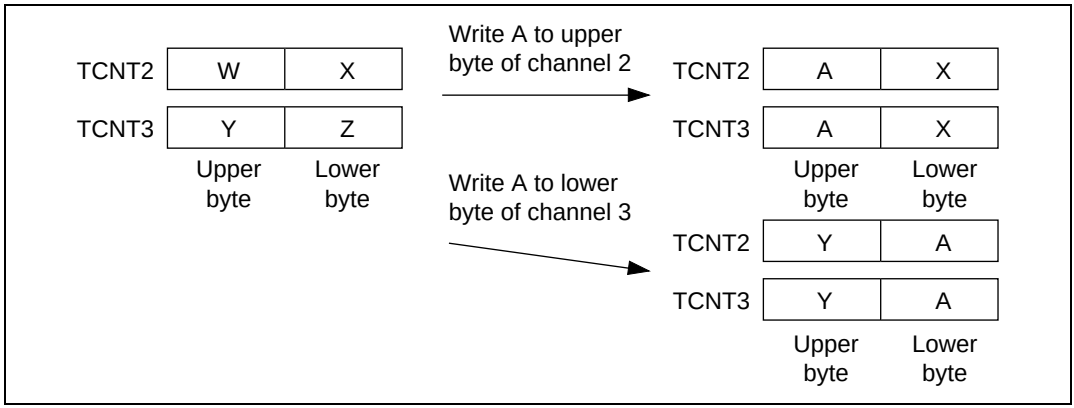


Figure 10.67 Byte Write to Channel 2 or Byte Write to Channel 3

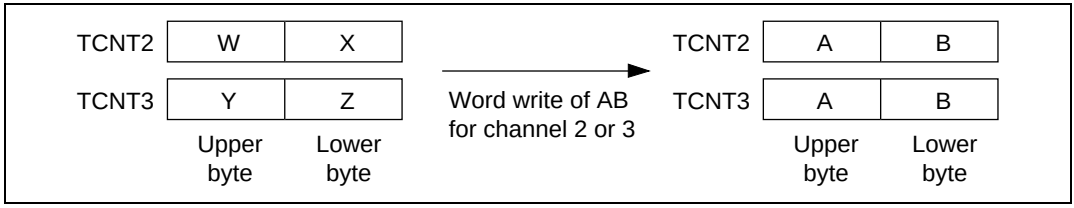


Figure 10.68 Word Write to Channel 2 or Word Write to Channel 3

10.6.12 Note on Setting Reset-Synchronized PWM Mode/Complementary PWM Mode

When the CMD1 and CMD0 bits in TFCR are set, note the following.

1. Writes to CMD1 and CMD0 should be carried out while TCNT3 and TCNT4 are halted.
2. Changes of setting from reset-synchronized PWM mode to complementary PWM mode and vice versa are prohibited. Set reset-synchronized PWM mode or complementary PWM mode after first setting normal operation (clear CMD1 bit to 0).

10.6.13 Clearing Complementary PWM Mode

Figure 10.69 shows the procedure for clearing complementary PWM mode. First, reset combination mode bits CMD1 and CMD0 in the timer function control register (TFCR) from 10 to either 00 or 01. The mode will switch from complementary PWM mode to normal operating mode. Next, wait for at least 1 cycle of the counter input clock being used for channels 3 and 4 and then clear counter start bits STR3 and STR4 in the timer start register (TSTR). The channel 3 and 4 counters, TCNT3 and TCNT4, will stop counting. Clearing complementary PWM mode by any other procedure may result in changes other than those set for the output waveform when complementary PWM mode is set again.

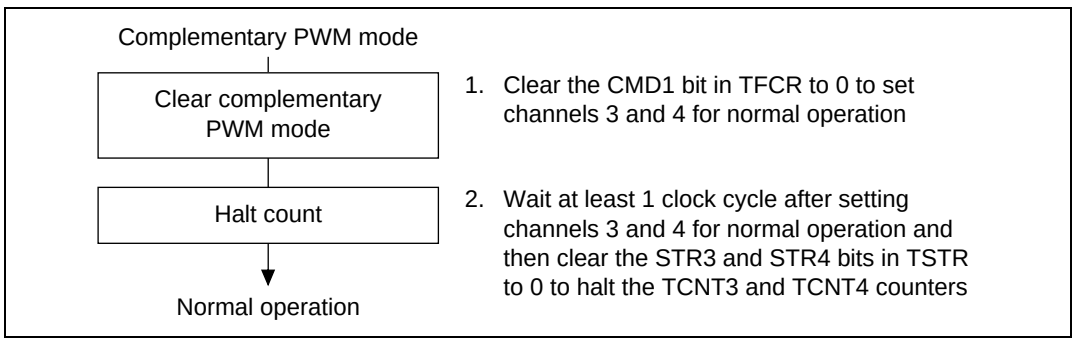


Figure 10.69 Clearing Complementary PWM Mode

10.6.14 Note on Counter Clearing by Input Capture

If TCNT is cleared (to H'0000) by input capture when its value is H'FFFF, overflow will not occur.

10.6.15 ITU Operating Modes

Table 10.18 ITU Operating Modes (Channel 0)

	Register Setting											
	TSNC	TMDR			TFCR			TOCR	TIOR0		TCR0	
Operating Mode	Sync	MDF	FDIR	PWM	Comp PWM	Reset Sync PWM	Buffer	Output Level Select	IOA	IOB	Clear Select	Clock Select
Synch-ronized preset	SYNC0 = 1	—	—	√	—	—	—	—	√	√	√	√
PWM	√	—	—	PWM0 = 1	—	—	—	—	—	√*	√	√
Output compare A function	√	—	—	PWM0 = 0	—	—	—	—	IOA2 = 0, others: don't care	√	√	√
Output compare B function	√	—	—	√	—	—	—	—	√	IOB2 = 0, others: don't care	√	√
Input capture A function	√	—	—	PWM0 = 0	—	—	—	—	IOA2 = 1, others: don't care	√	√	√
Input capture B function	√	—	—	PWM0 = 0	—	—	—	—	√	IOB2 = 1, others: don't care	√	√
Counter Clear Function												
Clear at compare match/ input capture A	√	—	—	√	—	—	—	—	√	√	CCLR1 = 0 CCLR0 = 1	√
Clear at compare match/ input capture B	√	—	—	√	—	—	—	—	√	√	CCLR1 = 1 CCLR0 = 0	√
Synch-ronized clear	SYNC0 = 1	—	—	√	—	—	—	—	√	√	CCLR1 = 1 CCLR0 = 1	√

√: Settable, —: Setting does not affect current mode

Note: * In PWM mode, the input capture function cannot be used. When compare match A and compare match B occur simultaneously, the compare match signal is inhibited.

Table 10.19 ITU Operating Modes (Channel 1)

	Register Setting											
	TSNC	TMDR			TFCR			TOCR	TIOR1		TCR1	
Operating Mode	Sync	MDF	FDIR	PWM	Comp PWM	Reset Sync PWM	Buffer	Output Level Select	IOA	IOB	Clear Select	Clock Select
Synch-ronized preset	SYNC1 = 1	—	—	√	—	—	—	—	√	√	√	√
PWM	√	—	—	PWM1 = 1	—	—	—	—	—	√*	√	√
Output compare A function	√	—	—	PWM1 = 0	—	—	—	—	IOA2 = 0, others: don't care	√	√	√
Output compare B function	√	—	—	√	—	—	—	—	√	IOB2 = 0, others: don't care	√	√
Input capture A function	√	—	—	PWM1 = 0	—	—	—	—	IOA2 = 1, others: don't care	√	√	√
Input capture B function	√	—	—	PWM1 = 0	—	—	—	—	√	IOB2 = 1, others: don't care	√	√
Counter Clear Function												
Clear at compare match/ input capture A	√	—	—	√	—	—	—	—	√	√	CCLR1 = 0 CCLR0 = 1	√
Clear at compare match/ input capture B	√	—	—	√	—	—	—	—	√	√	CCLR1 = 1 CCLR0 = 0	√
Synch-ronized clear	SYNC1 = 1	—	—	√	—	—	—	—	√	√	CCLR1 = 1 CCLR0 = 1	√

√: Settable, —: Setting does not affect current mode

Note: * In PWM mode, the input capture function cannot be used. When compare match A and compare match B occur simultaneously, the compare match signal is inhibited.

Table 10.20 ITU Operating Modes (Channel 2)

	Register Setting											
	TSNC	TMDR			TFCR			TOCR	TIOR2		TCR2	
Operating Mode	Sync	MDF	FDIR	PWM	Comp PWM	Reset Sync PWM	Buffer	Output Level Select	IOA	IOB	Clear Select	Clock Select
Synch-ronized preset	SYNC2 = 1	—	—	√	—	—	—	—	√	√	√	√
PWM	√	—	—	PWM2 = 1	—	—	—	—	—	√*	√	√
Output compare A function	√	—	—	PWM2 = 0	—	—	—	—	IOA2 = 0, others: don't care	√	√	√
Output compare B function	√	—	—	√	—	—	—	—	√	IOB2 = 0, others: don't care	√	√
Input capture A function	√	—	—	PWM2 = 0	—	—	—	—	IOA2 = 1, others: don't care	√	√	√
Input capture B function	√	—	—	PWM2 = 0	—	—	—	—	√	IOB2 = 1, others: don't care	√	√
Counter Clear Function												
Clear at compare match/ input capture A	√	—	—	√	—	—	—	—	√	√	CCLR1 = 0 CCLR0 = 1	√
Clear at compare match/ input capture B	√	—	—	√	—	—	—	—	√	√	CCLR1 = 1 CCLR0 = 0	√
Synch-ronized clear	SYNC2 = 1	—	—	√	—	—	—	—	√	√	CCLR1 = 1 CCLR0 = 1	√
Phase counting	√	MDF = 1	√	√	—	—	—	—	√	√	√	—

√: Settable, —: Setting does not affect current mode

Note: * In PWM mode, the input capture function cannot be used. When compare match A and compare match B occur simultaneously, the compare match signal is inhibited.

Table 10.21 ITU Operating Modes (Channel 3)

	Register Setting										
	TSNC	TMDR			TFCR			TOCR	TIOR3		TCR3	
Operating Mode	Sync	MDF	FDIR	PWM	Comp PWM	Reset Sync PWM	Buffer	Output Level Select	IOA	IOB	Clear Select	Clock Select
Synch-ronized preset	SYNC3 = 1	—	—	√	√*2	√	√	—	√	√	√	√
PWM mode	√	—	—	PWM3 = 1	CMD1 = 0	CMD1 = 0	√	—	—	√*1	√	√
Output compare A function	√	—	—	PWM3 = 0	CMD1 = 0	CMD1 = 0	√	—	IOA2 = 0, others: don't care	√	√	√
Output compare B function	√	—	—	√	CMD1 = 0	CMD1 = 0	√	—	√	IOB2 = 0, others: don't care	√	√
Input capture A function	√	—	—	PWM3 = 0	CMD1 = 0	CMD1 = 0	√	—	IOA2 = 1, others: don't care	√	√	√
Input capture B function	√	—	—	PWM3 = 0	CMD1 = 0	CMD1 = 0	√	—	√	IOB2 = 1, others: don't care	√	√
Counter Clear Function												
Clear at compare match/ input capture A	√	—	—	√	CMD1 = 1, CMD0 = 0 inhib-ited	√*3	√	—	√	√	CCLR1 = 0 CCLR0 = 1	√
Clear at compare match/ input capture B	√	—	—	√	CMD1 = 0	CMD1 = 0	√	—	√	√	CCLR1 = 1 CCLR0 = 0	√
Synch-ronized clear	SYNC3 = 1	—	—	√	CMD1 = 1, CMD0 = 0 inhib-ited	√	√	—	√	√	CCLR1 = 1 CCLR0 = 1	√

	Register Setting											
	TSNC	**TMDR**			**TFCR**			**TOCR**	**TIOR3**		**TCR3**	
Operating Mode	**Sync**	**MDF**	**FDIR**	**PWM**	**Comp PWM**	**Reset Sync PWM**	**Buffer**	**Output Level Select**	**IOA**	**IOB**	**Clear Select**	**Clock Select**
Complementary PWM mode	√*2	—	—	—	CMD1 = 1 CMD0 = 0	CMD1 = 1 CMD0 = 0	√	√	—	—	CCLR1 = 0 CCLR0 = 0	√*4
Reset synchronized PWM mode	√	—	—	—	CMD1 = 1 CMD0 = 1	CMD1 = 1 CMD0 = 1	√	√	—	—	CCLR1 = 0 CCLR0 = 1	√
Buffer (BRA)	√	—	—	√	√	√	BFA3 = 1, others: don't care	—	√	√	√	√
Buffer (BRB)	√	—	—	√	√	√	BFB3 = 1, others: don't care	—	√	√	√	√

√: Settable, —: Setting does not affect current mode

Notes: 1. In PWM mode, the input capture function cannot be used. When compare match A and compare match B occur simultaneously, the compare match signal is inhibited.

2. When set for complementary PWM mode, do not simultaneously set channel 3 and channel 4 to function synchronously.

3. Counter clearing by input capture A cannot be used when reset-synchronized PWM mode is set.

4. Clock selection when complementary PWM mode is set should be the same for channels 3 and 4.

Table 10.22 ITU Operating Modes (Channel 4)

	Register Setting										
	TSNC	TMDR			TFCR			TOCR	TIOR4		TCR4	
Operating Mode	Sync	MDF	FDIR	PWM	Comp PWM	Reset Sync PWM	Buffer	Output Level Select	IOA	IOB	Clear Select	Clock Select
Synchronized preset	SYNC4 = 1	—	—	√	√*2	√	√	—	√	√	√	√
PWM	√	—	—	PWM4 = 1	CMD1 = 0	CMD1 = 0	√	—	—	√*1	√	√
Output compare A function	√	—	—	PWM4 = 0	CMD1 = 0	CMD1 = 0	√	—	IOA2 = 0, others: don't care	√	√	√
Output compare B function	√	—	—	√	CMD1 = 0	CMD1 = 0	√	—	√	IOB2 = 0, others: don't care	√	√
Input capture A function	√	—	—	PWM4 = 0	CMD1 = 0	CMD1 = 0	√	—	IOA2 = 1, others: don't care	√	√	√
Input capture B function	√	—	—	PWM4 = 0	CMD1 = 0	CMD1 = 0	√	—	√	IOB2 = 1, others: don't care	√	√
Counter Clear Function												
Clear at compare match/ input capture A	√	—	—	√	CMD1 = 1, CMD0 = 0 inhibited	√*3	√	—	√	√	CCLR1 = 0 CCLR0 = 1	√
Clear at compare match/ input capture B	√	—	—	√	CMD1 = 1, CMD0 = 0 inhibited	√*3	√	—	√	√	CCLR1 = 1 CCLR0 = 0	√
Synchronized clear	SYNC4 = 1	—	—	√	CMD1 = 1, CMD1 = 0 inhibited	√*3	√	—	√	√	CCLR1 = 1 CCLR0 = 1	√

	Register Setting											
	TSNC	TMDR			TFCR			TOCR	TIOR4		TCR4	
Operating Mode	Sync	MDF	FDIR	PWM	Comp PWM	Reset Sync PWM	Buffer	Output Level Select	IOA	IOB	Clear Select	Clock Select
Complementary PWM	√*2	—	—	—	CMD1 = 1 CMD0 = 0	CMD1 = 1 CMD0 = 0	√	√	—	—	CCLR1 = 0 CCLR0 = 0	√*4
Reset synchronized PWM	√	—	—	—	CMD1 = 1 CMD0 = 1	CMD1 = 1 CMD0 = 1	√	√	—	—	√*5	√*5
Buffer (BRA)	√	—	—	√	√	√	BFA4 = 1, others: don't care	—	√	√	√	√
Buffer (BRB)	√	—	—	√	√	√	BFB4 = 1, others: don't care	—	√	√	√	√

√: Settable, —: Setting does not affect current mode

Notes: 1. In PWM mode, the input capture function cannot be used. When compare match A and compare match B occur simultaneously, the compare match signal is inhibited.

2. When set for complementary PWM mode, do not simultaneously set channel 3 and channel 4 to function synchronously.

3. Counter clearing works with reset-synchronized PWM mode, but TCNT4 runs independently. The output waveform is not affected.

4. Clock selection when complementary PWM mode is set should be the same for channels 3 and 4.

5. In reset-synchronized PWM mode, TCNT4 runs independently. The output waveform is not affected.

Section 11 Programmable Timing Pattern Controller (TPC)

11.1 Overview

The SuperH microcomputer has an on-chip programmable timing pattern controller (TPC). The TPC can provide pulse outputs by using the 16-bit integrated timer pulse unit (ITU) as a time base. The TPC pulse outputs are divided into 4-bit groups 3–0. These can operate simultaneously or independently.

11.1.1 Features

Features of the programmable timing pattern controller are listed below:

- 16-bit output data: Maximum 16-bit data can be output. TPC output can be enabled on a bit-by-bit basis.
- Four output groups: Output trigger signals can be selected in 4-bit groups to provide up to four different 4-bit outputs.
- Selectable output trigger signals: Output trigger signals can be selected by group from the 4-channel compare-match signals of the 16-bit integrated timer pulse unit (ITU).
- Non-overlap mode: A non-overlap interval can be set to come between multiple pulse outputs.
- Can connect to DMA controller: The compare-match signals selected as output trigger signals can activate the DMA controller for sequential output of data without CPU intervention.

11.1.2 Block Diagram

Figure 11.1 shows a block diagram of the TPC.

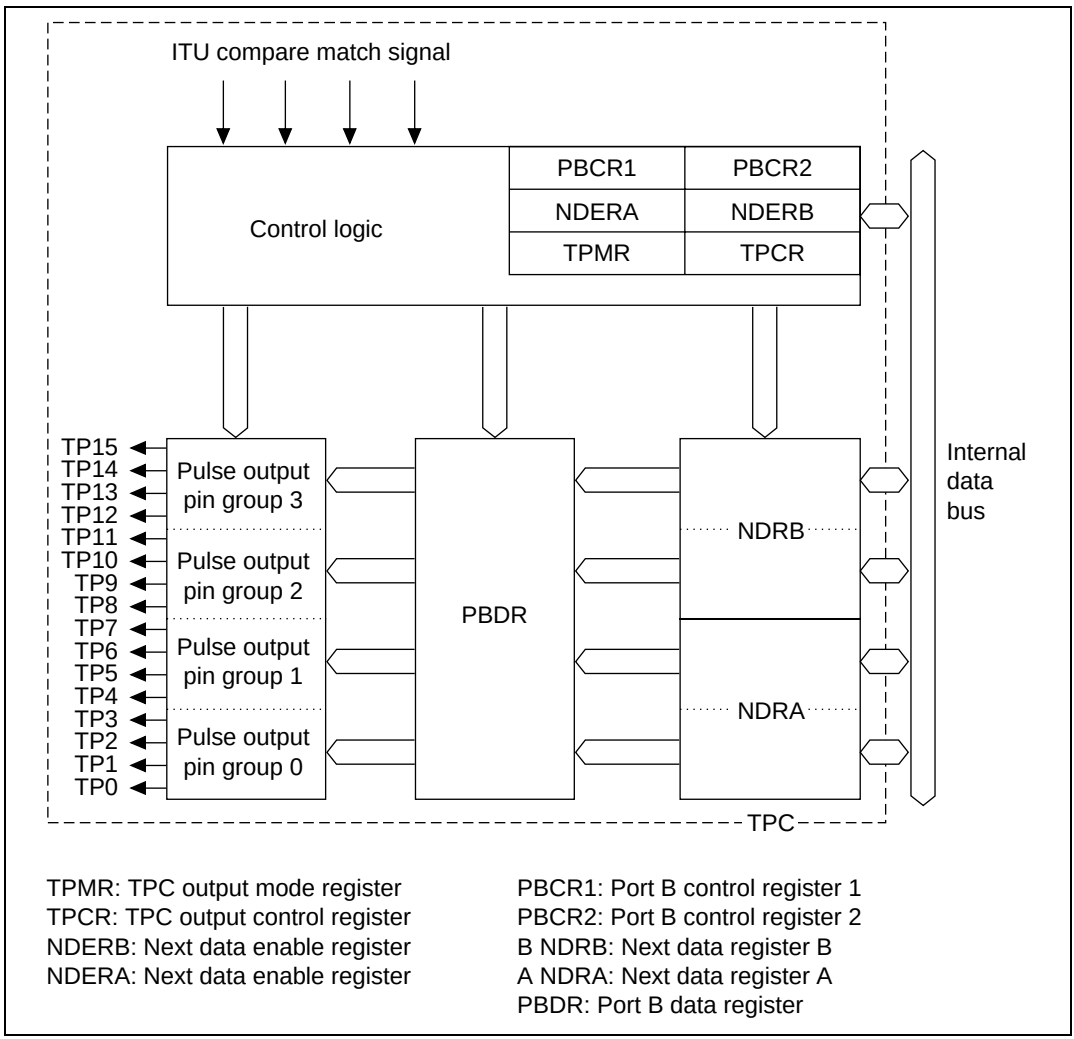


Figure 11.1 Block Diagram of TPC

11.1.3 Input/Output Pins

Table 11.1 summarizes the TPC input/output pins.

Table 11.1 TPC Pins

Name	Symbol	Input/Output	Function
TPC output 0	TP0	Output	Group 0 pulse output
TPC output 1	TP1	Output	
TPC output 2	TP2	Output	
TPC output 3	TP3	Output	
TPC output 4	TP4	Output	Group 1 pulse output
TPC output 5	TP5	Output	
TPC output 6	TP6	Output	
TPC output 7	TP7	Output	
TPC output 8	TP8	Output	Group 2 pulse output
TPC output 9	TP9	Output	
TPC output 10	TP10	Output	
TPC output 11	TP11	Output	
TPC output 12	TP12	Output	Group 3 pulse output
TPC output 13	TP13	Output	
TPC output 14	TP14	Output	
TPC output 15	TP15	Output	

11.1.4 Registers

Table 11.2 summarizes the TPC registers.

Table 11.2 TPC Registers

Name	Abbreviation	R/W	Initial Value	Address*1	Access Size
Port B control register 1	PBCR1	R/W	H'0000	H'5FFFFCC	8, 16
Port B control register 2	PBCR2	R/W	H'0000	H'5FFFFCE	8, 16
Port B data register	PBDR	R/(W)*2	H'0000	H'5FFFFC2	8, 16
TPC output mode register	TPMR	R/W	H'F0	H'5FFFFF0	8, 16
TPC output control register	TPCR	R/W	H'FF	H'5FFFFF1	8, 16
Next data enable register B	NDERB	R/W	H'00	H'5FFFFF2	8, 16
Next data enable register A	NDERA	R/W	H'00	H'5FFFFF3	8, 16
Next data register A	NDRA	R/W	H'00	H'5FFFFF5/ H'5FFFFF7*3	8, 16
Next data register B	NDRB	R/W	H'00	H'5FFFFF4/ H'5FFFFF6*3	8, 16

Notes: 1. Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.
2. Bits used for TPC output cannot be written to.
3. These addresses change depending on the TPCR settings. When TPC output groups 0 and 1 have the same output trigger, the NDRA address is H'5FFFFF5; when their output triggers are different, the NDRA address for group 0 is H'5FFFFF7 and the address for group 1 is H'5FFFFF5. Likewise, when TPC output groups 2 and 3 have the same output trigger, the NDRB address is H'5FFFFF4; when their output triggers are different, the NDRB address for group 0 is H'5FFFFF6 and the address for group 1 is H'5FFFFF4.

11.2 Register Descriptions

11.2.1 Port B Control Registers 1 and 2 (PBCR1, PCBR2)

Port B control registers 1 and 2 (PBCR1 and PBCR2) are 16-bit read/write registers that set the functions of port B pins. Port B consists of the dual-use pins TP15–TP0. Bits corresponding to the pins to be used for TPC output must be set to 11. For details, see the port B description in section 15, Pin Function Controller (PFC).

PCBR1

Bit	15	14	13	12	11	10	9	8
	PB15 MD1	PB15 MD0	PB14 MD1	PB14 MD0	PB13 MD1	PB13 MD0	PB12 MD1	PB12 MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB11 MD1	PB11 MD0	PB10 MD1	PB10 MD0	PB9 MD1	PB9 MD0	PB8 MD1	PB8 MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCBR2

Bit	15	14	13	12	11	10	9	8
	PB7MD1	PB7MD0	PB6MD1	PB6MD0	PB5MD1	PB5MD0	PB4MD1	PB4MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB3MD1	PB3MD0	PB2MD1	PB2MD0	PB1MD1	PB1MD0	PB0MD1	PB0MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

11.2.2 Port B Data Register (PBDR)

The port B data register (PBDR) is a 16-bit read/write register that stores output data for groups 0–3 when TPC output is used. For details of PBDR, see section 16, I/O Ports.

Bit	15	14	13	12	11	10	9	8
	PB15DR	PB14DR	PB13DR	PB12DR	PB11DR	PB10DR	PB9DR	PB8DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Bits set to TPC output by NDERA or NDERB are read-only.

Bit	7	6	5	4	3	2	1	0
	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Bits set to TPC output by NDERA or NDERB are read-only.

11.2.3 Next Data Register A (NDRA)

NDRA is an eight-bit read/write register that stores the next output data for TPC output groups 1 and 0 (TP7–TP0). When used for TPC output, the contents of NDRA are transferred to the corresponding PBDR bits when the ITU compare match specified in the TPC output control register, TPCR, occurs.

The address of NDRA differs depending on whether TPCR settings select the same trigger or different triggers for TPC output groups 1 and 0. NDRA is initialized to H'00 by a reset. It is not initialized in standby mode.

Same Trigger for TPC Output Groups 1 and 0: If TPC output groups 1 and 0 are triggered by the same compare match, the address of NDRA is H'FFFFF5. The upper 4 bits become group 1 and the lower 4 bits become group 0. Address H'5FFFFF7 in such cases consists entirely of reserved bits. These bits cannot be modified and are always read as 1.

Address H'5FFFFF5

Bits 7–4—Next Data 7–4 (NDR7–NDR4): NDR7–NDR4 store the next output data for TPC output group 1.

Bits 3–0—Next Data 3–0 (NDR3–NDR0): NDR3–NDR0 store the next output data for TPC output group 0.

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address H'5FFFFF7

Bits 7–0—Reserved: These bits are always read as 1. The write value should always be 1.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

Different Triggers for TPC Output Groups 1 and 0: If TPC output groups 1 and 0 are triggered by different compare matches, the address of the upper 4 bits of NDRA (group 1) is H'5FFFFF5 and the address of the lower 4 bits of NDRA (group 0) is H'5FFFFF7. Bits 3–0 of address H'5FFFFF5 and bits 7–4 of address H'5FFFFF7 are reserved bits. The write value should always be 1. These bits are always read as 1.

Address H'5FFFFF5

Bits 7–4—Next Data 7–4 (NDR7–NDR4): NDR7–NDR4 store the next output data for TPC output group 1.

Bits 3–0—Reserved: These bits are always read as 1. The write value should always be 1.

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Address H'5FFFFF7

Bits 7–4—Reserved: These bits are always read as 1. The write value should always be 1.

Bits 3–0—Next Data 3–0 (NDR3–NDR0): NDR3–NDR0 store the next output data for TPC output group 0.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	NDR3	NDR2	NDR1	NDR0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

11.2.4 Next Data Register B (NDRB)

NDRB is an eight-bit read/write register that stores the next output data for TPC output groups 3 and 2 (TP15–TP8). When used for TPC output, the contents of NDRB are transferred to the corresponding PBDR bits when the ITU compare match specified in the TPC output control register, TPCR, occurs.

The address of NDRB differs depending on whether TPCR settings select the same trigger or different triggers for TPC output groups 3 and 2. NDRB is initialized to H'00 by a reset. It is not initialized in standby mode.

Same Trigger for TPC Output Groups 3 and 2: If TPC output groups 3 and 2 are triggered by the same compare match, the address of NDRB is H'FFFFF4. The upper 4 bits become group 3 and the lower 4 bits become group 2. Address H'5FFFFF6 consists entirely of reserved bits. These bits are always read as 1, and the write value should always be 1.

Address H'5FFFFF4

Bits 7–4—Next Data 15–12 (NDR15–NDR12): NDR15–NDR12 store the next output data for TPC output group 3.

Bits 3–0—Next Data 11–8 (NDR11–NDR8): NDR11–NDR8 store the next output data for TPC output group 2.

Bit	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address H'5FFFFF6

Bits 7–0—Reserved: These bits are always read as 1. The write value should always be 1.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

Different Triggers for TPC Output Groups 3 and 2: If TPC output groups 3 and 2 are triggered by different compare matches, the address of the upper 4 bits of NDRB (group 3) is H'5FFFFF4 and the address of the lower 4 bits of NDRB (group 2) is H'5FFFFF6. Bits 3–0 of address H'5FFFFF4 and bits 7–4 of address H'5FFFFF6 are reserved bits. These bits are always read as 1. The write value should always be 1.

Address H'5FFFFF4

Bits 7–4—Next Data 15–12 (NDR15–NDR12): NDR15–NDR12 store the next output data for TPC output group 3.

Bits 3–0—Reserved: These bits are always read as 1. The write value should always be 1.

Bit	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Address H'5FFFFF6

Bits 7–4—Reserved: These bits are always read as 1. The write value should always be 1.

Bits 3–0—Next Data 11–8 (NDR11–NDR8): NDR11–NDR8 store the next output data for TPC output group 2.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	NDR11	NDR10	NDR9	NDR8
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

11.2.5 Next Data Enable Register A (NDERA)

NDERA is an eight-bit read/write register that enables TPC output groups 1 and 0 (TP7–TP0) on a bit-by-bit basis.

When the bits enabled for TPC output by NDERA generate the ITU compare match selected in the TPC output control register, the value of the next data register A (NDRA) is automatically transferred to the corresponding PBDR bits and the output value is updated. For disabled bits, there is no transfer and the output value does not change. NDERA is initialized to H'00 by a reset. It is not initialized in standby mode.

Bit	7	6	5	4	3	2	1	0
	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7–0—Next Data Enable 7–0 (NDER7–NDER0): NDER7–NDER0 select enabling/disabling for TPC output groups 1 and 0 (TP7–TP0) in bit units.

Bit 7–0: NDER7–NDER0	Description
0	Disables TPC outputs TP7–TP0 (transfer from NDR7–NDR0 to PB7–PB0 is disabled) (Initial value)
1	Enables TPC outputs TP7–TP0 (transfer from NDR7–NDR0 to PB7–PB0 is enabled)

11.2.6 Next Data Enable Register B (NDERB)

NDERB is an eight-bit read/write register that enables TPC output groups 3 and 2 (TP15–TP8) on a bit-by-bit basis.

When the bits enabled for TPC output by NDERB generate the ITU compare match selected in the TPC output control register, the value of the next data register B (NDRB) is automatically transferred to the corresponding PBDR bits and the output value is updated. For disabled bits, there is no transfer and the output value does not change. NDERB is initialized to H'00 by a reset. It is not initialized in standby mode.

Bit	7	6	5	4	3	2	1	0
	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7–0—Next Data Enable 15–8 (NDER15–NDER8): NDER15–NDER8 select enabling/disabling for TPC output groups 3 and 2 (TP15–TP8) in bit units.

Bit 7–0: NDER15–NDER8	Description
0	Disables TPC outputs TP15–TP8 (transfer from NDR15–NDR8 to PB15–PB8 is disabled) (Initial value)
1	Enables TPC outputs TP15–TP8 (transfer from NDR15–NDR8 to PB15–PB8 is enabled)

11.2.7 TPC Output Control Register (TPCR)

TPCR is an eight-bit read/write register that selects output trigger signals for TPC outputs. TPCR is initialized to H'FF by a reset. It is not initialized in standby mode.

Bit	7	6	5	4	3	2	1	0
	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 and 6—Group 3 Compare Match Select 1 and 0 (G3CMS1 and G3CMS0): G3CMS1 and G3CMS0 select the compare match that triggers TPC output group 3 (TP15–TP12).

Bit 7: G3CMS1	Bit 6: G3CMS0	Description
0	0	TPC output group 3 (TP15–TP12) output is triggered by compare match in ITU channel 0
	1	TPC output group 3 (TP15–TP12) output is triggered by compare match in ITU channel 1
1	0	TPC output group 3 (TP15–TP12) output is triggered by compare match in ITU channel 2
	1	TPC output group 3 (TP15–TP12) output is triggered by compare match in ITU channel 3 (Initial value)

Bits 5 and 4—Group 2 Compare Match Select 1 and 0 (G2CMS1 and G2CMS0): G2CMS1 and G2CMS0 select the ITU channel that triggers TPC output group 2 (TP11–TP8).

Bit 5: G2CMS1	Bit 4: G2CMS0	Description
0	0	TPC output group 2 (TP11–TP18) output is triggered by compare match in ITU channel 0
	1	TPC output group 2 (TP11–TP18) output is triggered by compare match in ITU channel 1
1	0	TPC output group 2 (TP11–TP18) output is triggered by compare match in ITU channel 2
	1	TPC output group 2 (TP11–TP18) output is triggered by compare match in ITU channel 3 (Initial value)

Bits 3 and 2—Group 1 Compare Match Select 1 and 0 (G1CMS1 and G1CMS0): G1CMS1 and G1CMS0 select the ITU channel that triggers TPC output group 1 (TP7–TP4).

Bit 3: G1CMS1	Bit 2: G1CMS0	Description
0	0	TPC output group 1 (TP7–TP4) output is triggered by compare match in ITU channel 0
	1	TPC output group 1 (TP7–TP4) output is triggered by compare match in ITU channel 1
1	0	TPC output group 1 (TP7–TP4) output is triggered by compare match in ITU channel 2
	1	TPC output group 1 (TP7–TP4) output is triggered by compare match in ITU channel 3 (Initial value)

Bits 1 and 0—Group 0 Compare Match Select 1 and 0 (G0CMS1 and G0CMS0): G0CMS1 and G0CMS0 select the ITU channel that triggers TPC output group 0 (TP3–TP0).

Bit 1: G0CMS1	Bit 0: G0CMS0	Description
0	0	TPC output group 0 (TP3–TP0) output is triggered by compare match in ITU channel 0
	1	TPC output group 0 (TP3–TP0) output is triggered by compare match in ITU channel 1
1	0	TPC output group 0 (TP3–TP0) output is triggered by compare match in ITU channel 2
	1	TPC output group 0 (TP3–TP0) output is triggered by compare match in ITU channel 3 (Initial value)

11.2.8 TPC Output Mode Register (TPMR)

TPMR is an eight-bit read/write register that selects between the TPC's ordinary output and non-overlap output modes in group units. During non-overlap operation, the output waveform cycle is set in ITU general register B (GRB) for use as the output trigger and a non-overlap period is set in general register A (GRA). The output value then changes on compare matches A and B. For details, see section 11.3.4, TPC Output Non-Overlap Operation. TPMR is initialized to H'F0 by a reset. It is not initialized in standby mode.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	G3NOV	G2NOV	G1NOV	G0NOV
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Bits 7–4—Reserved: These bits are always read as 1. The write value should always be 1.

Bit 3—Group 3 Non-Overlap Mode (G3NOV): G3NOV selects ordinary or non-overlap mode for TPC output group 3 (TP15–TP12).

Bit 3: G3NOV	Description
0	TPC output group 3 operates normally (output value updated according to compare match A of the ITU channel selected by TPCR) (Initial value)
1	TPC output group 3 operates in non-overlap mode (1 output and 0 output can be performed independently according to compare match A and B of the ITU channel selected by TPCR)

Bit 2—Group 2 Non-Overlap Mode (G2NOV): G2NOV selects ordinary or non-overlap mode for TPC output group 2 (TP11–TP8).

Bit 2: G2NOV	Description
0	TPC output group 2 operates normally (output value updated according to compare match A of the ITU channel selected by TPCR) (Initial value)
1	TPC output group 2 operates in non-overlap mode (1 output and 0 output can be performed independently according to compare match A and B of the ITU channel selected by TPCR)

Bit 1—Group 1 Non-Overlap Mode (G1NOV): G1NOV selects ordinary or non-overlap mode for TPC output group 1 (TP7–TP4).

Bit 1: G1NOV	Description
0	TPC output group 1 operates normally (output value updated according to compare match A of the ITU channel selected by TPCR) (Initial value)
1	TPC output group 1 operates in non-overlap mode (1 output and 0 output can be performed independently according to compare match A and B of the ITU channel selected by TPCR)

Bit 0—Group 0 Non-Overlap Mode (G0NOV): G0NOV selects ordinary or non-overlap mode for TPC output group 0 (TP3–TP0).

Bit 0: G0NOV	Description
0	TPC output group 0 operates normally (output value updated according to compare match A of the ITU channel selected by TPCR) (Initial value)
1	TPC output group 0 operates in non-overlap mode (1 output and 0 output can be performed independently according to compare match A and B of the ITU channel selected by TPCR)

11.3 Operation

11.3.1 Overview

When corresponding bits in the PBCR1, PBCR2, NDERA, and NDERB registers are set to 1, TPC output is enabled and the PBDR data register values are output. After that, when the compare match event selected by TPCR occurs, the next data register contents (NDRA and NDRB) are transferred to PBDR and output values are updated. Figure 11.2 illustrates the TPC output operation.

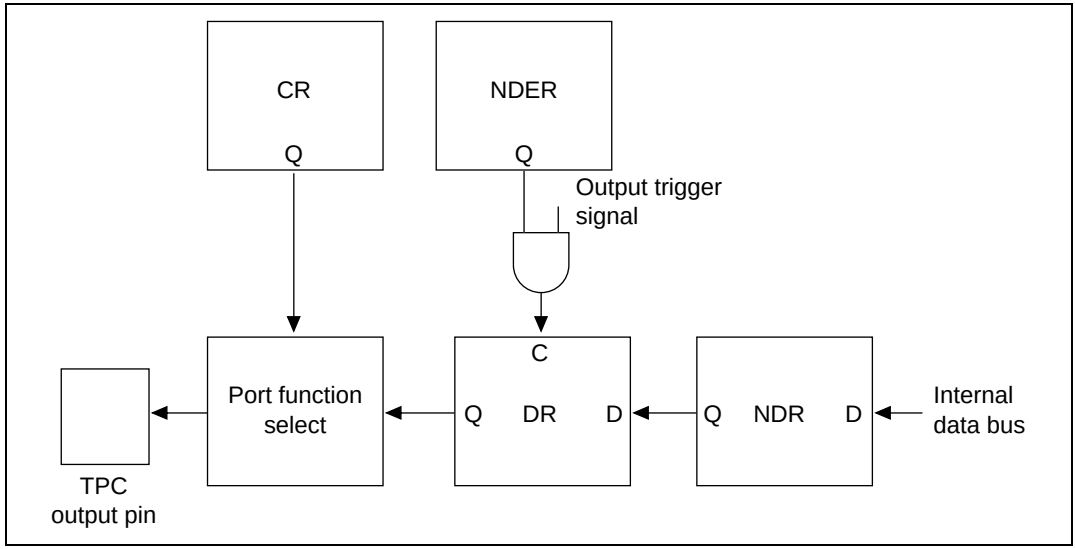


Figure 11.2 TPC Output Operation

If new data is written in next data registers A and B before the next compare match occurs, a maximum 16 bits of data can be output at each successive compare match. See section 11.3.4, TPC Output Non-Overlap Operation, for details on non-overlap operation.

11.3.2 Output Timing

If TPC output is enabled, next data register (NDRA/NDRB) contents are transferred to the data register (PBDR) and output when the selected compare match occurs. Figure 11.3 shows the timing of these operations. The example is for ordinary output upon compare match A with groups 2 and 3.

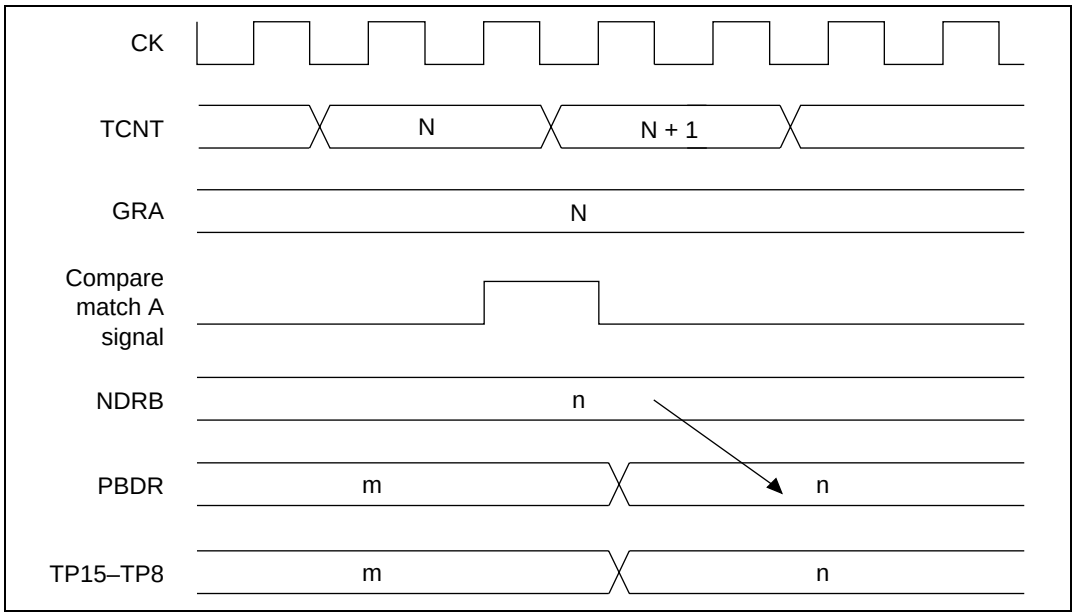


Figure 11.3 Transfer and Output Timing for NDRB Data (Example)

11.3.3 Examples of Use of Ordinary TPC Output

Settings for Ordinary TPC Output (Figure 11.4):

1. Select GRA as the output compare register (output disable) with the timer I/O control register (TIOR).
2. Set the TPC output trigger cycle.
3. Select the counter clock with the TPSC2–TPSC0 bits in the timer control register (TCR). Select the counter clear sources with the CCLR1 and CCLR0 bits.
4. Set the timer interrupt enable register (TIER) to enable IMIA interrupts. Transfers to NDR can also be set using the DMAC.
5. Set the initial output value in the I/O port data register to be used by the TPC.
6. Set the I/O port control register to be used by the TPC as the TP pin function (11).
7. Set to 1 the bit that performs TPC output to the next data enable register (NDER).
8. Select the ITU compare match that will be the TPC output trigger using the TPC output control register (TPCR).
9. Set the next TPC output value in NDR.
10. Set 1 in the STR bit of the timer start register (TSTR) and start the timer counter.
11. Set the next output value in NDR whenever an IMIA interrupt is generated.

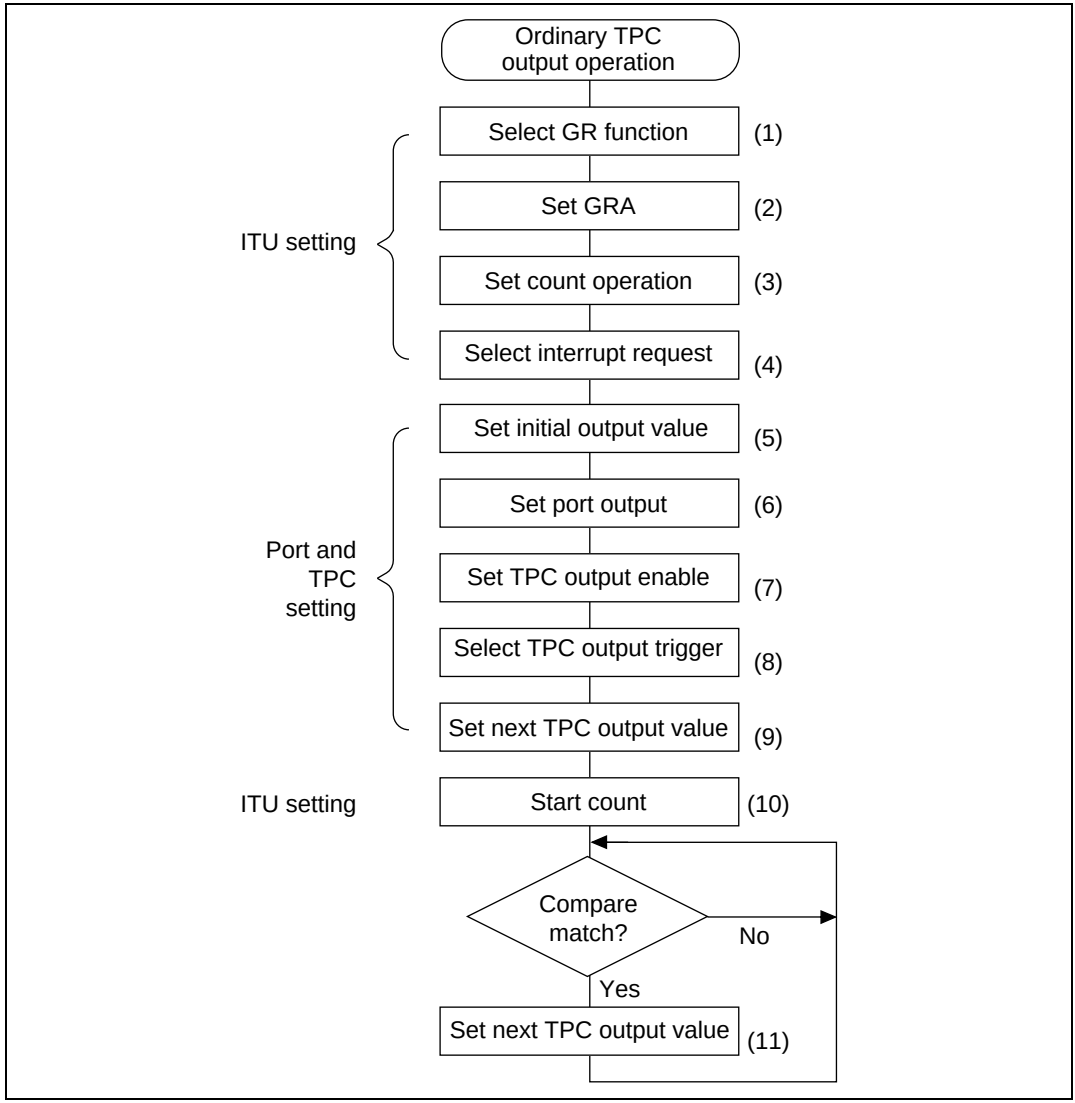


Figure 11.4 Example of Setting Procedure for Ordinary TPC Output

Five-Phase Pulse Output (Figure 11.5):

Figure 11.5 shows an example of 5-phase pulse output generated at regular intervals using TPC output.

1. Set the GRA register of the ITU that serves as output trigger as the output compare register. Set the cycle time in GRA of the ITU and select counter clearing upon compare match A. Set the IMIEA bit in TIER to 1 to enable the compare match A interrupt.
2. Write H'FFC0 in PBCR1, write H'F8 in NDERB, and set G3CMS0, G3CMS1, G2CMS1, and G2CMS0 in TPCR to set the ITU compare match selected in step 1 as the output trigger. Write output data H'80 in NDRB.
3. When the selected ITU channel starts operating and a compare match occurs, the values in NDRB are transferred to PBDR and output. The compare match/input capture A (IMIA) interrupt handling routine writes the next output data (H'C0) in NDRB.
4. Five-phase pulse output can be obtained by writing H'40, H'60, H'20, H'30, H'10, H'18, H'08, H'88… at successive compare match interrupts. If the DMA controller is set for activation by compare match, pulse output can be obtained without imposing a load on the CPU.

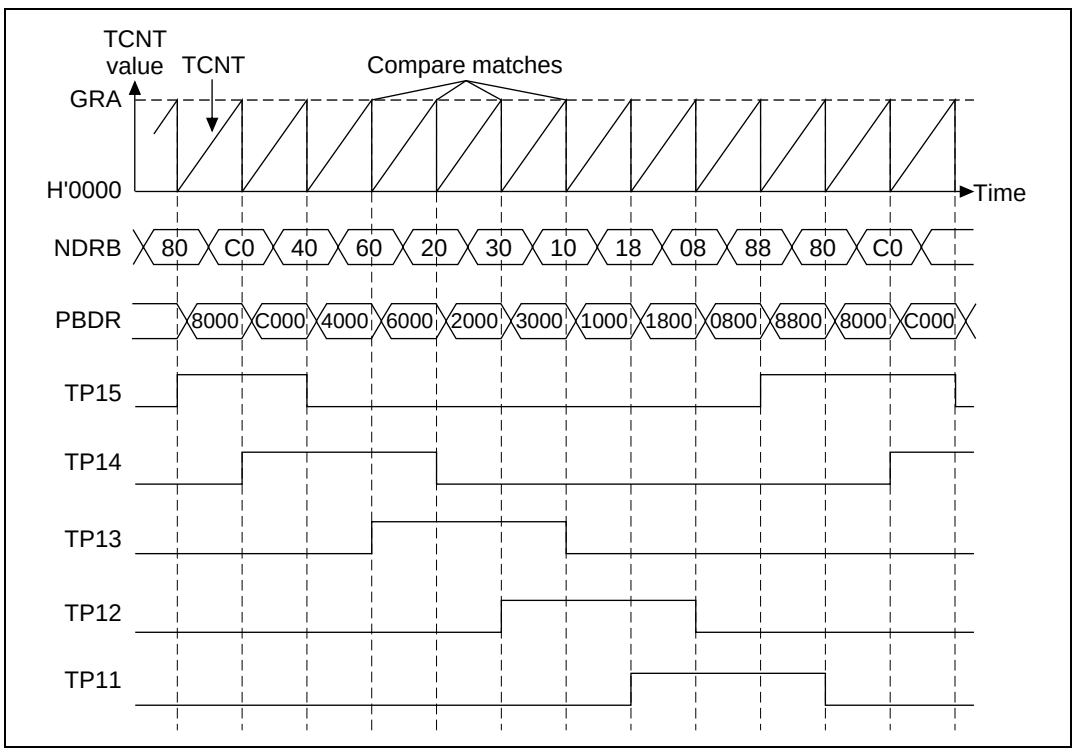


Figure 11.5 TPC Output Example (5-Phase Pulse Output)

11.3.4 TPC Output Non-Overlap Operation

Setting Procedures for TPC Output Non-Overlap Operation (Figure 11.6):

1. Select GRA and GRB as output compare registers (output disable) with the timer I/O control register (TIOR).
2. Set the TPC output trigger cycle in GRB and the non-overlap cycle in GRA.
3. Select the counter clock with the TPSC2–TPSC0 bits in the timer control register (TCR). Select the counter clear sources with the CCLR1 and CCLR0 bits.
4. Set the timer interrupt enable register (TIER) to enable IMIA interrupts. Transfers to NDR can also be set using the DMAC.
5. Set the initial output value in the I/O port data register to be used by the TPC.
6. Set the I/O port control register to be used by the TPC as the TP pin function (11).
7. Set to 1 the bit that performs TPC output to the next data enable register (NDER).
8. Select the ITU compare match that will be the TPC output trigger using the TPC output control register (TPCR).
9. Select the group that performs non-overlap operation in the TPC output mode register (TPMR).
10. Set the next TPC output value in NDR.
11. Set 1 in the STR bit of the timer start register (TSTR) and start the timer counter.
12. Set the next output value in NDR whenever an IMIA interrupt is generated.

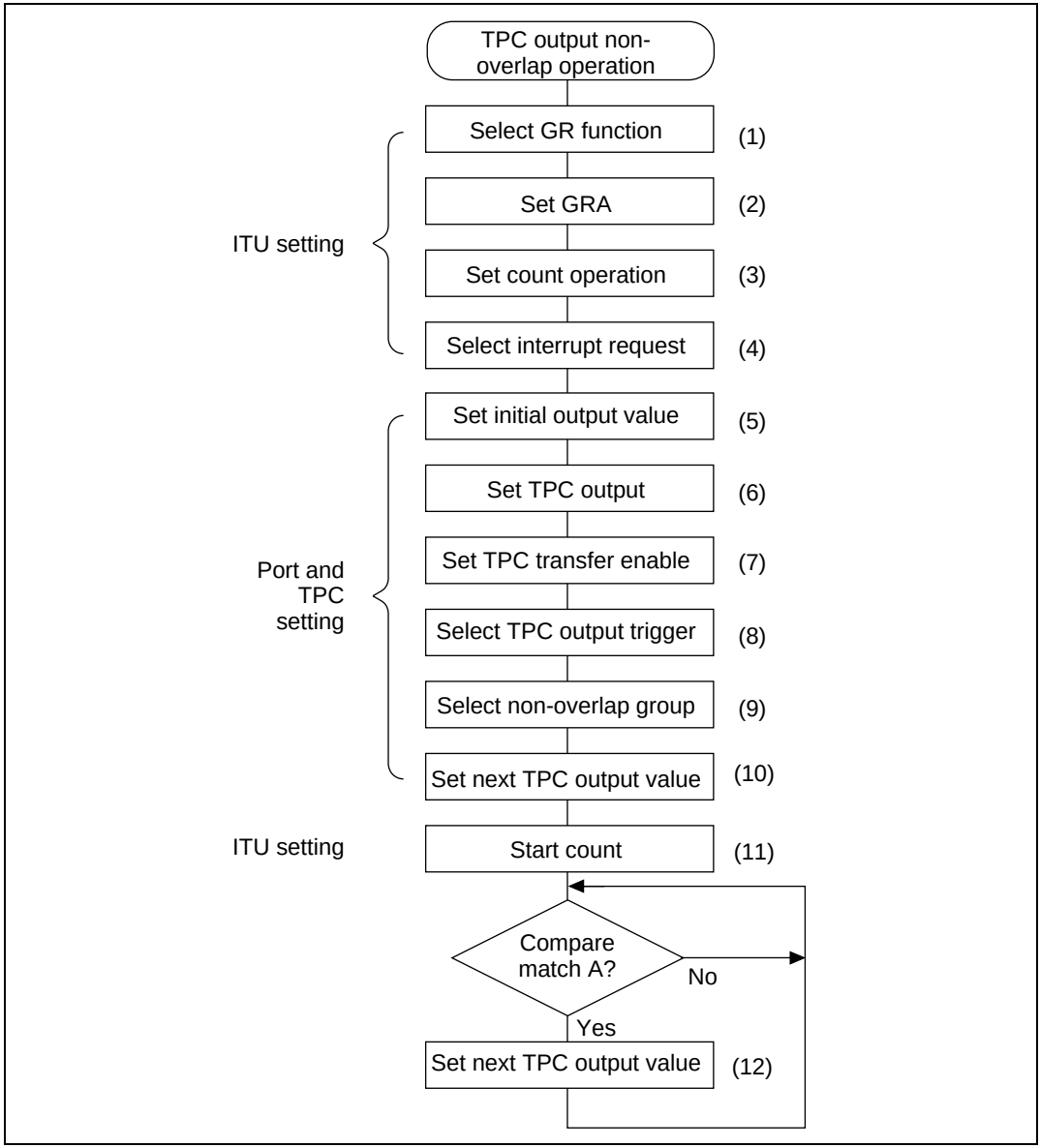


Figure 11.6 Example of Setting Procedure for TPC Output Non-Overlap Operation

TPC Output Non-Overlap Operation (Four-Phase Complementary Non-Overlap Output) (Figure 11.7):

1. Set the GRA and GRB registers of the ITU that serves as output triggers as output compare registers. Set the cycle in GRB and the non-overlap cycle time in GRA and select counter clearing upon compare match B. Set the IMIEA bit in TIER to 1 to enable the IMIA interrupt.
2. Write H'FFFF in PBCR1, write H'FF in NDERB, and set G3CMS1, G3CMS0, G2CMS1, and G2CMS0 in TPCR to set the ITU compare match selected in step 1 as the output trigger. Set the G3NOV and G2NOV bits in TPMR to 1 to set non-overlap operation. Write output data H'95 in NDRB.
3. When the selected ITU channel starts operating and a GRB compare match occurs, 1 output changes to 0 output; when a GRA compare match occurs, 0 output changes to 1 output. (The change from 0 output to 1 output is delayed by the value set in GRA.) The IMIA interrupt handling routine writes the next output data (H'65) in NDRB.
4. Four-phase complementary non-overlap output can be obtained by writing H'59, H'56, H'95… at successive IMIA interrupts. If the DMA controller is set for activation by compare match, pulse output can be obtained without imposing a load on the CPU.

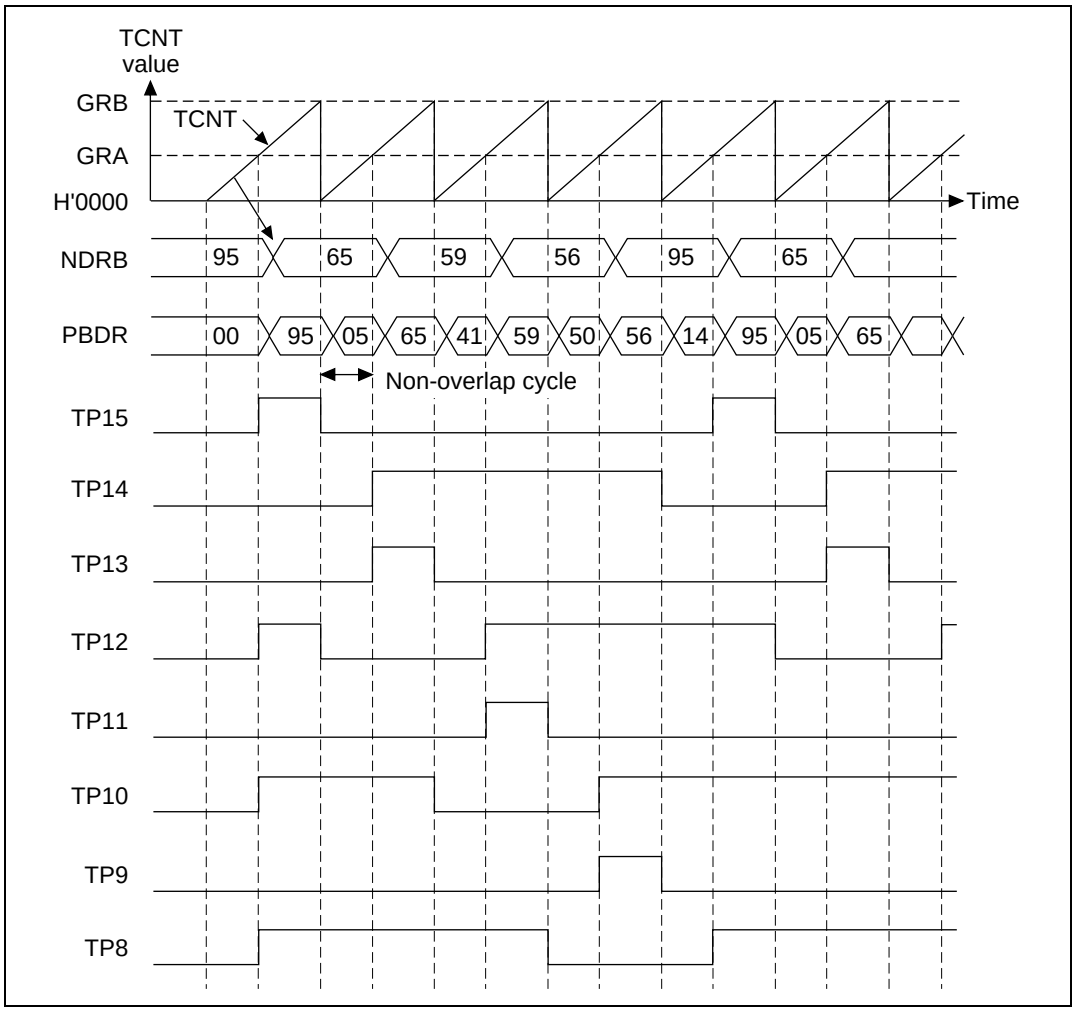


Figure 11.7 Non-Overlap Output Example (Four-Phase Complementary Output)

11.3.5 TPC Output by Input Capture

TPC can also be output by using input capture rather than ITU compare matches. The general register A (GRA) of the ITU selected by TPCR functions as an input capture register and TPC output occurs in response to an input capture signal. Figure 11.8 shows the timing.

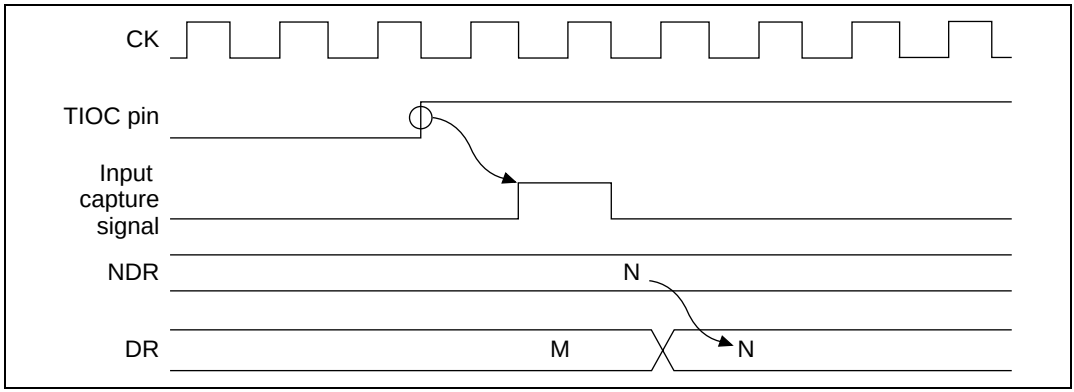


Figure 11.8 TPC Output by Input Capture

11.4 Usage Notes

11.4.1 Non-Overlap Operation

During non-overlap operation, transfers from NDR to data registers (DR) occur as follows.

1. NDR contents are always transferred to DR on compare match A.
2. The contents of bits transferred from NDR are only transferred on compare match B when they are 0. No transfer occurs for a 1.

Figure 11.9 illustrates TPC output during non-overlap operation.

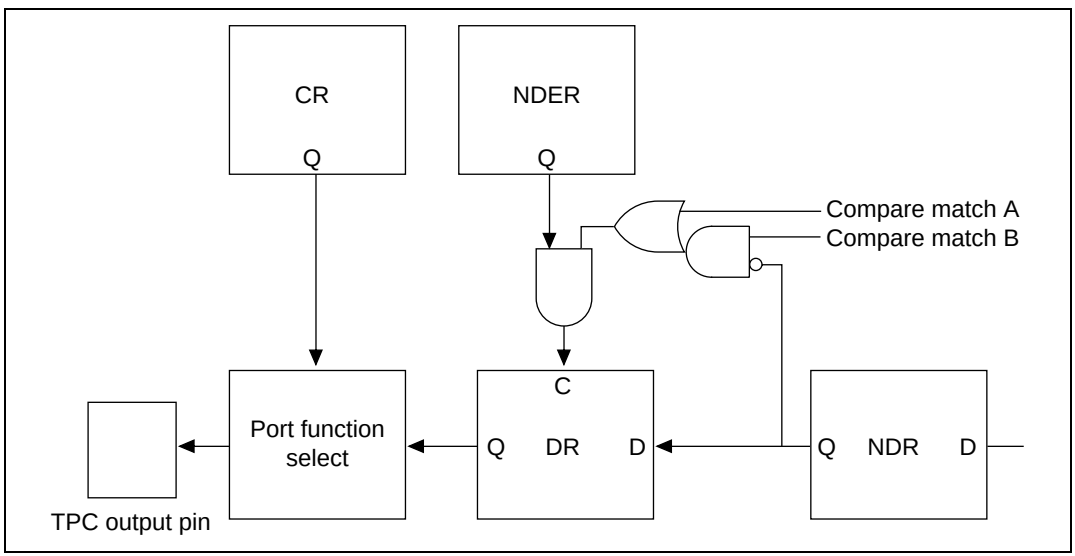


Figure 11.9 TPC Output Non-Overlap Operation

When a compare match B occurs before the compare match A, the 0 data transfer can be performed before the 1 data transfer, so a non-overlapping waveform can be output. In such cases, be sure not to change the NDR contents until the compare match A after the compare match B occurs (non-overlap period). This can be ensured by writing the next data to NDR in the IMIA interrupt handling routine. The DMAC can also be started using an IMIA interrupt. However, these write operations should be performed prior to the next compare match B. The timing is shown in figure 11.10.

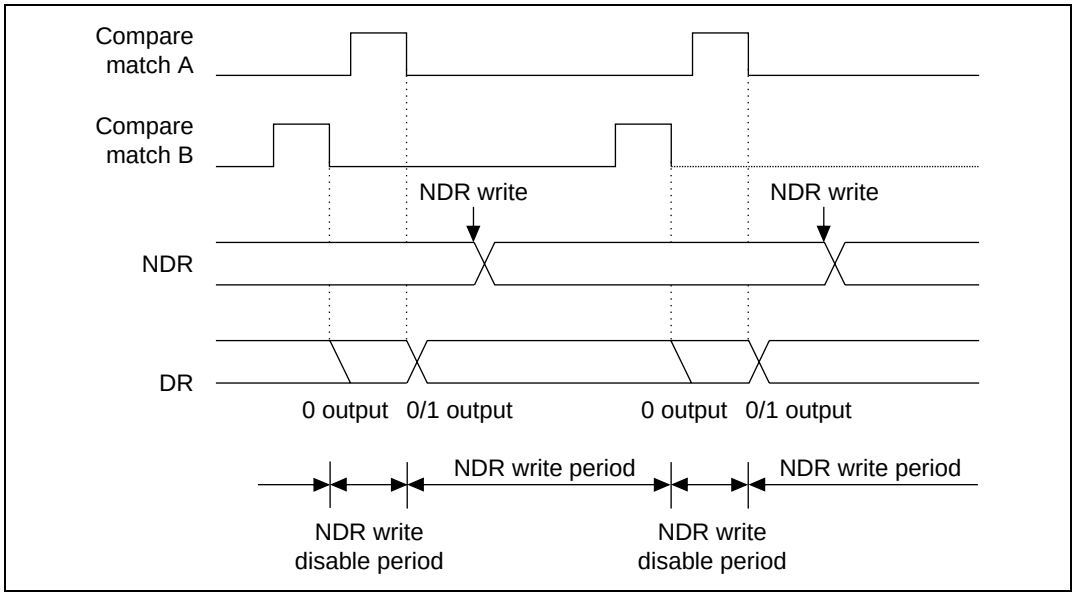


Figure 11.10 Non-Overlap Operation and NDR Write Timing

Section 12 Watchdog Timer (WDT)

12.1 Overview

The SuperH microcomputer has a one-channel watchdog timer (WDT) for monitoring system operations. If the system becomes uncontrolled and the timer counter overflows without being rewritten correctly by the CPU, an overflow signal ($\overline{\text{WDTOVF}}$) is output externally. The WDT can simultaneously generate an internal reset signal for the entire chip.

When this watchdog function is not needed, the WDT can be used as an interval timer. In the interval timer operation, an interval timer interrupt is generated at each counter overflow. The WDT is also used in recovering from standby mode.

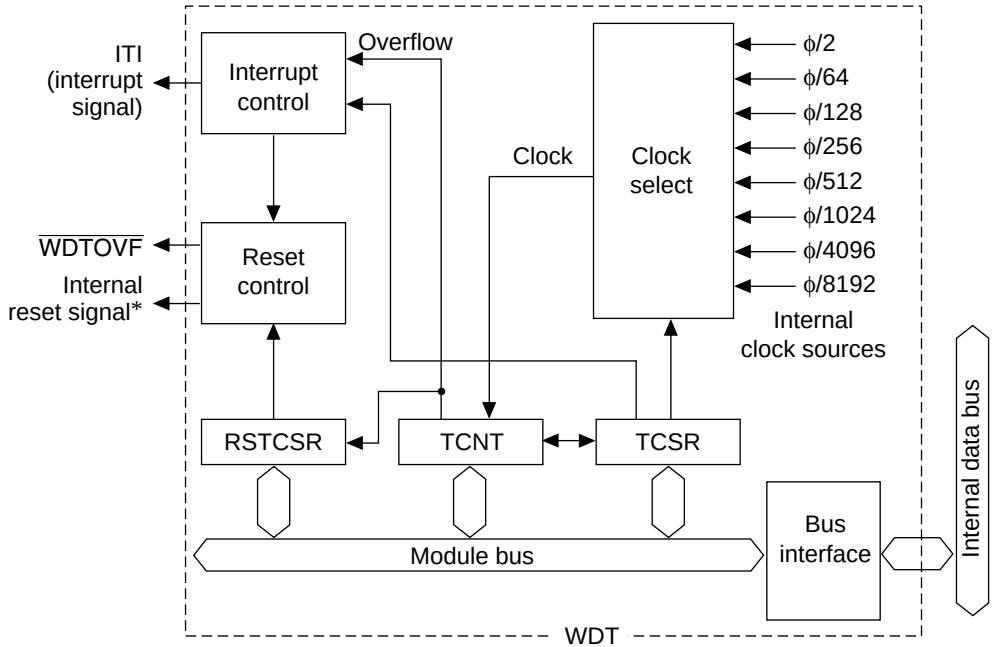
12.1.1 Features

WDT features are listed below:

- Watchdog timer mode interval timer mode can be selected.
- Outputs $\overline{\text{WDTOVF}}$ in or watchdog timer mode. When the counter overflows in watchdog timer mode, overflow signal $\overline{\text{WDTOVF}}$ is output externally. It is possible to select whether or not to reset the chip internally when this happens. Either the power-on reset or manual reset signal can be selected as the internal reset signal.
- Generates interrupts in interval timer mode. When the counter overflows, it generates an interval timer interrupt.
- Used to clear standby mode.
- Selection of eight counter clock sources

12.1.2 Block Diagram

Figure 12.1 shows a block diagram of the WDT.



TCSR: Timer control/status register
TCNT: Timer counter
RSTCSR: Reset control/status register
Note: * The internal reset signal can be generated by a register setting. The type of reset can be selected (power-on or manual reset).

Figure 12.1 Block Diagram of WDT

12.1.3 Pin Configuration

Table 12.1 shows the pin configuration.

Table 12.1 Pin Configuration

Pin	Abbreviation	I/O	Function
Watchdog timer overflow	$\overline{\text{WDTOVF}}$	O	Outputs the counter overflow signal in watchdog mode

12.1.4 Register Configuration

Table 12.2 summarizes the three WDT registers. They are used to select the clock, switch the WDT mode, and control the reset signal.

Table 12.2 WDT Registers

Name	Abbreviation	R/W	Initial Value	Address*4	
				Write*1	Read*2
Timer control/status register	TCSR	R/(W)*3	H'18	H'5FFFFB8	H'5FFFFB8
Timer counter	TCNT	R/W	H'00		H'5FFFFB9
Reset control/status register	RSTCSR	R/(W)*3	H'1F	H'5FFFFBA	H'5FFFFBB

Notes: 1. Write by word transfer. A byte or longword write cannot be used.
2. Read by byte transfer. The correct value cannot be obtained by a word or longword read.
3. Only 0 can be written in bit 7, to clear the flag.
4. Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions

12.2 Register Descriptions

12.2.1 Timer Counter (TCNT)

TCNT is an eight-bit readable and writable up-counter. TCNT differs from other registers in that it is more difficult to write. See section 12.2.4, Notes on Register Access, for details. When the timer enable bit (TME) in the timer control/status register (TCSR) is set to 1, the timer counter starts counting pulses of an internal clock source selected by clock select bits 2–0 (CKS2–CKS0) in TCSR. When the value of TCNT overflows (changes from H'FF to H'00), a watchdog timer overflow signal ($\overline{\text{WDTOVF}}$) or interval timer interrupt (ITI) is generated, depending on the mode selected with the WT/$\overline{\text{IT}}$ bit in TCSR. TCNT is initialized to H'00 by a reset and when the TME bit is cleared to 0. It is not initialized in standby mode.

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.2.2 Timer Control/Status Register (TCSR)

The timer control/status register (TCSR) is an eight-bit read/write register. TCSR differs from other registers in being more difficult to write. See section 12.2.4, Register Access, for details. Its functions include selecting the timer mode and clock source. Bits 7–5 are initialized to 000 by a reset and in standby mode. Bits 2–0 are initialized to 000 by a reset, but retain their values in standby mode.

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{\text{IT}}$	TME	—	—	CKS2	CKS1	CKS0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/(W)*	R/W	R/W	—	—	R/W	R/W	R/W

Note: * Only 0 can be written, to clear the flag.

Bit 7—Overflow Flag (OVF): OVF indicates that TCNT has overflowed from H'FF to H'00 in interval timer mode. It is not set in watchdog timer mode.

Bit 7: OVF	Description
0	No overflow of TCNT in interval timer mode (Initial value) Cleared by reading OVF, then writing 0 in OVF
1	TCNT overflow in interval timer mode

Bit 6—Timer Mode Select (WT/$\overline{\text{IT}}$): WT/$\overline{\text{IT}}$ selects whether to use the WDT as a watchdog timer or interval timer. When TCNT overflows, the WDT either generates an interval timer interrupt (ITI) or generates a $\overline{\text{WDTOVF}}$ signal, depending on the mode selected.

Bit 6: WT/$\overline{\text{IT}}$	Description
0	Interval timer mode: interval timer interrupt to the CPU when TCNT overflows (Initial value)
1	Watchdog timer mode: $\overline{\text{WDTOVF}}$ signal output externally when TCNT overflows. Section 12.2.3, Reset Control/Status Register (RSTCSR), describes in detail what happens when TCNT overflows in watchdog timer mode.

Bit 5—Timer Enable (TME): TME enables or disables the timer.

Bit 5: TME	Description
0	Timer disabled: TCNT is initialized to H'00 and count-up stops (Initial value)
1	Timer enabled: TCNT starts counting. A $\overline{\text{WDTOVF}}$ signal or interrupt is generated when TCNT overflows.

Bits 4 and 3—Reserved): These bits are always read as 1. The write value should always be 1.

Bits 2–0—Clock Select 2–0 (CKS2–CKS0): CKS2–CKS0 select one of eight internal clock sources for input to TCNT. The clock signals are obtained by dividing the frequency of the system clock (φ).

			Description	
Bit 2: CKS2	**Bit 1: CKS1**	**Bit 0: CKS0**	**Clock Source**	**Overflow Interval* (φ = 20 MHz)**
0	0	0	φ/2 (Initial value)	25.6 µs
0	0	1	φ/64	819.2 µs
0	1	0	φ/128	1.6 ms
0	1	1	φ/256	3.3 ms
1	0	0	φ/512	6.6 ms
1	0	1	φ/1024	13.1 ms
1	1	0	φ/4096	52.4 ms
1	1	1	φ/8192	104.9 ms

Note: * The overflow interval listed is the time from when the TCNT begins counting at H'00 until an overflow occurs.

12.2.3 Reset Control/Status Register (RSTCSR)

RSTCSR is an eight-bit read/write register that controls output of the reset signal generated by timer counter (TCNT) overflow and selects the internal reset signal type. RSTCSR differs from other registers in that it is more difficult to write. See section 12.2.4, Notes on Register Access, for details. RSTCR is initialized to H'1F by input of a reset signal from the $\overline{\text{RES}}$ pin, but is not initialized by the internal reset signal generated by overflow of the WDT. It is initialized to H'1F in standby mode.

Bit	7	6	5	4	3	2	1	0
	WOVF	RSTE	RSTS	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/(W)*	R/W	R/W	—	—	—	—	—

Note: * Only 0 can be written in bit 7, to clear the flag.

Bit 7—Watchdog Timer Overflow (WOVF): WOVF indicates that TCNT has overflowed (from H'FF to H'00) in watchdog timer mode. It is not set in interval timer mode.

Bit 7: WOVF	Description	
0	No TCNT overflow in watchdog timer mode	(Initial value)
	Cleared when software reads WOVF, then writes 0 in WOVF	
1	Set by TCNT overflow in watchdog timer mode	

Bit 6—Reset Enable (RSTE): RSTE selects whether to reset the chip internally if the TCNT overflows in watchdog timer mode.

Bit 6: RSTE	Description	
0	Not reset when TCNT overflows	(Initial value)
	LSI not reset internally, but TCNT and TCSR reset within WDT.	
1	Reset when TCNT overflows	

Bit 5—Reset Select (RSTS): RSTS selects the type of internal reset generated if TCNT overflows in watchdog timer mode.

Bit 5: RSTS	Description	
0	Power-on reset	(Initial value)
1	Manual reset	

Bits 4–0—Reserved: These bits are always read as 1. The write value should always be 1.

12.2.4 Notes on Register Access

The watchdog timer's TCNT, TCSR, and RSTCSR registers differ from other registers in that they are more difficult to write. The procedures for writing and reading these registers are given below.

Writing to TCNT and TCSR: These registers must be written by a word transfer instruction. They cannot be written by byte transfer instructions. TCNT and TCSR both have the same write

address. The write data must be contained in the lower byte of the written word. The upper byte must be H'5A (for TCNT) or H'A5 (for TCSR) (figure 12.2). This transfers the write data from the lower byte to TCNT or TCSR.

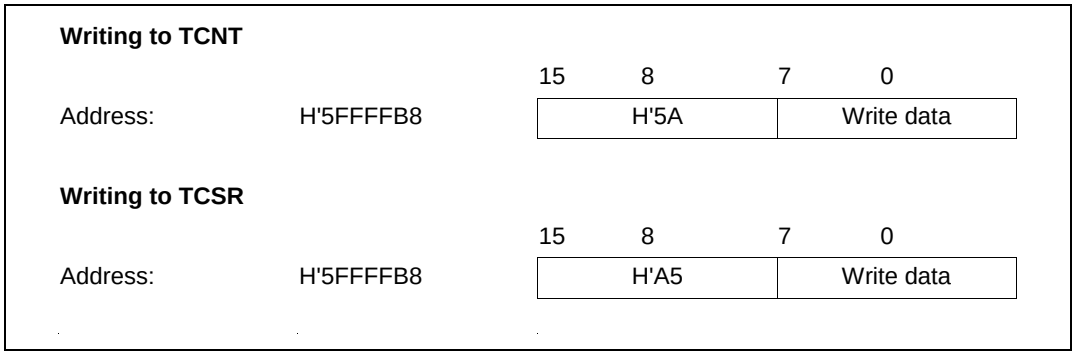


Figure 12.2 Writing to TCNT and TCSR

Writing to RSTCSR: RSTCSR must be written by a word access to address H'5FFFFFBA. It cannot be written by byte transfer instructions. Procedures for writing 0 in WOVF (bit 7) and for writing to RSTE (bit 6) and RSTS (bit 5) are different, as shown in figure 12.3. To write 0 in the WOVF bit, the write data must be H'A5 in the upper byte and H'00 in the lower byte. This clears the WOVF bit to 0. The RSTE and RSTS bits are not affected. To write to the RSTE and RSTS bits, the upper byte must be H'5A and the lower byte must be the write data. The values of bits 6 and 5 of the lower byte are transferred to the RSTE and RSTS bits, respectively. The WOVF bit is not affected.

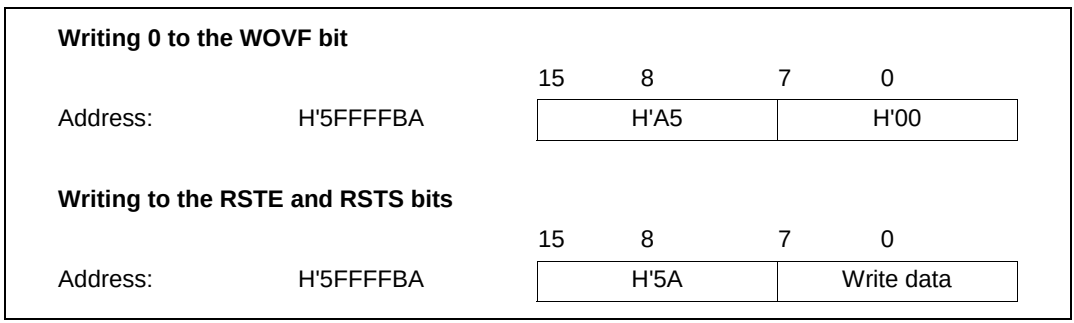


Figure 12.3 Writing to RSTCSR

Reading from TCNT, TCSR, and RSTCSR: TCNT, TCSR, and RSTCSR are read like other registers. Use byte transfer instructions. The read addresses are H'5FFFFB8 for TCSR, H'5FFFFB9 for TCNT, and H'5FFFFBB for RSTCSR.

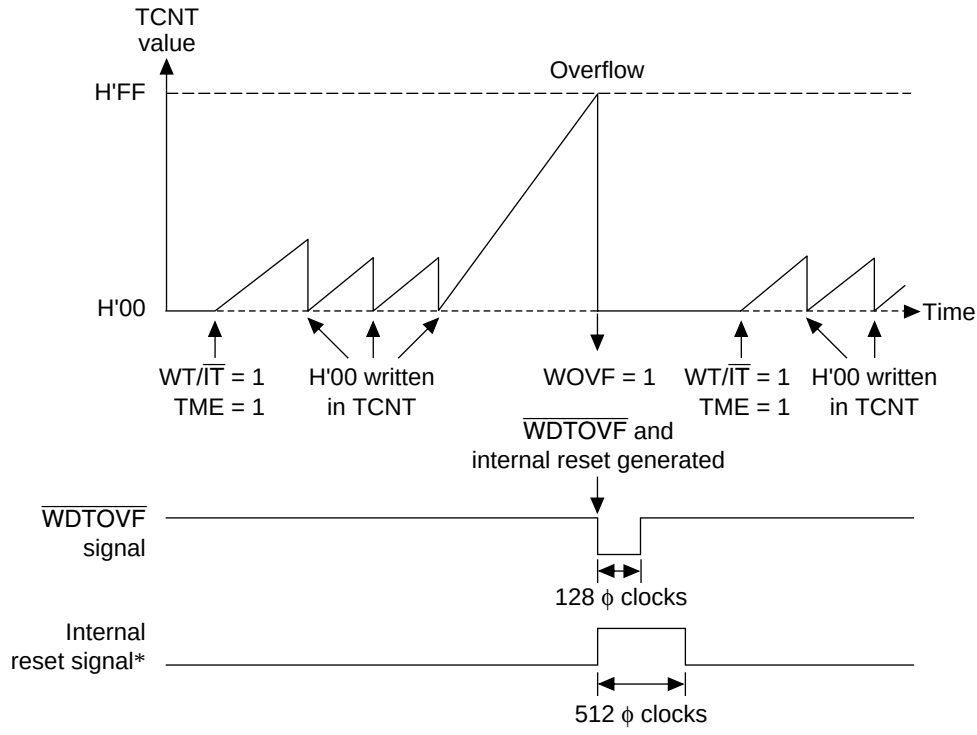
12.3 Operation

12.3.1 Operation in Watchdog Timer Mode

To use the WDT as a watchdog timer, set the WT/$\overline{IT}$ and TME bits in TCSR to 1. Software must prevent TCNT overflow by rewriting the TCNT value (normally by writing H'00) before overflow occurs. If TCNT fails to be rewritten and overflows due to a system crash or the like, a $\overline{WDTOVF}$ signal is output (figure 12.4). The $\overline{WDTOVF}$ signal can be used to reset external system devices. The $\overline{WDTOVF}$ signal is output for 128 ϕ clock cycles.

If the RSTE bit in RSTCSR is set to 1, a signal to reset the chip will be generated internally simultaneous to the $\overline{WDTOVF}$ signal when TCNT overflows. Either a power-on reset or a manual reset can be selected by the RSTS bit in RSTCSR. The internal reset signal is output for 512 ϕ clock cycles.

When a watchdog reset is generated simultaneously with input at the $\overline{RES}$ pin, the software distinguishes the $\overline{RES}$ reset from the watchdog reset by checking the WOVF bit in RSTCSR. The $\overline{RES}$ reset takes priority. The WOVF bit is cleared to 0.



WT/IT: Timer mode select bit
TME: Timer enable bit
Note: * The internal reset signal is only generated when the RSTE bit is 1.

Figure 12.4 Operation in Watchdog Timer Mode

12.3.2 Operation in Interval Timer Mode

To use the WDT as an interval timer, clear WT/$\overline{IT}$ to 0 and set TME to 1. An interval timer interrupt (ITI) is generated each time the timer counter overflows. This function can be used to generate interval timer interrupts at regular intervals (figure 12.5).

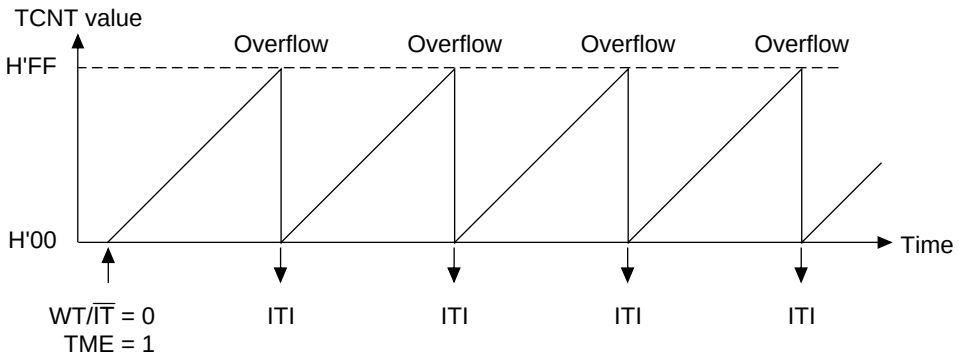


Figure 12.5 Operation in Interval Timer Mode

12.3.3 Operation in Standby Mode

The watchdog timer has a special function to clear standby mode with an NMI interrupt. When using standby mode, set the WDT as described below.

Transition to Standby Mode: The TME bit in TCSR must be cleared to 0 to stop the watchdog timer counter before it enters standby mode. The chip cannot enter standby mode while the TME bit is set to 1. Set bits CKS2–CKS0 so that the counter overflow interval is equal to or longer than the oscillation settling time. See sections 20.1.3 and 20.2.3, AC Characteristics, for the oscillation settling time.

Recovery from Standby Mode: When an NMI request signal is received in standby mode, the clock oscillator starts running and the watchdog timer starts counting at the rate selected by bits CKS2–CKS0 before standby mode was entered. When TCNT overflows (changes from H'FF to H'00), the system clock (ϕ) is presumed to be stable and usable; clock signals are supplied to the entire chip and standby mode ends.

For details on standby mode, see section 19, Power Down State.

12.3.4 Timing of Overflow Flag (OVF) Setting

In interval timer mode, when TCNT overflows the OVF flag in TCSR is set to 1 and an interval timer interrupt is requested (figure 12.6).

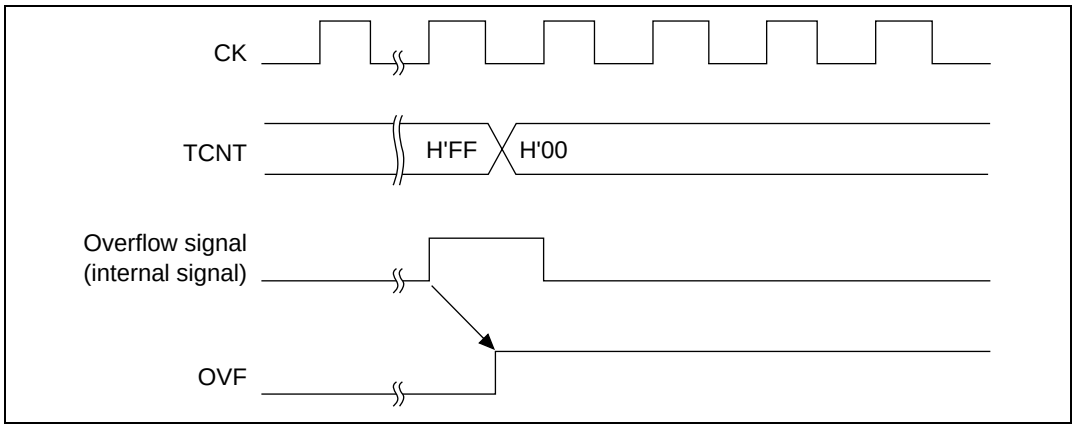


Figure 12.6 Timing of OVF Setting

12.3.5 Timing of Watchdog Timer Overflow Flag (WOVF) Setting

When TCNT overflows the WOVF bit in RSTCSR is set to 1 and a $\overline{\text{WDTOVF}}$ signal is output. When the RSTE bit is set to 1, TCNT overflow enables an internal reset signal to be generated for the entire chip (figure 12.7).

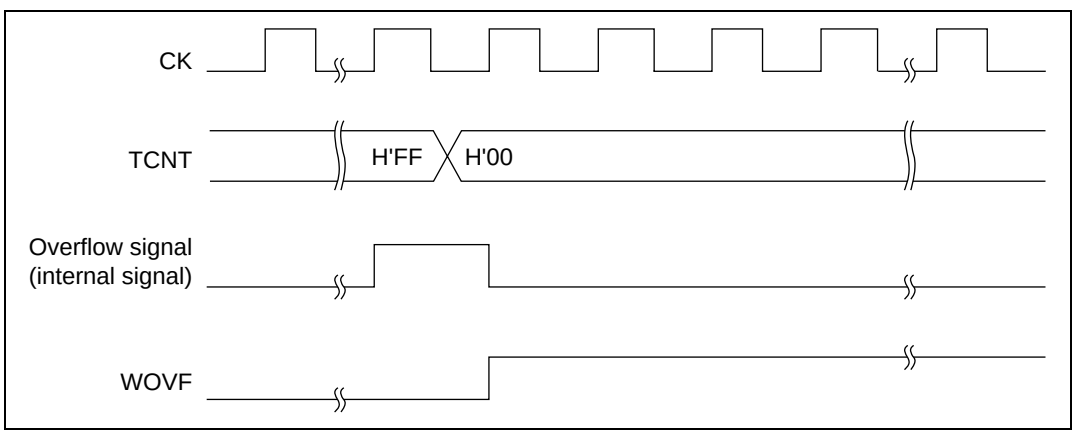


Figure 12.7 Timing of WOVF Bit Setting and Internal Reset

12.4 Usage Notes

12.4.1 TCNT Write and Increment Contention

If a timer counter clock pulse is generated during the T3 state of a write cycle to TCNT, the write takes priority and the timer counter is not incremented (figure 12.8).

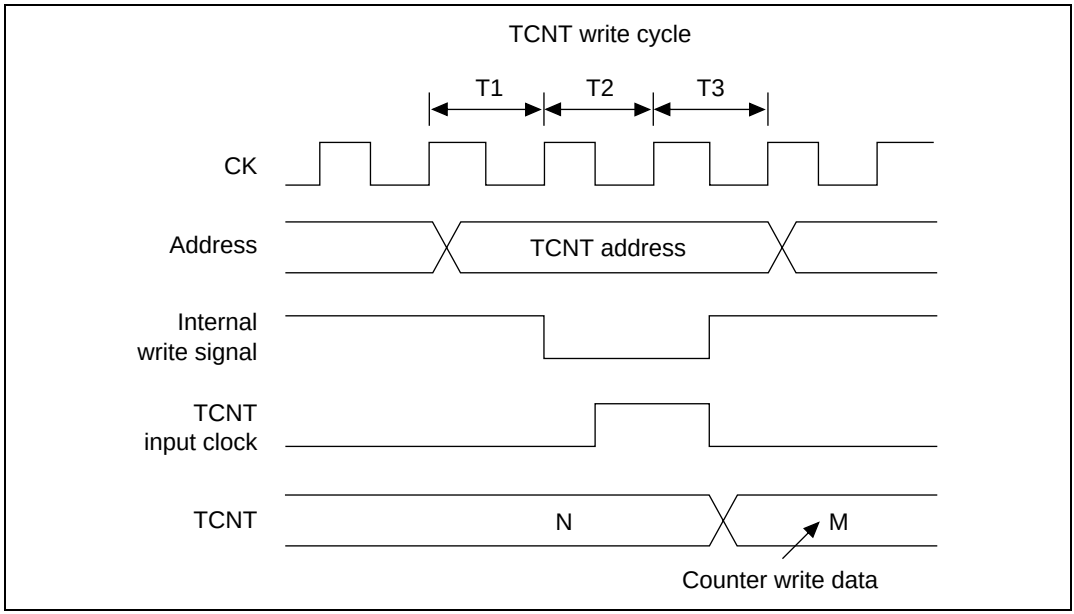


Figure 12.8 Contention between TCNT Write and Increment

12.4.2 Changing CKS2–CKS0 Bit Values

If the values of bits CKS2–CKS0 are altered while the WDT is running, the count may increment incorrectly. Always stop the watchdog timer (by clearing the TME bit to 0) before changing the values of bits CKS2–CKS0.

12.4.3 Changing Watchdog Timer/Interval Timer Modes

To prevent incorrect operation, always stop the watchdog timer (by clearing the TME bit to 0) before switching between interval timer mode and watchdog timer mode.

12.4.4 System Reset With $\overline{\text{WDTOVF}}$

If a $\overline{\text{WDTOVF}}$ signal is input to the $\overline{\text{RES}}$ pin, the chip cannot initialize correctly. Avoid logical input of the $\overline{\text{WDTOVF}}$ output signal to the $\overline{\text{RES}}$ input pin. To reset the entire system with the $\overline{\text{WDTOVF}}$ signal, use the circuit shown in figure 12.9.

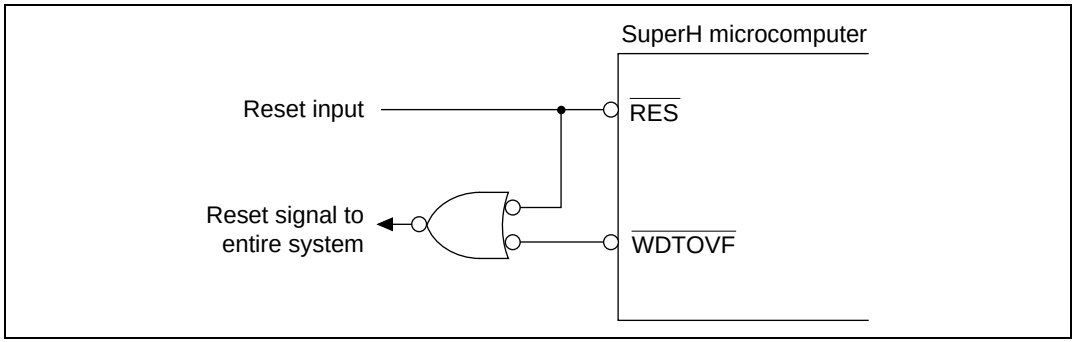


Figure 12.9 Example of System Reset Circuit Using $\overline{\text{WDTOVF}}$ Signal

12.4.5 Internal Reset With Watchdog Timer

If the RSTE bit is cleared to 0 in watchdog timer mode, the chip will not reset internally when a TCNT overflow occurs, but TCNT and TCSR in the WDT will reset.

Section 13 Serial Communication Interface (SCI)

13.1 Overview

The SuperH microcomputer has a serial communication interface (SCI) with two independent channels. Both channels are functionally identical. The SCI supports both asynchronous and synchronous serial communication. It also has a multiprocessor communication function for serial communication between two or more processors.

13.1.1 Features

SCI features are listed below:

- Asynchronous mode
  - Serial data communication is synchronized using a start-stop method in character units. The SCI can communicate with a universal asynchronous receiver/transmitter (UART), an asynchronous communication interface adapter (ACIA), or any other chip that employs standard asynchronous serial communication. It can also communicate with two or more other processors using the multiprocessor communication function. There are twelve selectable serial data communication formats.
  - Data length: seven or eight bits
  - Stop bit length: one or two bits
  - Parity: even, odd, or none
  - Multiprocessor bit: one or none
  - Receive error detection: parity, overrun, and framing errors
  - Break detection: by reading the RxD level directly when a framing error occurs
- Synchronous mode
  - Serial data communication is synchronized with a clock signal. The SCI can communicate with other chips having a synchronous communication function. There is one serial data communication format.
  - Data length: eight bits
  - Receive error detection: overrun errors
- Full duplex communication: The transmitting and receiving sections are independent, so the SCI can transmit and receive simultaneously. Both sections use double buffering, so continuous data transfer is possible in both the transmit and receive directions.
- On-chip baud rate generator with selectable bit rates

- Internal or external transmit/receive clock source: baud rate generator (internal) or SCK pin (external)
- Four types of interrupts: Transmit-data-empty, transmit-end, receive-data-full, and receive-error interrupts are requested independently. The transmit-data-empty and receive-data-full interrupts can start the direct memory access controller (DMAC) to transfer data.

13.1.2 Block Diagram

Figure 13.1 shows a block diagram of the SCI.

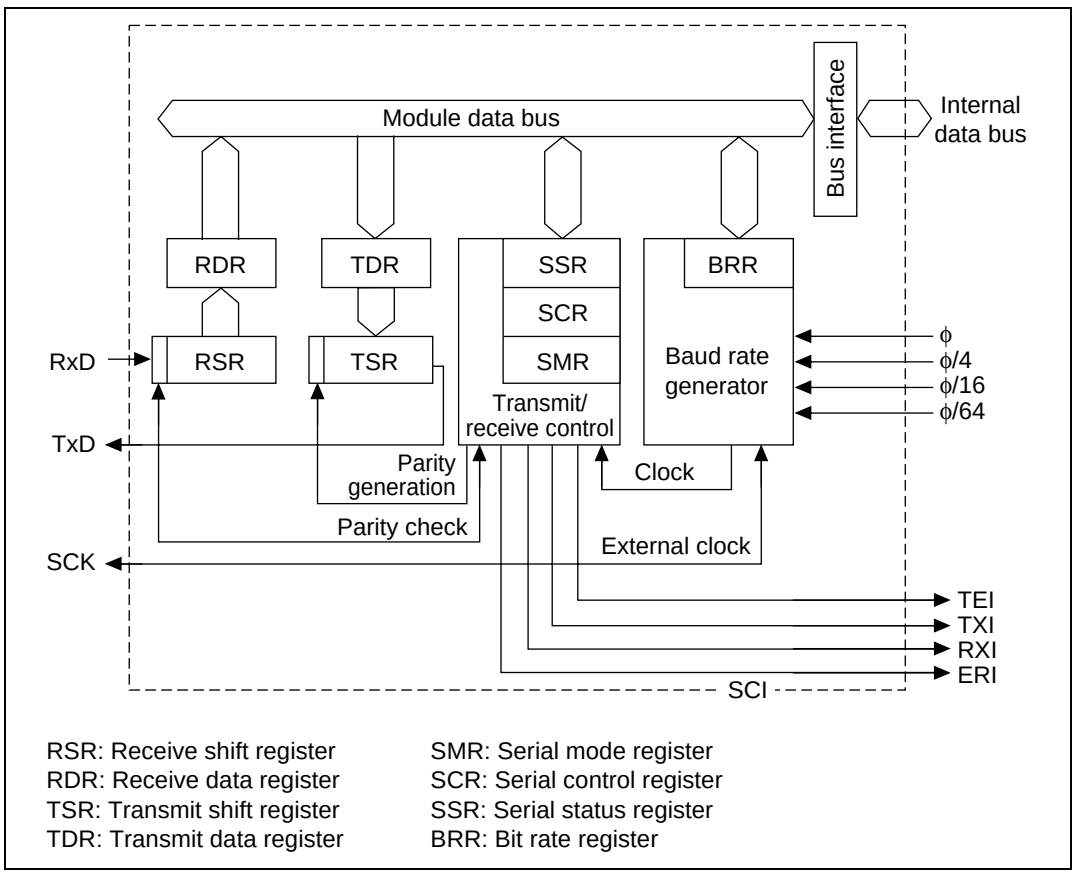


Figure 13.1 Block Diagram of SCI

13.1.3 Input/Output Pins

Table 13.1 summarizes the SCI pins by channel.

Table 13.1 SCI Pins

Channel	Pin Name	Abbreviation	Input/Output	Function
0	Serial clock pin	SCK0	Input/output	SCI0 clock input/output
	Receive data pin	RxD0	Input	SCI0 receive data input
	Transmit data pin	TxD0	Output	SCI0 transmit data output
1	Serial clock pin	SCK1	Input/output	SCI1 clock input/output
	Receive data pin	RxD1	Input	SCI1 receive data input
	Transmit data pin	TxD1	Output	SCI1 transmit data output

13.1.4 Register Configuration

Table 13.2 summarizes the SCI internal registers. These registers select the communication mode (asynchronous or synchronous), specify the data format and bit rate, and control the transmitter and receiver sections.

Table 13.2 Registers

Channel	Address*1	Name	Abbreviation	R/W	Initial Value	Access size
0	H'05FFFEC0	Serial mode register	SMR0	R/W	H'00	8, 16
	H'05FFFEC1	Bit rate register	BRR0	R/W	H'FF	8, 16
	H'05FFFEC2	Serial control register	SCR0	R/W	H'00	8, 16
	H'05FFFEC3	Transmit data register	TDR0	R/W	H'FF	8, 16
	H'05FFFEC4	Serial status register	SSR0	R/(W)*2	H'84	8, 16
	H'05FFFEC5	Receive data register	RDR0	R	H'00	8, 16
1	H'05FFFEC8	Serial mode register	SMR1	R/W	H'00	8, 16
	H'05FFFEC9	Bit rate register	BRR1	R/W	H'FF	8, 16
	H'05FFFECA	Serial control register	SCR1	R/W	H'00	8, 16
	H'05FFFECB	Transmit data register	TDR1	R/W	H'FF	8, 16
	H'05FFFECC	Serial status register	SSR1	R/(W)*2	H'84	8, 16
	H'05FFFECD	Receive data register	RDR1	R	H'00	8, 16

Notes: 1. Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.
2. Only 0 can be written, to clear flags.

13.2 Register Descriptions

13.2.1 Receive Shift Register

The receive shift register (RSR) receives serial data. Data input at the RxD pin is loaded into RSR in the order received, LSB (bit 0) first. In this way the SCI converts received data to parallel form. When one byte has been received, it is automatically transferred to the receive data register (RDR). The CPU cannot read or write to RSR directly.

Bit	7	6	5	4	3	2	1	0
Read/Write	—	—	—	—	—	—	—	—

13.2.2 Receive Data Register

The receive data register (RDR) stores serial receive data. The SCI completes the reception of one byte of serial data by moving the received data from the receive shift register (RSR) into RDR for

storage. RSR is then ready to receive the next data. This double buffering allows the SCI to receive data continuously.

The CPU can read but not write to RDR. RDR is initialized to H'00 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

13.2.3 Transmit Shift Register

The transmit shift register (TSR) transmits serial data. The SCI loads transmit data from the transmit data register (TDR) into TSR, then transmits the data serially from the TxD pin, LSB (bit 0) first. After transmitting one data byte, the SCI automatically loads the next transmit data from TDR into TSR and starts transmitting again. If the TDRE bit in SSR is 1, however, the SCI does not load the TDR contents into TSR. The CPU cannot read or write to TSR directly.

Bit	7	6	5	4	3	2	1	0
Read/Write	—	—	—	—	—	—	—	—

13.2.4 Transmit Data Register

The transmit data register (TDR) is an eight-bit register that stores data for serial transmission. When the SCI detects that the transmit shift register (TSR) is empty, it moves transmit data written in TDR into TSR and starts serial transmission. Continuous serial transmission is possible by writing the next transmit data in TDR during serial transmission from TSR.

The CPU can always read and write to TDR. TDR is initialized to H'FF by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.2.5 Serial Mode Register

The serial mode register (SMR) is an eight-bit register that specifies the SCI serial communication format and selects the clock source for the baud rate generator.

The CPU can always read and write to SMR. SMR is initialized to H'00 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7—Communication Mode (C/$\overline{A}$): C/$\overline{A}$ selects whether the SCI operates in asynchronous or synchronous mode.

Bit 7: C/$\overline{A}$	Description	
0	Asynchronous mode	(Initial value)
1	Synchronous mode	

Bit 6—Character Length (CHR): CHR selects seven-bit or eight-bit data in asynchronous mode. In synchronous mode, the data length is always eight bits, regardless of the CHR setting.

Bit 6: CHR	Description	
0	Eight-bit data	(Initial value)
1	Seven-bit data. When seven-bit data is selected, the MSB (bit 7) of the transmit data register is not transmitted.	

Bit 5—Parity Enable (PE): PE selects whether to add a parity bit to transmit data and check the parity of receive data, in asynchronous mode. In synchronous mode, a parity bit is neither added nor checked, regardless of the PE setting.

Bit 5: PE	Description	
0	Parity bit not added or checked	(Initial value)
1	Parity bit added and checked. When PE is set to 1, an even or odd parity bit is added to transmit data, depending on the parity mode (O/$\overline{E}$) setting. Receive data parity is checked according to the even/odd (O/$\overline{E}$) mode setting.	

Bit 4—Parity Mode (O/$\overline{E}$): O/$\overline{E}$ selects even or odd parity when parity bits are added and checked. The O/$\overline{E}$ setting is used only in asynchronous mode and only when the parity enable bit (PE) is set to 1 to enable parity addition and checking. The O/$\overline{E}$ setting is ignored in synchronous mode, or in asynchronous mode when parity addition and checking is disabled.

Bit 4: O/$\overline{E}$	Description
0	Even parity (Initial value) If even parity is selected, the parity bit added to transmit data makes an even number of 1s in the transmitted character and parity bit combined. Receive data must have an even number of 1s in the received character and parity bit combined.
1	Odd parity If odd parity is selected, the parity bit added to transmit data makes an odd number of 1s in the transmitted character and parity bit combined. Receive data must have an odd number of 1s in the received character and parity bit combined.

Bit 3—Stop Bit Length (STOP): STOP selects one or two bits as the stop bit length in asynchronous mode. This setting is used only in asynchronous mode. It is ignored in synchronous mode because no stop bits are added.

In receiving, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit. If the second stop bit is 0, it is treated as the start bit of the next incoming character.

Bit 3: STOP	Description
0	One stop bit (Initial value) In transmitting, a single 1-bit is added at the end of each transmitted character.
1	Two stop bits. In transmitting, two 1-bits are added at the end of each transmitted character.

Bit 2—Multiprocessor Mode (MP): MP selects multiprocessor format. When multiprocessor format is selected, settings of the parity enable (PE) and parity mode (O/$\overline{E}$) bits are ignored. The MP bit setting is used only in asynchronous mode; it is ignored in synchronous mode. For the multiprocessor communication function, see section 13.3.3, Multiprocessor Communication.

Bit 2: MP	Description
0	Multiprocessor function disabled (Initial value)
1	Multiprocessor format selected

Bits 1 and 0—Clock Select 1 and 0 (CKS1 and CKS0): CKS1 and CKS0 select the internal clock source of the on-chip baud rate generator. Four clock sources are available: ϕ, $\phi/4$, $\phi/16$, and $\phi/64$. For further information on the clock source, bit rate register settings, and baud rate, see section 13.2.8, Bit Rate Register (BRR).

Bit 1: CKS1	Bit 0: CKS0	Description	
0	0	System clock (ϕ)	(Initial value)
	1	$\phi/4$	
1	0	$\phi/16$	
	1	$\phi/64$	

13.2.6 Serial Control Register

The serial control register (SCR) enables the SCI transmitter/receiver, selects serial clock output in asynchronous mode, enables and disables interrupts, and selects the transmit/receive clock source. The CPU can always read and write to SCR. SCR is initialized to H'00 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7—Transmit Interrupt Enable (TIE): TIE enables or disables the transmit-data-empty interrupt (TXI) requested when the transmit data register empty bit (TDRE) in the serial status register (SSR) is set to 1 due to transfer of serial transmit data from TDR to TSR.

Bit 7: TIE	Description	
0	Transmit-data-empty interrupt request (TXI) is disabled	(Initial value)
	The TXI interrupt request can be cleared by reading TDRE after it has been set to 1, then clearing TDRE to 0, or by clearing TIE to 0.	
1	Transmit-data-empty interrupt request (TXI) is enabled	

Bit 6—Receive Interrupt Enable (RIE): RIE enables or disables the receive-data-full interrupt (RXI) requested when the receive data register full bit (RDRF) in the serial status register (SSR) is set to 1 due to transfer of serial receive data from RSR to RDR. Also enables or disables receive-error interrupt (ERI) requests.

Bit 6: RIE	Description
0	Receive-data-full interrupt (RXI) and receive-error interrupt (ERI) requests are disabled (Initial value) RXI and ERI interrupt requests can be cleared by reading the RDRF flag or error flag (FER, PER, or ORER) after it has been set to 1, then clearing the flag to 0, or by clearing RIE to 0.
1	Receive-data-full interrupt (RXI) and receive-error interrupt (ERI) requests are enabled

Bit 5—Transmit Enable (TE): TE enables or disables the SCI transmitter.

Bit 5: TE	Description
0	Transmitter disabled (Initial value) The transmit data register empty bit (TDRE) in the serial status register (SSR) is fixed at 1.
1	Transmitter enabled. Serial transmission starts when the transmit data register empty (TDRE) bit in the serial status register (SSR) is cleared to 0 after writing transmit data into TDR. Select the transmit format in SMR before setting TE to 1.

Bit 4—Receive Enable (RE): RE enables or disables the SCI receiver.

Bit 4: RE	Description
0	Receiver disabled (Initial value) Clearing RE to 0 does not affect the receive flags (RDRF, FER, PER, ORER). These flags retain their previous values.
1	Receiver enabled. Serial reception starts when a start bit is detected in asynchronous mode, or serial clock input is detected in synchronous mode. Select the receive format in SMR before setting RE to 1.

Bit 3—Multiprocessor Interrupt Enable (MPIE): MPIE enables or disables multiprocessor interrupts. The MPIE setting is used only in asynchronous mode, and only if the multiprocessor mode bit (MP) in the serial mode register (SMR) is set to 1 during reception. The MPIE setting is ignored in synchronous mode or when the MP bit is cleared to 0.

Bit 3: MPIE	Description
0	Multiprocessor interrupts are disabled (normal receive operation) (Initial value) MPE is cleared to 0 when: 1. MPIE is cleared to 0, or 2. Multiprocessor bit (MPB) is set to 1 in receive data.
1	Multiprocessor interrupts are enabled: Receive-data-full interrupt requests (RXI), receive-error interrupt requests (ERI), and setting of the RDRF, FER, and ORER status flags in the serial status register (SSR) are disabled until the multiprocessor bit is set to 1. The SCI does not transfer receive data from RSR to RDR, does not detect receive errors, and does not set the RDRF, FER, and ORER flags in the serial status register (SSR). When it receives data that includes MPB = 1, MPB is set to 1, and the SCI automatically clears MPIE to 0, generates RXI and ERI interrupts (if the TIE and RIE bits in SCR are set to 1), and allows FER and ORER to be set.

Bit 2—Transmit-End Interrupt Enable (TEIE): TEIE enables or disables the transmit-end interrupt (TEI) requested if TDR does not contain new transmit data when the MSB is transmitted.

Bit 2: TEIE	Description
0	Transmit-end interrupt (TEI) requests are disabled (Initial value) The TEI request can be cleared by reading the TDRE bit in the serial status register (SSR) after it has been set to 1, then clearing TDRE to 0; by clearing the transmit end (TEND) bit to 0; or by clearing the TEIE bit to 0.
1	Transmit-end interrupt (TEI) requests are enabled.

Bits 1 and 0—Clock Enable 1 and 0 (CKE1 and CKE0): CKE1 and CKE0 select the SCI clock source and enable or disable clock output from the SCK pin. Depending on the combination of CKE1 and CKE0, the SCK pin can be used for general-purpose input/output, serial clock output, or serial clock input. The SCK pin function should be selected in advance with the pin function controller (PFC).

The CKE0 setting is valid only in asynchronous mode, and only when the SCI is internally clocked (CKE1 = 0). The CKE0 setting is ignored in synchronous mode, or when an external clock source is selected (CKE1 = 1). Select the SCI operating mode in the serial mode register

(SMR) before setting CKE1 and CKE0. For further details on selection of the SCI clock source, see table 13.9 in section 13.3, Operation.

Bit 1: CKE1	Bit 0: CKE0	Description*1	
0	0	Asynchronous mode	Internal clock, SCK pin used for input pin (input signal is ignored) or output pin (output level is undefined)*2 (Initial value)
		Synchronous mode	Internal clock, SCK pin used for serial clock output*2 (Initial value)
0	1	Asynchronous mode	Internal clock, SCK pin used for clock output*3
		Synchronous mode	Internal clock, SCK pin used for serial clock output
1	0	Asynchronous mode	External clock, SCK pin used for clock input*4
		Synchronous mode	External clock, SCK pin used for serial clock input
1	1	Asynchronous mode	External clock, SCK pin used for clock input*4
		Synchronous mode	External clock, SCK pin used for serial clock input

Notes: 1. The SCK pin is multiplexed with other functions. Set the pin function controller (PFC) to select the SCK function and SCK input/output for the SCK pin.
2. Initial value
3. The output clock frequency is the same as the bit rate.
4. The input clock frequency is 16 times the bit rate.

13.2.7 Serial Status Register

The serial status register (SSR) is an 8-bit register containing multiprocessor bit values, and status flags that indicate the SCI operating status.

The CPU can always read and write to SSR, but cannot write 1 in the status flags (TDRE, RDRF, ORER, PER, and FER). These flags can be cleared to 0 only if they have first been read (after being set to 1). Bits 2 (TEND) and 1 (MPB) are read-only bits that cannot be written. SSR is initialized to H'84 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only 0 can be written, to clear the flag.

Bit 7—Transmit Data Register Empty (TDRE): TDRE indicates that the SCI has loaded transmit data from TDR into TSR and new serial transmit data can be written in TDR.

Bit 7: TDRE	Description
0	TDR contains valid transmit data TDRE is cleared to 0 when: • Software reads TDRE after it has been set to 1, then writes 0 in TDRE • The DMAC writes data in TDR
1	TDR does not contain valid transmit data (Initial value) TDRE is set to 1 when: • The chip is reset or enters standby mode • The TE bit in the serial control register (SCR) is cleared to 0 • TDR contents are loaded into TSR, so new data can be written in TDR

Bit 6—Receive Data Register Full (RDRF): RDRF indicates that RDR contains received data.

Bit 6: RDRF	Description
0	RDR does not contain valid received data (Initial value) RDRF is cleared to 0 when: • The chip is reset or enters standby mode • Software reads RDRF after it has been set to 1, then writes 0 in RDRF • The DMAC reads data from RDR
1	RDR contains valid received data. RDRF is set to 1 when serial data is received normally and transferred from RSR to RDR.

Note: RDR and RDRF are not affected by detection of receive errors or by clearing of the RE bit to 0 in the serial control register. They retain their previous contents. If RDRF is still set to 1 when reception of the next data ends, an overrun error (ORER) occurs and the received data is lost.

Bit 5—Overrun Error (ORER): Indicates that data reception ended abnormally due to an overrun error.

Bit 5: ORER	Description
0	Receiving is in progress or has ended normally*[1] (Initial value) ORER is cleared to 0 when: • The chip is reset or enters standby mode • Software reads ORER after it has been set to 1, then writes 0 in ORER
1	A receive overrun error occurred*[2] ORER is set to 1 if reception of the next serial data ends when RDRF is set to 1

Notes: 1. Clearing the RE bit to 0 in the serial control register does not affect the ORER bit, which retains its previous value.
2. RDR continues to hold the data received before the overrun error, so subsequent receive data is lost. Serial receiving cannot continue while ORER is set to 1. In synchronous mode, serial transmitting is disabled.

Bit 4—Framing Error (FER): FER indicates that data reception ended abnormally due to a framing error in the asynchronous mode.

Bit 4: FER	Description
0	Receiving is in progress or has ended normally (Initial value) Clearing the RE bit to 0 in the serial control register does not affect the FER bit, which retains its previous value. FER is cleared to 0 when: • The chip is reset or enters standby mode • Software reads FER after it has been set to 1, then writes 0 in FER
1	A receive framing error occurred. When the stop bit length is two bits, only the first bit is checked. The second stop bit is not checked. When a framing error occurs, the SCI transfers the receive data into RDR but does not set RDRF. Serial receiving cannot continue while FER is set to 1. In synchronous mode, serial transmitting is also disabled. FER is set to 1 if the stop bit at the end of receive data is checked and found to be 0.

Bit 3—Parity Error (PER): PER indicates that data reception (with parity) ended abnormally due to a parity error in asynchronous mode.

Bit 3: PER	Description
0	Receiving is in progress or has ended normally (Initial value) Clearing the RE bit to 0 in the serial control register does not affect the PER bit, which retains its previous value. PER is cleared to 0 when: • The chip is reset or enters standby mode • Software reads PER after it has been set to 1, then writes 0 in PER
1	A receive parity error occurred. When a parity error occurs, the SCI transfers the receive data into RDR but does not set RDRF. Serial receiving cannot continue while PER is set to 1. In synchronous mode, serial transmitting is also disabled. PER is set to 1 if the number of 1s in receive data, including the parity bit, does not match the even or odd parity setting of the parity mode bit (O/$\overline{E}$) in the serial mode register (SMR).

Bit 2—Transmit End (TEND): TEND indicates that when the last bit of a serial character was transmitted, TDR did not contain new transmit data, so transmission has ended. TEND is a read-only bit and cannot be written.

Bit 2: TEND	Description
0	Transmission is in progress TEND is cleared to 0 when: • Software reads TDRE after it has been set to 1, then writes 0 in TDRE • The DMAC writes data in TDR
1	End of transmission (Initial value) TEND is set to 1 when: • The chip is reset or enters standby mode • TE is cleared to 0 in the serial control register (SCR) • TDRE is 1 when the last bit of a one-byte serial character is transmitted

Bit 1—Multiprocessor Bit (MPB): MPB stores the value of the multiprocessor bit in receive data when a multiprocessor format is selected for receiving in asynchronous mode. The MPB is a read-only bit and cannot be written.

Bit 1: MPB	Description
0	Multiprocessor bit value in receive data is 0 (Initial value) If RE is cleared to 0 when a multiprocessor format is selected, MPB retains its previous value.
1	Multiprocessor bit value in receive data is 1

Bit 0—Multiprocessor Bit Transfer (MPBT): MPBT stores the value of the multiprocessor bit added to transmit data when a multiprocessor format is selected for transmitting in asynchronous mode. The MPBT setting is ignored in synchronous mode, when a multiprocessor format is not selected, or when the SCI is not transmitting.

Bit 0: MPBT	Description
0	Multiprocessor bit value in transmit data is 0 (Initial value)
1	Multiprocessor bit value in transmit data is 1

13.2.8 Bit Rate Register (BRR)

The bit rate register (BRR) is an eight-bit register that, together with the baud rate generator clock source selected by the CKS1 and CKS0 bits in the serial mode register (SMR), determines the serial transmit/receive bit rate.

The CPU can always read and write to BRR. BRR is initialized to H'FF by a reset and in standby mode. SCI0 and SCI1 have independent baud rate generator control, so different values can be set in the two channels.

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 13.3 shows examples of BRR settings in asynchronous mode; table 13.4 shows examples of BBR settings in synchronous mode.

Table 13.3 Bit Rates and BRR Settings in Asynchronous Mode

	φ (MHz)					
	2			2.097152		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)
110	1	141	0.03	1	148	–0.04
150	1	103	0.16	1	108	0.21
300	0	207	0.16	0	217	0.21
600	0	103	0.16	0	108	0.21
1200	0	51	0.16	0	54	–0.70
2400	0	25	0.16	0	26	1.14
4800	0	12	0.16	0	13	–2.48
9600	—	—	—	0	6	–2.48
19200	—	—	—	—	—	—
31250	0	1	0.00	—	—	—
38400	—	—	—	—	—	—

	φ (MHz)								
	2.4576			3			3.6864		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	174	–0.26	1	212	0.03	2	64	0.70
150	1	127	0.00	1	155	0.16	1	191	0.00
300	0	255	0.00	1	77	0.16	1	95	0.00
600	0	127	0.00	0	155	0.16	0	191	0.00
1200	0	63	0.00	0	77	0.16	0	95	0.00
2400	0	31	0.00	0	38	0.16	0	47	0.00
4800	0	15	0.00	0	19	–2.34	0	23	0.00
9600	0	7	0.00	0	9	–2.34	0	11	0.00
19200	0	3	0.00	0	4	–2.34	0	5	0.00
31250	—	—	—	0	2	0.00	—	—	—
38400	0	1	0.00	—	—	—	0	2	0.00

	φ (MHz)								
	4			4.9152			5		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	70	0.03	2	86	0.31	2	88	–0.25
150	1	207	0.16	1	255	0.00	2	64	0.16
300	1	103	0.16	1	127	0.00	1	129	0.16
600	0	207	0.16	0	255	0.00	1	64	0.16
1200	0	103	0.16	0	127	0.00	0	129	0.16
2400	0	51	0.16	0	63	0.00	0	64	0.16
4800	0	25	0.16	0	31	0.00	0	32	–1.36
9600	0	12	0.16	0	15	0.00	0	15	1.73
19200	—	—	—	0	7	0.00	0	7	1.73
31250	0	3	0.00	0	4	–1.70	0	4	0.00
38400	—	—	—	0	3	0.00	0	3	1.73

	φ (MHz)								
	6			6.144			7.3728		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	106	–0.44	2	108	0.08	2	130	–0.07
150	2	77	0.16	2	79	0.00	2	95	0.00
300	1	155	0.16	1	159	0.00	1	191	0.00
600	1	77	0.16	1	79	0.00	1	95	0.00
1200	0	155	0.16	0	159	0.00	0	191	0.00
2400	0	77	0.16	0	79	0.00	0	95	0.00
4800	0	38	0.16	0	39	0.00	0	47	0.00
9600	0	19	–2.34	0	19	0.00	0	23	0.00
19200	0	9	–2.34	0	9	0.00	0	11	0.00
31250	0	5	0.00	0	5	2.40	—	—	—
38400	0	4	–2.34	0	4	0.00	0	5	0.00

	φ (MHz)											
	8			9.8304			10			12		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	–2.34
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	–2.34

	φ (MHz)											
	12.288			14			14.7456			16		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	217	0.08	2	248	–0.17	3	64	0.70	3	70	0.03
150	2	159	0.00	2	181	0.16	2	191	0.00	2	207	0.16
300	2	79	0.00	2	90	0.16	2	95	0.00	2	103	0.16
600	1	159	0.00	1	181	0.16	1	191	0.00	1	207	0.16
1200	1	79	0.00	1	90	0.16	1	95	0.00	1	103	0.16
2400	0	159	0.00	0	181	0.16	0	191	0.00	0	207	0.16
4800	0	79	0.00	0	90	0.16	0	95	0.00	0	103	0.16
9600	0	39	0.00	0	45	–0.93	0	47	0.00	0	51	0.16
19200	0	19	0.00	0	22	–0.93	0	23	0.00	0	25	0.16
31250	0	11	2.40	0	13	0.00	0	14	–1.70	0	15	0.00
38400	0	9	0.00	—	—	—	0	11	0.00	0	12	0.16

	φ (MHz)											
	17.2032			18			19.6608			20		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	75	0.48	3	79	–0.12	3	86	0.31	3	88	–0.25
150	2	223	0.00	2	233	0.16	2	255	0.00	3	64	0.16
300	2	111	0.00	2	116	0.16	2	127	0.00	2	129	0.16
600	1	223	0.00	1	233	0.16	1	255	0.00	2	64	0.16
1200	1	111	0.00	1	116	0.16	1	127	0.00	1	129	0.16
2400	0	223	0.00	0	233	0.16	0	255	0.00	1	64	0.16
4800	0	111	0.00	0	116	0.16	0	127	0.00	0	129	0.16
9600	0	55	0.00	0	58	–0.69	0	63	0.00	0	64	0.16
19200	0	27	0.00	0	28	1.02	0	31	0.00	0	32	–1.36
31250	0	16	1.20	0	17	0.00	0	19	–1.70	0	19	0.00
38400	0	13	0.00	0	14	–2.34	0	15	0.00	0	15	1.73

Note: Settings with an error of 1% or less are recommended.

Table 13.4 Bit Rates and BRR Settings in Synchronous Mode

Bit Rate (bits/s)	φ (MHz)											
	2		4		8		10		16		20	
	n	N	n	N	n	N	n	N	n	N	n	N
110	3	70	—	—	—	—	—	—	—	—	—	—
250	2	124	2	249	3	124	—	—	3	249	—	—
500	1	249	2	124	2	249	—	—	3	124	—	—
1k	1	124	1	249	2	124	—	—	2	249	—	—
2.5k	0	199	1	99	1	199	1	249	2	99	2	124
5k	0	99	0	199	1	99	1	124	1	199	1	249
10k	0	49	0	99	0	199	0	249	1	99	1	124
25k	0	19	0	39	0	79	0	99	0	159	0	199
50k	0	9	0	19	0	39	0	49	0	79	0	99
100k	0	4	0	9	0	19	0	24	0	39	0	49
250k	0	1	0	3	0	7	0	9	0	15	0	19
500k	0	0*	0	1	0	3	0	4	0	7	0	9
1M			0	0*	0	1	—	—	0	3	0	4
2.5M					—	—	0	0*	—	—	0	1
5M									—	—	0	0*

Blank: No setting available

—: Setting possible, but error occurs

*: Continuous transmission/reception not possible

The BRR setting is calculated as follows:

Asynchronous mode

$$N = [\phi/(64 \times 2^{2n-1} \times B)] \times 10^6 - 1$$

Synchronous mode

$$N = [\phi/(8 \times 2^{2n-1} \times B)] \times 10^6 - 1$$

B: Bit rate (bits/s)

N: BRR setting for baud rate generator ($0 \leq N \leq 255$)

φ: φ frequency (MHz)

n: Baud rate generator clock source (n = 0, 1, 2, 3)

For the clock sources and values of n, see following table.

		SMR Settings	
n	**Clock Source**	**CKS1**	**CKS0**
0	ϕ	0	0
1	$\phi/4$	0	1
2	$\phi/16$	1	0
3	$\phi/64$	1	1

The bit rate error for asynchronous mode is given by the following formula:

$$\text{Error (\%)} = \{(\phi \times 10^6)/[(N + 1) \times B \times 64 \times 2^{2n-1}] - 1\} \times 100$$

Table 13.5 indicates the maximum bit rates in asynchronous mode when the baud rate generator is used. Tables 13.6 and 13.7 show the maximum rates for external clock input.

Table 13.5 Maximum Bit Rates for Various Frequencies with Baud Rate Generator (Asynchronous Mode)

		Settings	
ϕ (MHz)	**Maximum Bit Rate (bits/s)**	**n**	**N**
2	62500	0	0
2.097152	65536	0	0
2.4576	76800	0	0
3	93750	0	0
3.6864	115200	0	0
4	125000	0	0
4.9152	153600	0	0
5	156250	0	0
6	187500	0	0
6.144	192000	0	0
7.3728	230400	0	0
8	250000	0	0
9.8304	307200	0	0
10	312500	0	0
12	375000	0	0
12.288	384000	0	0
14	437500	0	0
14.7456	460800	0	0
16	500000	0	0
17.2032	537600	0	0
18	562500	0	0
19.6608	614400	0	0
20	625000	0	0

Table 13.6 Maximum Bit Rates with External Clock Input (Asynchronous Mode)

ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bits/s)
2	0.5000	31250
2.097152	0.5243	32768
2.4576	0.6144	38400
3	0.7500	46875
3.6864	0.9216	57600
4	1.0000	62500
4.9152	1.2288	76800
5	1.2500	78125
6	1.5000	93750
6.144	1.5360	96000
7.3728	1.8432	115200
8	2.0000	125000
9.8304	2.4576	153600
10	2.5000	156250
12	3.0000	187500
12.288	3.0720	192000
14	3.5000	218750
14.7456	3.6834	230400
16	4.0000	250000
17.2032	4.3008	268800
18	4.5000	281250
19.6608	4.9152	307200
20	5.0000	312500

Table 13.7 Maximum Bit Rates with External Clock Input (Synchronous Mode)

ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bits/s)
2	0.3333	333333.3
4	0.6667	666666.7
6	1.0000	1000000.0
8	1.3333	1333333.3
10	1.6667	1666666.7
12	2.0000	2000000.0
14	2.3333	2333333.3
16	2.6667	2666666.7
18	3.0000	3000000.0
20	3.3333	3333333.3

13.3 Operation

13.3.1 Overview

The SCI has an asynchronous mode in which characters are synchronized individually, and a synchronous mode in which communication is synchronized with clock pulses. Serial communication is possible in either mode. Asynchronous/synchronous mode and the communication format are selected in the serial mode register (SMR), as shown in table 13.8. The SCI clock source is selected by the C/$\overline{A}$ bit in the serial mode register (SMR) and the CKE1 and CKE0 bits in the serial control register (SCR), as shown in table 13.9.

Asynchronous Mode:

- Data length is selectable: seven or eight bits.
- Parity and multiprocessor bits are selectable, and so is the stop bit length (one or two bits). The preceding selections constitute the communication format and character length.
- In receiving, it is possible to detect framing errors (FER), parity errors (PER), overrun errors (ORER), and the break state.
- An internal or external clock can be selected as the SCI clock source.
  - When an internal clock is selected, the SCI operates using the on-chip baud rate generator, and can output a serial clock signal with a frequency matching the bit rate.
  - When an external clock is selected, the external clock input must have a frequency 16 times the bit rate. (The on-chip baud rate generator is not used.)

Synchronous Mode:

- The communication format has a fixed eight-bit data length.
- In receiving, it is possible to detect overrun errors (ORER).
- An internal or external clock can be selected as the SCI clock source.
  - When an internal clock is selected, the SCI operates using the on-chip baud rate generator, and outputs a serial clock signal to external devices.
  - When an external clock is selected, the SCI operates on the input serial clock. The on-chip baud rate generator is not used.

Table 13.8 Serial Mode Register Settings and SCI Communication Formats

	SMR Settings					SCI Communication Format			
Mode	Bit 7: C/A	Bit 6: CHR	Bit 5: PE	Bit 2: MP	Bit 3: STOP	Data Length	Parity Bit	Multipro-cessor Bit	Stop Bit Length
Asynchronous	0	0	0	0	0	8-bit	Absent	Absent	1 bit
					1				2 bits
			1		0		Present		1 bit
					1				2 bits
		1	0		0	7-bit	Absent		1 bit
					1				2 bits
			1		0		Present		1 bit
					1				2 bits
Asynchronous (multiprocesso r format)		0	*	1	0	8-bit	Absent	Present	1 bit
			*		1				2 bits
		1	*		0	7-bit			1 bit
			*		1				2 bits
Synchronous	1	*	*	*	*	8-bit		Absent	None

Note: Asterisks (*) in the table indicate don't-care bits.

Table 13.9 SMR and SCR Settings and SCI Clock Source Selection

	SMR	SCR Settings		SCI Transmit/Receive Clock	
Mode	Bit 7: C/$\overline{A}$	Bit 1: CKE1	Bit 0: CKE0	Clock Source	SCK Pin Function*
Asynchronous mode	0	0	0	Internal	SCI does not use the SCK pin
			1		Outputs a clock with frequency matching the bit rate
		1	0	External	Inputs a clock with frequency 16 times the bit rate
			1		
Synchronous mode	1	0	0	Internal	Outputs the serial clock
			1		
		1	0	External	Inputs the serial clock
			1		

Note: * Select the function in combination with the pin function controller (PFC).

13.3.2 Operation in Asynchronous Mode

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized one character at a time.

The transmitting and receiving sections of the SCI are independent, so full duplex communication is possible. The transmitter and receiver are both double buffered, so data can be written and read while transmitting and receiving are in progress, enabling continuous transmitting and receiving.

Figure 13.2 shows the general format of asynchronous serial communication. In asynchronous serial communication, the communication line is normally held in the mark (high) state. The SCI monitors the line and starts serial communication when the line goes to the space (low) state, indicating a start bit. One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in that order.

When receiving in asynchronous mode, the SCI synchronizes on the falling edge of the start bit. The SCI samples each data bit on the eighth pulse of a clock with a frequency 16 times the bit rate. Receive data is latched at the center of each bit.

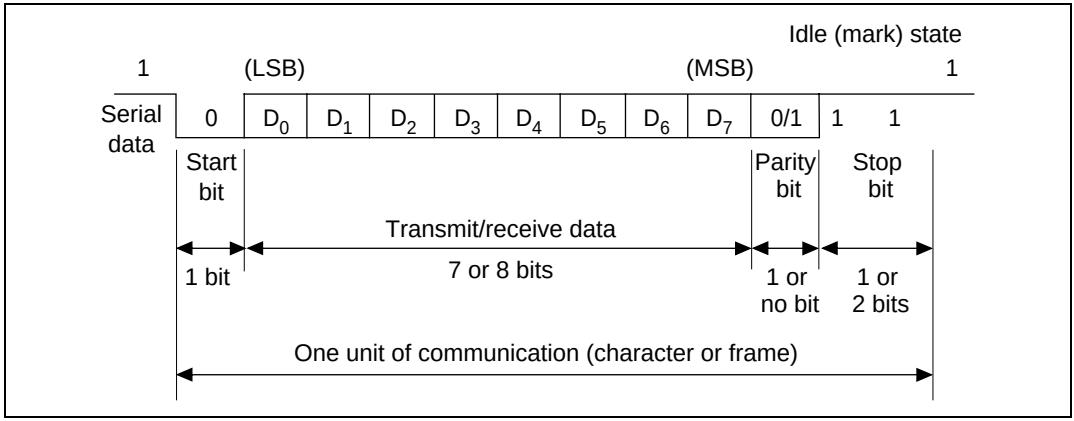


Figure 13.2 Data Format in Asynchronous Communication (Example: 8-Bit Data with Parity and Two Stop Bits)

Transmit/Receive Formats: Table 13.10 shows the 12 communication formats that can be selected in asynchronous mode. The format is selected by settings in the serial mode register (SMR).

Table 13.10 Serial Communication Formats (Asynchronous Mode)

SMR Bits													
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	START	8-bit data								STOP		
0	0	0	1	START	8-bit data								STOP	STOP	
0	1	0	0	START	8-bit data								P	STOP	
0	1	0	1	START	8-bit data								P	STOP	STOP
1	0	0	0	START	7-bit data							STOP			
1	0	0	1	START	7-bit data							STOP	STOP		
1	1	0	0	START	7-bit data							P	STOP		
1	1	0	1	START	7-bit data							P	STOP	STOP	
0	—	1	0	START	8-bit data								MPB	STOP	
0	—	1	1	START	8-bit data								MPB	STOP	STOP
1	—	1	0	START	7-bit data							MPB	STOP		
1	—	1	1	START	7-bit data							MPB	STOP	STOP	

—: Don't care bits.

Notes: START: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit

Clock: An internal clock generated by the on-chip baud rate generator or an external clock input from the SCK pin can be selected as the SCI transmit/receive clock. The clock source is selected by the C/$\overline{A}$ bit in the serial mode register (SMR) and bits CKE1 and CKE0 in the serial control register (SCR) (table 13.9).

When an external clock is input at the SCK pin, it must have a frequency equal to 16 times the desired bit rate.

When the SCI operates on an internal clock, it can output a clock signal at the SCK pin. The frequency of this output clock is equal to the bit rate. The phase is aligned as in figure 13.3 so that the rising edge of the clock occurs at the center of each transmit data bit.

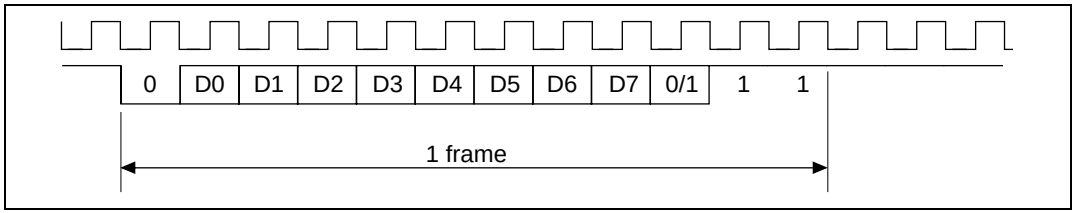


Figure 13.3 Phase Relationship Between Output Clock and Serial Data (Asynchronous Mode)

Transmitting and Receiving Data (SCI initialization (Asynchronous Mode)): Before transmitting or receiving, software must clear the TE and RE bits to 0 in the serial control register (SCR), then initialize the SCI as follows.

When changing the communication mode or format, always clear the TE and RE bits to 0 before following the procedure given below. Clearing TE to 0 sets TDRE to 1 and initializes the transmit shift register (TSR). Clearing RE to 0, however, does not initialize the RDRF, PER, FER, and ORER flags and receive data register (RDR), which retain their previous contents.

When an external clock is used, the clock should not be stopped during initialization or subsequent operation. SCI operation becomes unreliable if the clock is stopped.

Figure 13.4 shows a sample flowchart for initializing the SCI. The procedure for initializing the SCI is as follows:

1. Select the communication format in the serial mode register (SMR).
2. Write the value corresponding to the bit rate in the bit rate register (BRR) unless an external clock is used.
3. Select the clock source in the serial control register (SCR). Leave RIE, TIE, TEIE, MPIE, TE, and RE cleared to 0. If clock output is selected in asynchronous mode, clock output starts immediately after the setting is made in SCR.
4. Wait for at least the interval required to transmit or receive one bit, then set TE or RE in the serial control register (SCR) to 1. Also set RIE, TIE, TEIE, and MPIE as necessary. Setting TE or RE enables the SCI to use the TxD or RxD pin. The initial states are the mark transmit state, and the idle receive state (waiting for a start bit).

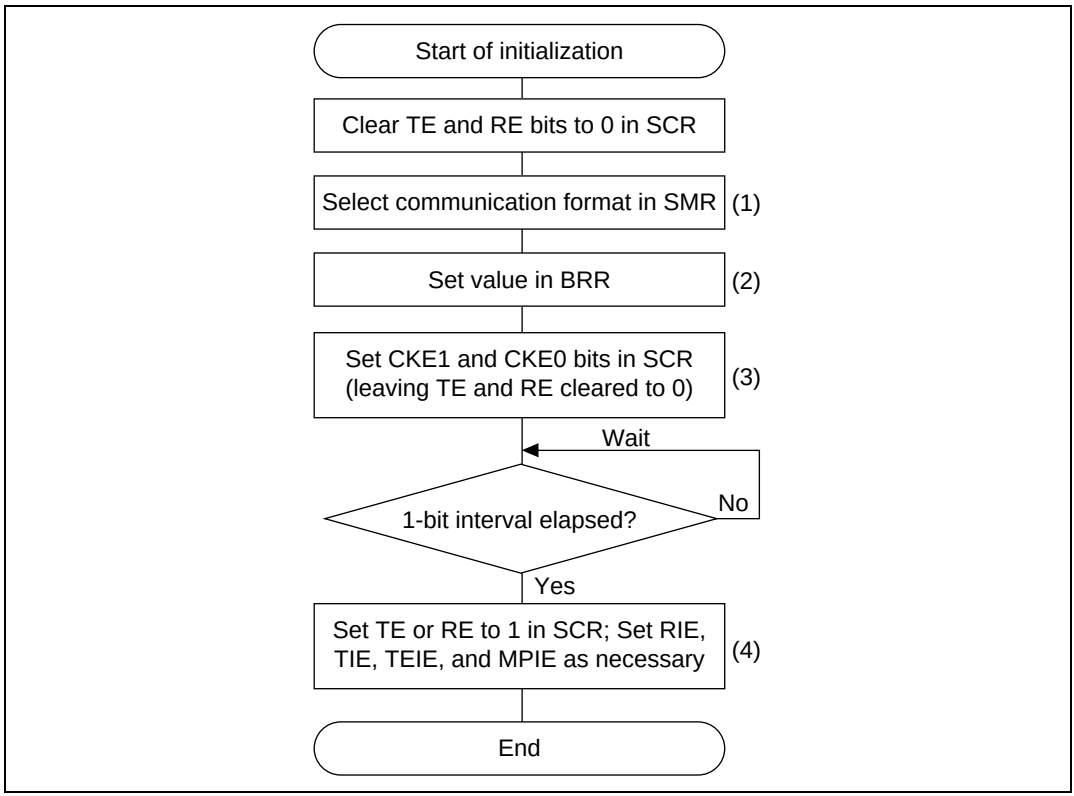


Figure 13.4 Sample Flowchart for SCI Initialization

Transmitting Serial Data (Asynchronous Mode): Figure 13.5 shows a sample flowchart for transmitting serial data. The procedure for transmitting serial data is as follows:

1. SCI initialization: select the TxD pin function with the PFC.
2. SCI status check and transmit data write: read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR) and clear TDRE to 0.
3. To continue transmitting serial data: read the TDRE bit to check whether it is safe to write (1); if so, write data in TDR, then clear TDRE to 0. When the DMAC is started by a transmit-data-empty interrupt request (TXI) to write data in TDR, the TDRE bit is checked and cleared automatically.
4. To output a break signal at the end of serial transmission: set the DR bit to 0, then clear TE to 0 in SCR and set the TxD pin function as output port with the PFC.

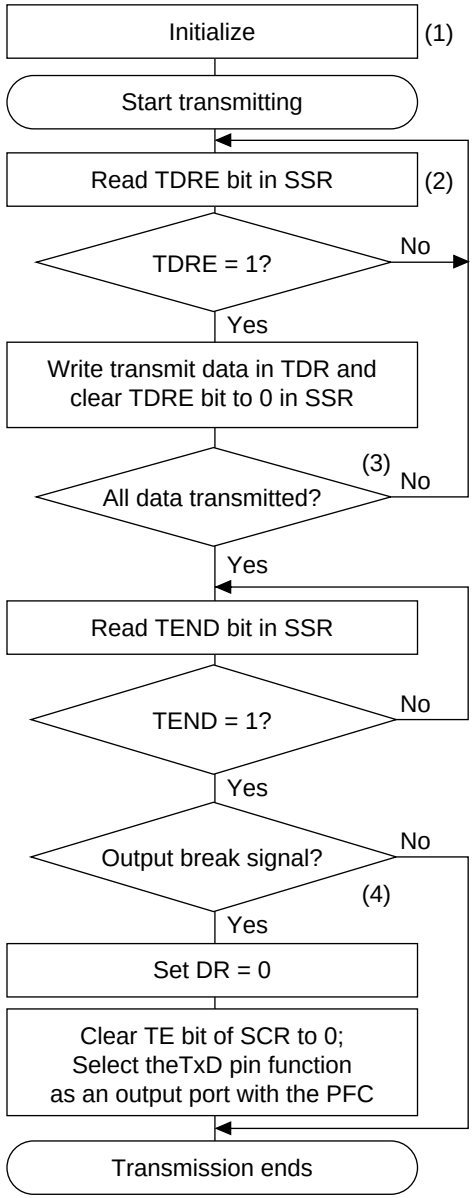


Figure 13.5 Sample Flowchart for Transmitting Serial Data

In transmitting serial data, the SCI operates as follows:

1. The SCI monitors the TDRE bit in SSR. When TDRE is cleared to 0, the SCI recognizes that the transmit data register (TDR) contains new data, and loads this data from TDR into the transmit shift register (TSR).
2. After loading the data from TDR into TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the transmit-data-empty interrupt enable bit (TIE) is set to 1 in SCR, the SCI requests a transmit-data-empty interrupt (TXI) at this time.

Serial transmit data is transmitted in the following order from the TxD pin:

   a. Start bit: one 0 bit is output.
   b. Transmit data: seven or eight bits of data are output, LSB first.
   c. Parity bit or multiprocessor bit: one parity bit (even or odd parity) or one multiprocessor bit is output. Formats in which neither a parity bit nor a multiprocessor bit is output can also be selected.
   d. Stop bit: one or two 1-bits (stop bits) are output.
   e. Mark state: output of 1-bits continues until the start bit of the next transmit data.

3. The SCI checks the TDRE bit when it outputs the stop bit. If TDRE is 0, the SCI loads new data from TDR into TSR, outputs the stop bit, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit to 1 in SSR, outputs the stop bit, then continues output of 1-bits in the mark state. If the transmit-end interrupt enable bit (TEIE) in SCR is set to 1, a transmit-end interrupt (TEI) is requested.

Figure 13.6 shows an example of SCI transmit operation in asynchronous mode.

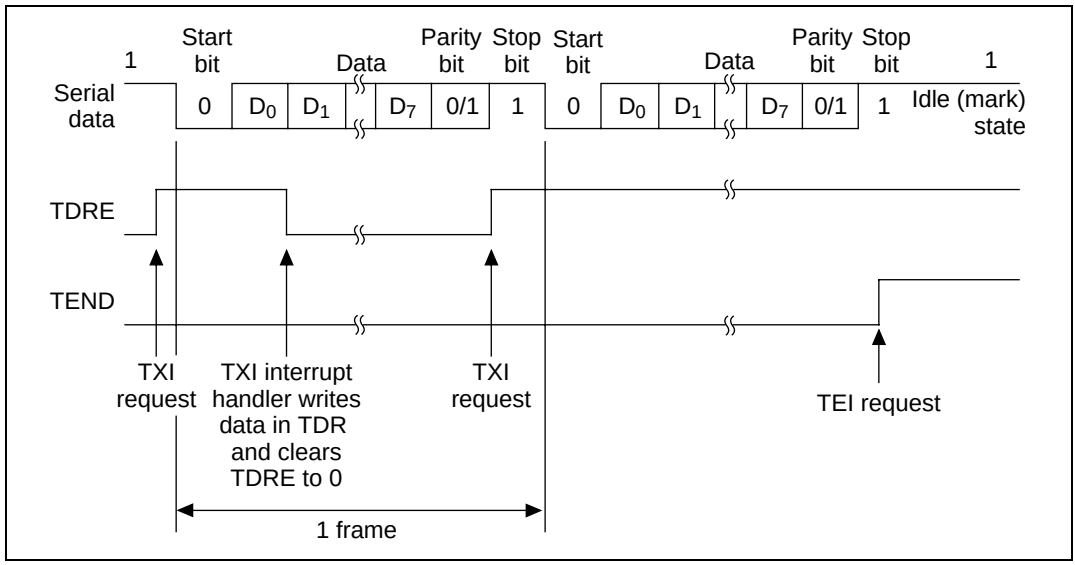


Figure 13.6 Example of SCI Transmit Operation in Asynchronous Mode (8-Bit Data with Parity and One Stop Bit)

Receiving Serial Data (Asynchronous Mode): Figure 13.7 shows a sample flowchart for receiving serial data. The procedure for receiving serial data is listed below.

1. SCI initialization: select the RxD pin function with the PFC.
2. Receive error handling and break detection: if a receive error occurs, read the ORER, PER and FER bits in SSR to identify the error. After executing the necessary error handling, clear ORER, PER, and FER all to 0. Receiving cannot resume if ORER, PER, or FER remains set to 1. When a framing error occurs, the RxD pin can be read to detect the break state.
3. SCI status check and receive data read: read the serial status register (SR), check that RDRF is set to 1, then read receive data from the receive data register (RDR) and clear RDRF to 0. The RXI interrupt can also be used to determine if the RDRF bit has changed from 0 to 1.
4. To continue receiving serial data: read RDRF and RDR, and clear RDRF to 0 before the stop bit of the current frame is received. If the DMAC is started by a receive-data-full interrupt (RXI) to read RDR, the RDRF bit is cleared automatically, so this step is unnecessary.

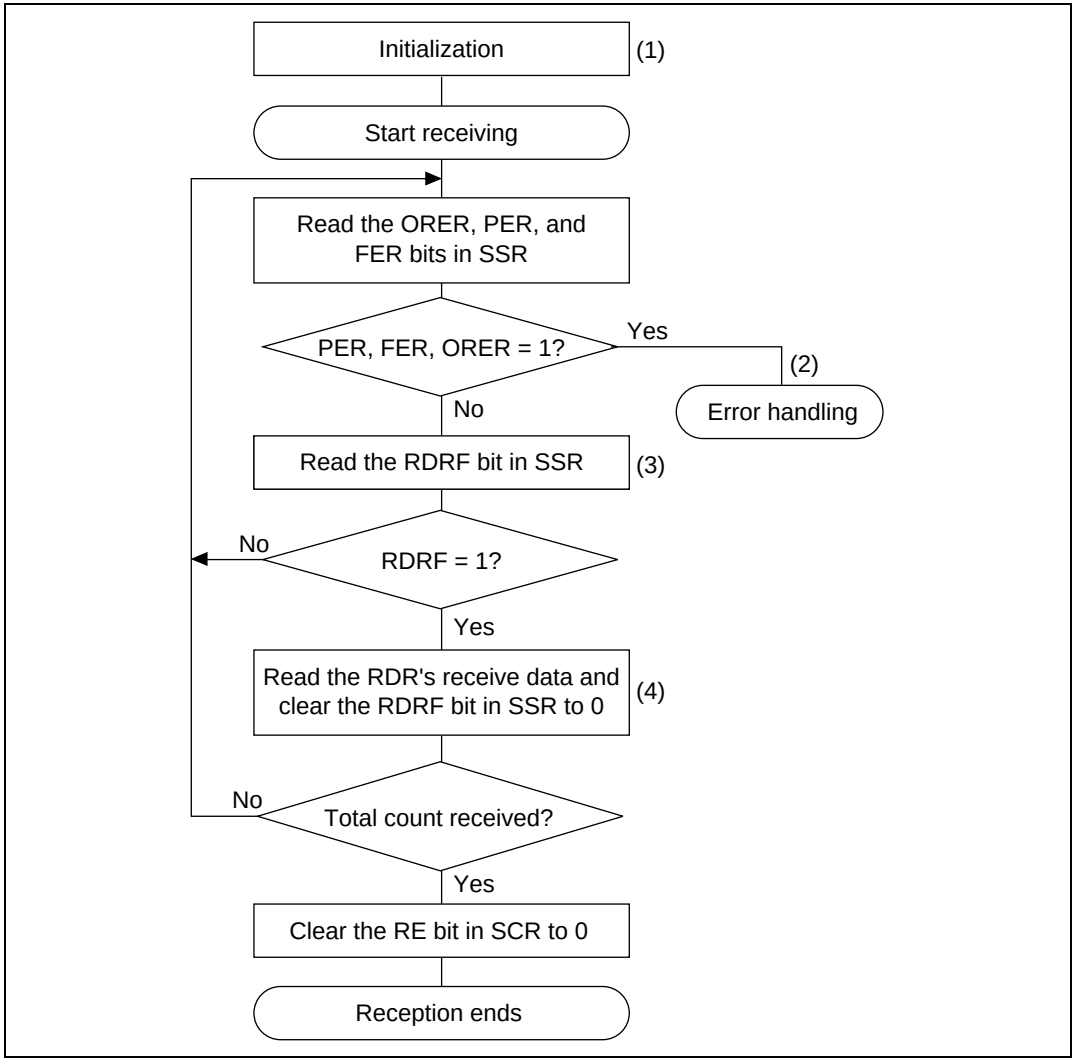


Figure 13.7 Sample Flowchart for Receiving Serial Data

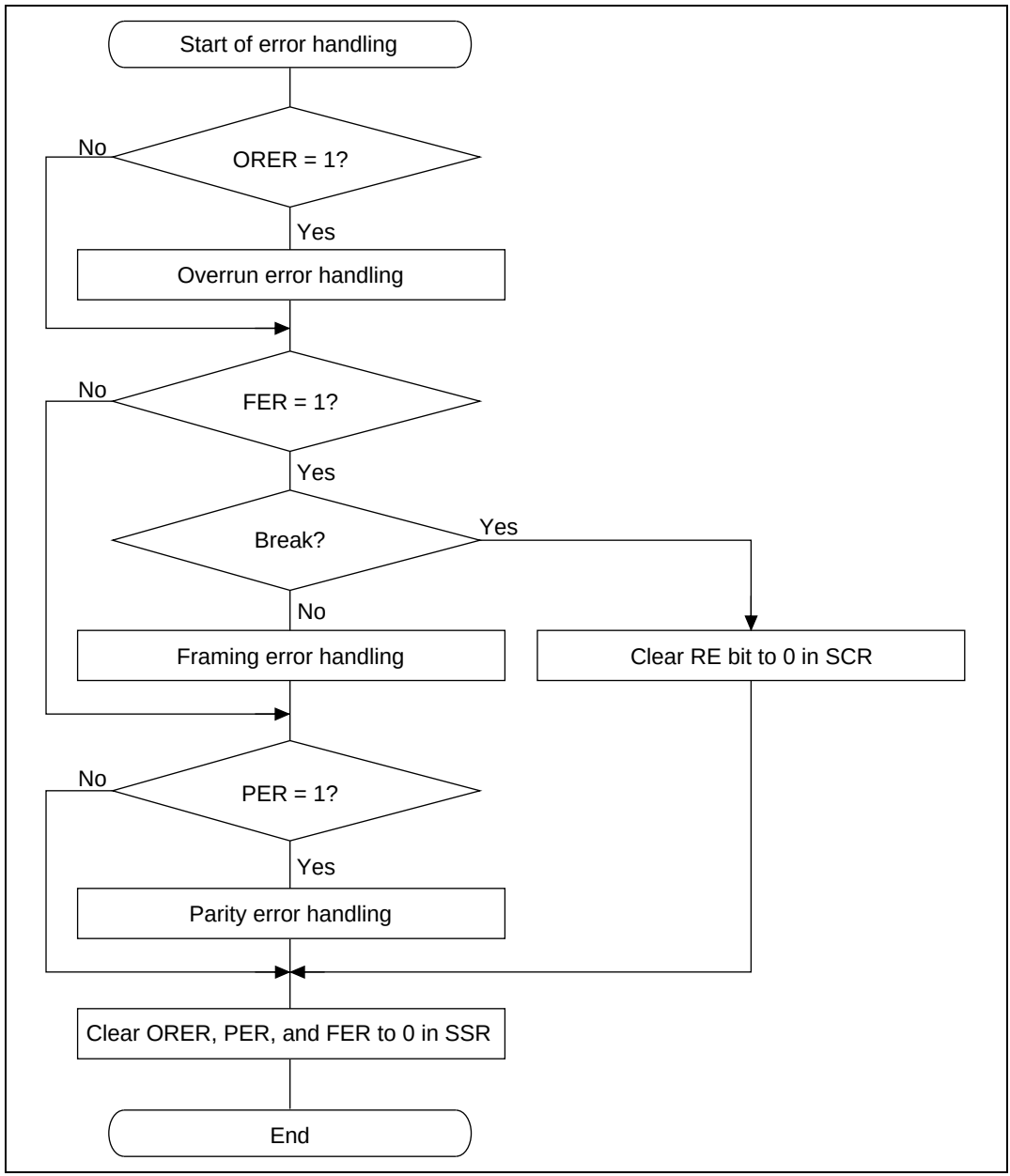


Figure 13.7 Sample Flowchart for Receiving Serial Data (cont)

In receiving, the SCI operates as follows:

1. The SCI monitors the receive data line. When it detects a start bit (0), the SCI synchronizes internally and starts receiving.
2. Receive data is shifted into RSR in order from the LSB to the MSB.
3. The parity bit and stop bit are received. After receiving these bits, the SCI makes the following checks:
   a. Parity check: The number of 1s in the receive data must match the even or odd parity setting of the O/$\overline{E}$ bit in SMR.
   b. Stop bit check: The stop bit value must be 1. If there are two stop bits, only the first stop bit is checked.
   c. Status check: RDRF must be 0 so that receive data can be loaded from RSR into RDR.

   If these checks all pass, the SCI sets RDRF to 1 and stores the received data in RDR. If one of the checks fails (receive error), the SCI operates as indicated in table 13.11.

   Note: When a receive error flag is set, further receiving is disabled. The RDRF bit is not set to 1. Be sure to clear the error flags.
2. After setting RDRF to 1, if the receive-data-full interrupt enable bit (RIE) is set to 1 in SCR, the SCI requests a receive-data-full interrupt (RXI). If one of the error flags (ORER, PER, or FER) is set to 1 and the receive-data-full interrupt enable bit (RIE) in SCR is also set to 1, the SCI requests a receive-error interrupt (ERI).

Figure 13.8 shows an example of SCI receive operation in asynchronous mode.

Table 13.11 Receive Error Conditions and SCI Operation

Receive Error	Abbreviation	Condition	Data Transfer
Overrun error	ORER	Receiving of next data ends while RDRF is still set to 1 in SSR	Receive data not loaded from RSR into RDR
Framing error	FER	Stop bit is 0	Receive data loaded from RSR into RDR
Parity error	PER	Parity of receive data differs from even/odd parity setting in SMR	Receive data loaded from RSR into RDR

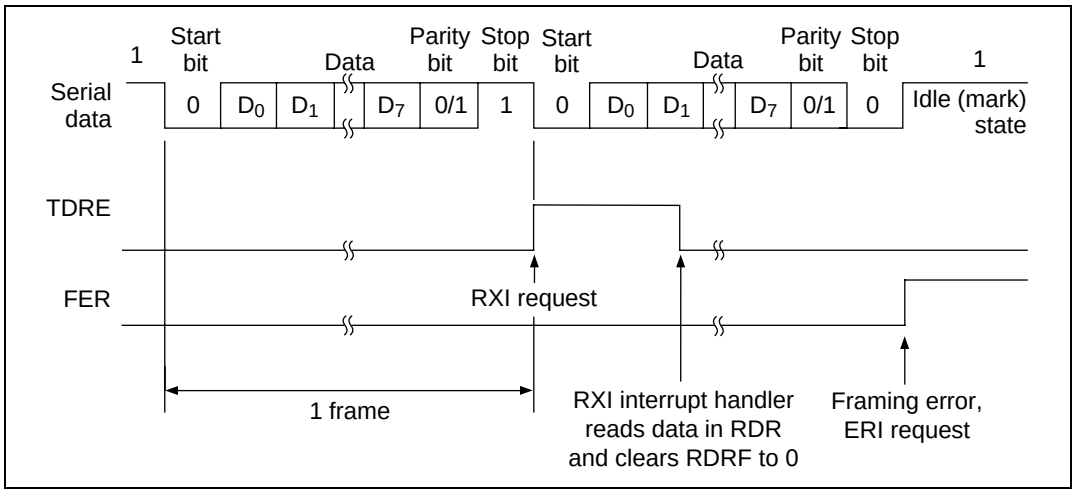


Figure 13.8 Example of SCI Receive Operation (8-Bit Data with Parity and One Stop Bit)

13.3.3 Multiprocessor Communication

The multiprocessor communication function enables several processors to share a single serial communication line. The processors communicate in asynchronous mode using a format with an additional multiprocessor bit (multiprocessor format).

In multiprocessor communication, each receiving processor is addressed by a unique ID. A serial communication cycle consists of an ID-sending cycle that identifies the receiving processor, and a data-sending cycle. The multiprocessor bit distinguishes ID-sending cycles from data-sending cycles. The transmitting processor starts by sending the ID of the receiving processor with which it wants to communicate as data with the multiprocessor bit set to 1. Next the transmitting processor sends transmit data with the multiprocessor bit cleared to 0.

Receiving processors skip incoming data until they receive data with the multiprocessor bit set to 1. When they receive data with the multiprocessor bit set to 1, receiving processors compare the data with their IDs. The receiving processor with a matching ID continues to receive further incoming data. Processors with IDs not matching the received data skip further incoming data until they again receive data with the multiprocessor bit set to 1. Multiple processors can send and receive data in this way.

Figure 13.9 shows an example of communication between processors using the multiprocessor format.

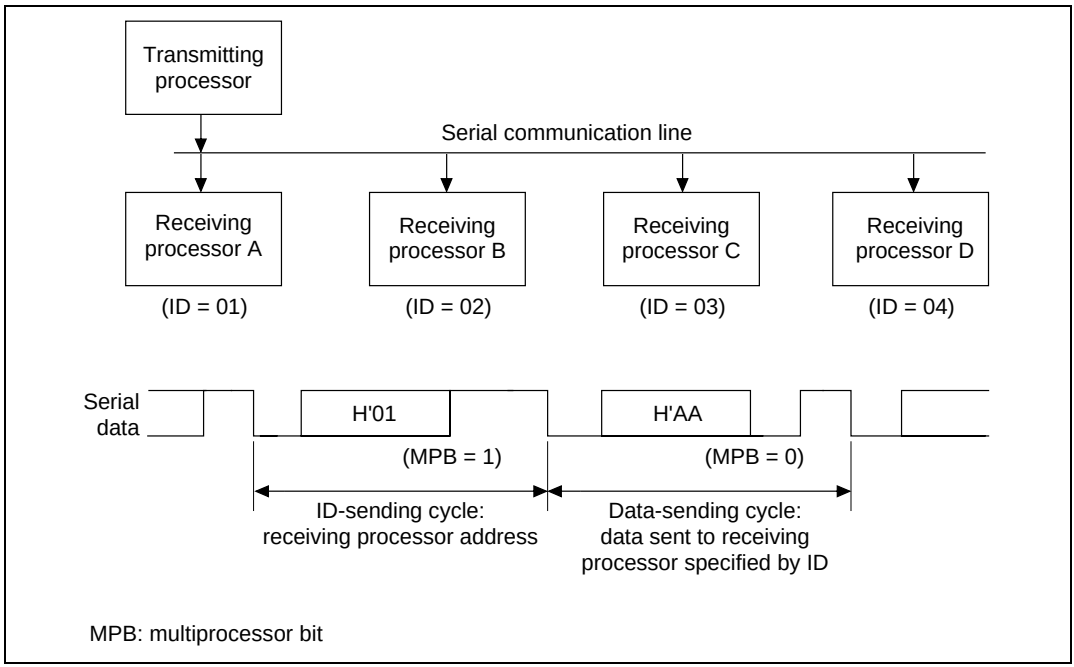


Figure 13.9 Example of Communication between Processors Using Multiprocessor Format (Sending Data H'AA to Receiving Processor A)

Communication Formats: Four formats are available. Parity-bit settings are ignored when a multiprocessor format is selected. For details see table 13.8.

Clock: See the description in the asynchronous mode section.

Transmitting Multiprocessor Serial Data: Figure 13.10 shows a sample flowchart for transmitting multiprocessor serial data. The procedure for transmitting multiprocessor serial data is listed below.

1. SCI initialization: select the TxD pin function with the PFC.
2. SCI status check and transmit data write: read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR). Also set MPBT (multiprocessor bit transfer) to 0 or 1 in SSR. Finally, clear TDRE to 0.
3. To continue transmitting serial data: read the TDRE bit to check whether it is safe to write (1); if so, write data in TDR, then clear TDRE to 0. When the DMAC is started by a transmit-data-empty interrupt request (TXI) to write data in TDR, the TDRE bit is checked and cleared automatically.
4. To output a break signal at the end of serial transmission: set the DR bit to 0 (I/O data port register), then clear TE to 0 in SCR and set the TxD pin function as output port with the PFC.

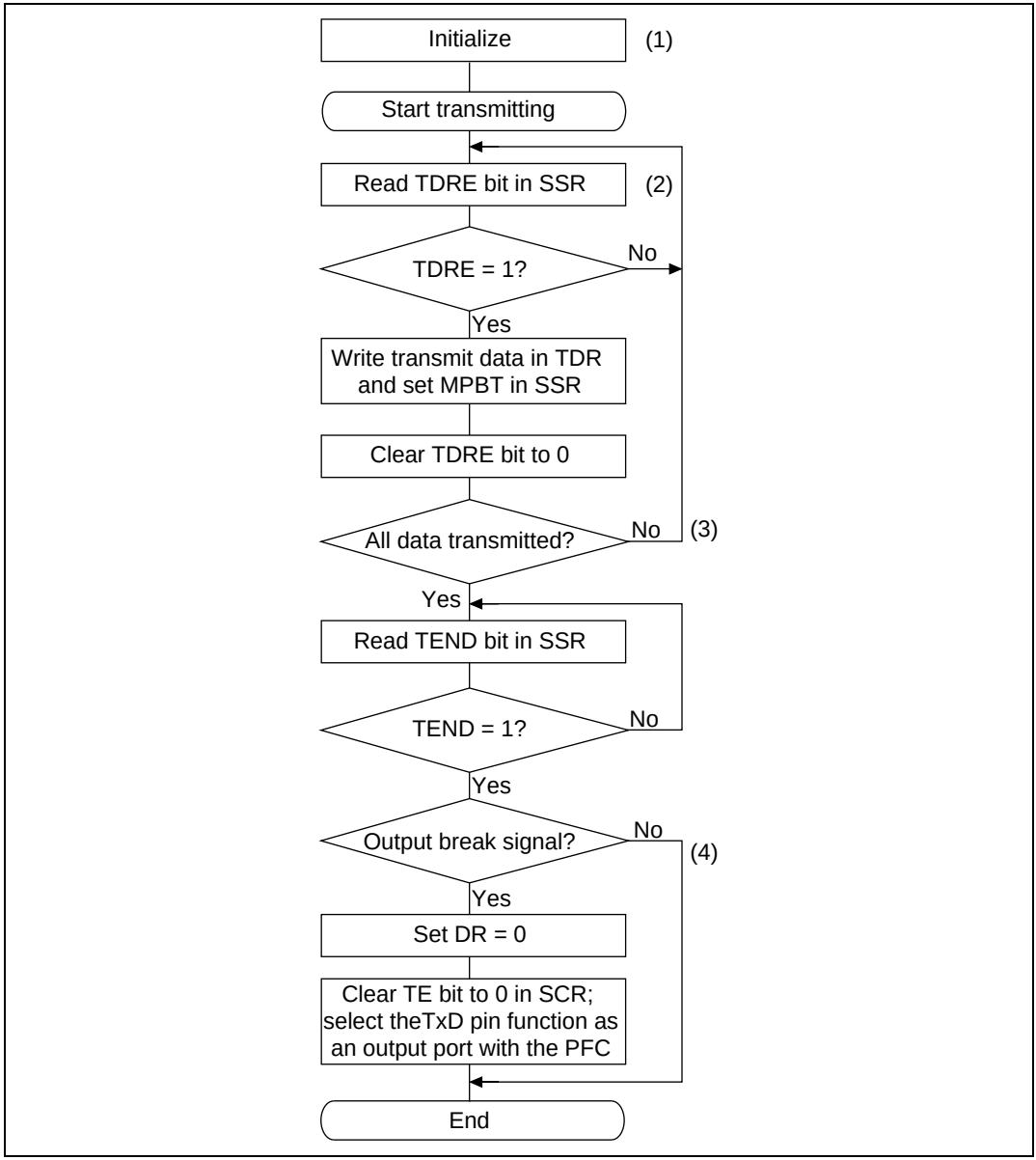


Figure 13.10 Sample Flowchart for Transmitting Multiprocessor Serial Data

In transmitting serial data, the SCI operates as follows:

1. The SCI monitors the TDRE bit in SSR. When TDRE is cleared to 0 the SCI recognizes that the transmit data register (TDR) contains new data, and loads this data from TDR into the transmit shift register (TSR).
2. After loading the data from TDR into TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the transmit-data-empty interrupt enable bit (TIE) in SCR is set to 1, the SCI requests a transmit-data-empty interrupt (TXI) at this time.

   Serial transmit data is transmitted in the following order from the TxD pin (figure 13.11):

   a. Start bit: one 0 bit is output.
   b. Transmit data: seven or eight bits are output, LSB first.
   c. Multiprocessor bit: one multiprocessor bit (MPBT value) is output.
   d. Stop bit: one or two 1-bits (stop bits) are output.
   e. Mark state: output of 1-bits continues until the start bit of the next transmit data.
3. The SCI checks the TDRE bit when it outputs the stop bit. If TDRE is 0, the SCI loads data from TDR into TSR, outputs the stop bit, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit in SSR to 1, outputs the stop bit, then continues output of 1-bits in the mark state. If the transmit-end interrupt enable bit (TEIE) in SCR is set to 1, a transmit-end interrupt (TEI) is requested at this time.

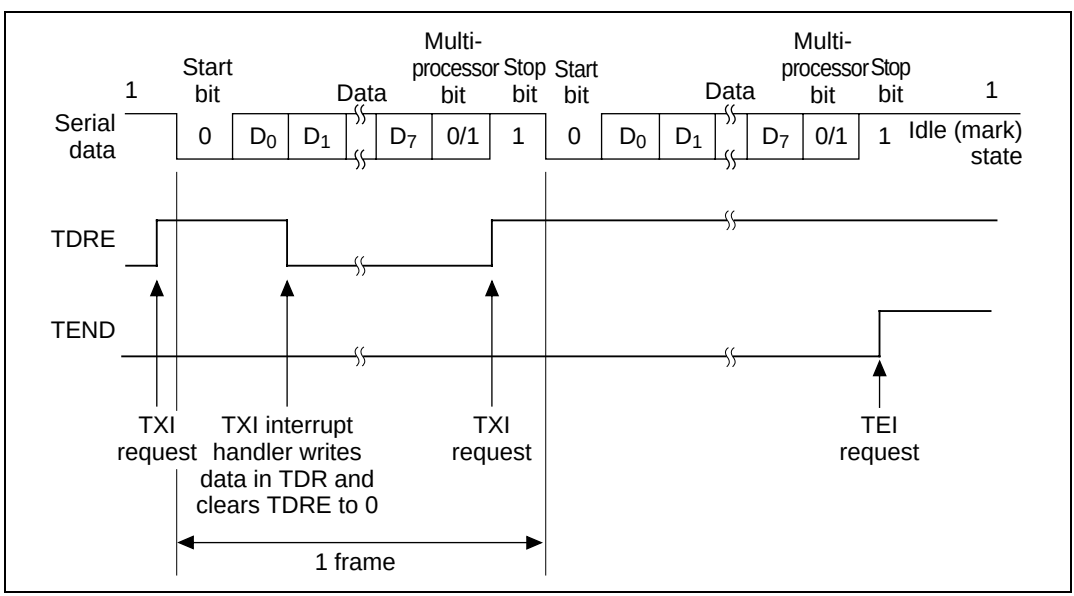


Figure 13.11 Example of SCI Multiprocessor Transmit Operation (8-Bit Data with Multiprocessor Bit and One Stop Bit)

Receiving Multiprocessor Serial Data: Figure 13.12 shows a sample flowchart for receiving multiprocessor serial data. The procedure for receiving multiprocessor serial data is listed below.

1. SCI initialization: select the RxD pin function with the PFC.
2. ID receive cycle: set the MPIE bit in the serial control register (SCR) to 1.
3. SCI status check and compare to ID reception: read the serial status register (SSR), check that RDRF is set to 1, then read data from the receive data register (RDR) and compare with the processor's own ID. If the ID does not match the receive data, set MPIE to 1 again and clear RDRF to 0. If the ID matches the receive data, clear RDRF to 0.
4. Receive error handling and break detection: if a receive error occurs, read the ORER and FER bits in SSR to identify the error. After executing the necessary error handling, clear both ORER and FER to 0. Receiving cannot resume if ORER or FER remain set to 1. When a framing error occurs, the RxD pin can be read to detect the break state.
5. SCI status check and data receiving: read SSR, check that RDRF is set to 1, then read data from the receive data register (RDR).

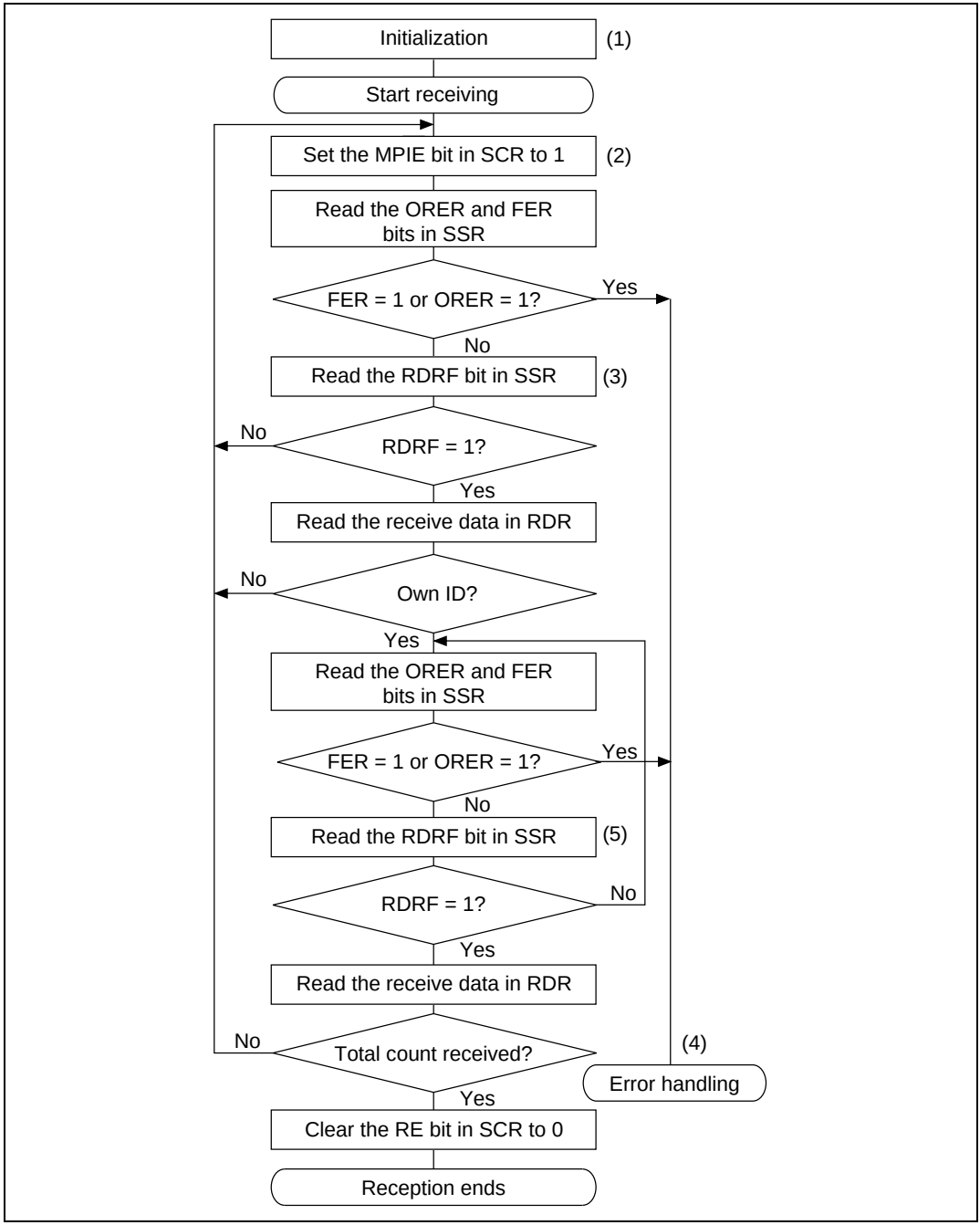


Figure 13.12 Sample Flowchart for Receiving Multiprocessor Serial Data

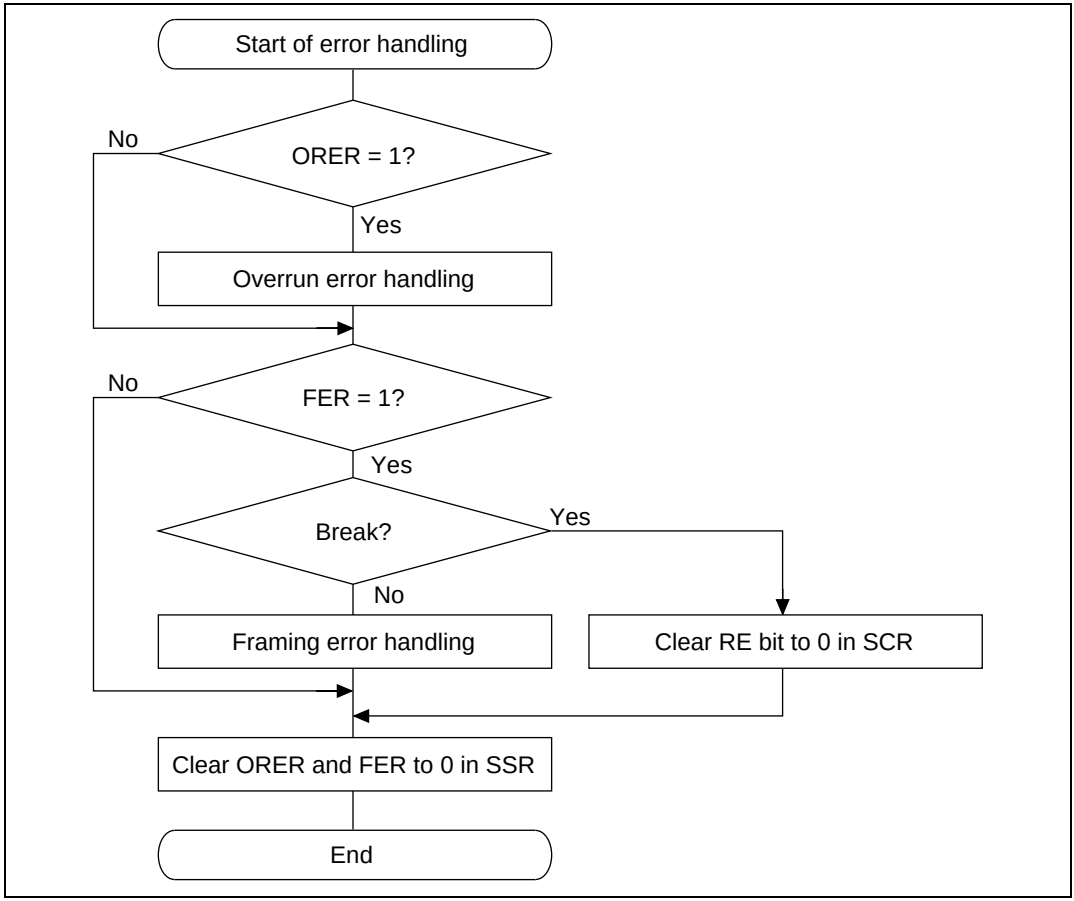


Figure 13.12 Sample Flowchart for Receiving Multiprocessor Serial Data (cont)

Figure 13.13 shows an example of SCI receive operation using a multiprocessor format.

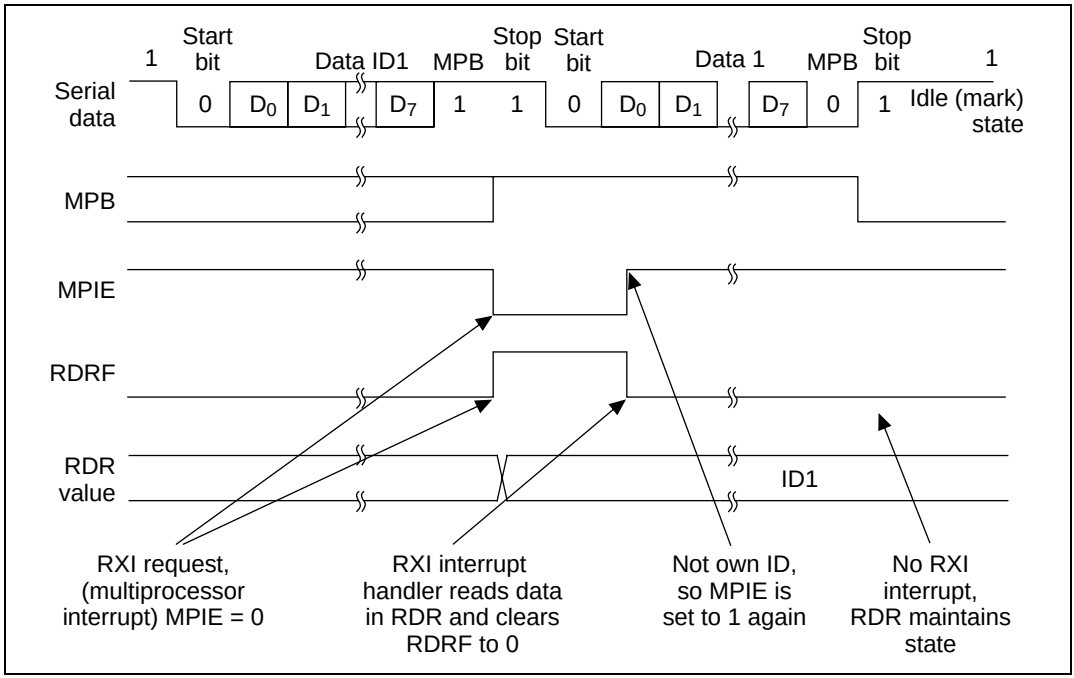


Figure 13.13 Example of SCI Receive Operation (Own ID Does Not Match Data) (8-Bit Data with Multiprocessor Bit and One Stop Bit)

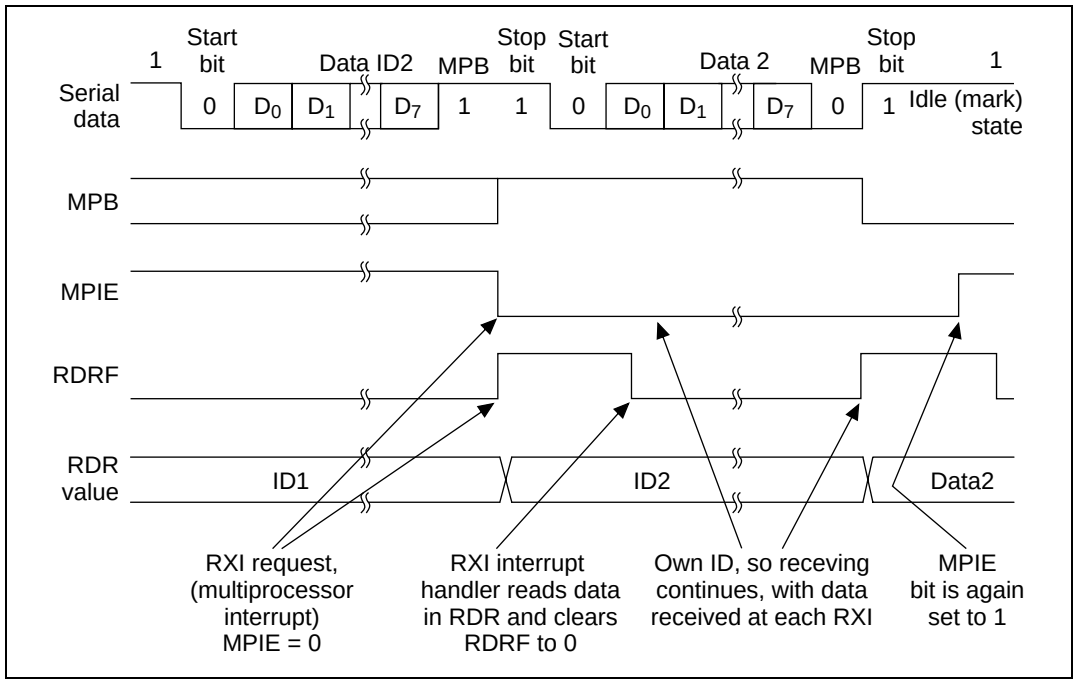


Figure 13.13 Example of SCI Receive Operation (Own ID Matches Data) (8-Bit Data with Multiprocessor Bit and One Stop Bit) (cont)

13.3.4 Synchronous Operation

In synchronous mode, the SCI transmits and receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communication.

The SCI transmitter and receiver share the same clock but are otherwise independent, so full duplex communication is possible. The transmitter and receiver are also double buffered, so continuous transmitting or receiving is possible by reading or writing data while transmitting or receiving is in progress.

Figure 13.14 shows the general format in synchronous serial communication.

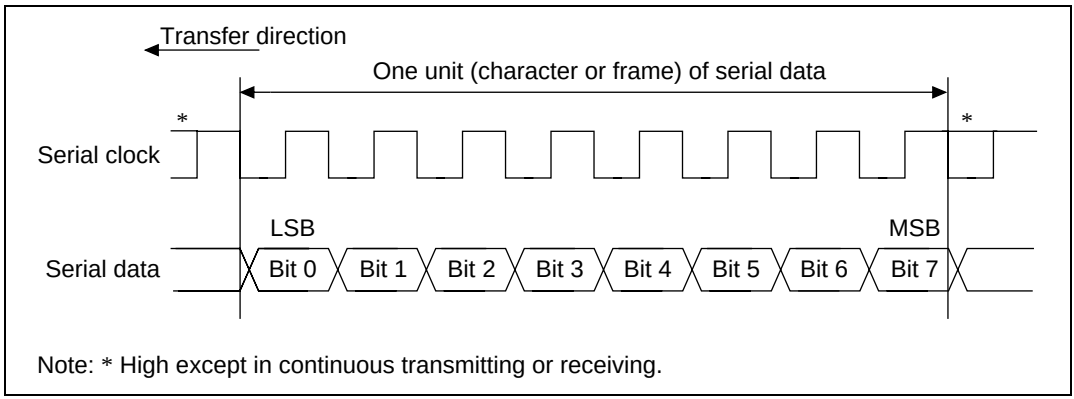


Figure 13.14 Data Format in Synchronous Communication

In synchronous serial communication, each data bit is output on the communication line from one falling edge of the serial clock to the next. Data is guaranteed valid at the rising edge of the serial clock. In each character, the serial data bits are transmitted in order from the LSB (first) to the MSB (last). After output of the MSB, the communication line remains in the state of the MSB. In synchronous mode, the SCI transmits or receives data by synchronizing with the falling edge of the serial clock.

Communication Format: The data length is fixed at eight bits. No parity bit or multiprocessor bit can be added.

Clock: An internal clock generated by the on-chip baud rate generator or an external clock input from the SCK pin can be selected as the SCI transmit/receive clock. The clock source is selected by the C/$\overline{A}$ bit in the serial mode register (SMR) and bits CKE1 and CKE0 in the serial control register (SCR). See table 13.6.

When the SCI operates on an internal clock, it outputs the clock signal at the SCK pin. Eight clock pulses are output per transmitted or received character. When the SCI is not transmitting or receiving, the clock signal remains in the high state.

Figure 13.15 shows an example of SCI transmit operation. In transmitting serial data, the SCI operates as follows.

1. The SCI monitors the TDRE bit in SSR. When TDRE is cleared to 0 the SCI recognizes that the transmit data register (TDR) contains new data, and loads this data from TDR into the transmit shift register (TSR).
2. After loading the data from TDR into TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the transmit-data-empty interrupt enable bit (TIE) in SCR is set to 1, the SCI requests a transmit-data-empty interrupt (TXI) at this time.

If clock output is selected, the SCI outputs eight serial clock pulses. If an external clock source is selected, the SCI outputs data in synchronization with the input clock. Data is output from the TxD pin in order from the LSB (bit 0) to the MSB (bit 7).

3. The SCI checks the TDRE bit when it outputs the MSB (bit 7). If TDRE is 0, the SCI loads data from TDR into TSR, transmits the MSB, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit in SSR to 1, transmits the MSB, then holds the transmit data pin (TxD) in the MSB state. If the transmit-end interrupt enable bit (TEIE) in SCR is set to 1, a transmit-end interrupt (TEI) is requested at this time.
4. After the end of serial transmission, the SCK pin is held in the high state.

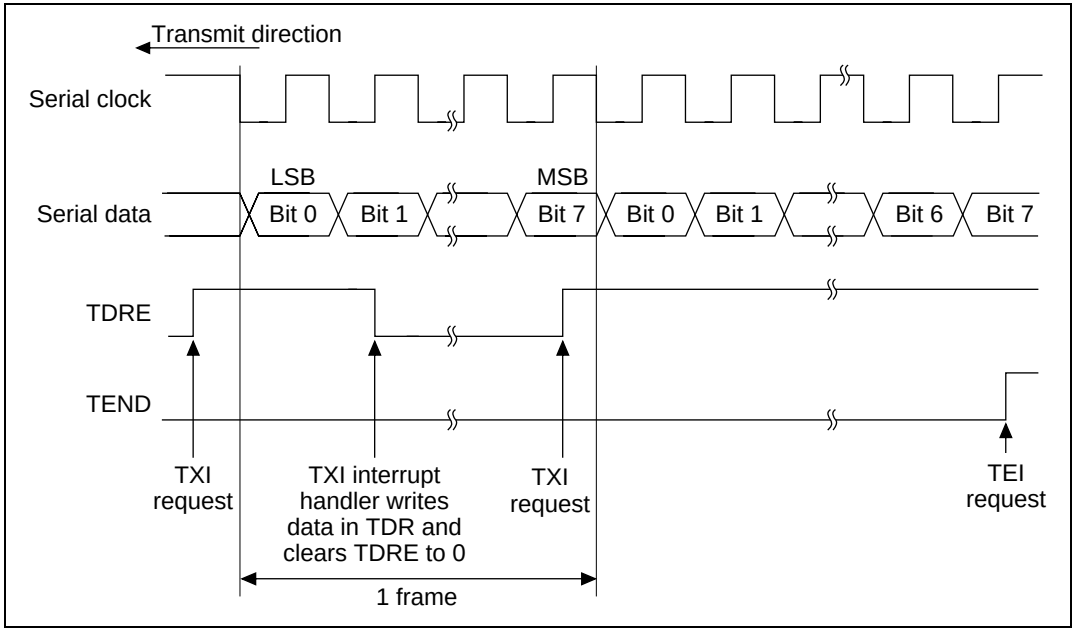


Figure 13.15 Example of SCI Transmit Operation

Transmitting and Receiving Data: SCI Initialization (Synchronous Mode): Before transmitting or receiving, software must clear the TE and RE bits to 0 in the serial control register (SCR), then initialize the SCI as follows.

When changing the communication mode or format, always clear the TE and RE bits to 0 before following the procedure given below. Clearing TE to 0 sets TDRE to 1 and initializes the transmit shift register (TSR). Clearing RE to 0, however, does not initialize the RDRF, PER, FER, and ORER flags and receive data register (RDR), which retain their previous contents.

Figure 13.16 shows a sample flowchart for initializing the SCI.

1. Select the communication format in the serial mode register (SMR).
2. Write the value corresponding to the bit rate in the bit rate register (BRR) unless an external clock is used.
3. Select the clock source in the serial control register (SCR). Leave RIE, TIE, TEIE, MPIE, TE, and RE cleared to 0.
4. Wait for at least the interval required to transmit or receive one bit, then set TE or RE in the serial control register (SCR) to 1. Also set RIE, TIE, TEIE, and MPIE. Setting the corresponding bit of the pin function controller, TE, and RE enables the SCI to use the TxD or RxD pin.

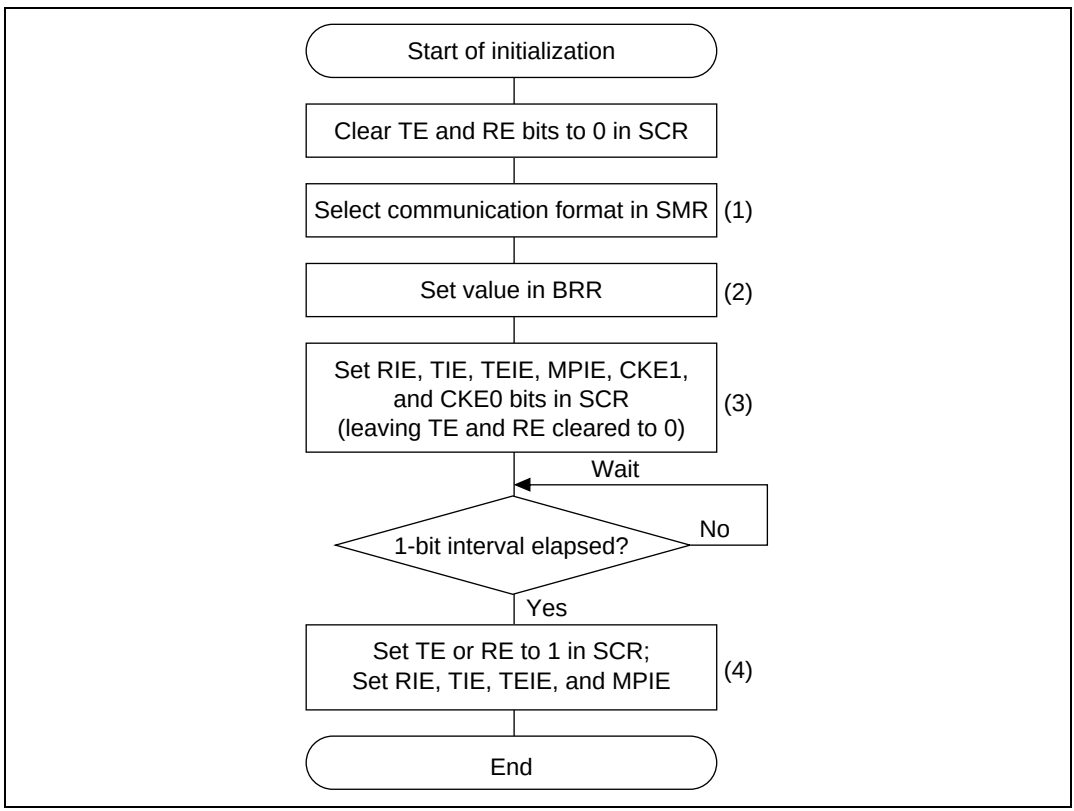


Figure 13.16 Sample Flowchart for SCI Initialization

Transmitting Serial Data (Synchronous Mode): Figure 13.17 shows a sample flowchart for transmitting serial data. The procedure for transmitting serial data is listed below.

1. SCI initialization: select the TxD pin function with the PFC.
2. SCI status check and transmit data write: read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR) and clear TDRE to 0.
3. To continue transmitting serial data: read the TDRE bit to check whether it is safe to write (1); if so, write data in TDR, then clear TDRE to 0. When the DMAC is started by a transmit-data-empty interrupt request (TXI) to write data in TDR, the TDRE bit is checked and cleared automatically.

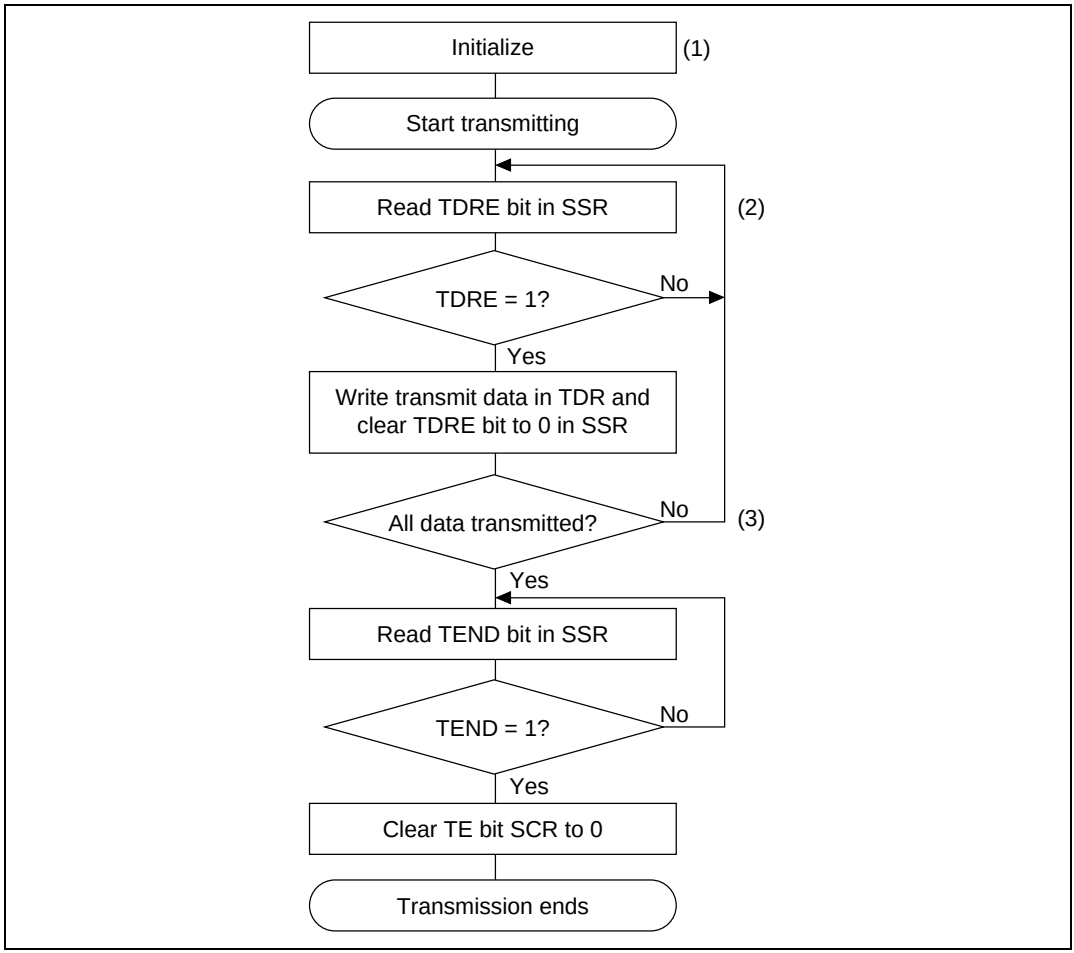


Figure 13.17 Sample Flowchart for Serial Transmitting

Receiving Serial Data (Synchronous Mode): Figure 13.18 shows a sample flowchart for receiving serial data. When switching from asynchronous mode to synchronous mode, make sure that ORER, PER, and FER are cleared to 0. If PER or FER is set to 1, the RDRF bit will not be set and both transmitting and receiving will be disabled. Figure 13.19 shows an example of SCI receive operation.

The procedure for receiving serial data is listed below.

1. SCI initialization: select the RxD pin function with the PFC.
2. Receive error handling and break detection: if a receive error occurs, read the ORER bit in SSR to identify the error. After executing the necessary error handling, clear ORER to 0. Transmitting/receiving cannot resume if ORER remains set to 1.
3. SCI status check and receive data read: read the serial status register (SSR), check that RDRF is set to 1, then read receive data from the receive data register (RDR) and clear RDRF to 0. The RXI interrupt can also be used to determine if the RDRF bit has changed from 0 to 1.
4. To continue receiving serial data: read RDR, and clear RDRF to 0 before the frame MSB (bit 7) of the current frame is received. If the DMAC is started by a receive-data-full interrupt (RXI) to read RDR, the RDRF bit is cleared automatically, so this step is unnecessary.

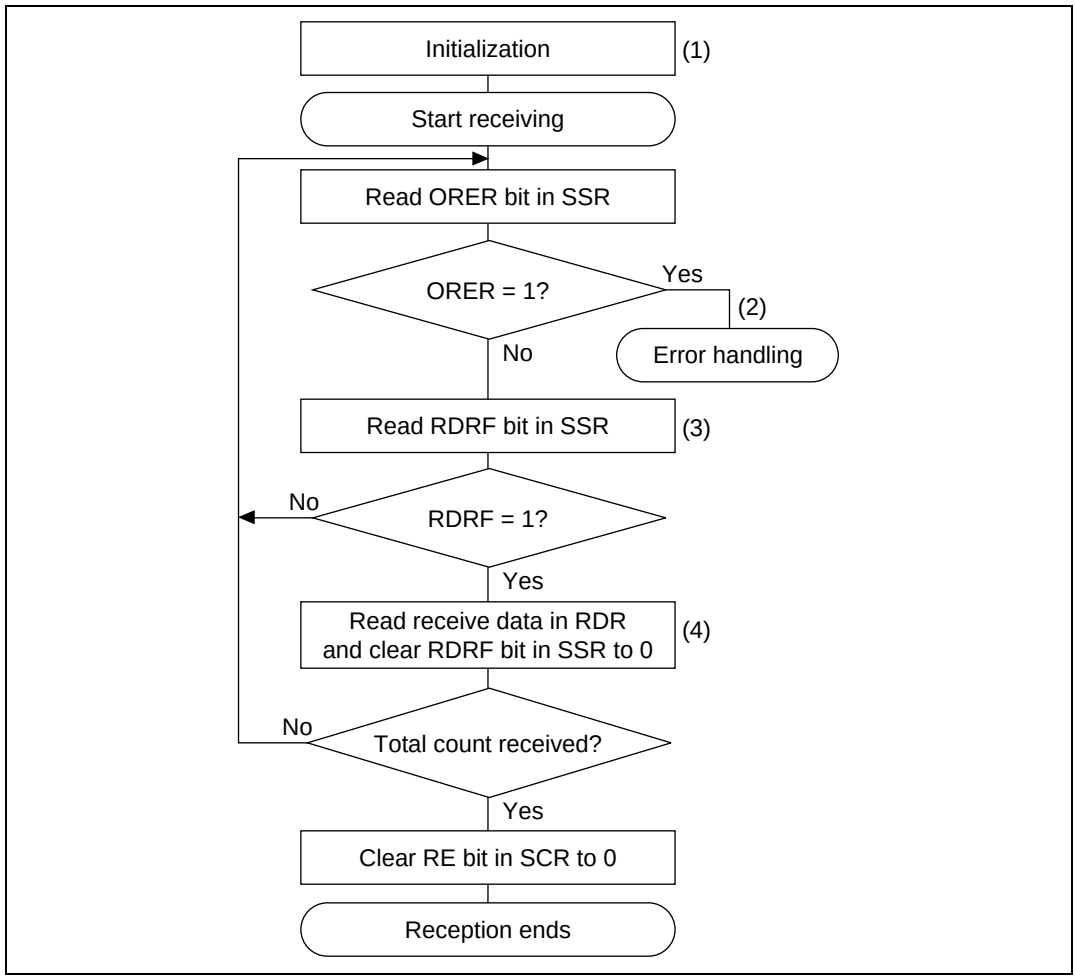


Figure 13.18 Sample Flowchart for Serial Receiving

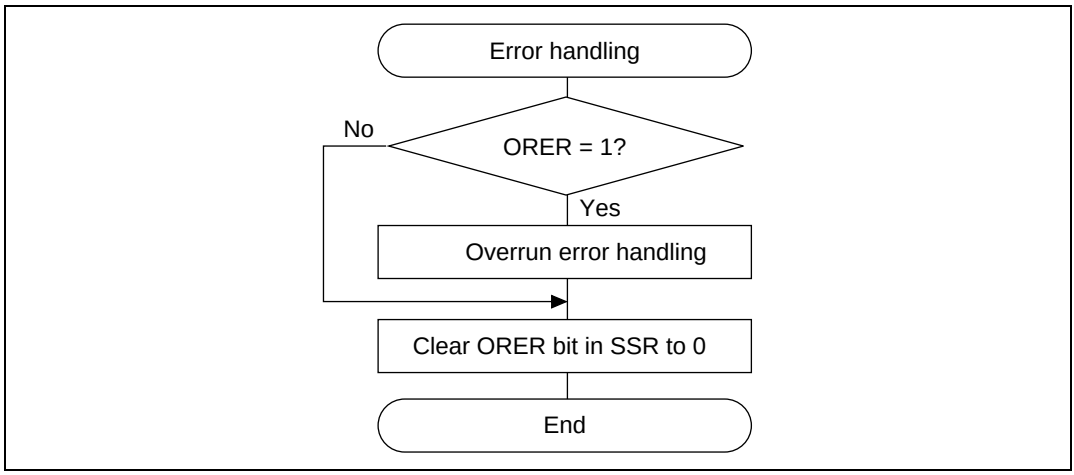


Figure 13.18 Sample Flowchart for Serial Receiving (cont)

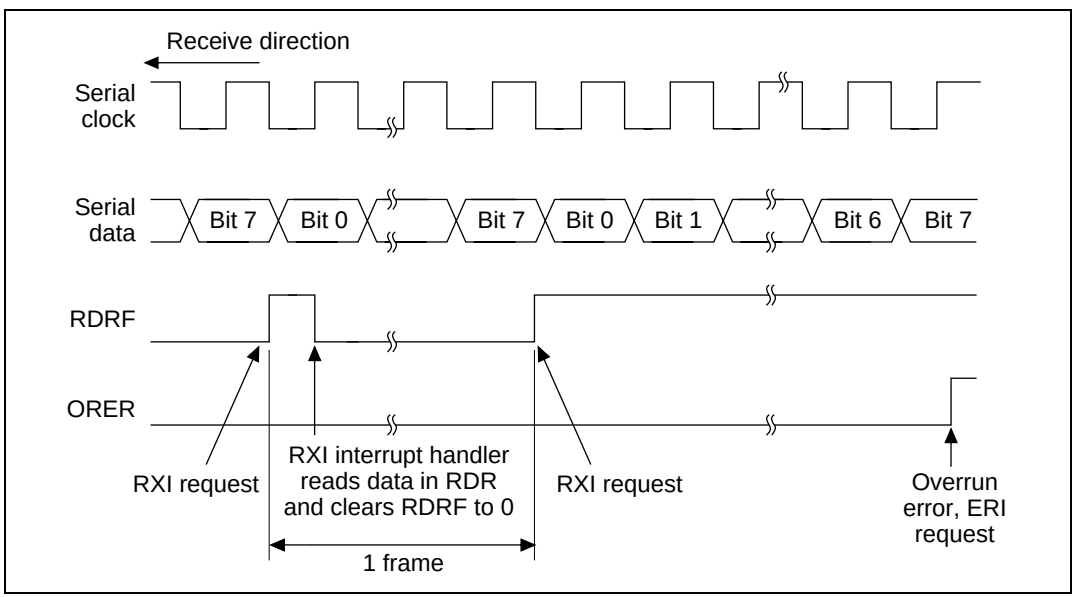


Figure 13.19 Example of SCI Receive Operation

In receiving, the SCI operates as follows:

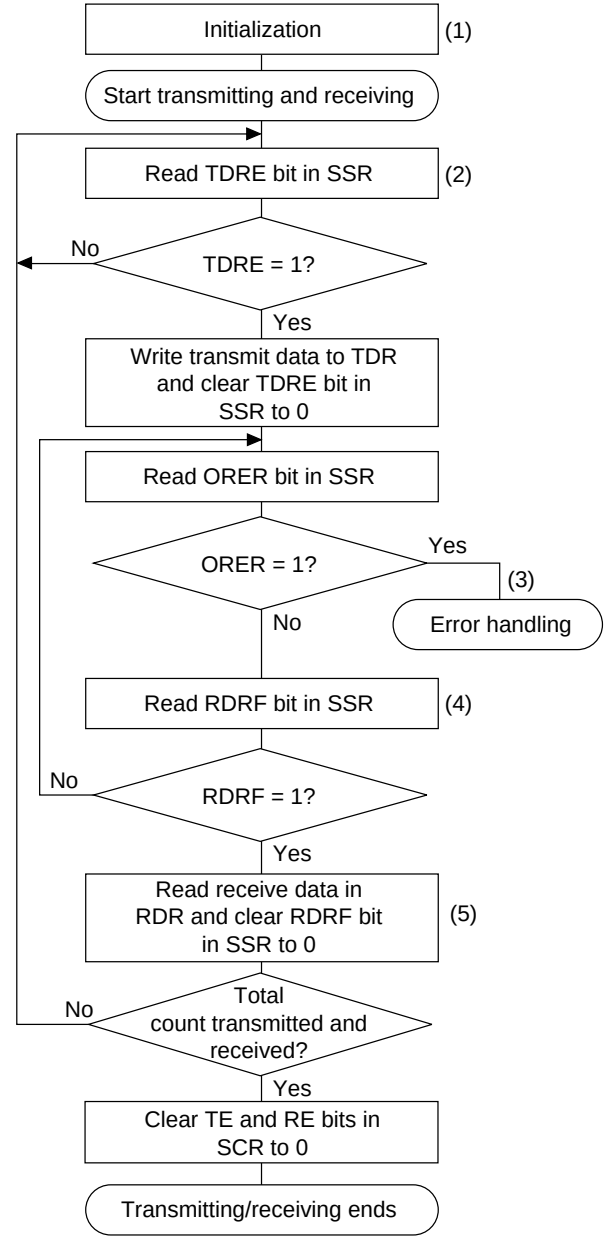
1. The SCI synchronizes with serial clock input or output and initializes internally.
2. Receive data is shifted into RSR in order from the LSB to the MSB. After receiving the data, the SCI checks that RDRF is 0 so that receive data can be loaded from RSR into RDR. If this check passes, the SCI sets RDRF to 1 and stores the received data in RDR. If the check does

not pass (receive error), the SCI operates as indicated in table 13.8. When the error flag is set to 1 and the RDRF bit is cleared to 0, the RDRF bit will not be set to 1 during reception. When restarting reception, be sure to clear the error flag to 0.

3. After setting RDRF to 1, if the receive-data-full interrupt enable bit (RIE) is set to 1 in SCR, the SCI requests a receive-data-full interrupt (RXI). If the ORER bit is set to 1 and the receive-data-full interrupt enable bit (RIE) in SCR is also set to 1, the SCI requests a receive-error interrupt (ERI).

Transmitting and Receiving Serial Data Simultaneously (Synchronous Mode): Figure 13.20 shows a sample flowchart for transmitting and receiving serial data simultaneously. The procedure for transmitting and receiving serial data simultaneously is listed below.

1. SCI initialization: select the TxD and RxD pin function with the PFC.
2. SCI status check and transmit data write: read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR) and clear TDRE to 0. The TXI interrupt can also be used to determine if the TDRE bit has changed from 0 to 1.
3. Receive error handling: if a receive error occurs, read the ORER bit in SSR to identify the error. After executing the necessary error handling, clear ORER to 0. Transmitting/receiving cannot resume if ORER remains set to 1.
4. SCI status check and receive data read: read the serial status register (SSR), check that RDRF is set to 1, then read receive data from the receive data register (RDR) and clear RDRF to 0. The RXI interrupt can also be used to determine if the RDRF bit has changed from 0 to 1.
5. To continue transmitting and receiving serial data: read the RDRF bit and RDR, and clear RDRF to 0 before the MSB (bit 7) of the current frame is received. Also read the TDRE bit to check whether it is safe to write (1); if so, write data in TDR, then clear TDRE to 0 before the MSB (bit 7) of the current frame is transmitted. When the DMAC is started by a transmit-data-empty interrupt request (TXI) to write data in TDR, the TDRE bit is checked and cleared automatically. When the DMAC is started by a receive-data-full interrupt (RXI) to read RDR, the RDRF bit is cleared automatically.



Note: When switching from transmitting or receiving to simultaneous transmitting and receiving, clear both the TE bit and the RE bit to 0, then set both this to 1 simultaneously.

Figure 13.20 Sample Flowchart for Serial Transmitting and Receiving

13.4 SCI Interrupt Sources and the DMAC

The SCI has four interrupt sources in each channel: transmit-end (TEI), receive-error (ERI), receive-data-full (RXI), and transmit-data-empty (TXI). Table 13.12 lists the interrupt sources and indicates their priority. These interrupts can be enabled and disabled by the TIE, RIE, and TEIE bits in the serial control register (SCR). Each interrupt request is sent separately to the interrupt controller.

TXI is requested when the TDRE bit in SSR is set to 1. TXI can start the direct memory access controller (DMAC) to transfer data. TDRE is automatically cleared to 0 when the DMAC executes a data transfer to the transmit data register (TDR).

RXI is requested when the RDRF bit in SSR is set to 1. RXI can start the DMAC to transfer data. RDRF is automatically cleared to 0 when the DMAC executes a data transfer to the receive data register (RDR). ERI is requested when the ORER, PER, or FER bit in SSR is set to 1. ERI cannot start the DMAC.

TEI is requested when the TEND bit in SSR is set to 1. TEI cannot start the DMAC. A TXI interrupt indicates that transmit data writing is enabled. A TEI interrupt indicates that the transmit operation is complete.

Table 13.12 SCI Interrupt Sources

Interrupt Source	Description	DMAC Activation	Priority
ERI	Receive error (ORER, PER, or FER)	No	High
RXI	Receive data full (RDRF)	Yes	↑
TXI	Transmit data empty (TDRE)	Yes	↓
TEI	Transmit end (TEND)	No	Low

13.5 Usage Notes

Note the following points when using the SCI.

TDR Write and TDRE Flags: The TDRE bit in the serial status register (SSR) is a status flag indicating loading of transmit data from TDR into TSR. The SCI sets TDRE to 1 when it transfers data from TDR to TSR. Data can be written in TDR regardless of the status of the TDRE bit. If new data is written in TDR when TDRE is 0, the old data stored in TDR will be lost because this data has not yet been transferred to TSR. Before writing transmit data to TDR, be sure to check that TDRE is set to 1.

Simultaneous Multiple Receive Errors: Table 13.13 indicates the state of the SSR status flags when multiple receive errors occur simultaneously. When an overrun error occurs, the RSR contents cannot be transferred to RDR, so receive data is lost.

Table 13.13 SSR Status Flags and Transfer of Receive Data

	SSR Status Flags				Receive Data Transfer
Receive Error Status	**RDRF**	**ORER**	**FER**	**PER**	**RSR → RDR**
Overrun error	1	1	0	0	X
Framing error	0	0	1	0	O
Parity error	0	0	0	1	O
Overrun error + framing error	1	1	1	0	X
Overrun error + parity error	1	1	0	1	X
Framing error + parity error	0	0	1	1	O
Overrun error + framing error + parity error	1	1	1	1	X

O: Receive data is transferred from RSR to RDR.

X: Receive data is not transferred from RSR to RDR.

Break Detection and Processing: Break signals can be detected by reading the RxD pin directly when a framing error (FER) is detected. In the break state, the input from the RxD pin consists of all 0s, so FER is set and the parity error flag (PER) may also be set. In the break state, the SCI receiver continues to operate, so if the FER bit is cleared to 0, it will be set to 1 again.

Sending a Break Signal: When TE is cleared to 0 the TxD pin becomes an I/O port, the level and direction (input or output) of which are determined by the data register (DR) of the I/O port and the control register (CR) of the PFC. This feature can be used to send a break signal. The DR value substitutes for the mark state until the PFC setting is performed. The DR bits should therefore be set as an output port that outputs 1 beforehand. To send a break signal during serial transmission, clear the DR bit to 0, and select output port as the TxD pin function by the PFC. When TE is cleared to 0, the transmitter is initialized, regardless of its current state.

Receive Error Flags and Transmitter Operation (Synchronous Mode Only): When a receive error flag (ORER, PER, or FER) is set to 1, the SCI will not start transmitting even if TDRE is set to 1. Be sure to clear the receive error flags to 0 before starting to transmit. Note that clearing RE to 0 does not clear the receive error flags.

Receive Data Sampling Timing and Receive Margin in Asynchronous Mode: In asynchronous mode, the SCI operates on a base clock of 16 times the bit rate frequency. In receiving, the SCI

synchronizes internally with the falling edge of the start bit, which it samples on the base clock. Receive data is latched on the rising edge of the eighth base clock pulse. See figure 13.21.

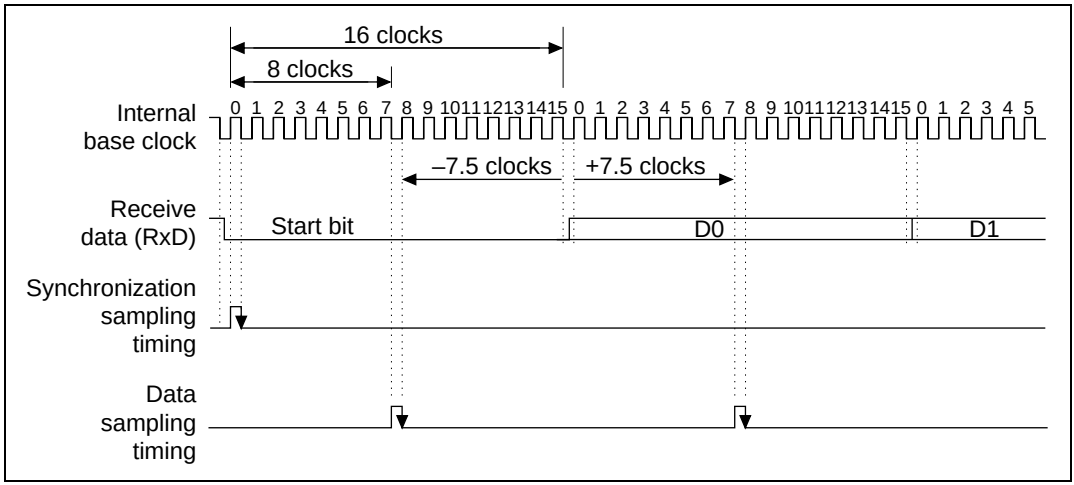


Figure 13.21 Receive Data Sampling Timing in Asynchronous Mode

The receive margin in asynchronous mode can therefore be expressed as shown in equation 1.

Equation 1:

$$M = \left| \left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F) \right| \times 100\%$$

M: Receive margin (%)
N: Ratio of clock frequency to bit rate (N = 16)
D: Clock duty cycle (D = 0 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute deviation of clock frequency

From equation (1), if F = 0 and D = 0.5 the receive margin is 46.875%, as given by equation 2.

Equation 2:

$$D = 0.5, F = 0$$
$$M = (0.5 - 1/(2 \times 16)) \times 100\%$$
$$= 46.875\% \quad (2)$$

This is a theoretical value. A reasonable margin to allow in system designs is 20–30%.

Constraints on DMAC Use:

- When using an external clock source for the serial clock, update TDR with the DMAC, and then input the transmit clock after the elapse of five system clocks or more. If a transmit clock is input in the first four system clocks after TDR is written, an error may occur (figure 13.22).
- Before reading the receive data register (RDR) with the DMAC, select the receive-data-full interrupt of the SCI as an activation source using the resource select bit (RS) in the channel control register (CHCR).

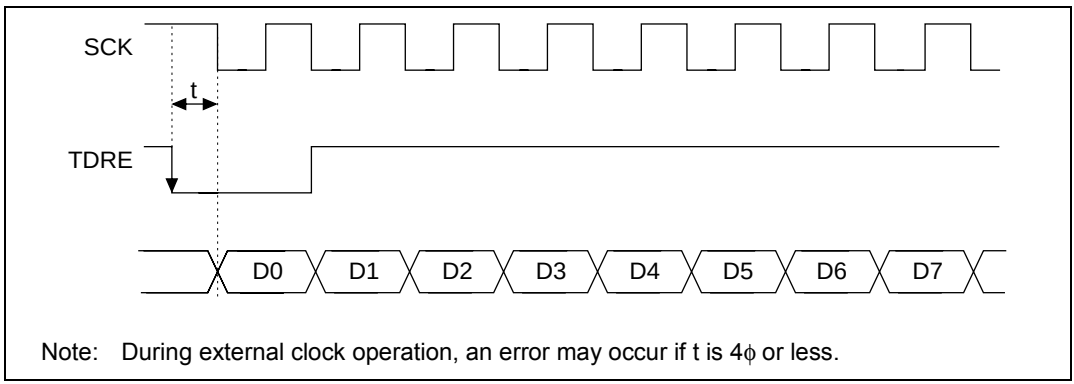


Figure 13.22 Example of Synchronous Transmitting with DMAC

Cautions on Use of Synchronous External Clock Mode:

- Set TE = RE = 1 only when the external clock SCI is 1.
- Do not set TE = RE = 1 until at least 4 clocks after the external clock SCK has changed from 0 to 1.
- When receiving, RDRF is set to 1 when RE is cleared to 0 2.5–3.5 clocks after the rising edge of the RxD D7 bit SCK input, but copying to RDR is not possible.

Caution on Synchronous Internal Clock Mode: When receiving, RDRF is set to 1 when RE is cleared to 0 1.5 clocks after the rising edge of the RxD D7 bit SCK output, but copying to RDR is not possible.

Section 14 A/D Converter

14.1 Overview

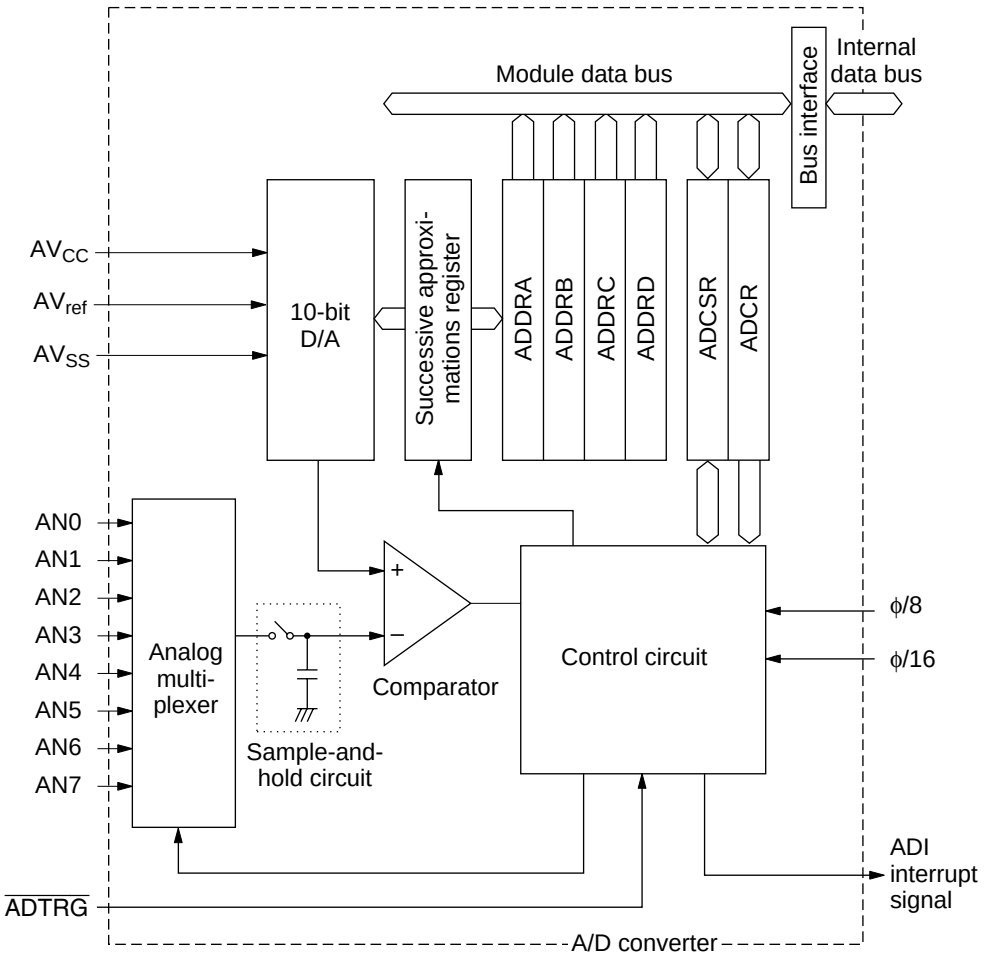
The SuperH microcomputer includes an analog-to-digital converter module which can be programmed for input of analog signals up to eight channels. A/D conversion is performed by the successive approximations method with 10-bit resolution.

14.1.1 Features

- 10-bit resolution
- Eight analog input channels
- User definable analog conversion voltage range
- The analog conversion voltage range can be set with the analog reference power pin (AVref) as the analog reference voltage
- Rapid conversion time: 6.7 µs per channel (at 20 MHz)
- Single mode or scan mode (selectable)
  - Single mode: One-channel A/D conversion
  - Scan mode: A/D conversion repeated on one to four channels
- Four 16-bit data registers: A/D conversion results are transferred to and stored in the data registers corresponding to channels
- Sample-and-hold circuit
- External trigger input can start A/D conversion
- ADI: A/D interrupt request
  - Can be generated at end of each conversion cycle
  - Can start direct memory access controller (DMAC)

14.1.2 Block Diagram

Figure 14.1 shows a block diagram of the A/D converter.



ADCR: A/D control register
ADCSR: A/D control/status register
ADDRA: A/D data register A
ADDRB: A/D data register B
ADDRC: A/D data register C
ADDRD: A/D data register D

Figure 14.1 Block Diagram of A/D Converter

14.1.3 Configuration of Input Pins

Table 14.1 lists input pins for the A/D converter. The eight analog input pins are grouped into two sets. Group 0 comprises analog input pins 0–3 (AN_0–AN_3) and group 1 comprises pins 4–7 (AN_4–AN_7). Pins AV_{CC} and AV_{SS} are the power supply pins for the analog circuits of the A/D converter. AV_{ref} is the analog reference voltage for A/D conversion.

Table 14.1 Input Pins

Pin Name	Abbreviation	I/O	Function
Analog supply voltage	AV_{CC}	I	Power supply for the analog circuits
Analog ground	AV_{SS}	I	Ground and reference voltage for the analog circuits
Analog reference power supply	AV_{ref}	I	Reference voltage for the analog circuits
Analog input 0	AN0	I	Analog input pins, group 0
Analog input 1	AN1	I	
Analog input 2	AN2	I	
Analog input 3	AN3	I	
Analog input 4	AN4	I	Analog input pins, group 1
Analog input 5	AN5	I	
Analog input 6	AN6	I	
Analog input 7	AN7	I	
A/D conversion trigger input	$\overline{\text{ADTRG}}$	I	A/D conversion start external trigger input

14.1.4 Configuration of A/D Registers

The A/D converter includes the registers listed in table 14.2.

Table 14.2 A/D Registers

Register Name	Abbreviation	R/W	Initial Value	Address*1	Access Size
A/D data register A (high)	ADDRAH	R	H'00	H'05FFFEE0	8, 16
A/D data register A (low)	ADDRAL	R	H'00	H'05FFFEE1	16
A/D data register B (high)	ADDRBH	R	H'00	H'05FFFEE2	8, 16
A/D data register B (low)	ADDRBL	R	H'00	H'05FFFEE3	16
A/D data register C (high)	ADDRCH	R	H'00	H'05FFFEE4	8, 16
A/D data register C (low)	ADDRCL	R	H'00	H'05FFFEE5	16
A/D data register D (high)	ADDRDH	R	H'00	H'05FFFEE6	8, 16
A/D data register D (low)	ADDRDL	R	H'00	H'05FFFEE7	16
A/D control/status register	ADCSR	R/(W)*2	H'00	H'05FFFEE8	8, 16
A/D control register	ADCR	R/W	H'7F	H'05FFFEE9	8, 16

Notes: 1. Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.
2. Only 0 can be written in bit 7, to clear the flag.

14.2 Register Descriptions

14.2.1 A/D Data Registers A–D (ADDRA–ADDRD)

The four A/D data registers (ADDRA–ADDRD) are 16-bit read-only registers that store the results of the A/D conversion. Each result consists of 10 bits. The first 8 bits are stored in the upper byte of the data register corresponding to the selected channel. The last two bits are stored in the lower byte of the data register. Bits 5–0 of the lower byte are reserved and are always read as 0. Each data register is assigned to two analog input channels (table 14.3).

The A/D data registers are always readable by the CPU. The upper byte can be read directly and the lower byte is read via a temporary register (TEMP). See section 14.3, CPU Interface, for details. The A/D data registers are initialized to H'0000 by a reset and in standby mode.

Bit	15	14	13	12	11	10	9	8
	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
	AD1	AD0	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

n = A–D

Table 14.3 Assignment of Data Registers to Analog Input Channels

Analog Input Channel		
Group 0	**Group 1**	**A/D Data Register**
AN0	AN4	ADDRA
AN1	AN5	ADDRB
AN2	AN6	ADDRC
AN3	AN7	ADDRD

14.2.2 A/D Control/Status Register (ADCSR)

The A/D control/status register (ADCSR) is an 8-bit read/write register that controls the operation of the A/D converter (mode selection, etc.). ADCSR is initialized to H'00 by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Only 0 can be written, to clear the flag.

Bit 7—A/D End Flag (ADF): ADF indicates that A/D conversion is completed.

Bit 7 (ADF)	Description
0	Cleared to 0 under the following conditions: (Initial value) • The CPU reads the ADF bit while the bit is set to 1, then writes 0 in the bit • The ADI starts the DMAC and the A/D conversion register is accessed
1	Set to 1 at the following times: • Single mode: When A/D conversion is complete • Scan mode: When A/D conversion of all selected channels is complete

Bit 6—A/D Interrupt Enable (ADIE): ADIE selects whether or not an A/D interrupt (ADI) is requested when A/D conversion is completed.

Bit 6 (ADIE)	Description
0	The A/D interrupt (ADI) request is disabled (Initial value)
1	The A/D interrupt (ADI) request is enabled

Bit 5—A/D Start (ADST): ADST selects the start or halting of A/D conversion. Whenever the A/D converter is operating, this bit is set to 1. It can also be set to 1 by the A/D conversion trigger input pin ($\overline{\text{ADTRG}}$).

Bit 5 (ADST)	Description
0	A/D conversion is halted (Initial value)
1	• Single mode: A/D conversion is performed. This bit is automatically cleared to 0 at the end of the conversion. • Scan mode: A/D conversion starts and continues cyclically on the selected channels until this bit is cleared to 0 by software, a reset, or standby mode.

Bit 4—Scan Mode (SCAN): SCAN selects either scan mode or single mode for operation. See section 14.4, Operation, for descriptions of these modes. The mode should be changed only when the ADST bit is cleared to 0.

Bit 4 (SCAN)	Description
0	Single mode (Initial value)
1	Scan mode

Bit 3—Clock Select (CKS): CKS selects the A/D conversion time. The conversion time should be changed only when the ADST bit is cleared to 0.

Bit 3 (CKS)	Description	
0	Conversion time = 266 states (maximum)	(Initial value)
1	Conversion time = 134 states (maximum)	

Bits 2–0—Channel Select 2–0 (CH2–CH0): CH2–CH0 select analog input channels together with the SCAN bit. The channel selection should be changed only when the ADST bit is cleared to 0.

Group Select	Channel Select		Selected Channels	
CH2	CH1	CH0	Single Mode	Scan Mode
0	0	0	AN0	AN0 (Initial value)
	0	1	AN1	AN0 and AN1
	1	0	AN2	AN0–AN2
	1	1	AN3	AN0–AN3
1	0	0	AN4	AN4
	0	1	AN5	AN4 and AN5
	1	0	AN6	AN4–AN6
	1	1	AN7	AN4–AN7

14.2.3 A/D Control Register (ADCR)

The A/D control register (ADCR) is an 8-bit read/write register that selects whether or not to start the A/D conversion when an external trigger is input. ADCR is initialized to H'7F by a reset and in standby mode.

Bit	7	6	5	4	3	2	1	0
	TRGE	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

Bit 7—Trigger Enable (TRGE): TRGE selects whether or not to start A/D conversion when an external trigger is input.

Bit 7 (TRGE)	Description
0	When an external trigger is input, A/D conversion does not start (Initial value)
1	A/D conversion starts at the falling edge of an input signal from the external trigger pin ($\overline{\text{ADTRG}}$).

Bits 6–0—Reserved): These bits are always read as 1. The write value should always be 1.

14.3 CPU Interface

The A/D data registers (ADDRA–ADDRD) are 16-bit registers, but they are connected to the CPU by an 8-bit data bus. Therefore, the upper byte of each register can be read directly, but the lower byte is accessed through an 8-bit temporary register (TEMP).

When the CPU reads the upper byte of an A/D data register, the upper byte is transferred to the CPU and the lower byte to TEMP. When the lower byte is accessed, the value in TEMP is transferred to the CPU.

A program should first read the upper byte, then the lower byte of the A/D data register. This can be performed by reading ADDR from the upper byte end using a word transfer instruction (MOV.W, etc.). Reading only the upper byte would assure the CPU of obtaining consistent data. If the program reads only the lower byte, however, consistent data will not be guaranteed.

Figure 14.2 shows the data flow during access to A/D data registers.

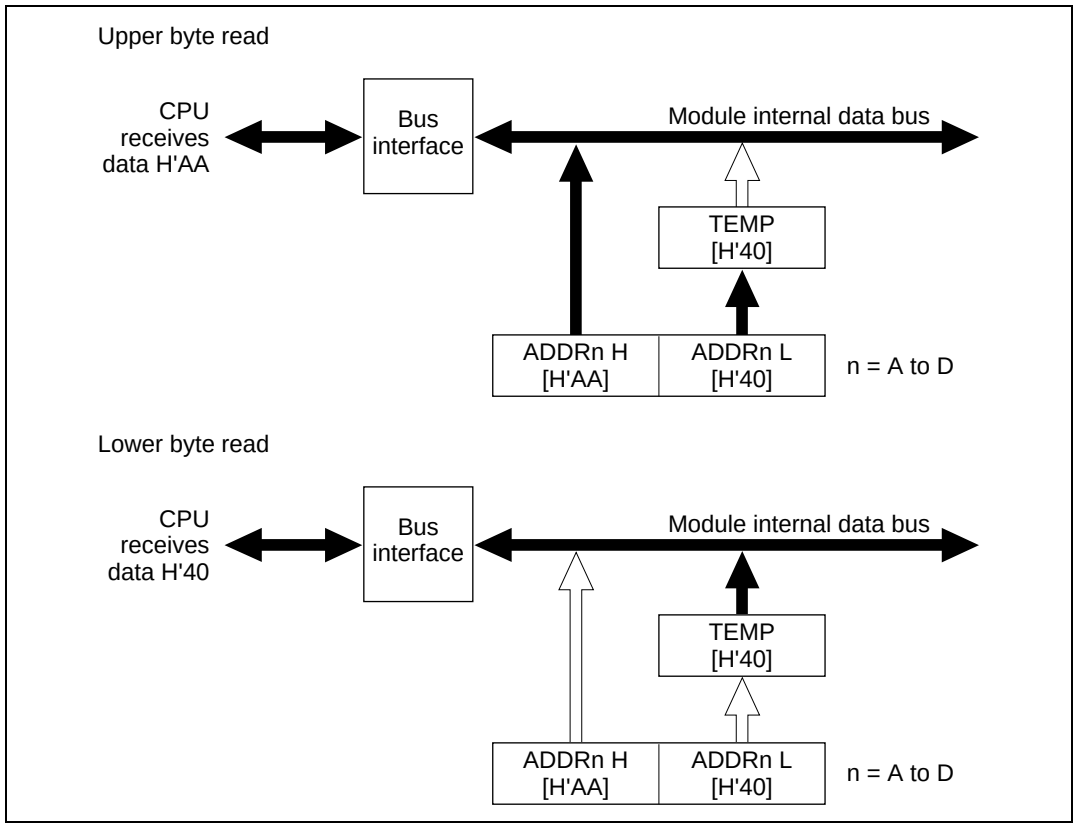


Figure 14.2 Read Access to A/D Data Register (Reading H'AA40)

14.4 Operation

The A/D converter operates by successive approximations with a 10-bit resolution. Its two modes, single mode and scan mode, are described below.

14.4.1 Single Mode (SCAN = 0)

In single mode, A/D conversion is performed on a single channel. A/D conversion starts when the ADST bit in the A/D control/status register (ADCSR) is set to 1 by software or an external trigger input. During the conversion process the ADST bit remains set at 1. When the conversion is completed, the ADST bit is automatically cleared to 0.

When the conversion is completed, the ADF bit is set to 1. If the interrupt enable bit (ADIE) in ADCSR is also set to 1, an A/D conversion interrupt (ADI) is requested. When ADCSR is read and 1 is written in the ADF bit, the ADF bit is cleared to 0.

Before changing a mode or analog input channel, clear the ADST bit in ADCSR to 0 to stop A/D conversion in order to prevent malfunctions. Setting the ADST bit to 1 after changing the mode or channel starts A/D conversion again (changing the mode or channel and setting the ADST bit can be performed simultaneously).

The following is an example of the A/D conversion process in single mode when channel 1 (AN1) is selected. See figure 14.3 for the timing.

1. The program selects single mode (SCAN = 0) and input channel AN1 (CH2 = CH1 = 0, CH0 = 1), enables the A/D interrupt request (ADIE = 1), and sets the ADST bit to 1 to start A/D conversion.
2. At the end of the conversion process the A/D converter transfers the result to register ADDRB, sets the ADF bit to 1, clears the ADST bit to 0, and halts.
3. Since ADF = 1 and ADIE = 1, an A/D interrupt is requested.
4. The A/D interrupt handling routine is started.
5. The interrupt handling routine reads the ADF value; since it is 1, it writes a 0 into the ADF bit.
6. The interrupt handling routine reads and processes the A/D conversion result (ADDRB).
7. The routine ends.

Steps 2–7 can now be repeated by setting the ADST bit to 1 again.

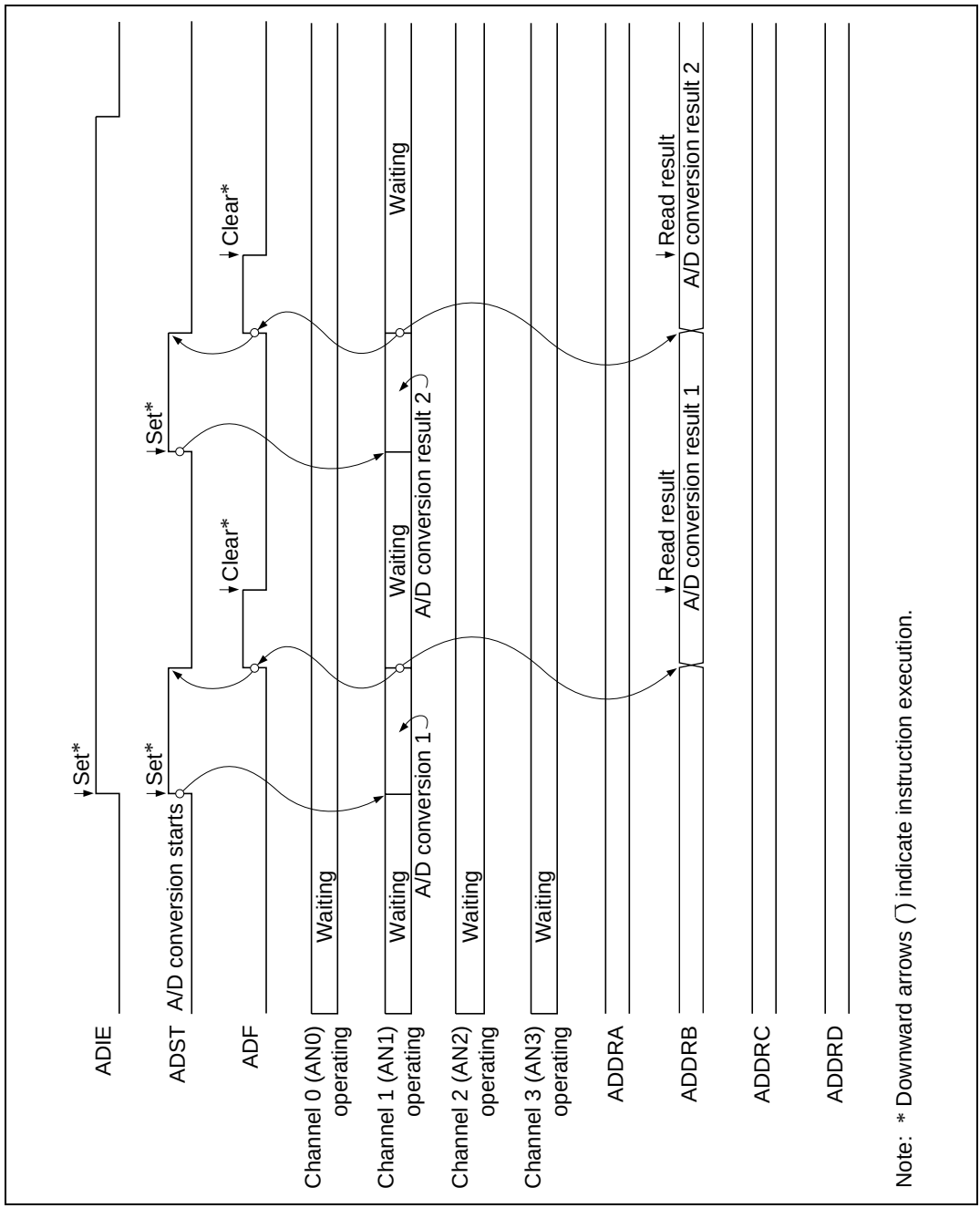


Figure 14.3 A/D Operation in Single Mode (Channel 1 Selected)

14.4.2 Scan Mode (SCAN = 1)

Scan mode can be used to monitor analog inputs on one or more channels. When the ADST bit in ADCSR is set to 1 by software or an external trigger input, A/D conversion starts with the first channel (AN0 when CH2 = 0, AN4 when CH2 = 1) in the group.

If the scan group includes more than one channel, conversion of the second channel (AN1 or AN5) begins as soon as conversion of the first channel ends.

Conversion of the selected channels continues cyclically until the ADST bit is cleared to 0. The conversion results are stored in the data registers corresponding to the selected channels.

Before changing a mode or analog input channels, clear the ADST bit in ADCSR to 0 to stop A/D conversion in order to prevent malfunctions. Setting the ADST bit to 1 after changing the mode or channel selects the first channel and starts A/D conversion again (changing the mode or channel and setting the ADST bit can be performed simultaneously).

The following is an example of the A/D conversion process in scan mode when three channels in group 0 are selected (AN0, AN1, and AN2). See figure 14.4 for the timing.

1. The program selects scan mode (SCAN = 1), scan group 0 (CH2 = 0), and analog input channels AN0–AN2 (CH1 = 1, CH2 = CH0 = 0), then sets the ADST bit to 1 to start A/D conversion.
2. The A/D converter samples the input at the first channel (AN0), converts the voltage level to a digital value, and transfers the result to register ADDRA. Next, the second channel (AN1) is automatically selected and conversion begins.
3. Then it does the same for the third channel (AN2).
4. After all selected channels (AN0–AN2) have been converted, the A/D converter sets the ADF bit to 1 and begins conversion on channel AN0 again. If the ADIE bit is set to 1, an A/D interrupt (ADI) is requested after the A/D conversion.
5. Steps 2–4 are repeated cyclically as long as the ADST bit remains set at 1.

   To stop A/D conversion, clear the ADST bit to 0. The moment the ADST bit is set to 1 again, A/D conversion begins with the first channel (AN0).

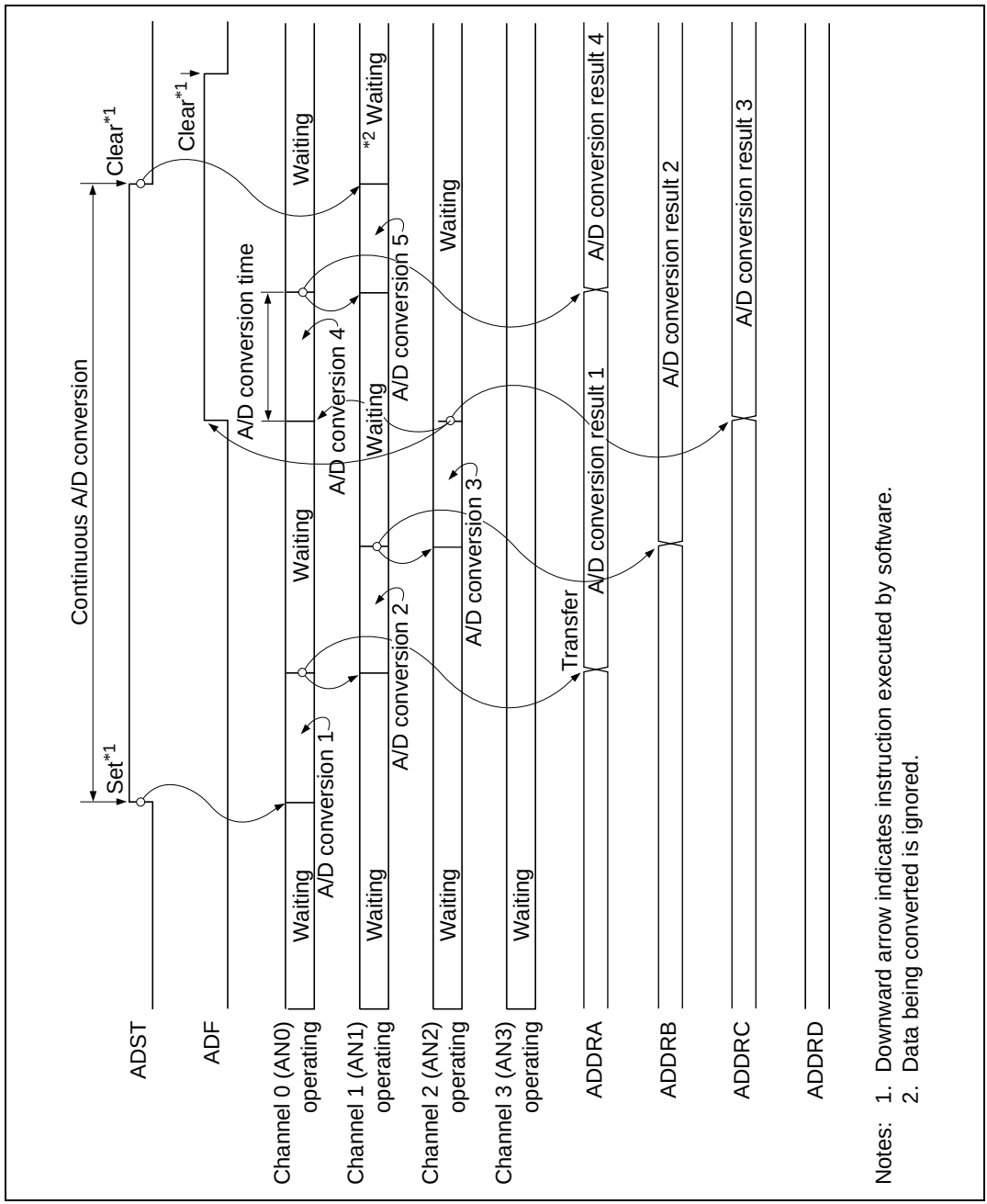


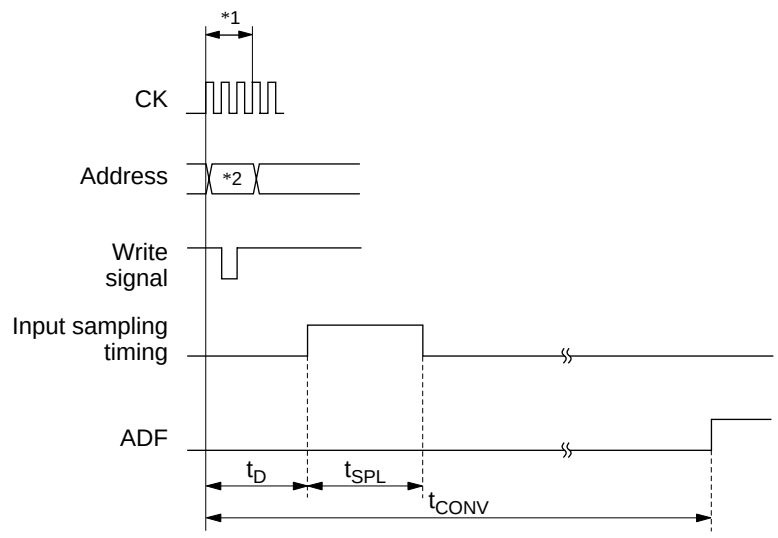
Figure 14.4 A/D Operation in Scan Mode (Channels 0–2 Selected)

14.4.3 Input Sampling Time and A/D Conversion Time

With a built-in sample-and-hold circuit, the A/D converter performs input sampling at time t_D after control/status register (ADSCR) access is started. See figure 14.5 for A/D conversion timing and table 14.4 for A/D conversion times.

The total conversion time includes t_D and the input sampling time, as shown in figure 14.5. The purpose of t_D is to synchronize the ADCSR write time with the A/D conversion process; therefore the duration of t_D is variable. As a result, the total conversion time varies within the ranges shown in table 14.4.

In scan mode, the ranges given in table 14.4 apply to the first conversion. The duration of the second and subsequent conversion processes is fixed at 256 states (CKS = 0) or 128 states (CKS = 1).



t_D A/D start delay
t_{SPL} Input sampling time
t_{CONV} A/D conversion time
Notes: 1. ADSCR write cycle
2. ADSCR address

Figure 14.5 A/D Conversion Timing

Table 14.4 A/D Conversion Time (Single Mode)

		CKS = 0			CKS = 1		
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
A/D start delay	t_D	10	—	17	6	—	9
Input sampling time	t_{SPL}	—	64	—	—	32	—
Total A/D conversion time	t_{CONV}	259	—	266	131	—	134

Note: Values are the number of states (tcyc).

14.4.4 A/D Conversion Start by External Trigger Input

The A/D converter can be started when an external trigger is input. The external trigger is input from the $\overline{\text{ADTRG}}$ input pin when the trigger enable (TRGE) bit in the A/D control register (ADCR) is set to 1. When the $\overline{\text{ADTRG}}$ input pin is asserted low, the A/D start (ADST) bit in the A/D control/status register (ADCSR) is set to 1 and A/D conversion begins. All other operations are the same as when the ADST bit is set to 1, regardless of whether the mode is single or scan. For the timing, see figure 14.6.

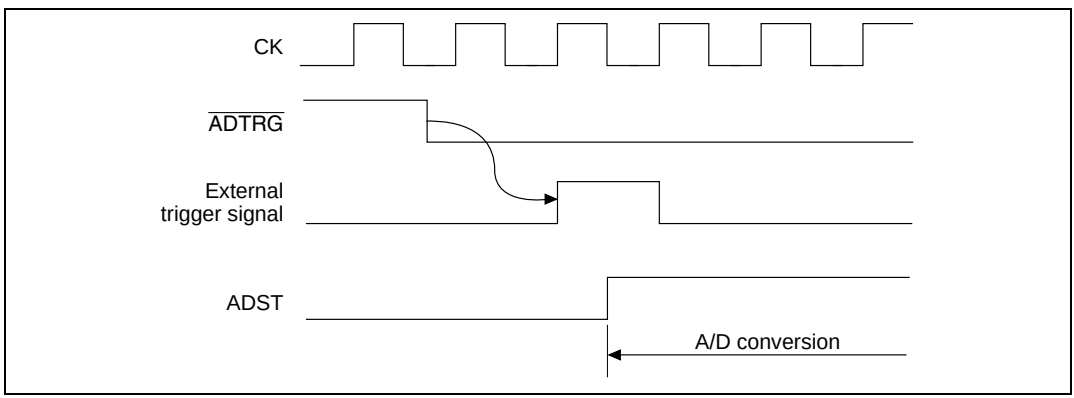


Figure 14.6 External Trigger Input Timing

14.5 Interrupts and DMA Transfer Requests

The A/D converter can generate an A/D interrupt (ADI) request at the end of conversion. The ADI request is enabled by setting the ADIE bit in ADCSR to 1, or is disabled by clearing the bit to 0. When ADI is generated, the DMAC can be started. DMA transfers can be performed by requesting an ADI interrupt by setting the resource select bits (RS3–RS0) in the DMA channel control register (CHCR) of the direct memory access controller (DMAC). The ADF bit in the A/D control/status register (ADCSR) is automatically cleared to 0 when the DMAC accesses an A/D converter register.

14.6 Definitions of A/D Conversion Accuracy

The A/D converter compares an analog value input from an analog input channel to its analog reference value and converts it into 10-bit digital data. The absolute accuracy of this A/D conversion is the deviation between the input analog value and the output digital value. It includes the following errors:

- Offset error
- Full-scale error
- Quantization error
- Nonlinearity error

These four error quantities are explained below using figure 14.7. In the figure, the 10 bits of the A/D converter have been simplified to 3 bits.

Offset error is the deviation between actual and ideal A/D conversion characteristics when the digital output value changes from the minimum (zero voltage) 0000000000 (000 in the figure) to 000000001 (001 in the figure)(figure 14.7, item (1)). Full-scale error is the deviation between actual and ideal A/D conversion characteristics when the digital output value changes from 1111111110 (110 in the figure) to the maximum 1111111111 (111 in the figure)(figure 14.7, item (2)). Quantization error is the intrinsic error of the A/D converter and is expressed as 1/2 LSB (figure 14.7, item (3)). Nonlinearity error is the deviation between actual and ideal A/D conversion characteristics between zero voltage and full-scale voltage (figure 14.7, item (4)). Note that it does not include offset, full-scale, or quantization error.

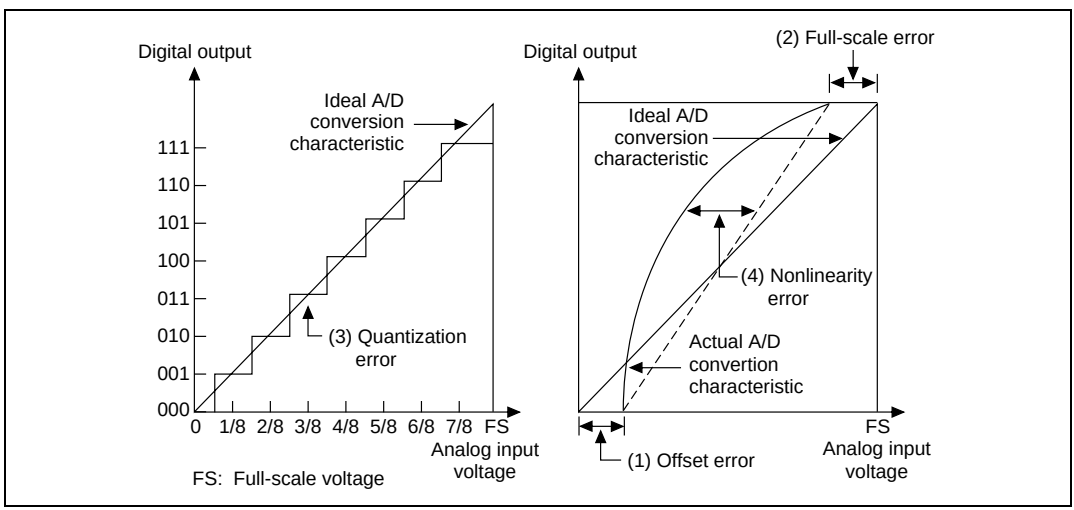


Figure 14.7 Definitions of A/D Conversion Accuracy

14.7 A/D Converter Usage Notes

When using the A/D converter, note the points listed in section 14.7.1 below.

14.7.1 Setting Analog Input Voltage

- Analog Input Voltage Range: During A/D conversion, the voltages input to the analog input pins ANn should be in the range $AV_{SS} \leq ANn \leq AV_{ref}$.
- Relationships of AV_{CC} and AV_{SS} to V_{CC} and V_{SS}: AV_{CC}, AV_{SS}, V_{CC} and V_{SS} should be related as follows: $AV_{CC} = V_{CC} \pm 10\%$ and $AV_{SS} = V_{SS}$. If the A/D converter is not used, set $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$.
- AV_{ref} Input Range: The analog reference voltage input at the AV_{ref} pin should be in the range $AV_{ref} \leq AV_{CC}$. If the converter is not used, set $AV_{ref} = V_{CC}$.
- When the converter is neither in use nor in standby mode, connect AV_{CC} and AV_{ref} to the power voltage (V_{CC}).

14.7.2 Handling of Analog Input Pins

To prevent damage from voltage surges at the analog input pins (AN0–AN7), connect an input protection circuit like the one shown in figure 14.8. The circuit shown also includes an RC filter to prevent errors due to noise. This circuit is shown as an example: The circuit constants should be selected according to actual application conditions. Table 14.5 list the analog input pin specifications and figure 14.9 shows an equivalent circuit diagram of the analog input ports.

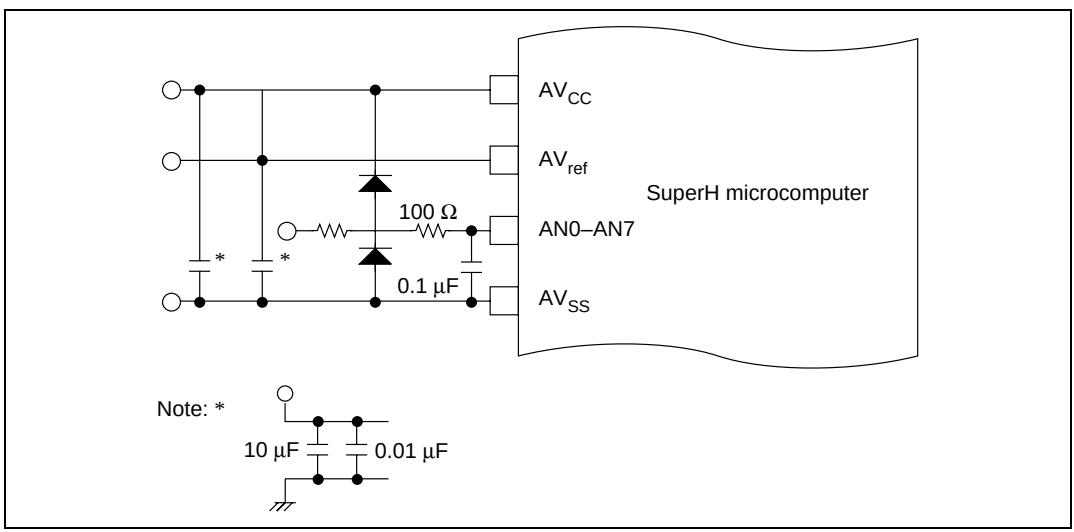
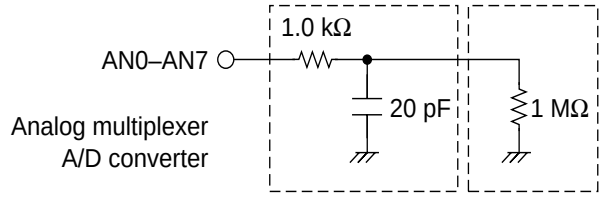


Figure 14.8 Example of Analog Input Protection Circuit



Note: All figures are reference values.

Figure 14.9 Analog Input Pin Equivalent Circuit

Table 14.5 Analog Input Pin Ratings

Item	Min	Max	Unit
Analog input capacitance	—	20	pF
Allowable signal-source impedance	—	3	kΩ

14.7.3 Switchover between Analog Input and General Port Functions

1. Switchover to/from general port function

   When the A/D converter is started by setting the A/D start bit (ADST) to 1 in the A/D control/status register (ADCSR), or by asserting the $\overline{\text{ADTRG}}$ pin, port C pins begin functioning as analog input pins (ANn). When A/D conversion ends, the pins are switched back to the general port (digital input) function.
2. Port C pins not used for A/D conversion

   Pins not selected as AN pins by the channel select setting can be used in the following combinations as general port pins in both single mode and scan mode.
   a. When any or all of pins AN0 to AN3 are used for A/D conversion, AN4 to AN7 can be used as general port pins.
   b. When any or all of pins AN4 to AN7 are used for A/D conversion, AN0 to AN3 can be used as general port pins.

Section 15 Pin Function Controller (PFC)

15.1 Overview

The pin function controller (PFC) is composed of registers for selecting the function of multiplexed pins and the direction of input/output. The pin function and input/output direction can be selected for each pin individually without regard to the operating mode of the chip. Table 15.1 lists the multiplexed pins.

Table 15.1 List of Multiplexed Pins

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Pin No. (PRQP0112 JA-A)	Pin No. (PTQP0120 LA-A)
A	PA15 I/O (port)	$\overline{\text{IRQ3}}$ input (INTC)	$\overline{\text{DREQ1}}$ input (DMAC)	—	69	74
A*3	PA14 I/O (port)	$\overline{\text{IRQ2}}$ input (INTC)	DACK1 output (DMAC)	—	68	73
A	PA13 I/O (port)	$\overline{\text{IRQ1}}$ input (INTC)	TCLKB input (ITU)	$\overline{\text{DREQ0}}$ input (DMAC)	67	72
A*3	PA12 I/O (port)	$\overline{\text{IRQ0}}$ input (INTC)	TCLKA input (ITU)	DACK0 output (DMAC)	66	71
A	PA11 I/O (port)	DPH I/O (D bus)	TIOCB1 I/O (ITU)	—	65	70
A	PA10 I/O (port)	DPL I/O (D bus)	TIOCA1 I/O (ITU)	—	64	69
A	PA9 I/O (port)	$\overline{\text{AH}}$ output (BSC)	$\overline{\text{ADTRG}}$ input (A/D)	$\overline{\text{IRQOUT}}$ output (INTC)	63	68
A	PA8 I/O (port)	$\overline{\text{BREQ}}$ input (system)	—	—	62	67
A	PA7 I/O (port)	$\overline{\text{BACK}}$ output (system)	—	—	60	65
A	PA6 I/O (port)	$\overline{\text{RD}}$ output (BSC)	—	—	59	64
A	PA5 I/O (port)	$\overline{\text{WRH}}$ output (BSC) ($\overline{\text{LBS}}$ output (BSC))*1	—	—	58	63
A	PA4 I/O (port)	$\overline{\text{WRL}}$ output (BSC) ($\overline{\text{WR}}$ output (BSC))*1	—	—	57	62
A	PA3 I/O (port)	$\overline{\text{CS7}}$ output (BSC)	$\overline{\text{WAIT}}$ input (BSC)	—	56	59
A	PA2 I/O (port)	$\overline{\text{CS6}}$ output (BSC)	TIOCB0 I/O (ITU)	—	55	58
A	PA1 I/O (port)	$\overline{\text{CS5}}$ output (BSC)	$\overline{\text{RAS}}$ output (BSC)	—	54	57
A	PA0 I/O (port)	$\overline{\text{CS4}}$ output (BSC)	TIOCA0 I/O (ITU)	—	53	56
B	PB15 I/O (port)	$\overline{\text{IRQ7}}$ input (INTC)	—	TP15 output (TPC)	2	3
B	PB14 I/O (port)	$\overline{\text{IRQ6}}$ input (INTC)	—	TP14 output (TPC)	1	2
B	PB13 I/O (port)	$\overline{\text{IRQ5}}$ input (INTC)	SCK1 I/O (SCI)	TP13 output (TPC)	112	119
B	PB12 I/O (port)	$\overline{\text{IRQ4}}$ input (INTC)	SCK0 I/O (SCI)	TP12 output (TPC)	111	118
B	PB11 I/O (port)	TxD1 output (SCI)	TP11 output (TPC)	—	110	117
B	PB10 I/O (port)	RxD1 input (SCI)	TP10 output (TPC)	—	109	116

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Pin No. (PRQP0112 JA-A)	Pin No. (PTQP0120 LA-A)
B	PB9 I/O (port)	TxD0 output (SCI)	TP9 output (TPC)	—	108	115
B	PB8 I/O (port)	RxD0 input (SCI)	TP8 output (TPC)	—	107	114
B	PB7 I/O (port)	TCLKD input (ITU)	TOCXB4 output (ITU)	TP7 output (TPC)	105	112
B	PB6 I/O (port)	TCLKC input (ITU)	TOCXA4 output (ITU)	TP6 output (TPC)	104	111
B	PB5 I/O (port)	TIOCB4 I/O (ITU)	TP5 output (TPC)	—	103	110
B	PB4 I/O (port)	TIOCA4 I/O (ITU)	TP4 output (TPC)	—	102	109
B	PB3 I/O (port)	TIOCB3 I/O (ITU)	TP3 output (TPC)	—	101	108
B	PB2 I/O (port)	TIOCA3 I/O (ITU)	TP2 output (TPC)	—	100	107
B	PB1 I/O (port)	TIOCB2 I/O (ITU)	TP1 output (TPC)	—	98	105
B	PB0 I/O (port)	TIOCA2 I/O (ITU)	TP0 output (TPC)	—	97	103
C*2	PC7 input (port)	AN7 input (A/D)	—	—	95	101
C*2	PC6 input (port)	AN6 input (A/D)	—	—	94	100
C*2	PC5 input (port)	AN5 input (A/D)	—	—	93	99
C*2	PC4 input (port)	AN4 input (A/D)	—	—	92	98
C*2	PC3 input (port)	AN3 input (A/D)	—	—	90	96
C*2	PC2 input (port)	AN2 input (A/D)	—	—	89	95
C*2	PC1 input (port)	AN1 input (A/D)	—	—	88	94
C*2	PC0 input (port)	AN0 input (A/D)	—	—	87	93
—	$\overline{\text{CS1}}$ output (BSC)	$\overline{\text{CASH}}$ output (BSC)	—	—	49	52
—	$\overline{\text{CS3}}$ output (BSC)	$\overline{\text{CASL}}$ output (BSC)	—	—	51	54

INTC: Interrupt controller

DMAC: Direct memory access controller

ITU: 16-bit integrated timer pulse unit

D bus: Data bus control

BSC: Bus state controller

System: System control

A/D: A/D converter

SCI: Serial communication interface

TPC: Programmable timing pattern controller

Port: I/O port

Notes: 1. The bus control register of the bus state controller handles switching between the two functions.

2. The function of port C pins automatically changes to analog input (AN0–AN7) when the A/D converter begins to operate.

3. The initial setting is DACK (output).

15.2 Register Configuration

Table 15.2 summarizes the registers of the pin function controller.

Table 15.2 Pin Function Controller Registers

Name	Abbreviation	R/W	Initial Value	Address*	Access Size
Port A I/O register	PAIOR	R/W	H'0000	H'5FFFFC4	8, 16, 32
Port A control register 1	PACR1	R/W	H'3302	H'5FFFFC8	8, 16, 32
Port A control register 2	PACR2	R/W	H'FF95	H'5FFFFCA	8, 16, 32
Port B I/O register	PBIOR	R/W	H'0000	H'5FFFFC6	8, 16, 32
Port B control register 1	PBCR1	R/W	H'0000	H'5FFFFCC	8, 16, 32
Port B control register 2	PBCR2	R/W	H'0000	H'5FFFFCE	8, 16, 32
Column address strobe pin control register	CASCR	R/W	H'5FFF	H'5FFFFEE	8, 16, 32

Note: * Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.

15.3 Register Descriptions

15.3.1 Port A I/O Register (PAIOR)

The port A I/O register (PAIOR) is a 16-bit read/write register that selects input or output for the 16 pins of port A. Bits PA15IOR–PA0IOR correspond to pins PA15/$\overline{\text{IRQ3}}$/$\overline{\text{DREQ1}}$–PA0/$\overline{\text{CS4}}$/TIOCA0. PAIOR is enabled when the port A pins function as input/outputs (PA15–PA0) and for ITU input capture and output compare (TIOCA1, TIOCA0, TIOCB1, and TIOCB0).

For other functions, they are disabled. For port A pin functions PA15–PA0 and TIOCA1, TIOCA0, TIOCB1, and TIOCB0, a given pin in port A is an output pin if its corresponding PAIOR bit is set to 1, and an input pin if the bit is cleared to 0.

PAIOR is initialized to H'0000 by a power-on reset; however, it is not initialized by a manual reset, or in standby mode or sleep mode.

Bit	15	14	13	12	11	10	9	8
	PA15 IOR	PA14 IOR	PA13 IOR	PA12 IOR	PA11 IOR	PA10 IOR	PA9 IOR	PA8 IOR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PA7 IOR	PA6 IOR	PA5 IOR	PA4 IOR	PA3 IOR	PA2 IOR	PA1 IOR	PA0 IOR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.3.2 Port A Control Registers (PACR1 and PACR2)

PACR1 and PACR2 are 16-bit read/write registers that select the functions of the sixteen multiplexed pins of port A. PACR1 selects the function of the upper eight bits of port A; PACR2 selects the function of the lower eight bits of port A. PACR1 and PACR2 are initialized to H'3302 and H'FF95 respectively by a power-on reset but are not initialized by a manual reset, or in standby mode or sleep mode.

PACR1:

Bit	15	14	13	12	11	10	9	8
	PA15 MD1	PA15 MD0	PA14 MD1	PA14 MD0	PA13 MD1	PA13 MD0	PA12 MD1	PA12 MD0
Initial value	0	0	1	1	0	0	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PA11 MD1	PA11 MD0	PA10 MD1	PA10 MD0	PA9 MD1	PA9 MD0	—	PA8 MD
Initial value	0	0	0	0	0	0	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	—	R/W

Bits 15 and 14—PA15 Mode (PA15MD1 and PA15MD0): PA15MD1 and PA15MD0 select the function of the PA15/$\overline{\text{IRQ3}}$/$\overline{\text{DREQ1}}$ pin.

Bit 15: PA15MD1	Bit 14: PA15MD0	Function	
0	0	Input/output (PA15)	(Initial value)
	1	Interrupt request input ($\overline{\text{IRQ3}}$)	
1	0	Reserved	
	1	DMA transfer request input ($\overline{\text{DREQ1}}$)	

Bits 13 and 12—PA14 Mode (PA14MD1 and PA14MD0): PA14MD1 and PA14MD0 select the function of the PA14/$\overline{\text{IRQ2}}$/DACK1 pin.

Bit 13: PA14MD1	Bit 12: PA14MD0	Function	
0	0	Input/output (PA14)	
	1	Interrupt request input ($\overline{\text{IRQ2}}$)	
1	0	Reserved	
	1	DMA transfer acknowledge output (DACK1)	(Initial value)

Bits 11 and 10—PA13 Mode (PA13MD1 and PA13MD0): PA13MD1 and PA13MD0 select the function of the PA13/$\overline{\text{IRQ1}}$/$\overline{\text{DREQ0}}$/TCLKB pin.

Bit 11: PA13MD1	Bit 10: PA13MD0	Function	
0	0	Input/output (PA13)	(Initial value)
	1	Interrupt request input ($\overline{\text{IRQ1}}$)	
1	0	ITU timer clock input (TCLKB)	
	1	DMA transfer request input ($\overline{\text{DREQ0}}$)	

Bits 9 and 8—PA12 Mode (PA12MD1 and PA12MD0): PA12MD1 and PA12MD0 select the function of the PA12/$\overline{\text{IRQ0}}$/DACK0/TCLKA pin.

Bit 9: PA12MD1	Bit 8: PA12MD0	Function	
0	0	Input/output (PA12)	
	1	Interrupt request input ($\overline{\text{IRQ0}}$)	
1	0	ITU timer clock input (TCLKA)	
	1	DMA transfer acknowledge output (DACK0)	(Initial value)

Bits 7 and 6—PA11 Mode (PA11MD1 and PA11MD0): PA11MD1 and PA11MD0 select the function of the PA11/DPH/TIOCB1 pin.

Bit 7: PA11MD1	Bit 6: PA11MD0	Function	
0	0	Input/output (PA11)	(Initial value)
	1	Upper data bus parity input/output (DPH)	
1	0	ITU input capture/output compare (TIOCB1)	
	1	Reserved	

Bits 5 and 4—PA10 Mode (PA10MD1 and PA10MD0): PA10MD1 and MA10MD0 select the function of the PA10/DPL/TIOCA1 pin.

Bit 5: PA10MD1	Bit 4: PA10MD0	Function	
0	0	Input/output (PA10)	(Initial value)
	1	Lower data bus parity input/output (DPL)	
1	0	ITU input capture/output compare (TIOCA1)	
	1	Reserved	

Bits 3 and 2—PA9 Mode (PA9MD1 and PA9MD0): PA9MD1 and PA9MD0 select the function of the PA9/$\overline{\text{AH}}$/IRQOUT/$\overline{\text{ADTRG}}$ pin.

Bit 3: PA9MD1	Bit 2: PA9MD0	Function	
0	0	Input/output (PA9)	(Initial value)
	1	Address hold output ($\overline{\text{AH}}$)	
1	0	A/D conversion trigger input ($\overline{\text{ADTRG}}$)	
	1	Interrupt request output ($\overline{\text{IRQOUT}}$)	

Bit 1—Reserved: This bit is always read as 1. The write value should always be 1.

Bit 0—PA8 Mode (PA8MD): PA8MD selects the function of the PA8/$\overline{\text{BREQ}}$ pin.

Bit 0: PA8MD	Function	
0	Input/output (PA8)	(Initial value)
1	Bus request input ($\overline{\text{BREQ}}$)	

PACR2:

Bit	15	14	13	12	11	10	9	8
	—	PA7MD	—	PA6MD	—	PA5MD	—	PA4MD
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	R/W	—	R/W	—	R/W	—	R/W

Bit	7	6	5	4	3	2	1	0
	PA3MD1	PA3MD0	PA2MD1	PA2MD0	PA1MD1	PA1MD0	PA0MD1	PA0MD0
Initial value	1	0	0	1	0	1	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 15—Reserved: This bit is always read as 1. The write value should always be 1.

Bit 14—PA7 Mode (PA7MD): PA7MD selects the function of the PA7/$\overline{\text{BACK}}$ pin.

Bit 14: PA7MD	Function	
0	Input/output (PA7)	
1	Bus request acknowledge output ($\overline{\text{BACK}}$)	(Initial value)

Bit 13—Reserved: This bit is always read as 1. The write value should always be 1.

Bit 12—PA6 Mode (PA6MD): PA6MD selects the function of the PA6/$\overline{\text{RD}}$ pin.

Bit 12: PA6MD	Function	
0	Input/output (PA6)	
1	Read output ($\overline{\text{RD}}$)	(Initial value)

Bit 11—Reserved: This bit is always read as 1. The write value should always be 1.

Bit 10—PA5 Mode (PA5MD): PA5MD selects the function of the PA5/$\overline{\text{WRH}}$ ($\overline{\text{LBS}}$) pin.

Bit 10: PA5MD	Function	
0	Input/output (PA5)	
1	Upper write output ($\overline{\text{WRH}}$) or lower byte strobe output ($\overline{\text{LBS}}$)	(Initial value)

Bit 9—Reserved: This bit is alway read as 1. The write value should always be 1.

Bit 8—PA4 Mode (PA4MD): PA4MD selects the function of the PA4/$\overline{\text{WRL}}$ ($\overline{\text{WR}}$) pin.

Bit 8: PA4MD	Function	
0	Input/output (PA4)	
1	Lower write output ($\overline{\text{WRL}}$) or write output ($\overline{\text{WR}}$)	(Initial value)

Bits 7 and 6—PA3 Mode (PA3MD1 and PA3MD0): PA3MD1 and PA3MD0 select the function of the PA3/$\overline{\text{CS7}}$/$\overline{\text{WAIT}}$ pin. This pin has a pull-up MOS that is used when it functions as a $\overline{\text{WAIT}}$ pin to allow selection of pull-up or no pull-up (for the $\overline{\text{WAIT}}$ pin) using the wait state control register of the bus state controller (BSC). There is no pull-up when it functions as PA3 or $\overline{\text{CS7}}$.

Bit 7: PA3MD1	Bit 6: PA3MD0	Function	
0	0	Input/output (PA3)	
	1	Chip select output ($\overline{\text{CS7}}$)	
1	0	Wait state input ($\overline{\text{WAIT}}$)	(Initial value)
	1	Reserved	

Bits 5 and 4—PA2 Mode (PA2MD1 and PA2MD0): PA2MD1 and PA2MD0 select the function of the PA2/$\overline{\text{CS6}}$/TIOCB0 pin.

Bit 5: PA2MD1	Bit 4: PA2MD0	Function	
0	0	Input/output (PA2)	
	1	Chip select output ($\overline{\text{CS6}}$)	(Initial value)
1	0	ITU input capture/output compare (TIOCB0)	
	1	Reserved	

Bits 3 and 2—PA1 Mode (PA1MD1 and PA1MD0): PA1MD1 and PA1MD0 select the function of the PA1/$\overline{\text{CS5}}$/$\overline{\text{RAS}}$ pin.

Bit 3: PA1MD1	Bit 2: PA1MD0	Function	
0	0	Input/output (PA1)	
	1	Chip select output ($\overline{\text{CS5}}$)	(Initial value)
1	0	Row address strobe output ($\overline{\text{RAS}}$)	
	1	Reserved	

Bits 1 and 0—PA0 Mode (PA0MD1 and PA0MD0): PA0MD1 and PA0MD0 select the function of the PA0/$\overline{CS4}$/TIOCA0 pin.

Bit 1: PA0MD1	Bit 0: PA0MD0	Function	
0	0	Input/output (PA0)	
	1	Chip select output ($\overline{CS4}$)	(Initial value)
1	0	ITU input capture/output compare (TIOCA0)	
	1	Reserved	

15.3.3 Port B I/O Register (PBIOR)

The port A I/O register (PAIOR) is a 16-bit read/write register that selects input or output for the 16 pins of port A. Bits PB15IOR–PB0IOR correspond to pins of port B. PBIOR is enabled when the port B pins function as input/outputs (PB15–PB0), for ITU input capture and output compare (TIOCA4, TIOCA3, TIOCA2, TIOCB4, TIOCB3, and TIOCB2), and as serial clocks (SCK1, SCK0). For other functions, they are disabled. For port B pin functions PB15–PB0, and TIOCA4, TIOCA3, TIOCA2, TIOCB4, TIOCB3, and TIOCB2, and SCK1/SCK0, a given pin in port B is an output pin if its corresponding PBIOR bit is set to 1, and an input pin if the bit is cleared to 0.

PBIOR is initialized to H'0000 by a power-on reset; however, it is not initialized by a manual reset, or in standby mode or sleep mode.

Bit	15	14	13	12	11	10	9	8
	PB15 IOR	PB14 IOR	PB13 IOR	PB12 IOR	PB11 IOR	PB10 IOR	PB9 IOR	PB8 IOR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB7 IOR	PB6 IOR	PB5 IOR	PB4 IOR	PB3 IOR	PB2 IOR	PB1 IOR	PB0 IOR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.3.4 Port B Control Registers (PBCR1 and PBCR2)

PBCR1 and PBCR2 are 16-bit read/write registers that select the functions of the sixteen multiplexed pins of port B. PBCR1 selects the function of the upper eight bits of port B; PBCR2 selects the function of the lower eight bits of port B. PBCR1 and PBCR2 are initialized to H'0000 by a power-on reset, but are not initialized by a manual reset, or in standby mode or sleep mode.

PBCR1:

Bit	15	14	13	12	11	10	9	8
	PB15 MD1	PB15 MD0	PB14 MD1	PB14 MD0	PB13 MD1	PB13 MD0	PB12 MD1	PB12 MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB11 MD1	PB11 MD0	PB10 MD1	PB10 MD0	PB9 MD1	PB9 MD0	PB8 MD1	PB8 MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 15 and 14—PB15 Mode (PB15MD1 and PB15MD0): PB15MD1 and PB15MD0 select the function of the PB15/TP15/$\overline{\text{IRQ7}}$ pin.

Bit 15: PB15MD1	Bit 14: PB15MD0	Function	
0	0	Input/output (PB15)	(Initial value)
	1	Interrupt request input ($\overline{\text{IRQ7}}$)	
1	0	Reserved	
	1	Timing pattern output (TP15)	

Bits 13 and 12—PB14 Mode (PB14MD1 and PB14MD0): PB14MD1 and PB14MD0 select the function of the PB14/TP14/$\overline{\text{IRQ6}}$ pin.

Bit 13: PB14MD1	Bit 12: PB14MD0	Function	
0	0	Input/output (PB14)	(Initial value)
	1	Interrupt request input ($\overline{\text{IRQ6}}$)	
1	0	Reserved	
	1	Timing pattern output (TP14)	

Bits 11 and 10—PB13 Mode (PB13MD1 and PB13MD0): PB13MD1 and PB13MD0 select the function of the PB13/TP13/$\overline{\text{IRQ5}}$/SCK1 pin.

Bit 11: PB13MD1	Bit 10: PB13MD0	Function	
0	0	Input/output (PB13)	(Initial value)
	1	Interrupt request input ($\overline{\text{IRQ5}}$)	
1	0	Serial clock input/output (SCK1)	
	1	Timing pattern output (TP13)	

Bits 9 and 8—PB12 Mode (PB12MD1 and PB12MD0): PB12MD1 and PB12MD0 select the function of the PB12/TP12/$\overline{\text{IRQ4}}$/SCK0 pin.

Bit 9: PB12MD1	Bit 8: PB12MD0	Function	
0	0	Input/output (PB12)	(Initial value)
	1	Interrupt request input ($\overline{\text{IRQ4}}$)	
1	0	Serial clock input/output (SCK0)	
	1	Timing pattern output (TP12)	

Bits 7 and 6: PB11 Mode—PB11MD1 and PB11MD0): PB11MD1 and PB11MD0 select the function of the PB11/TP11/TxD1 pin.

Bit 7: PB11MD1	Bit 6: PB11MD0	Function	
0	0	Input/output (PB11)	(Initial value)
	1	Reserved	
1	0	Transmit data output (TxD1)	
	1	Timing pattern output (TP11)	

Bits 5 and 4—PB10 Mode (PB10MD1 and PB10MD0): PB10MD1 and PB10MD0 select the function of the PB10/TP10/RxD1 pin.

Bit 5: PB10MD1	Bit 4: PB10MD0	Function	
0	0	Input/output (PB10)	(Initial value)
	1	Reserved	
1	0	Receive data input (RxD1)	
	1	Timing pattern output (TP10)	

Bits 3 and 2—PB9 Mode (PB9MD1 and PB9MD0): PB9MD1 and PB9MD0 select the function of the PB9/TP9/TxD0 pin.

Bit 3: PB9MD1	Bit 2: PB9MD0	Function	
0	0	Input/output (PB9)	(Initial value)
	1	Reserved	
1	0	Transmit data output (TxD0)	
	1	Timing pattern output (TP9)	

Bits 1 and 0—PB8 Mode (PB8MD1 and PB8MD0): PB8MD1 and PB8MD0 select the function of the PB8/TP8/RxD0 pin.

Bit 1: PB8MD1	Bit 0: PB8MD0	Function	
0	0	Input/output (PB8)	(Initial value)
	1	Reserved	
1	0	Receive data input (RxD0)	
	1	Timing pattern output (TP8)	

PBCR2:

Bit	15	14	13	12	11	10	9	8
	PB7MD1	PB7MD0	PB6MD1	PB6MD0	PB5MD1	PB5MD0	PB4MD1	PB4MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB3MD1	PB3MD0	PB2MD1	PB2MD0	PB1MD1	PB1MD0	PB0MD1	PB0MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 15 and 14—PB7 Mode (PB7MD1 and PB7MD0): PB7MD1 and PB7MD0 select the function of the PB7/TP7/TOCXB4/TCLKD pin.

Bit 15: PB7MD1	Bit 14: PB7MD0	Function	
0	0	Input/output (PB7)	(Initial value)
	1	ITU timer clock input (TCLKD)	
1	0	ITU output compare (TOCXB4)	
	1	Timing pattern output (TP7)	

Bits 13 and 12—PB6 Mode (PB6MD1 and PB6MD0): PB6MD1 and PB6MD0 select the function of the PB6/TP6/TOCXA4/TCLKC pin.

Bit 13: PB6MD1	Bit 12: PB6MD0	Function	
0	0	Input/output (PB6)	(Initial value)
	1	ITU timer clock input (TCLKC)	
1	0	ITU output compare (TOCXA4)	
	1	Timing pattern output (TP6)	

Bits 11 and 10—PB5 Mode (PB5MD1 and PB5MD0): PB5MD1 and PB5MD0 select the function of the PB5/TP5/TIOCB4 pin.

Bit 11: PB5MD1	Bit 10: PB5MD0	Function	
0	0	Input/output (PB5)	(Initial value)
	1	Reserved	
1	0	ITU input capture/output compare (TIOCB4)	
	1	Timing pattern output (TP5)	

Bits 9 and 8—PB4 Mode (PB4MD1 and PB4MD0): PB4MD1 and PB4MD0 select the function of the PB4/TP4/TIOCA4 pin.

Bit 9: PB4MD1	Bit 8: PB4MD0	Function	
0	0	Input/output (PB4)	(Initial value)
	1	Reserved	
1	0	ITU input capture/output compare (TIOCA4)	
	1	Timing pattern output (TP4)	

Bits 7 and 6—PB3 Mode (PB3MD1 and PB3MD0): PB3MD1 and PB3MD0 select the function of the PB3/TP3/TIOCB3 pin.

Bit 7: PB3MD1	Bit 6: PB3MD0	Function	
0	0	Input/output (PB3)	(Initial value)
	1	Reserved	
1	0	ITU input capture/output compare (TIOCB3)	
	1	Timing pattern output (TP3)	

Bits 5 and 4—PB2 Mode (PB2MD1 and PB2MD0): PB2MD1 and PB2MD0 select the function of the PB2/TP2/TIOCA3 pin.

Bit 5: PB2MD1	Bit 4: PB2MD0	Function	
0	0	Input/output (PB2)	(Initial value)
	1	Reserved	
1	0	ITU input capture/output compare (TIOCA3)	
	1	Timing pattern output (TP2)	

Bits 3 and 2—PB1 Mode (PB1MD1 and PB1MD0): PB1MD1 and PB1MD0 select the function of the PB1/TP1/TIOCB2 pin.

Bit 3: PB1MD1	Bit 2: PB1MD0	Function	
0	0	Input/output (PB1)	(Initial value)
	1	Reserved	
1	0	ITU input capture/output compare (TIOCB2)	
	1	Timing pattern output (TP1)	

Bits 1 and 0—PB0 Mode (PB0MD1 and PB0MD0): PB0MD1 and PB0MD0 select the function of the PB0/TP0/TIOCA2 pin.

Bit 1: PB0MD1	Bit 0: PB0MD0	Function	
0	0	Input/output (PB0)	(Initial value)
	1	Reserved	
1	0	ITU input capture/output compare (TIOCA2)	
	1	Timing pattern output (TP0)	

15.3.5 Column Address Strobe Pin Control Register (CASCR)

CASCR is a 16-bit read/write register that allows selection between column address strobe and chip select pin functions. CASCR is initialized to H'5FFF by a power-on reset, but is not initialized by a manual reset, or in standby mode or sleep mode.

Bit	15	14	13	12	11	10	9	8
	CASH MD1	CASH MD0	CASL MD1	CASL MD0	—	—	—	—
Initial value	0	1	0	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

Bits 15 and 14—CASH Mode (CASHMD1 and CASHMD0): CASHMD1 and CASHMD0 select the function of the $\overline{CS1}$/$\overline{CASH}$ pin.

Bit 15: CASHMD1	Bit 14: CASHMD0	Function	
0	0	Reserved	
	1	Chip select output ($\overline{CS1}$)	(Initial value)
1	0	Column address strobe output ($\overline{CASH}$)	
	1	Reserved	

Bits 13 and 12—CASL Mode (CASLMD1 and CASLMD0): CASLMD1 and CASLMD0 select the function of the $\overline{CS3}$/$\overline{CASL}$ pin.

Bit 13: CASLMD1	Bit 12: CASLMD0	Function	
0	0	Reserved	
	1	Chip select output ($\overline{CS3}$)	(Initial value)
1	0	Column address strobe output ($\overline{CASL}$)	
	1	Reserved	

Bits 11–0—Reserved: These bits are always read as 1. The write value should always be 1.

Section 16 I/O Ports (I/O)

16.1 Overview

There are three ports, A, B, and C. Ports A and B are 16-bit I/O ports, while port C is an 8-bit input port. The pins of the ports are all multiplexed for use as general-purpose I/Os (or inputs in the case of port C) or for other functions. (Use the pin function controller (PFC) to select the function of multiplexed pins.) Ports A, B, and C each have one data register for storing pin data.

16.2 Port A

Port A is a 16-pin input/output port, as shown in figure 16.1. The PA3/$\overline{CS7}$/$\overline{WAIT}$ pin of port A has a pull-up MOS so that when it is functioning as a $\overline{WAIT}$ pin, the wait state control register of the bus state controller can be used to select whether to pull up the $\overline{WAIT}$ pin or not. It is not pulled up when the pin is functioning as either PA3 or $\overline{CS7}$.

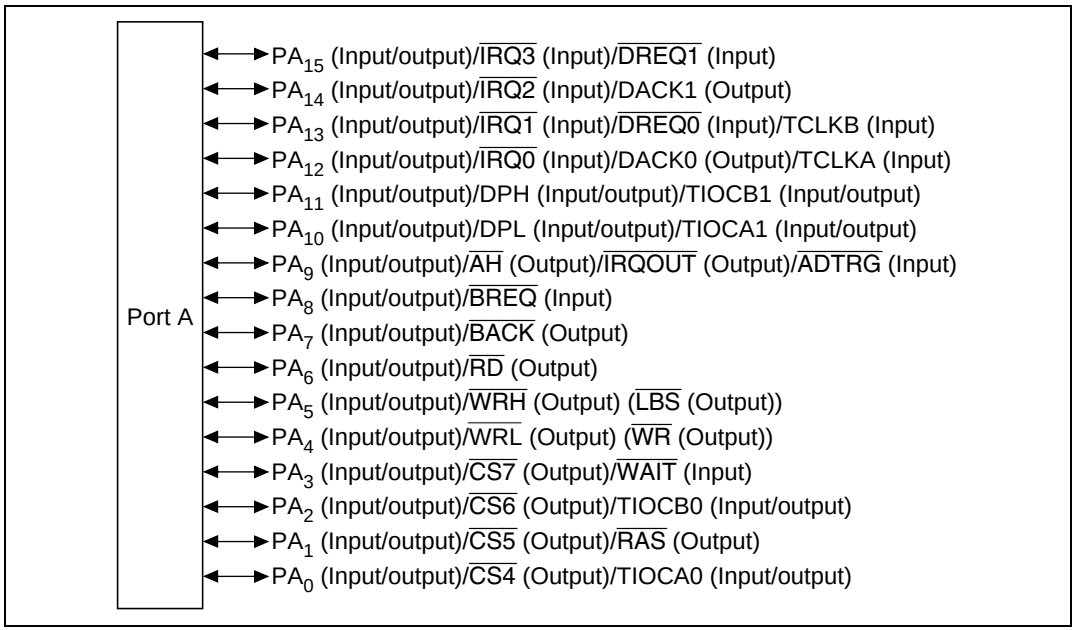


Figure 16.1 Port A Configuration

16.2.1 Register Configuration

Table 16.1 summarizes the port A register.

Table 16.1 Port A Register

Name	Abbreviation	R/W	Initial Value	Address*	Access Size
Port A data register	PADR	R/W	H'0000	H'5FFFFC0	8, 16, 32

Note: * Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.

16.2.2 Port A Data Register (PADR)

PADR is a 16-bit read/write register that stores data for port A. Bits PA15DR–PA0DR correspond to the PA15/$\overline{\text{IRQ3}}$/$\overline{\text{DREQ1}}$–PA0/$\overline{\text{CS4}}$/TIOCA0 pins. When the pins are used as ordinary outputs, they will output whatever value is written in PADR; when PADR is read, the register value will be output regardless of the pin status. When the pins are used as ordinary inputs, the pin status rather than the register value is read directly when PADR is read. When a value is written to PADR, that value can be written into PADR, but it will not affect the pin status. Table 16.2 shows port A data register read/write operations.

PADR is initialized by a power-on reset. However, PADR is not initialized by a manual reset, or in standby mode or sleep mode.

Bit	15	14	13	12	11	10	9	8
	PA15DR	PA14DR	PA13DR	PA12DR	PA11DR	PA10DR	PA9DR	PA8DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 16.2 Port A Data Register (PADR) Read/Write Operations

PAIOR	Pin Status	Read	Write
0	Input	Pin status	Can write to PADR, but it has no effect on pin status.
	Other function	Pin status	Can write to PADR, but it has no effect on pin status.
1	Output	PADR value	Value written is output by pin
	Other function	PADR value	Can write to PADR, but it has no effect on pin status.

16.3 Port B

Port B is a 16-bit input/output port as shown in figure 16.2.

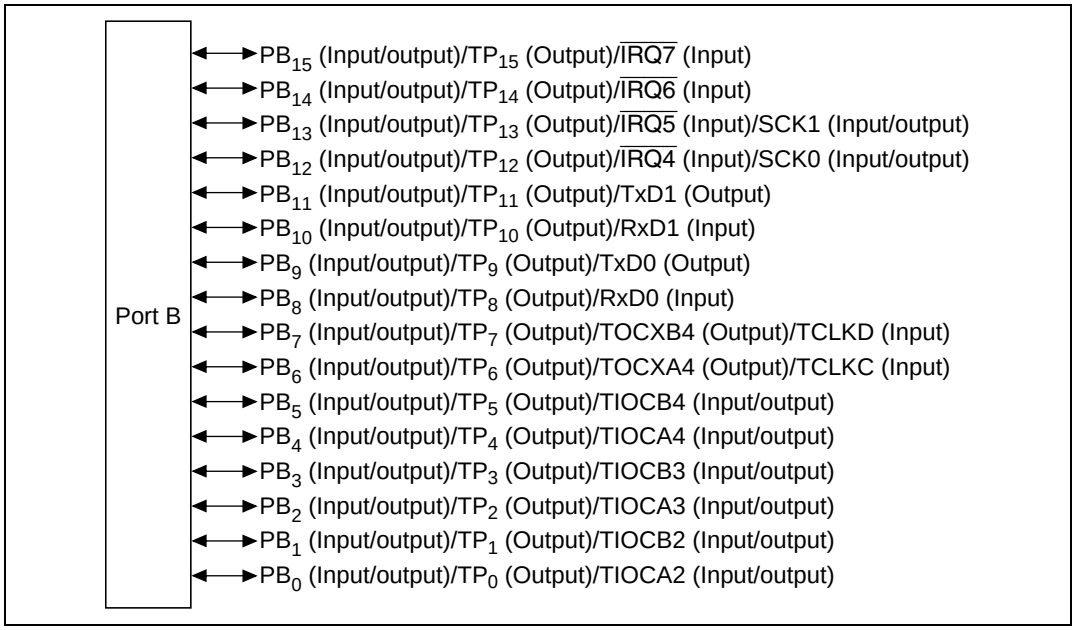


Figure 16.2 Port B Configuration

16.3.1 Register Configuration

Table 16.3 summarizes the port B register.

Table 16.3 Port B Register

Name	Abbreviation	R/W	Initial Value	Address*	Access Size
Port B data register	PBDR	R/W	H'0000	H'5FFFFC2	8, 16, 32

Note: * Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.

16.3.2 Port B Data Register (PBDR)

PBDR is a 16-bit read/write register that stores data for port B. Bits PB15DR–PB0DR correspond to the PB15/TP15/$\overline{\text{IRQ7}}$–PB0/TP0/TIOCA2 pins. When the pins are used as ordinary outputs, they will output whatever value is written in PBDR; when PBDR is read, the register value will be output regardless of the pin status. When the pins are used as ordinary inputs, the pin status rather than the register value is read directly when PBDR is read. When a value is written to PBDR, that value can be written into PBDR, but it will not affect the pin status. When the pin function is set to timing pattern output and the TPC output is enabled by the TPC next data enable register (NDER), no value can be written to PBDR. Table 16.4 shows port B data register read/write operations.

PBDR is initialized by a power-on reset. However, PBDR is not initialized by a manual reset, or in standby mode or sleep mode.

Bit	15	14	13	12	11	10	9	8
	PB15DR	PB14DR	PB13DR	PB12DR	PB11DR	PB10DR	PB9DR	PB8DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 16.4 Port B Data Register (PBDR) Read/Write Operations

PBIOR	Pin Status	Read	Write
0	Input	Pin status	Can write to PBDR, but it has no effect on pin status
	TPn	Pin status	Disabled
	Other function	Pin status	Can write to PBDR, but it has no effect on pin status
1	Output	PBDR value	Value written is output by pin
	TPn	PBDR value	Disabled
	Other function	PBDR value	Can write to PBDR, but it has no effect on pin status

TPn: Timing pattern output

16.4 Port C

Port C is an eight-bit input port as shown in figure 16.3.

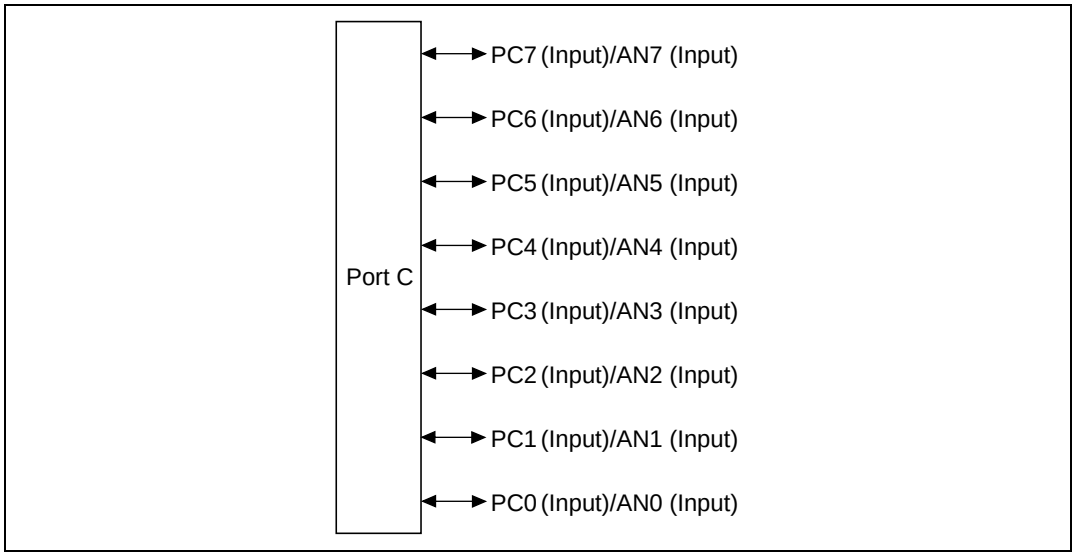


Figure 16.3 Port C Configuration

16.4.1 Register Configuration

Table 16.5 summarizes the port C register.

Table 16.5 Port C Register

Name	Abbreviation	R/W	Initial Value	Address*	Access Size
Port C data register	PCDR	R/W	—	H'5FFFFD0	8, 16, 32

Note: * Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.

16.4.2 Port C Data Register (PCDR)

PCDR is an 16-bit read-only register that stores data for port C (writes to bits 15–8 are ignored, and the read value is always undefined). Bits PC7DR–PC0DR correspond to the PC7/AN7–PC0/AN0 pins respectively. Any values written to these bits will be ignored and will not affect the pin status. When the bits are read, the pin status rather than the bit value is read directly. When analog input of the A/D converter is being sampled, however, every bit is read as 1. Table 16.6 shows port C data register read/write operations (bits 7–0).

PCDR is not initialized by a power-on reset or manual reset, or in standby mode or sleep mode (bits 15–8 are always undefined; bits 7–0 always reflect the pin status).

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

Table 16.6 Port C Data Register (PCDR) Read/Write Operations

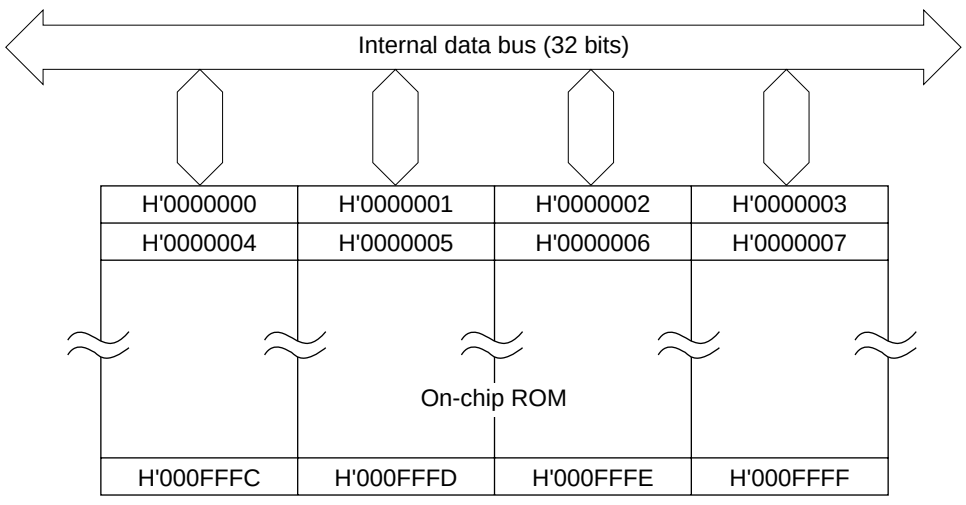
Pin I/O	Pin Function	Read	Write
Input	General purpose	Pin status read	Ignored (no effect on pin status)
	ANn	Read as 1	Ignored (no effect on pin status)

ANn: Analog input

Section 17 ROM

17.1 Overview

The SH7034 microcomputer has 64 kbytes of on-chip ROM (mask ROM or PROM). The on-chip ROM is connected to the CPU and the direct memory access controller (DMAC) through a 32-bit data bus (figure 17.1). The CPU can access the on-chip ROM in 8-, 16- and 32-bit widths and the DMAC can access the ROM in 8- and 16-bit widths. Data in the on-chip ROM can always be accessed in one cycle.



Note: The addresses shown in the figure are the uppermost shadow addresses in the on-chip ROM space.

Figure 17.1 Block Diagram of ROM

The operating mode determines whether the on-chip ROM is valid or not. The operating mode is selected using mode-setting pins MD0–MD2 as shown in table 17.1. When using the on-chip ROM, select mode 2; otherwise, select mode 0 or 1. The on-chip ROM is allocated to addresses H'0000000–H'000FFFF of memory area 0. Memory area 0 (H'0000000–H'0FFFFFF and H'8000000–H'8FFFFFF) is divided into 64-kbyte shadows. No matter which shadow is accessed, the on-chip ROM is accessed. See section 8, Bus State Controller (BSC), for more information on shadows.

Table 17.1 Operating Modes and ROM

	Mode Setting Pins			
Operating Mode	**MD2**	**MD1**	**MD0**	**Area 0**
Mode 0 (MCU mode 0)	0	0	0	On-chip ROM disabled, external 8-bit space
Mode 1 (MCU mode 1)	0	0	1	On-chip ROM disabled, external 16-bit space
Mode 2 (MCU mode 2)	0	1	0	On-chip ROM enabled
Mode 7 (PROM mode)	1	1	1	—

0: Low
1: High

When the SH7034 is set to PROM mode, programs can be written in the PROM version in the same way as with ordinary EPROM, using a general-purpose EPROM programmer.

17.2 PROM Mode

17.2.1 Setting PROM Mode

To program the on-chip PROM, set the pins as shown in figure 17.2 and use the chip in PROM mode.

17.2.2 Socket Adapter Pin Correspondence and Memory Map

Mount the socket adapter on the SH7034 as shown in figure 17.2. This allows the on-chip PROM to be programmed in exactly the same way as ordinary 32-pin EPROMs (HN27C101). Figure 17.2 shows the correspondence between SH7034 pins and HN27C101 pins. Figure 17.3 shows the memory map of the on-chip ROM.

The address range of the HN27C101 (128 kbytes) is H'00000–H'1FFFF. The on-chip PROM (64 kbytes) is not found in the latter half (H'10000–H'1FFFF).

When programming with a PROM programmer, the program address range must be set to H'0000–H'FFFF. The data for the H'10000–H'1FFFF address area should all be H'FF. Set byte mode, not page mode.

SH7034		EPROM Socket Adapter	HN27C101	
Pin Number	Pin Name		Pin Name	Pin Number
77	V_{PP}		V_{PP}	1
76	NMI		A9	26
4	AD0		I/O0	13
5	AD1		I/O1	14
6	AD2		I/O2	15
7	AD3		I/O3	17
8	AD4		I/O4	18
9	AD5		I/O5	19
10	AD6		I/O6	20
11	AD7		I/O7	21
23	A0/$\overline{HBS}$		A0	12
24	A1		A1	11
25	A2		A2	10
26	A3		A3	9
27	A4		A4	8
28	A5		A5	7
29	A6		A6	6
30	A7		A7	5
32	A8		A8	27
33	A9		$\overline{OE}$	24
34	A10		A10	23
35	A11		A11	25
36	A12		A12	4
37	A13		A13	28
38	A14		A14	29
39	A15		A15	3
41	A16		A16	2
55	PA2/$\overline{CS6}$/TIOCB0		$\overline{PGM}$	31
56	PA3/$\overline{CS7}$/$\overline{WAIT}$		$\overline{CE}$	22
42	A17		V_{CC}	32
44	A18		V_{SS}	16
15, 43, 70, 75, 83, 84, 99	V_{CC}			
80	MD0			
81	MD1			
82	MD2			
85, 86	AV_{CC}, AV_{ref}			
79	$\overline{RES}$			
3, 12, 22, 31, 40, 52, 61, 72, 96, 106	V_{SS}			
87–90, 92–95	PC0/AN0–PC3/AN3 PC4/AN4–PC7/AN7			
91	AV_{SS}			
Pins other than the above	NC (leave open)			

- V_{PP}: PROM program power adapter (12.5 V)
- A16–A0: Address input
- I/O7–I/O0: Data input/ output
- $\overline{OE}$: Output enable
- $\overline{PGM}$: Program enable
- $\overline{CE}$: Chip enable

Figure 17.2 Correspondence Between SH7034 Pins and HN27C101 Pins

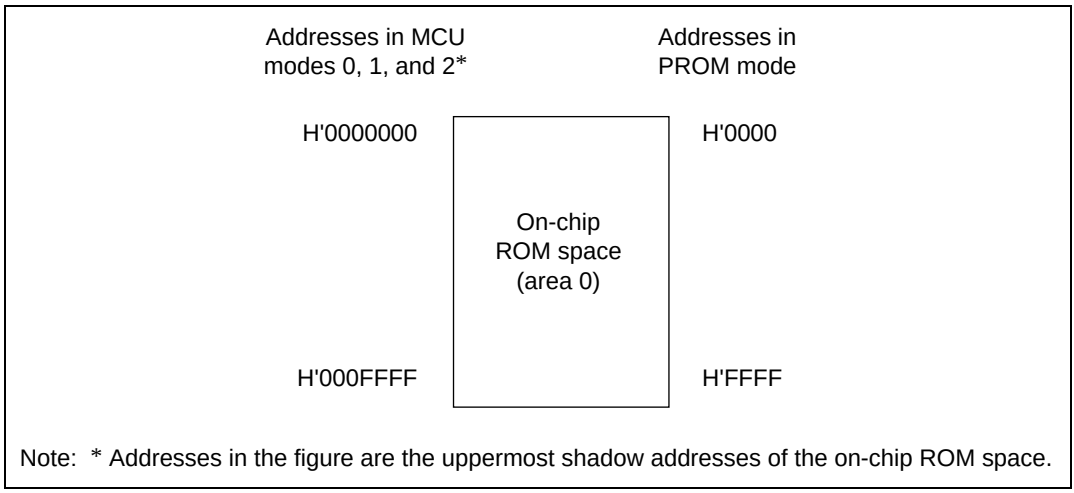


Figure 17.3 Memory Map of On-chip ROM

17.3 PROM Programming

The write/verify specifications in PROM mode are the same as for the standard EPROM HN27C101. Page programming is not supported, so *do not set the PROM programmer to page programming mode*. Naturally, PROM programmers that only support page programming mode cannot be used. When selecting a PROM programmer, check that the byte-by-byte high-speed, high-reliability programming method is supported.

17.3.1 Selecting the Programming Mode

There are two on-chip PROM programming modes: write and verify (which reads and confirms the data written). Use the pins to select the modes (table 17.2).

Table 17.2 Selecting PROM Programming Mode

	Pin						
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{PGM}$**	**V_{PP}**	**V_{CC}**	**I/O7–I/O0**	**A16–A0**
Write	0	1	0	V_{PP}	V_{CC}	Data input	Address input
Verify	0	0	1			Data output	
Program inhibit	0	0	0			High impedance	
	0	1	1				
	1	0	0				
	1	1	1				

Legend:
0: Low
1: High
V_{PP}: V_{PP} level
V_{CC}: V_{CC} level

17.3.2 Write/Verify and Electrical Characteristics

Write/Verify: Write/verify can be accomplished by an efficient high-speed, high-reliability programming method. This method can write data quickly and accurately without placing voltage stress on the device. The basic flowchart for this high-speed, high-reliability programming method is shown in figure 17.4.

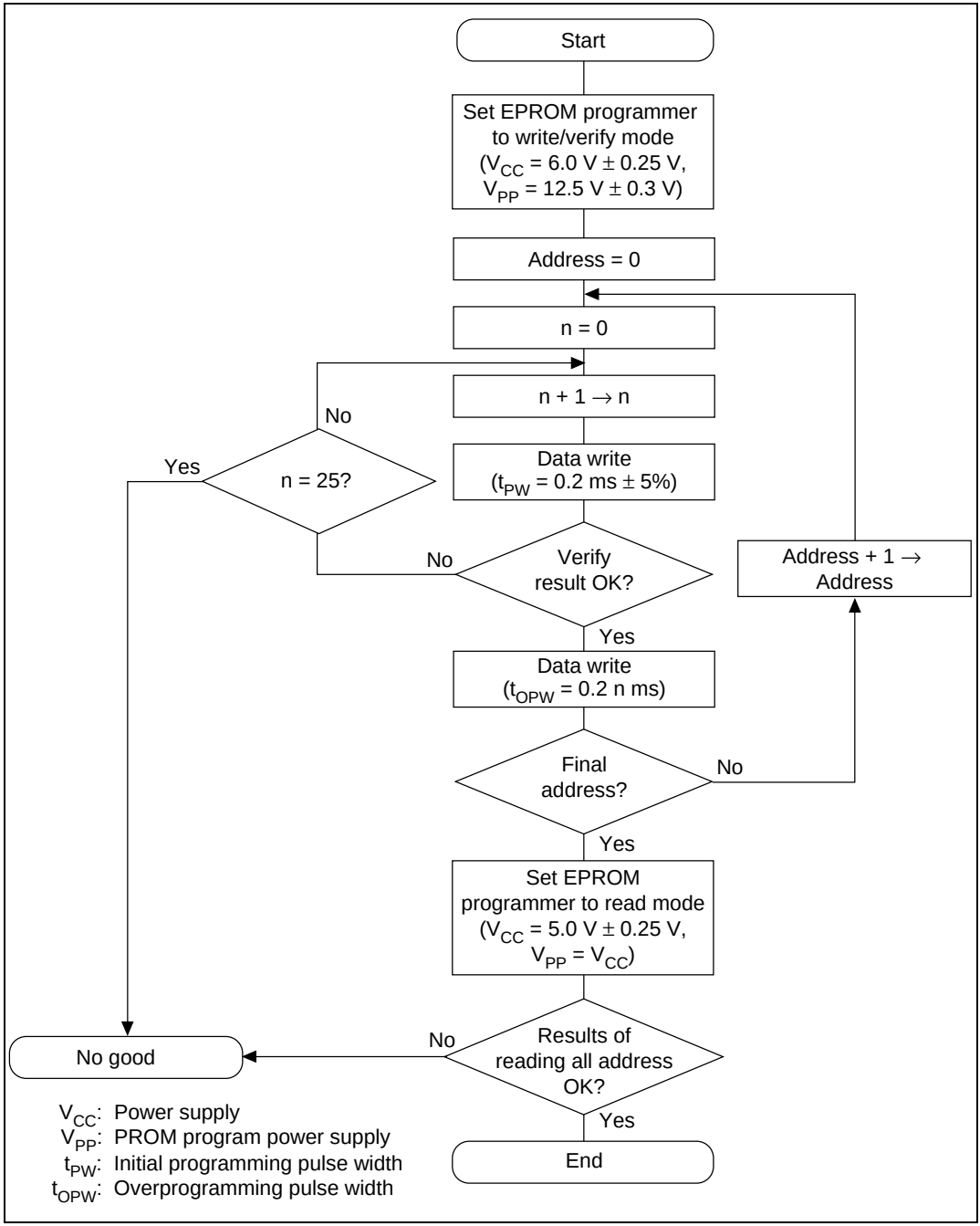


Figure 17.4 Basic Flowchart of High-Speed, High-Reliability Programming

Electrical Characteristics: Tables 17.3 and 17.4 show the electrical characteristics of programming. Figure 17.5 shows the timing.

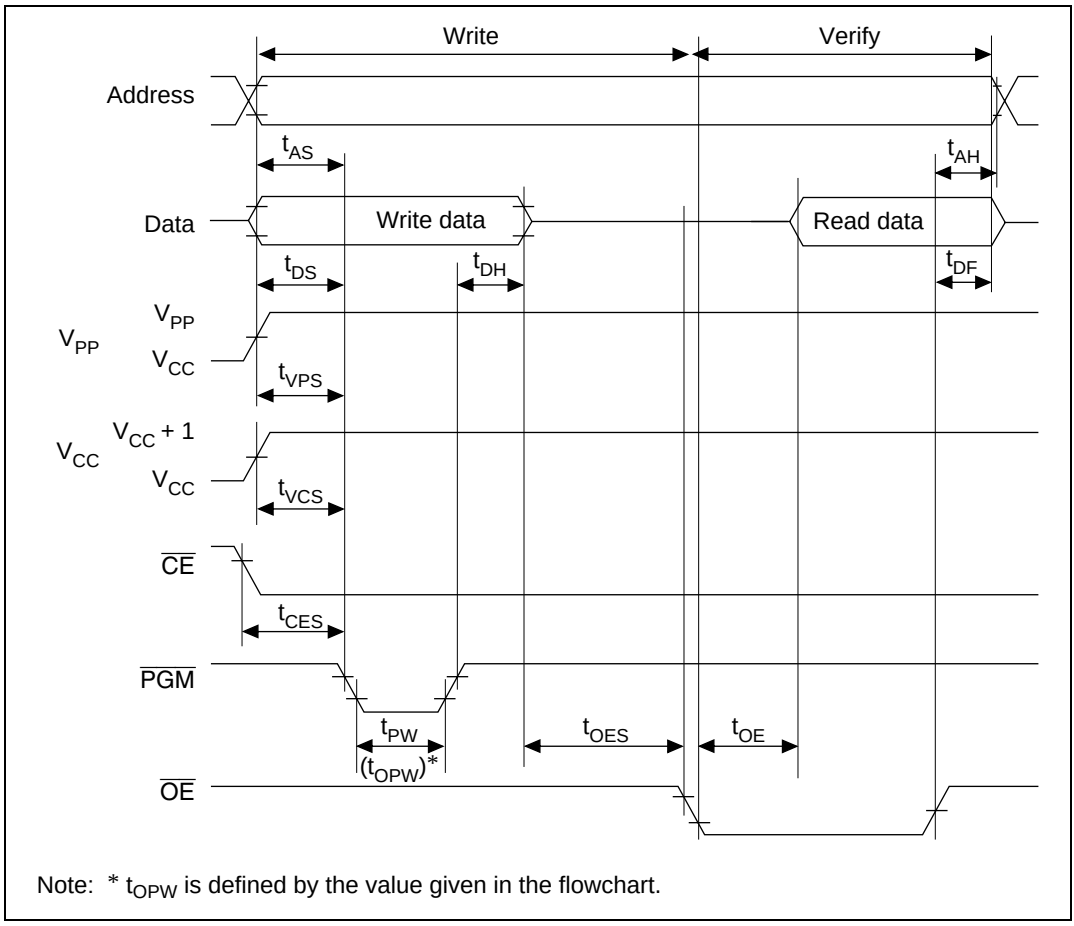
Table 17.3 DC Characteristics (V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V, Ta = 25 ± 5°C)

Item	Pins	Symbol	Min	Typ	Max	Unit	Test Conditions
Input high voltage	I/O7–I/O0, A16–A0, $\overline{OE}$, $\overline{CE}$, $\overline{PGM}$	V_{IH}	2.4	—	V_{CC} + 0.3	V	
Input low voltage	I/O7–I/O0, A16–A0, $\overline{OE}$, $\overline{CE}$, $\overline{PGM}$	V_{IL}	–0.3	—	0.8	V	
Output high voltage	I/O7–I/O0	V_{OH}	2.4	—	—	V	I_{OH} = -200 µA
Output low voltage	I/O7–I/O0	V_{OL}	—	—	0.45	V	I_{OL} = 1.6 mA
Input leakage current	I/O7–I/O0, A16–A0, $\overline{OE}$, $\overline{CE}$, $\overline{PGM}$	$\|I_{LI}\|$	—	—	2	µA	V_{IN} = 5.25 V/0.5 V
V_{CC} current		I_{CC}	—	—	40	mA	
V_{PP} current		I_{PP}	—	—	40	mA	

Table 17.4 AC Characteristics (V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V, Ta = 25 ± 5°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	µs	Figure 17.5*1
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
Data output disable time	t_{DF}*2	—	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
$\overline{PGM}$ pulse width in initial programming	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ pulse width in overprogramming	t_{OPW}*3	0.19	—	5.25	ms	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs	
Data output delay time	t_{OE}	0	—	150	ns	

Notes: 1. Input pulse level: 0.45–2.4 V
Input rise, fall time ≤ 20 ns
Input timing reference levels: 0.8 V, 2.0 V
Output timing reference levels: 0.8 V, 2.0 V
2. t_{DF} is defined at the point where the output is in the open state and the output level cannot be referenced.
3. t_{OPW} is defined by the value given in the flowchart.



Note: * t_{OPW} is defined by the value given in the flowchart.

Figure 17.5 Write/Verify Timing

17.3.3 Notes on Writing

1. Always write using the prescribed voltage and timing. The write voltage (programming voltage) V_{PP} is 12.5 V (when the EPROM programmer is set to the Renesas specifications for HN27C101, V_{PP} is 12.5 V.) Applying a voltage in excess of the rated voltage may damage the device. Pay particular attention to overshoot in the EPROM programmer.
2. Before programming, always check that the index marks on the EPROM programmer socket, socket adapter, and device are aligned with each other. If they are not correctly aligned, an overcurrent may be generated, damaging the device.
3. Do not touch the socket adapter or device during writing. Contact can cause malfunctions that will prevent data from being written accurately.

4. Page programming mode cannot be used. Always set the equipment to byte programming mode.
5. The capacity of the on-chip ROM is 64 kbytes, so the data of PROM programmer addresses H'10000–H'1FFFF should be H'FF. Always set the range for PROM addresses to H'0000–H'FFFF.
6. When write errors occur on consecutive addresses, stop writing. Check to see if there are any abnormalities in the EPROM programmer and socket adapter.

17.3.4 Reliability after Writing

After programming, it is recommended that the device be left to stand at a high temperature to increase the reliability of data retention. Letting it stand at a high temperature is a type of screening method that can eliminate of initial data retention defects of the on-chip PROM's memory cells within a short period of time. Figure 17.6 shows the flow from programming of the on-chip PROM, including screening, to mounting on the device board.

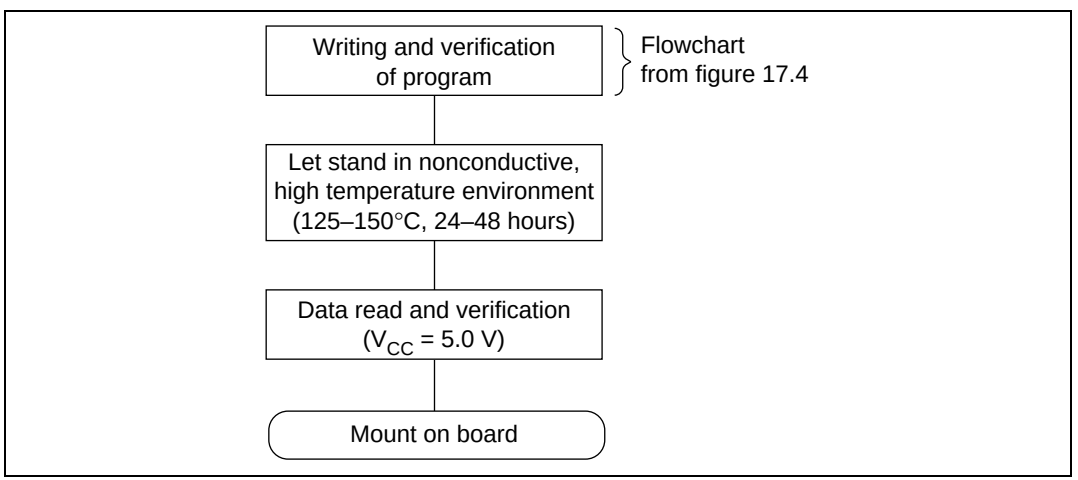


Figure 17.6 Screening Flow

If abnormalities are found when the program is written and verified or the program is read and checked after writing/verification or letting the chip stand at high temperature, contact Renesas' engineering department.

Section 18 RAM

18.1 Overview

The SH7032 microcomputer has 8-kbytes of on-chip RAM; the SH7034 has 4 kbytes. The on-chip RAM is linked to the CPU and direct memory access controller (DMAC) with a 32-bit data bus (figure 18.1). The CPU can access data in the on-chip RAM in byte, word, or longword units. The DMAC can access byte or word data. On-chip RAM data can always be accessed in one state, making the RAM ideal for use as a program area, stack area, or data area, which require high-speed access. The contents of the on-chip RAM are held in both the sleep and standby modes. Memory area 7 addresses H'FFFE000 to H'FFFFFFF are allocated to the on-chip RAM in the SH7032. In the SH7034, addresses H'FFFF000 to H'FFFFFFF are allocated.

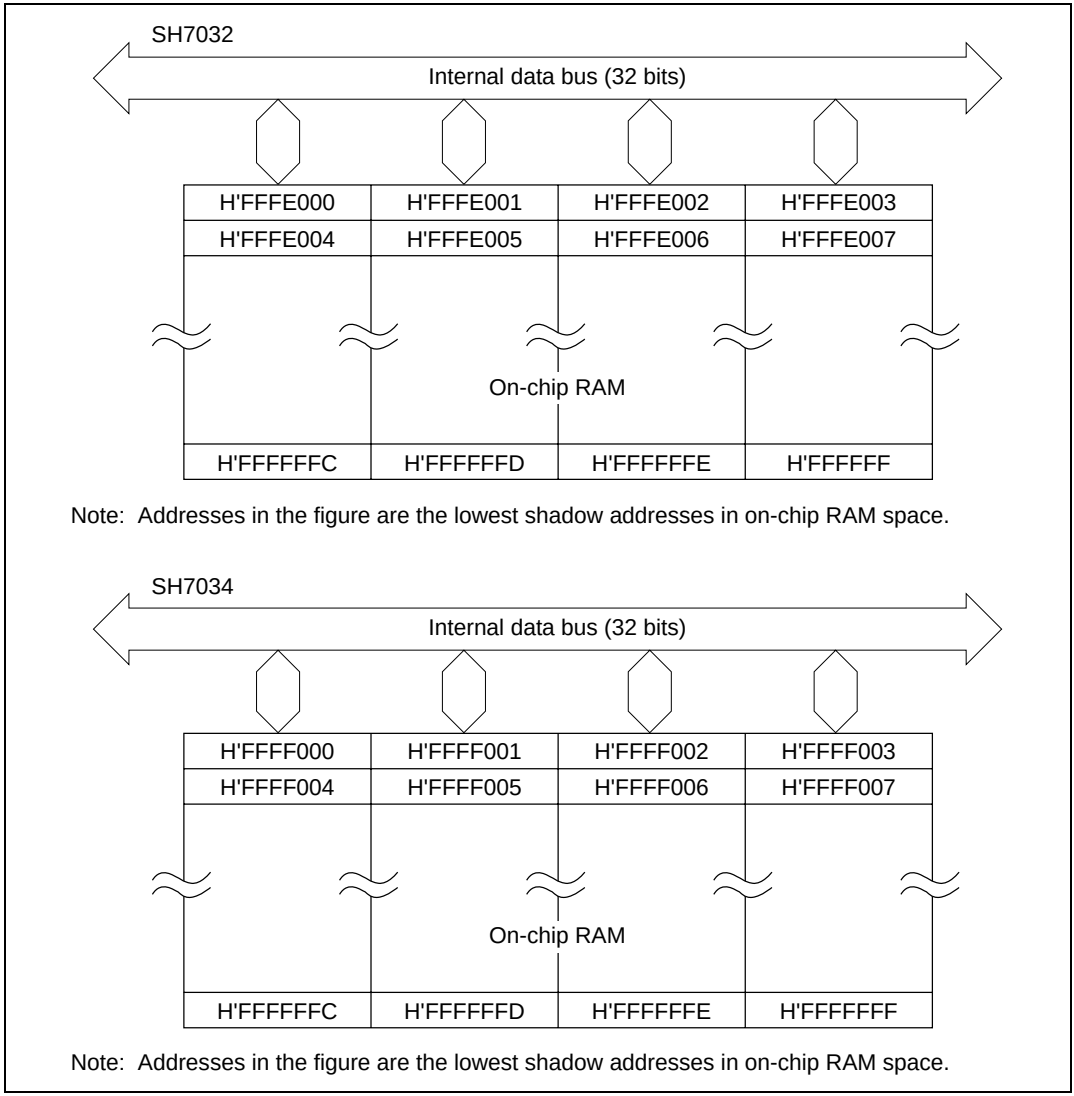


Figure 18.1 Block Diagram of RAM

18.2 Operation

Accesses to addresses H'FFFE000–H'FFFFFFF (SH7032) or addresses H'FFFF000–H'FFFFFFF (SH7034) are directed to the on-chip RAM. Memory area 7 (H'F000000–H'FFFFFFF) is divided into shadows in 8 kbyte units for the SH7032 and 4-kbyte units for the SH7034. All shadow accesses are on-chip RAM accesses. For more information on shadows, see section 8, Bus State Controller (BSC).

Section 19 Power-Down State

19.1 Overview

In the power-down state, all CPU functions are halted. This lowers power consumption of the SH microprocessor dramatically.

19.1.1 Power-Down Modes

The power-down state includes the following two modes:

1. Sleep mode
2. Standby mode

Sleep mode and standby mode are entered from the program execution state according to the transition conditions given in table 19.1. Table 19.1 also describes procedures for exiting each mode and the states of the CPU and supporting functions.

Table 19.1 Power-Down State

		State						
Mode	**Entering Procedure**	**Clock**	**CPU**	**Supporting Functions**	**CPU Registers**	**RAM**	**I/O Ports**	**Exiting Procedure**
Sleep mode	Execute SLEEP instruction with SBY bit set to 0 in SBYCR	Runs	Halted	Run	Held	Held	Held	• Interrupt • DMA address error • Power-on reset • Manual reset
Standby mode	Execute SLEEP instruction with SBY bit set to 1 in SBYCR	Halted	Halted	Halted*1	Held	Held	Held or high-Z*2	• NMI interrupt • Power-on reset • Manual reset

SBYCR: Standby control register

SBY: Standby bit

Notes: 1. Some of the registers of the on-chip supporting modules are not initialized in standby mode. For details, see table 19.3, Register States in Standby Mode, in section 19.4.1, Transition to Standby Mode, or the descriptions of registers given where the on-chip supporting modules are covered.

2. The status of I/O ports in standby mode are set by the port high-impedance bit (HIZ) in SBYCR. See section 19.2, Standby Control Register (SBYCR), for details. The status of pins other than the I/O ports are described in appendix B, Pin States.

19.1.2 Register

Table 19.2 summarizes the register related to the power-down state.

Table 19.2 Standby Control Register (SBYCR)

Name	Abbreviation	R/W	Initial Value	Address*	Access size
Standby control register	SBYCR	R/W	H'1F	H'5FFFFBC	8, 16, 32

Note: * Only the values of bits A27–A24 and A8–A0 are valid; bits A23–A9 are ignored. For details on the register addresses, see section 8.3.5, Area Descriptions.

19.2 Standby Control Register (SBYCR)

The standby control register (SBYCR) is an 8-bit read/write register. It is used to enter standby mode and also sets the port states in standby mode. SBYCR is initialized to H'1F by a reset.

Bit	7	6	5	4	3	2	1	0
	SBY	HIZ	—	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/W	R/W	—	—	—	—	—	—

Bit 7—Standby (SBY): SBY enables transition to standby mode. The SBY bit cannot be set to 1 while the timer enable bit (bit TME) in timer control/status register TCSR of the watchdog timer (WDT) is set to 1. To enter standby mode, clear the TME bit to 0 to halt the WDT and then set the SBY bit.

SBY	Description	
0	Executing SLEEP instruction puts the chip into sleep mode	(Initial value)
1	Executing SLEEP instruction puts the chip into standby mode	

Bit 6—Port High-Impedance (HIZ): HIZ selects whether I/O ports remain in their previous states during standby, or are placed in the high-impedance state when standby mode is entered. The HIZ bit cannot be set to 1 while the TME bit is set to 1. To place the pins of the I/O ports in high impedance, clear the TME bit to 0 before setting the HIZ bit.

HIZ	Description	
0	Port states are maintained during standby	(Initial value)
1	Ports are placed in the high-impedance state in standby	

Bits 5–0—Reserved: Bit 5 is a read-only bit that is always read as 0. Only write 0 in bit 5. Writing to bits 4–0 is disabled. These bits are always read as 1.

19.3 Sleep Mode

19.3.1 Transition to Sleep Mode

Execution of the SLEEP instruction when the standby bit (SBY) in the standby control register (SBYCR) is cleared to 0 causes a transition from the program execution state to sleep mode. Although the CPU halts immediately after executing the SLEEP instruction, the contents of its internal registers remain unchanged. The on-chip supporting modules do not halt in sleep mode.

19.3.2 Exiting Sleep Mode

Sleep mode is exited by an interrupt, DMA address error, power-on reset, or manual reset.

Exit by Interrupt: When an interrupt occurs, sleep mode is exited and interrupt exception handling is executed. Sleep mode is not exited if the interrupt cannot be accepted because its priority level is equal to or less than the mask level set in the CPU's status register (SR). Likewise, sleep mode is not exited if the interrupt is disabled by the on-chip supporting module.

Exit by DMA Address Error: If the DMAC operates during sleep mode and a DMA address error occurs, sleep mode is exited and DMA address error exception handling is executed.

Exit by Power-On Reset: If the $\overline{\text{RES}}$ signal goes low while the NMI signal is high, sleep mode is exited and the power-on reset state is entered. If the NMI signal is brought from low to high in order to set the chip for a power-on reset, an NMI interrupt will occur whenever the rising edge of NMI is selected as the valid edge (with NMI edge select bit NMIE in the interrupt control register (ICR) of the interrupt controller). When this occurs, the NMI interrupt clears sleep mode.

Exit by Manual Reset: If the $\overline{\text{RES}}$ signal goes low while the NMI signal is low, sleep mode is exited and the manual reset state is entered. If the NMI signal is brought from high to low in order to set the chip for a manual reset, sleep mode will be exited by an NMI interrupt whenever the falling edge of NMI is selected as the valid edge (with the NMIE bit).

19.4 Standby Mode

19.4.1 Transition to Standby Mode

To enter standby mode, set the standby bit (SBY) to 1 in the standby control register (SBYCR), then execute the SLEEP instruction. The chip switches from the program execution state to standby mode. Standby mode greatly reduces power consumption by halting not only the CPU, but the clock and on-chip supporting modules as well. Some registers of the on-chip supporting modules are initialized, others are not (See table 19.3). As long as the specified voltage is supplied, however, CPU register contents and on-chip RAM data are held. The I/O port state (hold or high impedance) depends on the port high-impedance bit (HIZ) in SBYCR. For details on the states of these pins, see appendix B, Pin States.

Table 19.3 Register States in Standby Mode

Module	Registers Initialized	Registers That Hold Data
Interrupt controller (INTC)	—	All registers
User break controller (UBC)	—	All registers
Bus state controller (BSC)	—	All registers
Pin function controller (PFC)	—	All registers
I/O ports	—	All registers
Direct memory access controller (DMAC)	All registers	—
Watchdog timer (WDT)	• Bits 7–5 (OVF, WT/$\overline{IT}$, TME) in timer control status register (TCSR) • Reset control/status register (RSTCSR)	• Bits 2–0 (CKS2–CKS0) in timer control status register (TCSR) • Timer counter (TCNT)
16-bit integrated timer pulse unit (ITU)	All registers	—
Programmable timing pattern controller (TPC)	—	All registers
Serial communication interface (SCI)	• Receive data register (RDR) • Transmit data register (TDR) • Serial mode register (SMR) • Serial control register (SCR) • Serial status register (SSR) • Bit rate register (BBR)	—
A/D converter (A/D)	All registers	—
Power-down state register	—	Standby control register (SBYCR)

19.4.2 Exiting Standby Mode

Standby mode is exited by an NMI interrupt, a power-on reset, or a manual reset.

Exit by NMI: When a rising edge or falling edge (as selected by the NMIE bit in the interrupt control register (ICR) of the interrupt controller (INTC)) is detected at the NMI pin, the clock oscillator begins operating. At first, clock pulses are supplied only to the watchdog timer. After the time that was selected before entering standby mode using clock select bits 2–0 (CKS2–CKS0) in the timer control/status register (TCSR) of the watchdog timer (WDT), the watchdog timer overflows. After the overflow, the clock is considered stable and supplied to the entire chip. Standby mode is exited and the NMI exception handling sequence begins.

When standby mode is cleared by an NMI interrupt, bits CKS2–CKS0 must be set so that the WDT overflow interval is equal to or greater than the clock settling time. When standby mode is cleared when the falling edge has been selected with the NMI bit, be sure that the NMI pin is high when standby mode is entered (when the clock is halted) and low when the chip returns from standby mode (clock starts up after the oscillator is stabilized). Likewise, when standby mode is cleared when the rising edge has been selected with the NMI bit, be sure that the NMI pin is low when standby mode is entered (clock halted) and high when the chip returns from standby mode (clock starts up after the oscillator is stabilized).

Exit by Power-On Reset: If the $\overline{\text{RES}}$ signal goes low while the NMI signal is high, standby mode is exited and the power-on reset state is entered. If the NMI signal is brought from low to high in order to set the chip for a power-on reset, standby mode will not be exited by an NMI interrupt, because the NMI signal is initialized for the falling edge in standby mode (by the NMIE bit).

Exit by Manual Reset: If the $\overline{\text{RES}}$ signal goes low while the NMI signal is low, standby mode is exited and the manual reset state is entered. If the NMI signal is brought from high to low in order to set the chip for a manual reset, standby mode will first be exited by an NMI interrupt, because the NMI signal is initialized for the falling edge in standby mode (by the NMIE bit).

19.4.3 Standby Mode Application

In this example, standby mode is entered on the falling edge of the NMI signal and exited on the rising edge of the NMI signal. Figure 19.1 shows the timing.

After an NMI interrupt is accepted on a high-to-low transition at the NMI pin while NMI edge select bit NMIE in the interrupt control register (ICR) is cleared to 0 to select falling edge detection, the NMI exception handling routine sets NMIE to 1 (selecting rising edge detection) and sets the SBY bit to 1. Finally, it executes a SLEEP instruction to enter standby mode.

Standby mode is exited on the rising edge of the NMI signal.

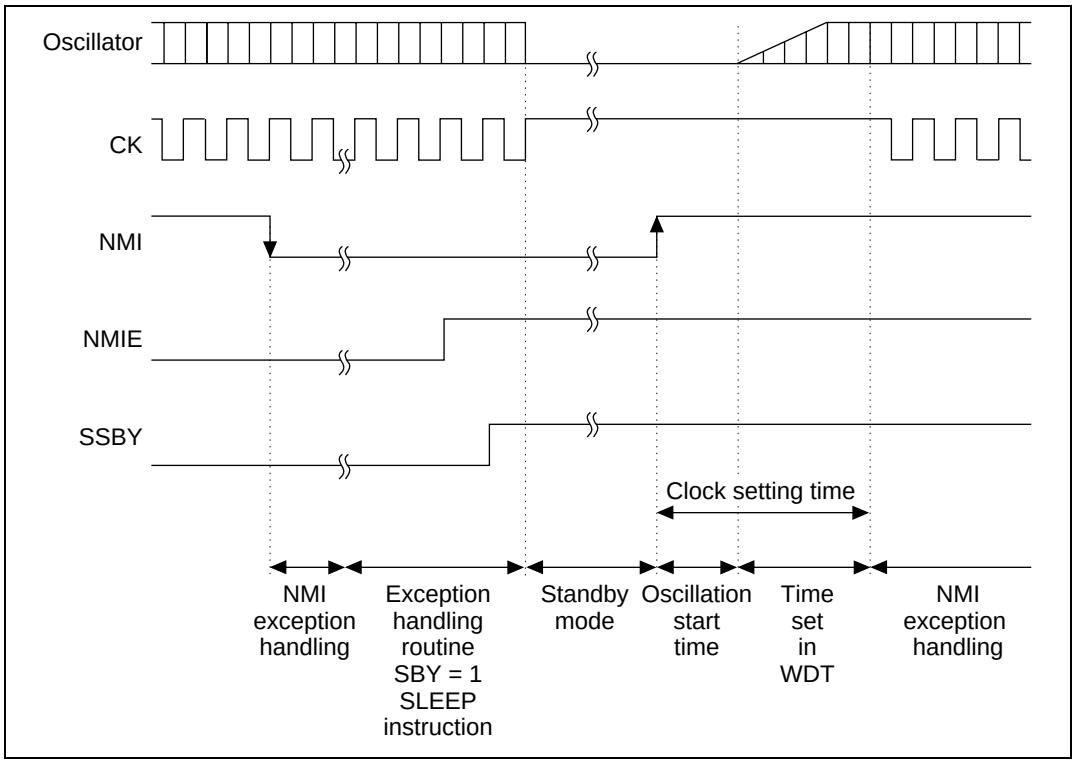


Figure 19.1 NMI Timing for Standby Mode (Example)

Section 20 Electrical Characteristics

20.1 SH7032 and SH7034 Electrical Characteristics

20.1.1 Absolute Maximum Ratings

Table 20.1 shows the absolute maximum ratings.

Table 20.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Program voltage	V_{PP}	–0.3 to +13.5	V
Input voltage (except port C)	V_{in}	–0.3 to V_{CC} + 0.3	V
Input voltage (port C)	V_{in}	–0.3 to AV_{CC} + 0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog reference voltage	AV_{ref}	–0.3 to AV_{CC} + 0.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75*	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Operating the chip in excess of the absolute maximum rating may result in permanent damage.

Note: * Regular-specification products; for wide-temperature-range products, T_{opr} = –40 to +85°C

20.1.2 DC Characteristics

Table 20.2 lists DC characteristics. Table 20.3 lists the permissible output current values.

Table 20.2 DC Characteristics (1)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*)

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Port C		2.2	—	AV_{CC} + 0.3	V	
	Other input pins		2.2	—	V_{CC} + 0.3	V	
Input low-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IL}	–0.3	—	0.5	V	
	Other input pins		–0.3	—	0.8	V	
Schmidt trigger input voltage	PA13–PA10, PA2, PA0, PB7–PB0	V_T^+	4.0	—	—	V	
		V_T^-	—	—	1.0	V	
		$V_T^+ – V_T^-$	0.4	—	—	V	
Input leakage current	$\overline{RES}$	|Iin|	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	NMI, MD2–MD0		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	Port C		—	—	1.0	µA	Vin = 0.5 to AV_{CC} – 0.5 V
3-state leakage current (off state)	Ports A and B, $\overline{CS3}$–$\overline{CS0}$, A21–A0, AD15–AD0	$\|I_{TSI}\|$	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	PA3	–Ip	20	—	300	µA	Vin = 0V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
			—	—	1.2	V	I_{OL} = 8 mA

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	$\overline{RES}$	Cin	—	—	30	pF	Vin = 0 V Input signal f = 1 MHz Ta = 25°C
	NMI		—	—	30	pF	
	All other input pins		—	—	20	pF	
Current consumption	Ordinary operation	I_{CC}	—	60	90	mA	f = 12.5 MHz
			—	100	130	mA	f = 20 MHz
	Sleep		—	40	70	mA	f = 12.5 MHz
			—	60	90	mA	f = 20 MHz
	Standby		—	0.01	5*[1]	µA	Ta ≤ 50°C
			—	—	20.0*[2]	µA	50°C < Ta
Analog power supply current	During A/D conversion	AI_{CC}	—	1.0	2	mA	
	While A/D converter is waiting		—	0.01	5	µA	
Reference power supply current	During A/D conversion	AI_{ref}	—	0.5	1	mA	AV_{ref} = 5.0 V
	While A/D converter is waiting		—	0.01	5	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. 50 µA for the SH7032.
2. 300 µA for the SH7032.

Usage Notes:

1. If the A/D converter is not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open. Connect AV_{CC} and AV_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IH} min = V_{CC} - 0.5 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. When the A/D converter is not used, and in standby mode, AV_{CC} and AV_{ref} must still be connected to the power supply (V_{CC}).
4. The ZTAT and mask versions have the same functions, and the electrical characteristics of both are within specification, but characteristic-related performance values, operating margins, noise margins, noise emission, etc., are different. Caution is therefore required in carrying out system design, and when switching between ZTAT and mask versions.

Table 20.2 DC Characteristics (2)

Conditions: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*)

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Port C		$V_{CC} \times 0.7$	—	AV_{CC} + 0.3	V	
	Other input pins		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
Input low-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	Other input pins		–0.3	—	$V_{CC} \times 0.2$	V	
Schmidt trigger input voltage	PA13–10, PA2, PA0, PB7–PB0	V_T^+	$V_{CC} \times 0.9$	—	—	V	
		V_T^-	—	—	$V_{CC} \times 0.2$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input leakage current	$\overline{RES}$	|Iin|	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	NMI, MD2–MD0		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	Port C		—	—	1.0	µA	Vin = 0.5 to AV_{CC} – 0.5 V
3-state leakage current (off state)	Ports A and B, $\overline{CS3}$–$\overline{CS0}$, A21–A0, AD15–AD0	$\|I_{TSI}\|$	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	PA3	–Ip	20	—	300	µA	Vin = 0V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
			—	—	1.2	V	I_{OL} = 8 mA

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	$\overline{RES}$	Cin	—	—	30	pF	Vin = 0 V Input signal f = 1 MHz Ta = 25°C
	NMI		—	—	30	pF	
	All other input pins		—	—	20	pF	
Current consumption	Ordinary operation	I_{CC}	—	60	90	mA	f = 12.5 MHz
	Sleep		—	40	70	mA	f = 12.5 MHz
	Standby		—	0.01	5.0*1	µA	Ta ≤ 50°C
			—	—	20.0*2	µA	50°C < Ta
Analog power supply current	During A/D conversion	AI_{CC}	—	0.5	1.5	mA	AV_{CC} = 3.0 V
			—	1.0	2.0	mA	AV_{CC} = 5.0 V
	While A/D converter is waiting		—	0.01	5.0	µA	
	During A/D conversion	AI_{ref}	—	0.4	0.8	mA	AV_{ref} = 3.0 V
			—	0.5	1	mA	AV_{ref} = 5.0 V
	While A/D converter is waiting		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. 50 µA for the SH7032.
2. 300 µA for the SH7032.

Usage Notes:

1. If the A/D converter is not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open. Connect AV_{CC} and AV_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IH} min = V_{CC} - 0.5 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. ICC depends on V_{CC} and f as follows:
   I_{CC} max = 1.0 (mA) + 1.29 (mA/MHz · V) × V_{CC} × f [ordinary operation]
   I_{CC} max = 1.0 (mA) + 1.00 (mA/MHz · V) × V_{CC} × f [sleep]
4. When the A/D converter is not used, and in standby mode, AV_{CC} and AV_{ref} must still be connected to the power supply (V_{CC}).
5. The ZTAT and mask versions have the same functions, and the electrical characteristics of both are within specification, but characteristic-related performance values, operating margins, noise margins, noise emission, etc., are different. Caution is therefore required in carrying out system design, and when switching between ZTAT and mask versions.

Table 20.3 Permitted Output Current Values

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Case B: V_{CC} = 5.0 V ±10%, AV_{CC}= 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		Case A			Case B			
		12.5 MHz			20 MHz			
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Output low-level permissible current (per pin)	I_{OL}	—	—	10	—	—	10	mA
Output low-level permissible current (total)	$\sum I_{OL}$	—	—	80	—	—	80	mA
Output high-level permissible current (per pin)	$-I_{OH}$	—	—	2.0	—	—	2.0	mA
Output high-level permissible current (total)	$-\sum I_{OH}$	—	—	25	—	—	25	mA

Caution: To ensure reliability of the chip, do not exceed the output current values given in table 20.3.

20.1.3 AC Characteristics

The following AC timing chart represents the AC characteristics, not signal functions. For signal functions, see the explanation in the text.

(1) Clock Timing

Table 20.4 Clock Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		Case A		Case B			
		12.5 MHz		20 MHz			
Item	Sym-bol	Min	Max	Min	Max	Unit	Figures
EXTAL input high level pulse width	t_{EXH}	20	—	10	—	ns	20.1
EXTAL input low level pulse width	t_{EXL}	20	—	10	—	ns	
EXTAL input rise time	t_{EXr}	—	10	—	5	ns	
EXTAL input fall time	t_{EXf}	—	10	—	5	ns	
Clock cycle time	t_{cyc}	80	500	50	500	ns	20.1, 20.2
Clock high pulse width	t_{CH}	30	—	20	—	ns	20.2
Clock low pulse width	t_{CL}	30	—	20	—	ns	
Clock rise time	t_{Cr}	—	10	—	5	ns	
Clock fall time	t_{Cf}	—	10	—	5	ns	
Reset oscillation settling time	t_{OSC1}	10	—	10	—	ms	20.3
Software standby oscillation settling time	t_{OSC2}	10	—	10	—	ms	

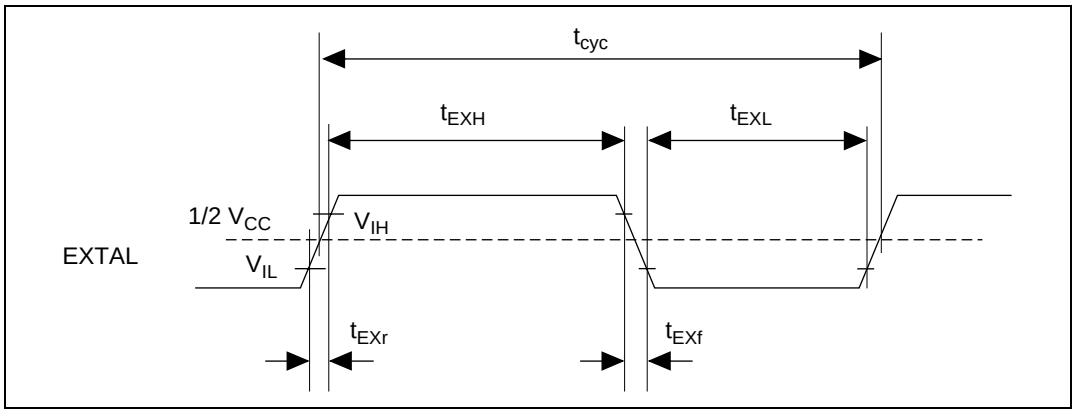


Figure 20.1 EXTAL Input Timing

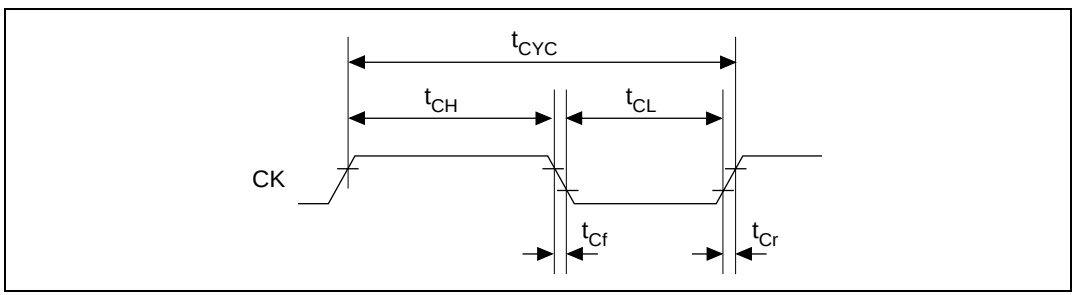


Figure 20.2 System Clock Timing

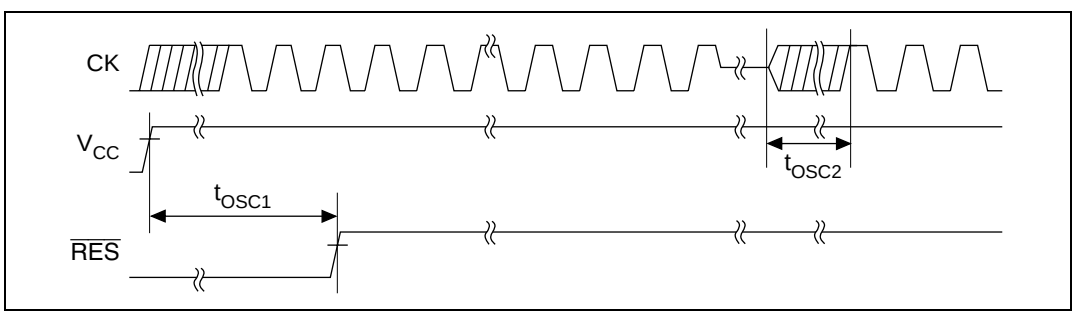


Figure 20.3 Oscillation Settling Time

(2) Control Signal Timing

Table 20.5 Control Signal Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*)

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		Case A		Case B			
		12.5 MHz		20 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Figure**
$\overline{RES}$ setup time	t_{RESS}	320	—	200	—	ns	20.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI reset setup time	t_{NMIRS}	320	—	200	—	ns	
NMI reset hold time	t_{NMIRH}	320	—	200	—	ns	
NMI setup time	t_{NMIS}	160	—	100	—	ns	20.5
NMI hold time	t_{NMIH}	80	—	50	—	ns	
$\overline{IRQ0}$–$\overline{IRQ7}$ setup time (edge detection)	t_{IRQES}	160	—	100	—	ns	
$\overline{IRQ0}$–$\overline{IRQ7}$ setup time (level detection)	t_{IRQLS}	160	—	100	—	ns	
$\overline{IRQ0}$–$\overline{IRQ7}$ hold time	t_{IRQEH}	80	—	50	—	ns	
$\overline{IRQOUT}$ output delay time	t_{IRQOD}	—	80	—	50	ns	20.6
Bus request setup time	t_{BRQS}	80	—	50	—	ns	20.7
Bus acknowledge delay time 1	t_{BACD1}	—	80	—	50	ns	
Bus acknowledge delay time 2	t_{BACD2}	—	80	—	50	ns	
Bus 3-state delay time	t_{BZD}	—	80	—	50	ns	

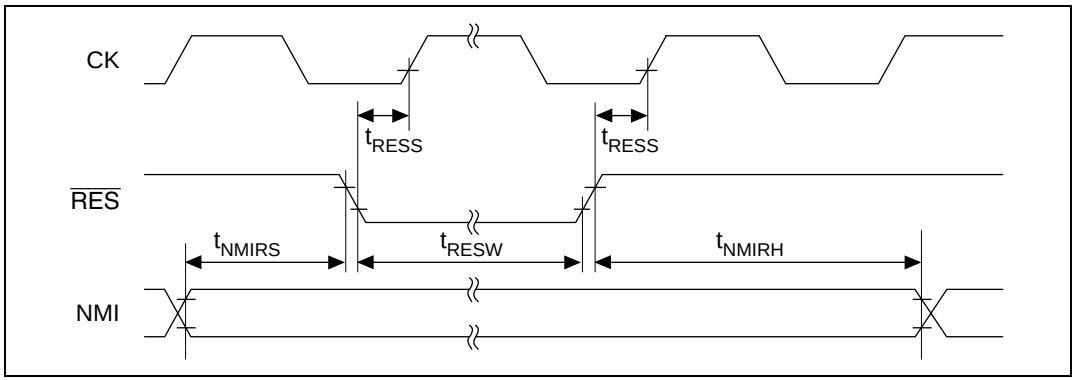


Figure 20.4 Reset Input Timing

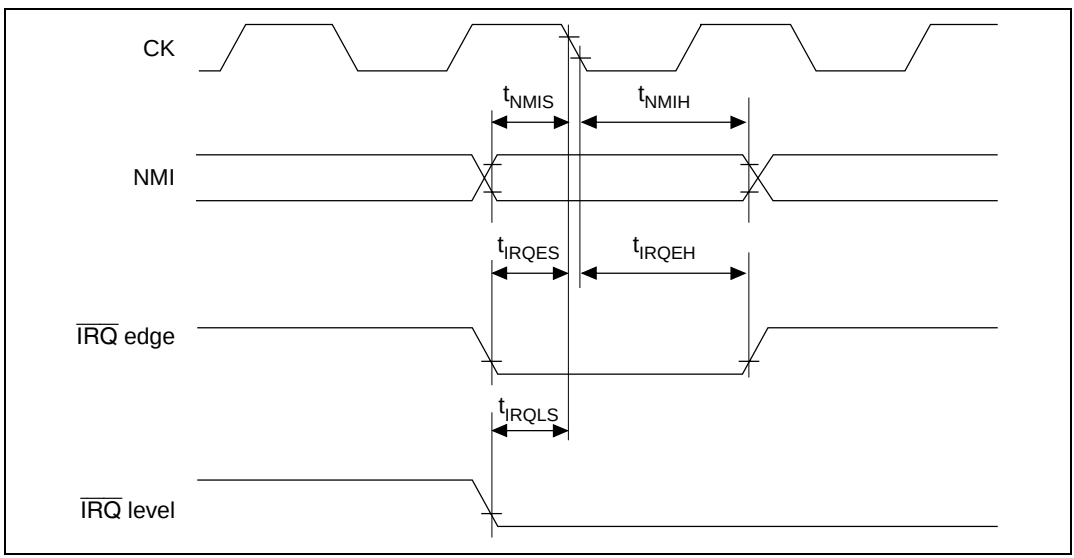


Figure 20.5 Interrupt Signal Input Timing

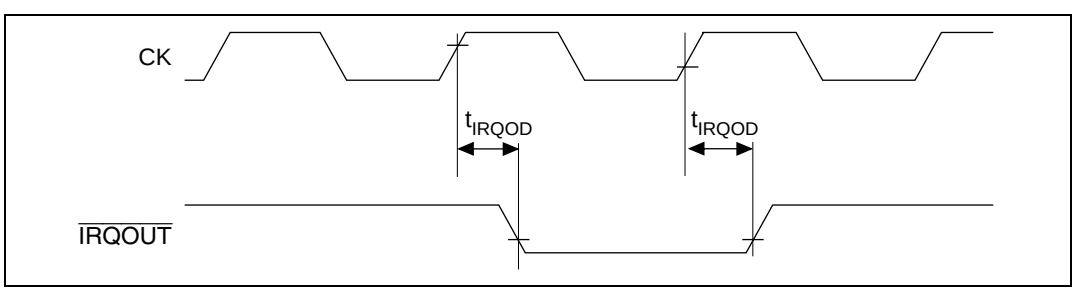


Figure 20.6 Interrupt Signal Output Timing

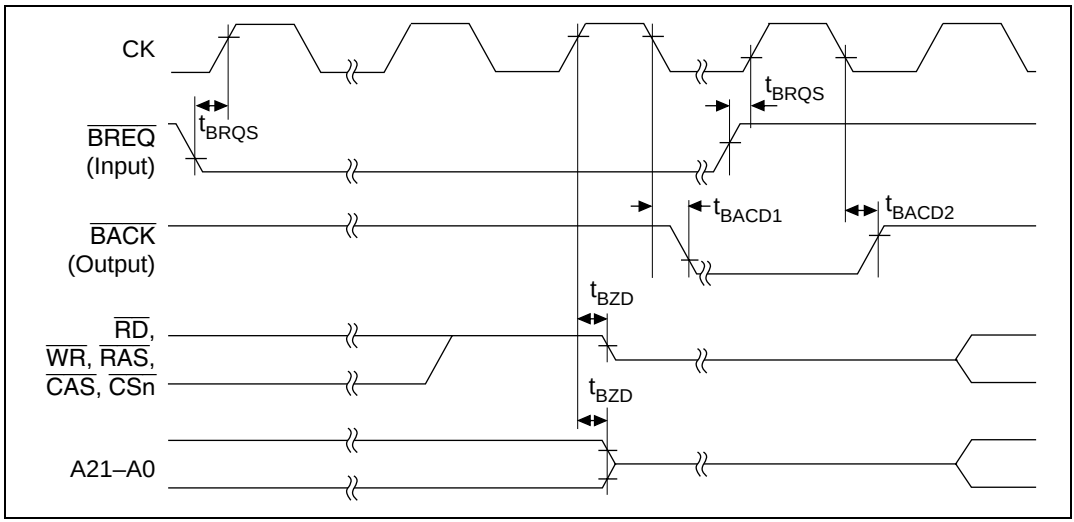


Figure 20.7 Bus Release Timing

(3) Bus Timing

Tables 20.6 to 20.8 show the bus timing.

Table 20.6 Bus Timing (1)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*

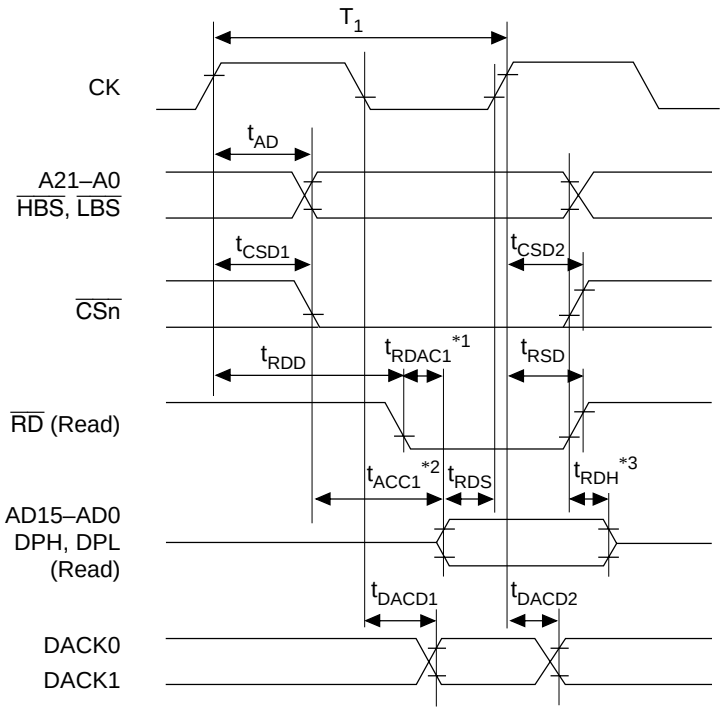
Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item		Symbol	Min	Max	Unit	Figures
Address delay time		t_{AD}	—	20*[1]	ns	20.8, 20.9, 20.11–20.14, 20.19, 20.20
$\overline{CS}$ delay time 1		t_{CSD1}	—	25	ns	20.8, 20.9, 20.20
$\overline{CS}$ delay time 2		t_{CSD2}	—	25	ns	
$\overline{CS}$ delay time 3		t_{CSD3}	—	20	ns	20.19
$\overline{CS}$ delay time 4		t_{CSD4}	—	20	ns	
Access time 1*[6] from read strobe	35% duty*[2]	t_{RDAC1}	$t_{cyc} \times 0.65 - 20$	—	ns	20.8,
	50% duty		$t_{cyc} \times 0.5 - 20$	—	ns	
Access time 2*[6] from read strobe	35% duty*[2]	t_{RDAC2}	$t_{cyc} \times (n+1.65) - 20$*[3]	—	ns	20.9, 20.10
	50% duty		$t_{cyc} \times (n+1.5) - 20$*[3]	—	ns	
Access time 3*[6] from read strobe	35% duty*[2]	t_{RDAC3}	$t_{cyc} \times (n+0.65) - 20$*[3]	—	ns	20.19
	50% duty		$t_{cyc} \times (n+0.5) - 20$*[3]	—	ns	
Read strobe delay time		t_{RSD}	—	20	ns	20.8, 20.9, 20.11–20.15, 20.19
Read data setup time		t_{RDS}	15	—	ns	20.8, 20.9, 20.11–20.14, 20.19
Read data hold time		t_{RDH}	0	—	ns	
Write strobe delay time 1		t_{WSD1}	—	20	ns	20.9, 20.13, 20.14, 20.19, 20.20
Write strobe delay time 2		t_{WSD2}	—	20	ns	20.9, 20.13, 20.14, 20.19
Write strobe delay time 3		t_{WSD3}	—	20	ns	20.11, 20.12
Write strobe delay time 4		t_{WSD4}	—	20	ns	20.11, 20.12, 20.20
Write data delay time 1		t_{WDD1}	—	35	ns	20.9, 20.13, 20.14, 19
Write data delay time 2		t_{WDD2}	—	20	ns	20.11, 20.12

Item	Symbol	Min	Max	Unit	Figures
Write data hold time	t_{WDH}	0	—	ns	20.9, 20.11–20.14
Parity output delay time 1	t_{WPDD1}	—	40	ns	20.9, 20.13, 20.14
Parity output delay time 2	t_{WPDD2}	—	20	ns	20.11, 20.12
Parity output hold time	t_{WPDH}	0	—	ns	20.9, 20.11–20.14
Wait setup time	t_{WTS}	14	—	ns	20.10, 20.15, 20.19
Wait hold time	t_{WTH}	10	—	ns	
Read data access time 1*6	t_{ACC1}	$t_{cyc} - 30$*4	—	ns	20.8, 20.11, 20.12
Read data access time 2*6	t_{ACC2}	$t_{cyc} \times (n+2) - 30$*3	—	ns	20.9, 20.10, 20.13–20.15
$\overline{RAS}$ delay time 1	t_{RASD1}	—	20	ns	20.11–20.14, 20.16–20.18
$\overline{RAS}$ delay time 2	t_{RASD2}	—	30	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	—	20	ns	20.11
$\overline{CAS}$ delay time 2*7	t_{CASD2}	—	20	ns	20.13, 20.14, 20.16–20.18
$\overline{CAS}$ delay time 3*7	t_{CASD3}	—	20	ns	
Column address setup time	t_{ASC}	0	—	ns	20.11, 20.12
Read data access time from $\overline{CAS}$ 1*6 35% duty*2	t_{CAC1}	$t_{cyc} \times 0.65 - 19$	—	ns	
50% duty		$t_{cyc} \times 0.5 - 19$	—	ns	
Read data access time from $\overline{CAS}$ 2*6	t_{CAC2}	$t_{cyc} \times (n+1) - 25$*3	—	ns	20.13–20.15
Read data access time from $\overline{RAS}$ 1*6	t_{RAC1}	$t_{cyc} \times 1.5 - 20$	—	ns	20.11, 20.12
Read data access time from $\overline{RAS}$ 2*6	t_{RAC2}	$t_{cyc} \times (n+2.5) - 20$*3	—	ns	20.13–20.15
High-speed page mode $\overline{CAS}$ precharge time	t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.12

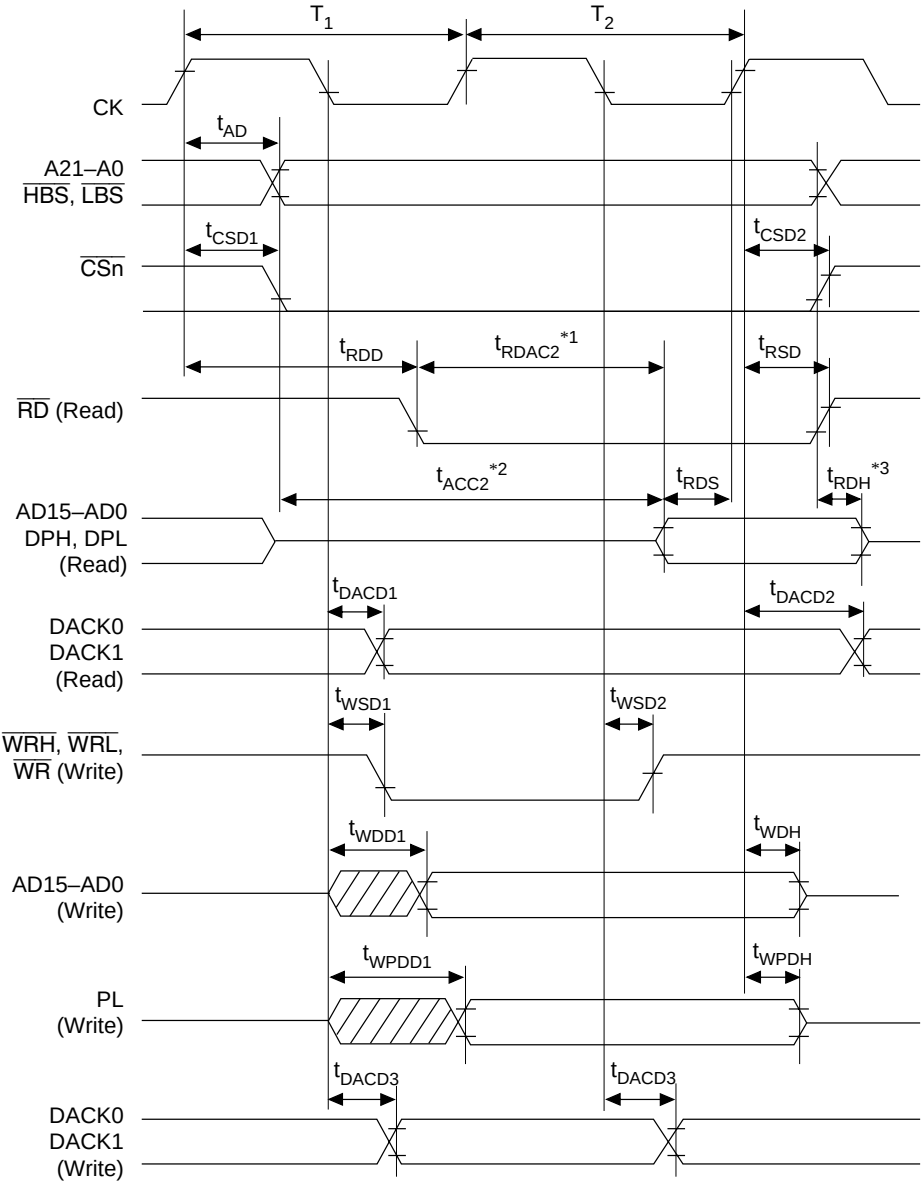
Item		Symbol	Min	Max	Unit	Figures
$\overline{AH}$ delay time 1		t_{AHD1}	—	20	ns	20.19
$\overline{AH}$ delay time 2		t_{AHD2}	—	20	ns	
Multiplexed address delay time		t_{MAD}	—	30	ns	
Multiplexed address hold time		t_{MAH}	0	—	ns	
DACK0, DACK1 delay time 1		t_{DACD1}	—	23	ns	20.8, 20.9, 20.11–20.14, 20.19, 20.20
DACK0, DACK1 delay time 2		t_{DACD2}	—	23	ns	
DACK0, DACK1 delay time 3*7		t_{DACD3}	—	20	ns	20.9, 20.13, 20.14, 20.19
DACK0, DACK1 delay time 4		t_{DACD4}	—	20	ns	20.11, 20.12
DACK0, DACK1 delay time 5		t_{DACD5}	—	20	ns	
Read delay time	35% duty*2	t_{RDD}	—	$t_{cyc} \times 0.35 + 12$	ns	20.8, 20.9, 20.11–20.15, 20.19
	50% duty		—	$t_{cyc} \times 0.5 + 15$	ns	
Data setup time for $\overline{CAS}$		t_{DS}	0*5	—	ns	20.11, 20.13
$\overline{CAS}$ setup time for $\overline{RAS}$		t_{CSR}	10	—	ns	20.16–20.18
Row address hold time		t_{RAH}	10	—	ns	20.11, 20.13
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*2	t_{WCS}	0	—	ns	20.11
	50% duty	t_{WCS}	0	—	ns	
Access time from $\overline{CAS}$ precharge*6		t_{ACP}	t_{cyc} –20	—	ns	20.12

Notes: 1. HBS and LBS signals are 25 ns.
2. When frequency is 10 MHz or more.
3. n is the number of wait cycles.
4. Access time from addresses A0 to A21 is tcyc-25 ns.
5. –5ns for parity output of DRAM long-pitch access.
6. It is not necessary to meet the t_{RDS} specification as long as the access time specification is met.
7. In the relationship of t_{CASD2} and t_{CASD3} with respect to t_{DACD3}, a Min-Max combination does not occur because of the logic structure.



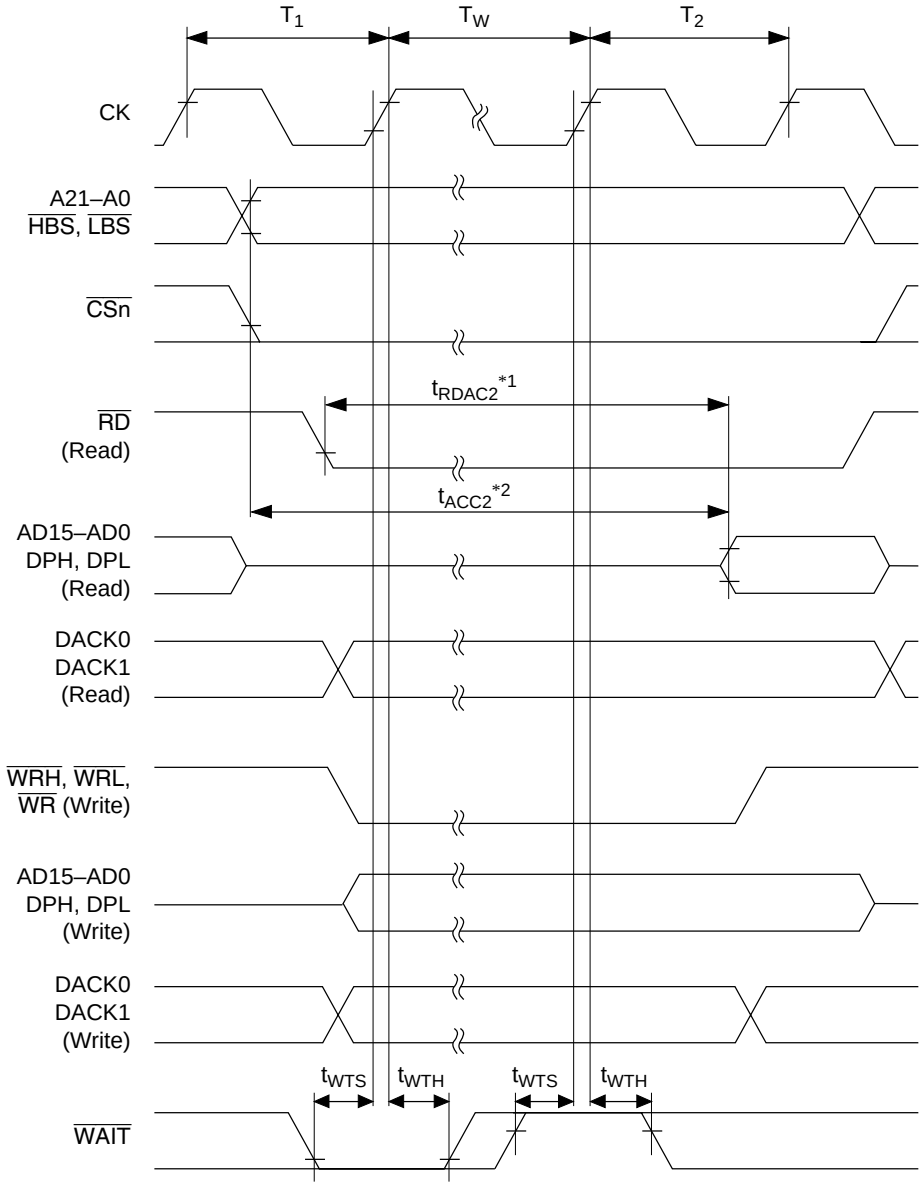
Notes: 1. For t_{RDAC1}, use $t_{cyc} \times 0.65 - 20$ (for 35% duty) or $t_{cyc} \times 0.5 - 20$ (for 50% duty) instead of $t_{cyc} - t_{RDD} - t_{RDS}$.
2. For t_{ACC1}, use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD}$ (or t_{CSD1}) – t_{RDS}.
3. t_{RDH} is measured from A21–A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.8 Basic Bus Cycle: One-State Access



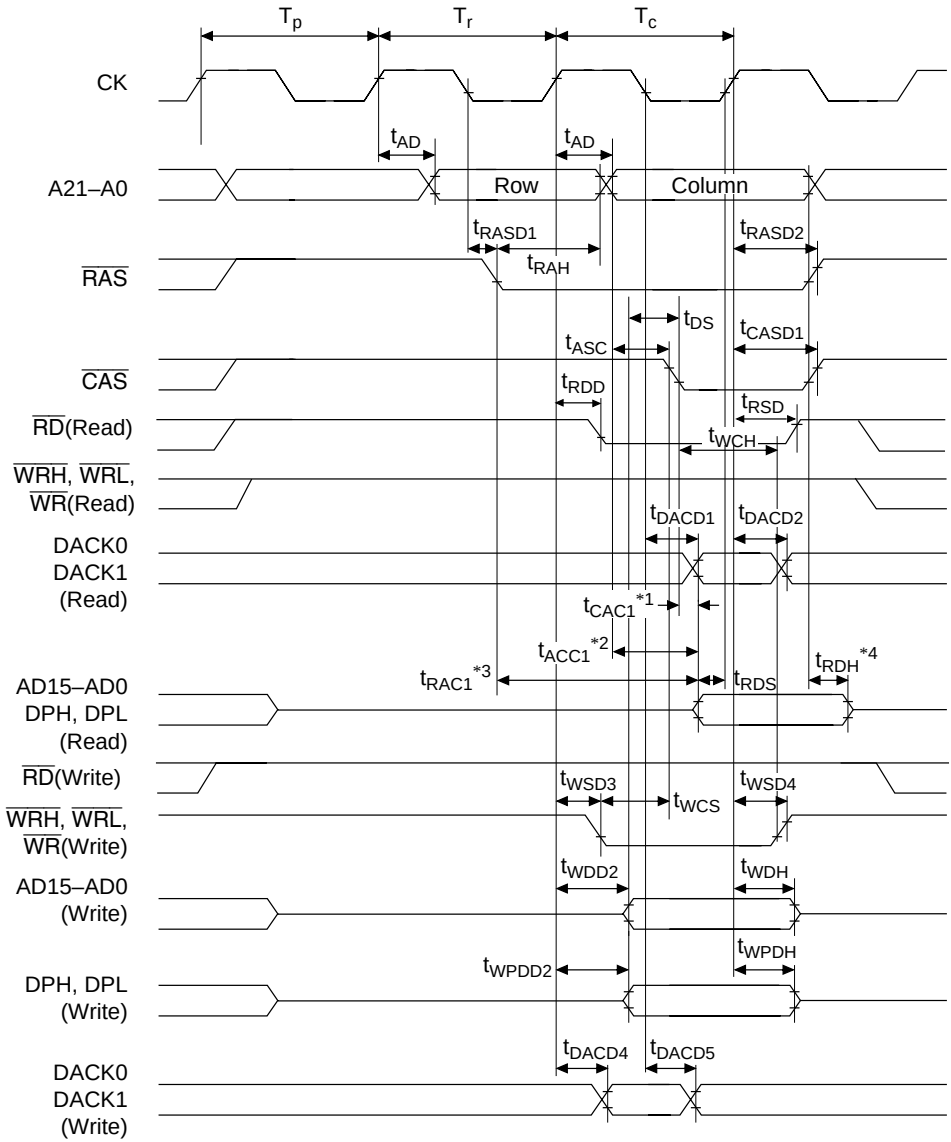
Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n + 1.65) - 20$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 20$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) – t_{RDS}.
3. t_{RDH} is measured from A21–A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.9 Basic Bus Cycle: Two-State Access



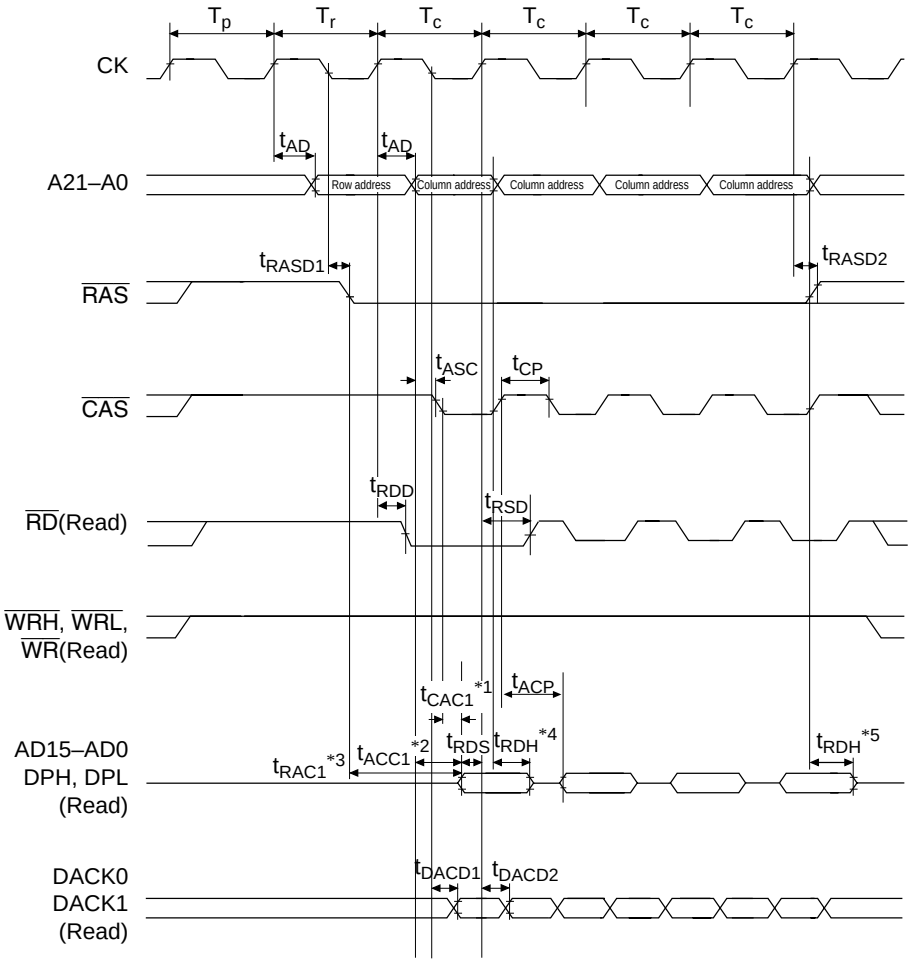
Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n+1.65) - 20$ (for 35% duty) or $t_{cyc} \times (n+1.5) - 20$ (for 50% duty) instead of $t_{cyc} \times (n+2) - t_{RDD} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n+2) - 30$ instead of $t_{cyc} \times (n+2) - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

Figure 20.10 Basic Bus Cycle: Two States + Wait State



Notes: 1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 19$ (for 35% duty) or $t_{cyc} \times 0.5 - 19$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
2. For t_{ACC1}, use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 20$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.11 DRAM Bus Cycle (Short-Pitch, Normal Mode)



Notes: 1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 19$ (for 35% duty) or $t_{cyc} \times 0.5 - 19$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
It is not necessary to meet the t_{RDS} specification as long as the t_{CAC1} specification is met.

2. For t_{ACC1}, use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
It is not necessary to meet the t_{RDS} specification as long as the t_{ACC1} specification is met.

3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 20$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
It is not necessary to meet the t_{RDS} specification as long as the t_{RAC1} specification is met.

4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.

5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.12 (a) DRAM Bus Cycle (Short-Pitch, High-Speed Page Mode: Read)

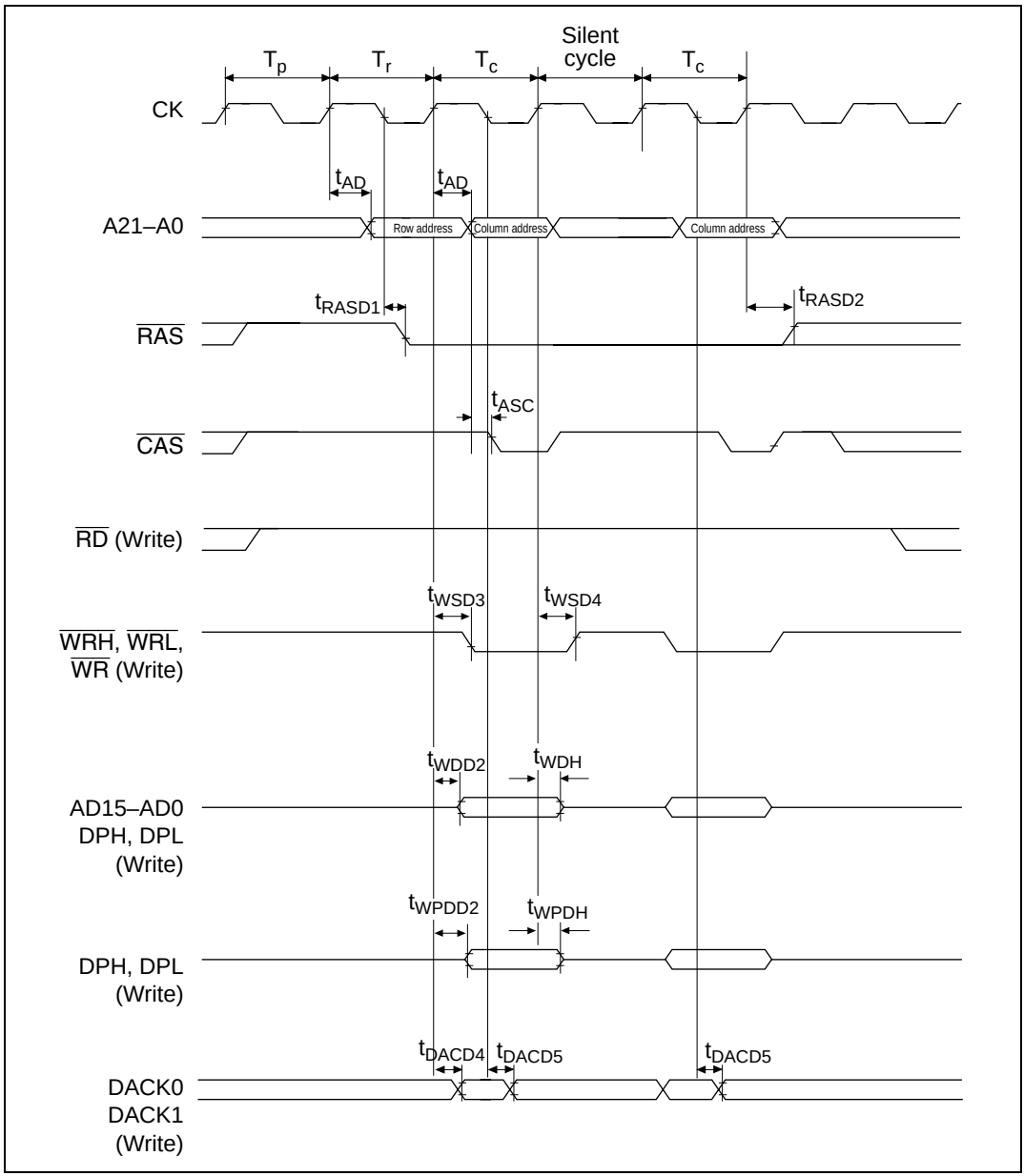
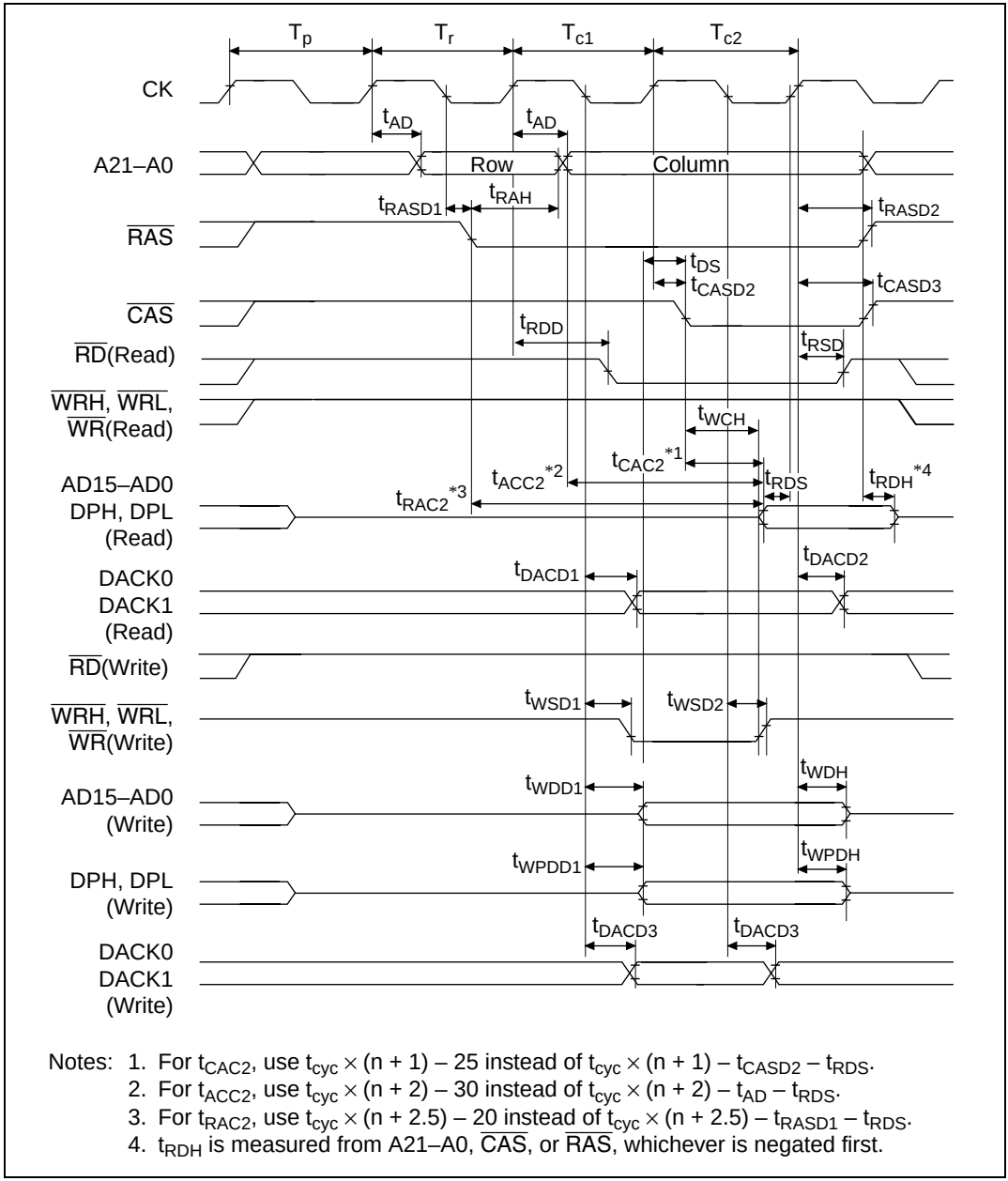


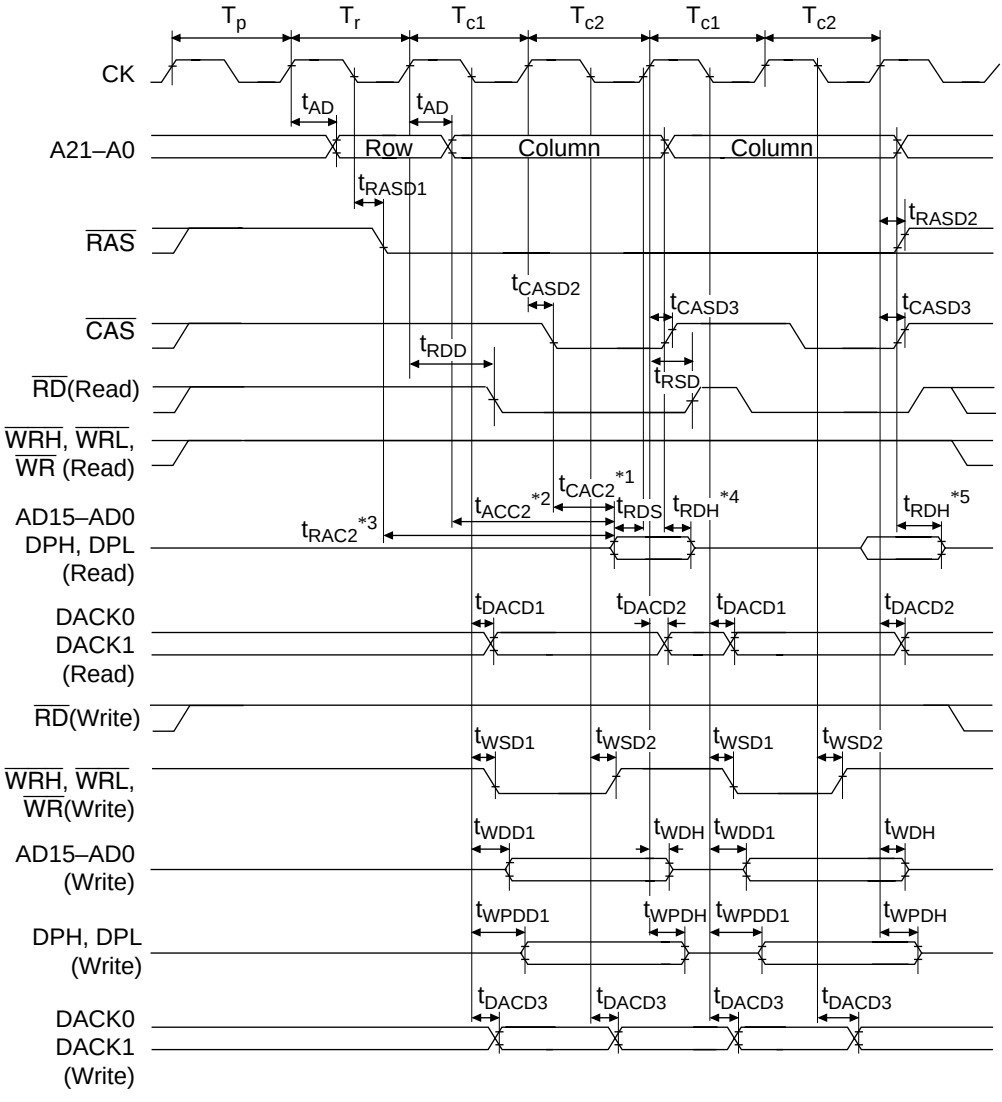
Figure 20.12 (b) DRAM Bus Cycle (Short-Pitch, High-Speed Page Mode: Write)

Note: For details of the silent cycle, see section 8.5.5, DRAM Burst Mode.



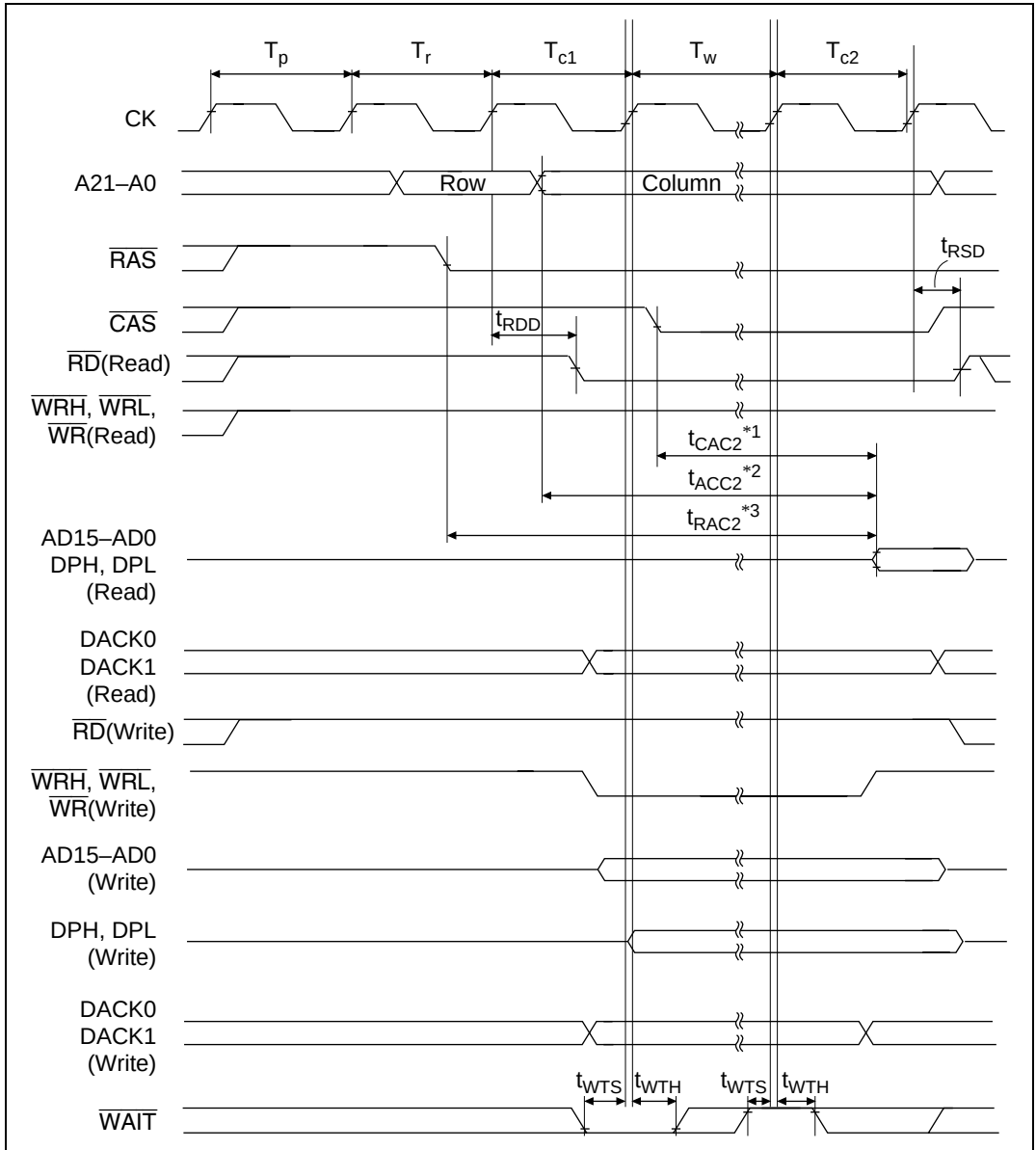
Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0, $\overline{CAS}$, or $\overline{RAS}$, whichever is negated first.

Figure 20.13 DRAM Bus Cycle: (Long-Pitch, Normal Mode)



Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD2} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.
5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$ whichever is negated first.

Figure 20.14 DRAM Bus Cycle: (Long-Pitch, High-Speed Page Mode)



Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.

Figure 20.15 DRAM Bus Cycle: (Long-Pitch, High-Speed Page Mode + Wait State)

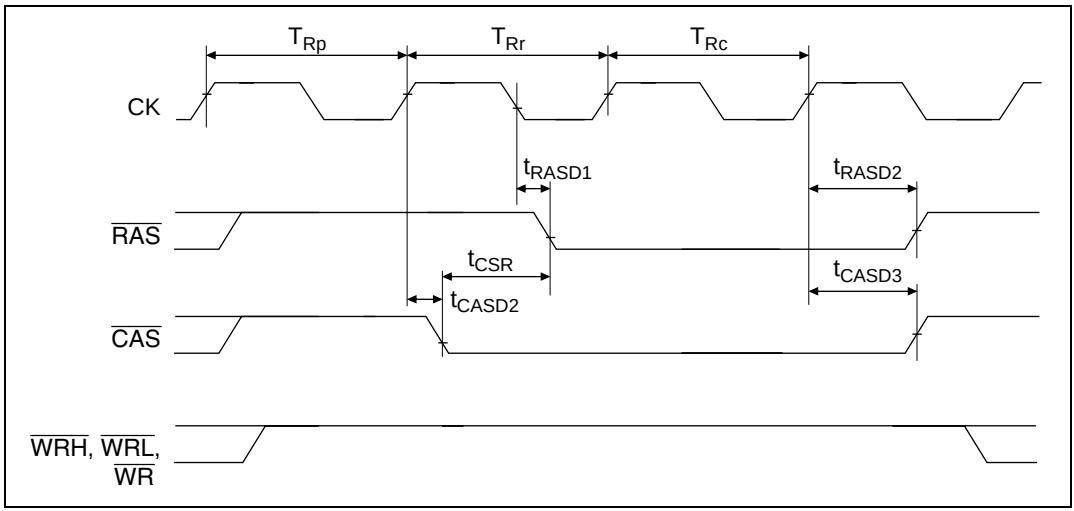


Figure 20.16 CAS-before-RAS Refresh (Short-Pitch)

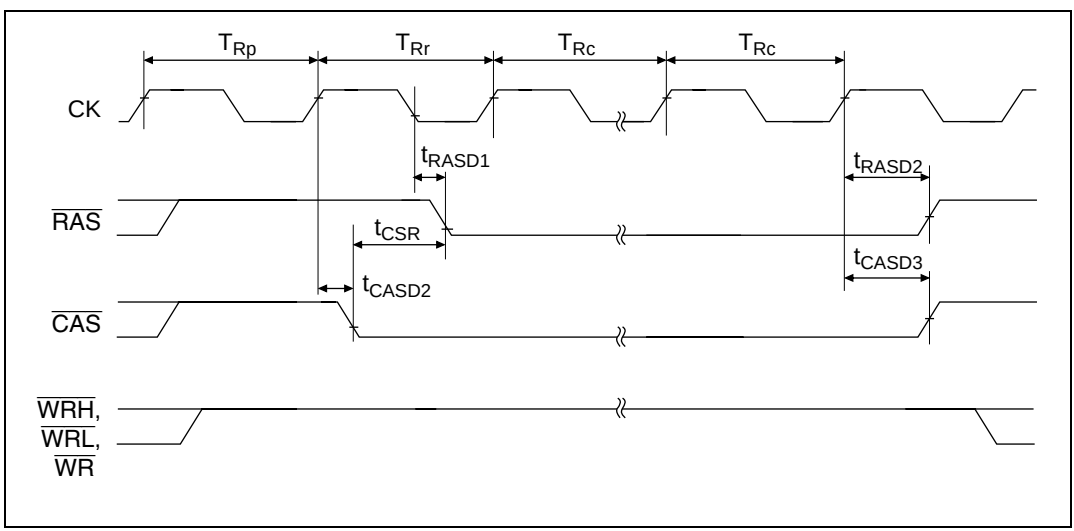


Figure 20.17 CAS-before-RAS Refresh (Long-Pitch)

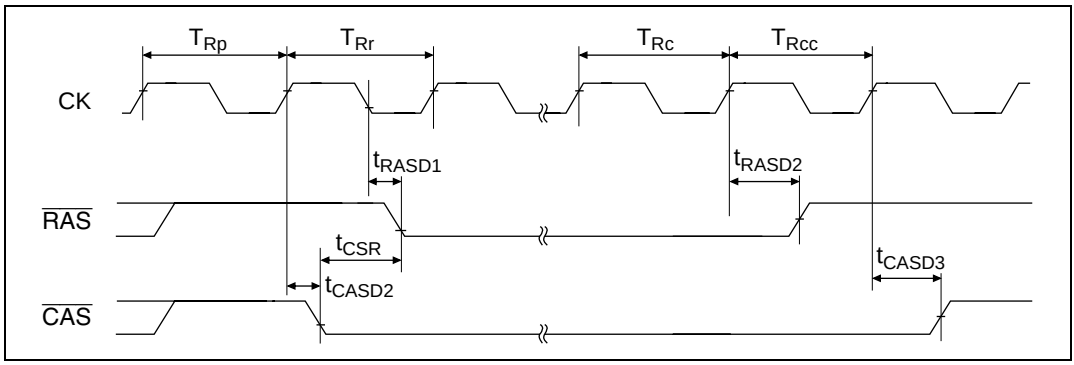


Figure 20.18 Self-Refresh

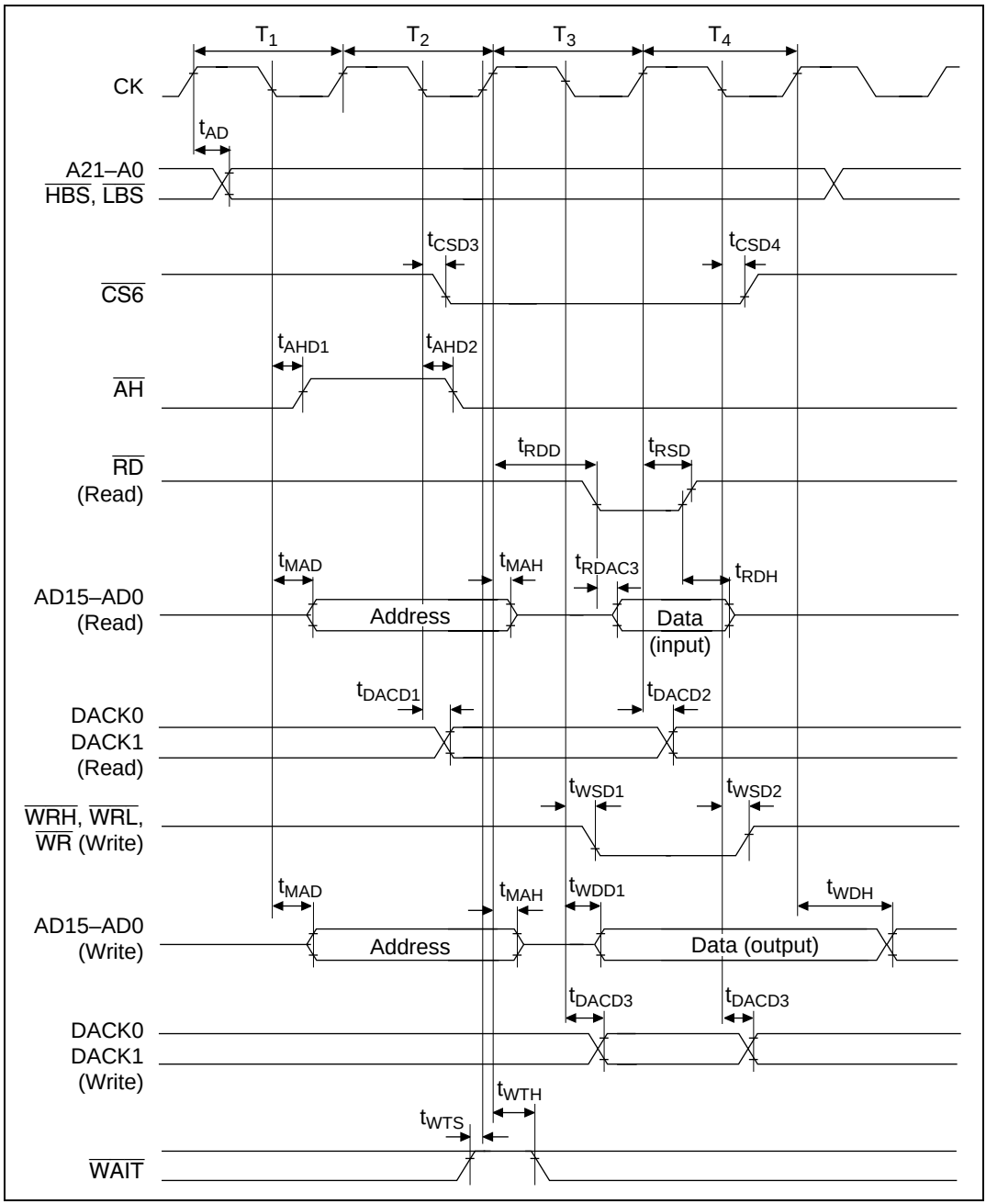


Figure 20.19 Address/Data Multiplex I/O Bus Cycle

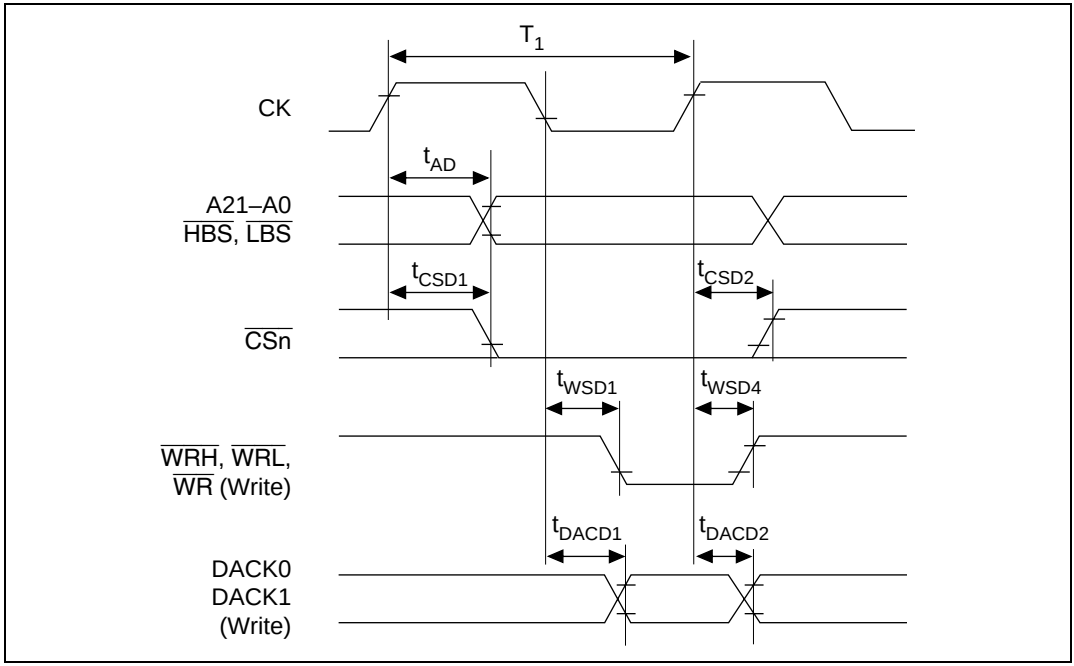


Figure 20.20 DMA Single Transfer/One-State Access Write

Table 20.7 Bus Timing (2)

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 12.5 MHz, Ta = –20 to +75°C*

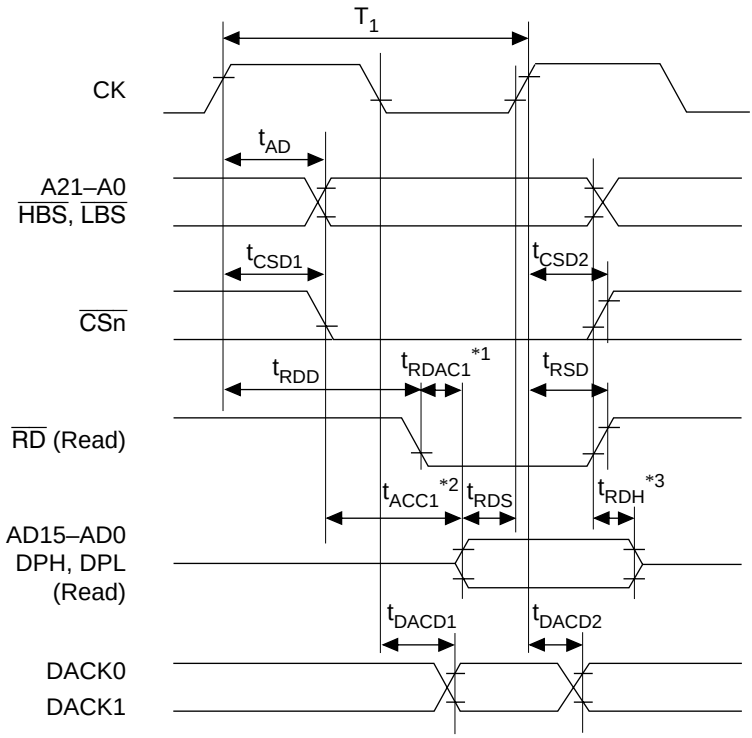
Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item		Symbol	Min	Max	Unit	Figures
Address delay time		t_{AD}	—	40	ns	20.21, 20.22, 20.24–20.27, 20.32, 20.33
$\overline{CS}$ delay time 1		t_{CSD1}	—	40	ns	20.21, 20.22, 20.33
$\overline{CS}$ delay time 2		t_{CSD2}	—	40	ns	
$\overline{CS}$ delay time 3		t_{CSD3}	—	40	ns	20.32
$\overline{CS}$ delay time 4		t_{CSD4}	—	40	ns	
Access time 1*4 from read strobe	35% duty*1	t_{RDAC1}	$t_{cyc} \times 0.65 - 35$	—	ns	20.21,
	50% duty		$t_{cyc} \times 0.5 - 35$	—	ns	
Access time 2*4 from read strobe	35% duty*1	t_{RDAC2}	$t_{cyc} \times (n+1.65) - 35$*2	—	ns	20.22, 20.23
	50% duty		$t_{cyc} \times (n+1.5) - 35$*2	—	ns	
Access time 3*4 from read strobe	35% duty*1	t_{RDAC3}	$t_{cyc} \times (n+0.65) - 35$*2	—	ns	20.32
	50% duty		$t_{cyc} \times (n+0.5) - 35$*2	—	ns	
Read strobe delay time		t_{RSD}	—	40	ns	20.21, 20.22, 20.24–20.28, 20.32
Read data setup time		t_{RDS}	25	—	ns	20.21, 20.22,
Read data hold time		t_{RDH}	0	—	ns	20.24-20.27, 20.32
Write strobe delay time 1		t_{WSD1}	—	40	ns	20.22, 20.26, 20.27, 20.32, 20.33
Write strobe delay time 2		t_{WSD2}	—	30	ns	20.22, 20.26, 20.27, 20.32
Write strobe delay time 3		t_{WSD3}	—	40	ns	20.24, 20.25
Write strobe delay time 4		t_{WSD4}	—	40	ns	20.24, 20.25, 20.33
Write data delay time 1		t_{WDD1}	—	70	ns	20.22, 20.26, 20.27, 20.32
Write data delay time 2		t_{WDD2}	—	40	ns	20.24, 20.26
Write data hold time		t_{WDH}	–10	—	ns	20.22, 20.24–20.27, 20.32
Parity output delay time 1		t_{WPDD1}	—	80	ns	20.22, 20.24, 20.27
Parity output delay time 2		t_{WPDD2}	—	40	ns	20.24, 20.25
Parity output hold time		t_{WPDH}	–10	—	ns	20.22, 20.23–20.27

Item		Symbol	Min	Max	Unit	Figures
Wait setup time		t_{WTS}	40	—	ns	20.23, 20.28, 20.32
Wait hold time		t_{WTH}	10	—	ns	
Read data access time 1*4		t_{ACC1}	$t_{cyc} - 44$	—	ns	20.21, 20.24, 20.25
Read data access time 2*4		t_{ACC2}	$t_{cyc} \times (n+2) - 44$*2	—	ns	20.22, 20.23, 20.26–20.28
$\overline{RAS}$ delay time 1		t_{RASD1}	—	40	ns	20.24–20.27, 20.29–20.31
$\overline{RAS}$ delay time 2		t_{RASD2}	—	40	ns	
$\overline{CAS}$ delay time 1		t_{CASD1}	—	40	ns	20.24
$\overline{CAS}$ delay time 2*5		t_{CASD2}	—	40	ns	20.26, 20.27, 20.29–20.31
$\overline{CAS}$ delay time 3*5		t_{CASD3}	—	40	ns	
Column address setup time		t_{ASC}	0	—	ns	20.24, 20.25
Read data access time from $\overline{CAS}$ 1*4	35% duty*1	t_{CAC1}	$t_{cyc} \times 0.65 - 35$	—	ns	
	50% duty		$t_{cyc} \times 0.5 - 35$	—	ns	
Read data access time from $\overline{CAS}$ 2*4		t_{CAC2}	$t_{cyc} \times (n+1) - 35$*2	—	ns	20.26–20.28
Read data access time from $\overline{RAS}$ 1*4		t_{RAC1}	$t_{cyc} \times 1.5 - 35$	—	ns	20.24, 20.25
Read data access time from $\overline{RAS}$ 2*4		t_{RAC2}	$t_{cyc} \times (n+2.5) - 35$*2	—	ns	20.26–20.28
High-speed page mode $\overline{CAS}$ precharge time		t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.25
$\overline{AH}$ delay time 1		t_{AHD1}	—	40	ns	20.32
$\overline{AH}$ delay time 2		t_{AHD2}	—	40	ns	
Multiplexed address delay time		t_{MAD}	—	40	ns	
Multiplexed address hold time		t_{MAH}	–10	—	ns	

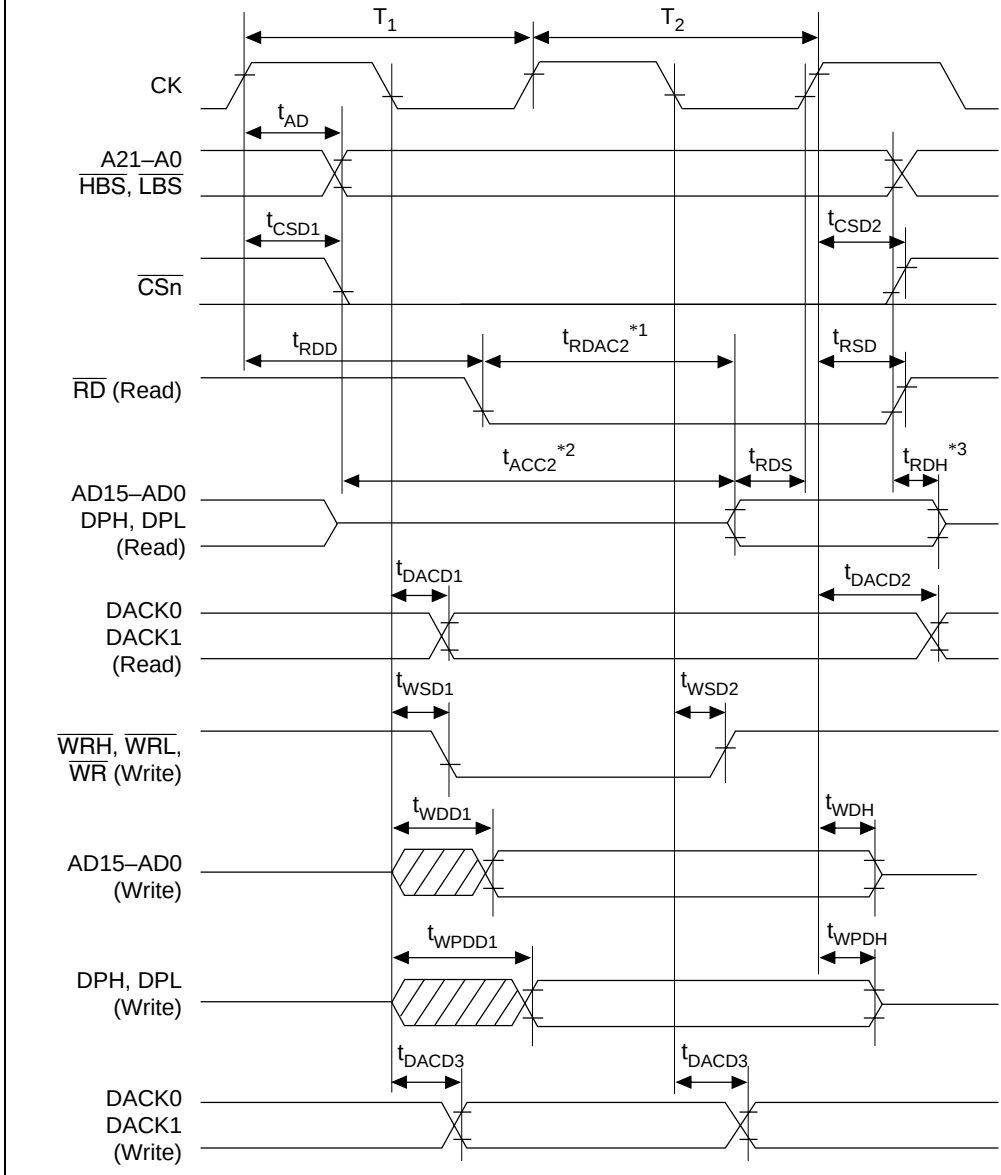
Item		Symbol	Min	Max	Unit	Figures
DACK0, DACK1 delay time 1		t_{DACD1}	—	40	ns	20.21, 20.22, 20.24–20.27, 20.32, 20.33
DACK0, DACK1 delay time 2		t_{DACD2}	—	40	ns	
DACK0, DACK1 delay time 3*5		t_{DACD3}	—	40	ns	20.22, 20.26, 20.27, 20.32
DACK0, DACK1 delay time 4		t_{DACD4}	—	40	ns	20.24, 20.25
DACK0, DACK1 delay time 5		t_{DACD5}	—	40	ns	
Read delay time	35% duty*1	t_{RDD}	—	$t_{cyc} \times 0.35 + 35$	ns	20.21, 20.22, 20.24-20.28, 20.32
	50% duty		—	$t_{cyc} \times 0.5 + 35$	ns	
Data setup time for $\overline{CAS}$		t_{DS}	0*3	—	ns	20.24, 20.26
$\overline{CAS}$ setup time for $\overline{RAS}$		t_{CSR}	10	—	ns	20.29–20.31
Row address hold time		t_{RAH}	10	—	ns	20.24, 20.26
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*1	t_{WCS}	0	—	ns	20.24
	50% duty	t_{WCS}	0	—	ns	
Access time from $\overline{CAS}$ precharge*4		t_{ACP}	tcyc –20	—	ns	20.25

Notes: 1. When frequency is 10 MHz or more.
2. n is the number of wait cycles.
3. –5 ns for parity output of DRAM long-pitch access
4. It is not necessary to meet the t_{RDS} specification as long as the access time specification is met.
5. In the relationship of t_{CASD2} and t_{CASD3} with respect to t_{DACD3}, a Min-Max combination does not occur because of the logic structure.



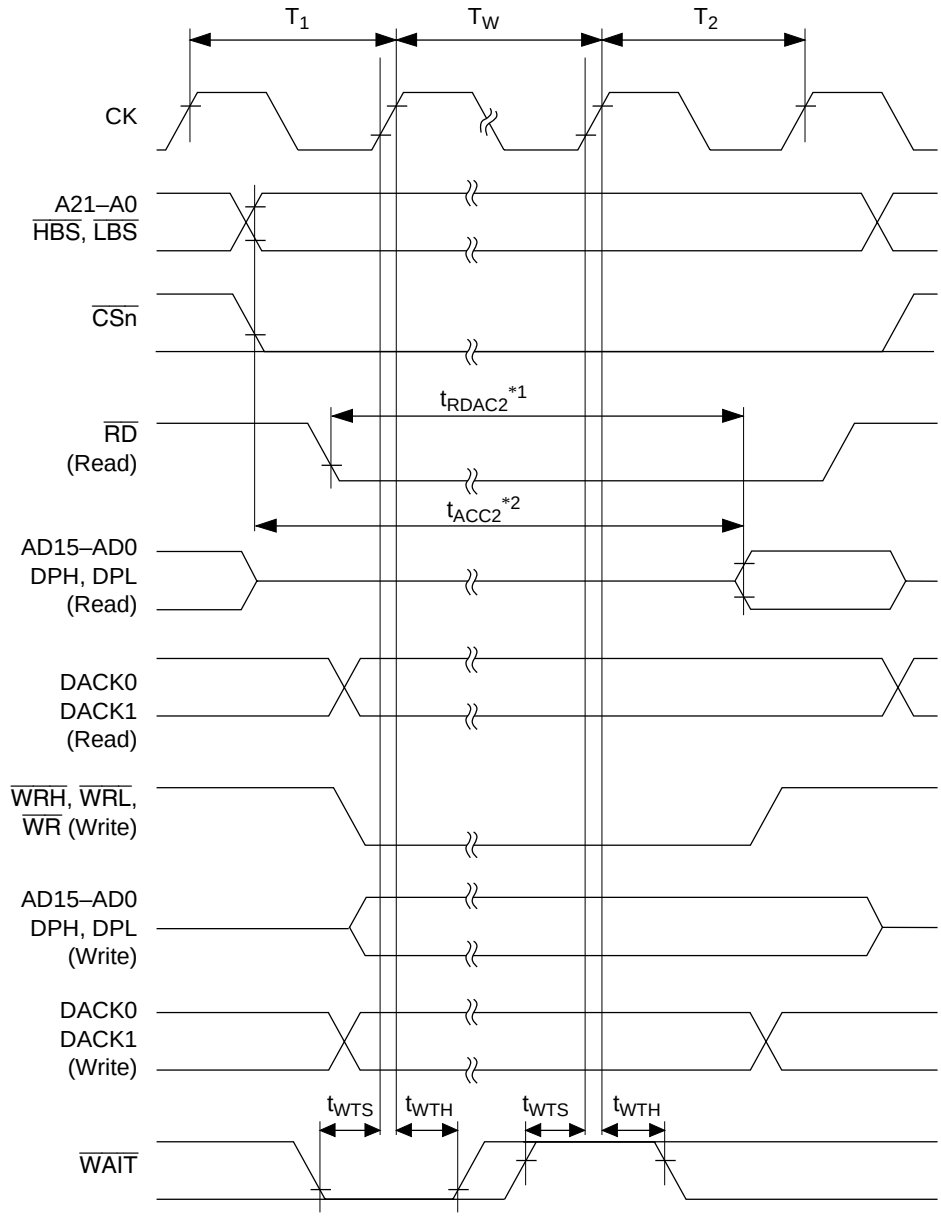
Notes: 1. For t_{RDAC1}, use $t_{cyc} \times 0.65 - 35$ (for 35% duty) or $t_{cyc} \times 0.5 - 35$ (for 50% duty) instead of $t_{cyc} - t_{RDD} - t_{RDS}$.
2. For t_{ACC1}, use $t_{cyc} - 44$ instead of $t_{cyc} - t_{AD}$ (or t_{CSD1}) – t_{RDS}.
3. t_{RDH} is measured from A21–A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.21 Basic Bus Cycle: One-State Access



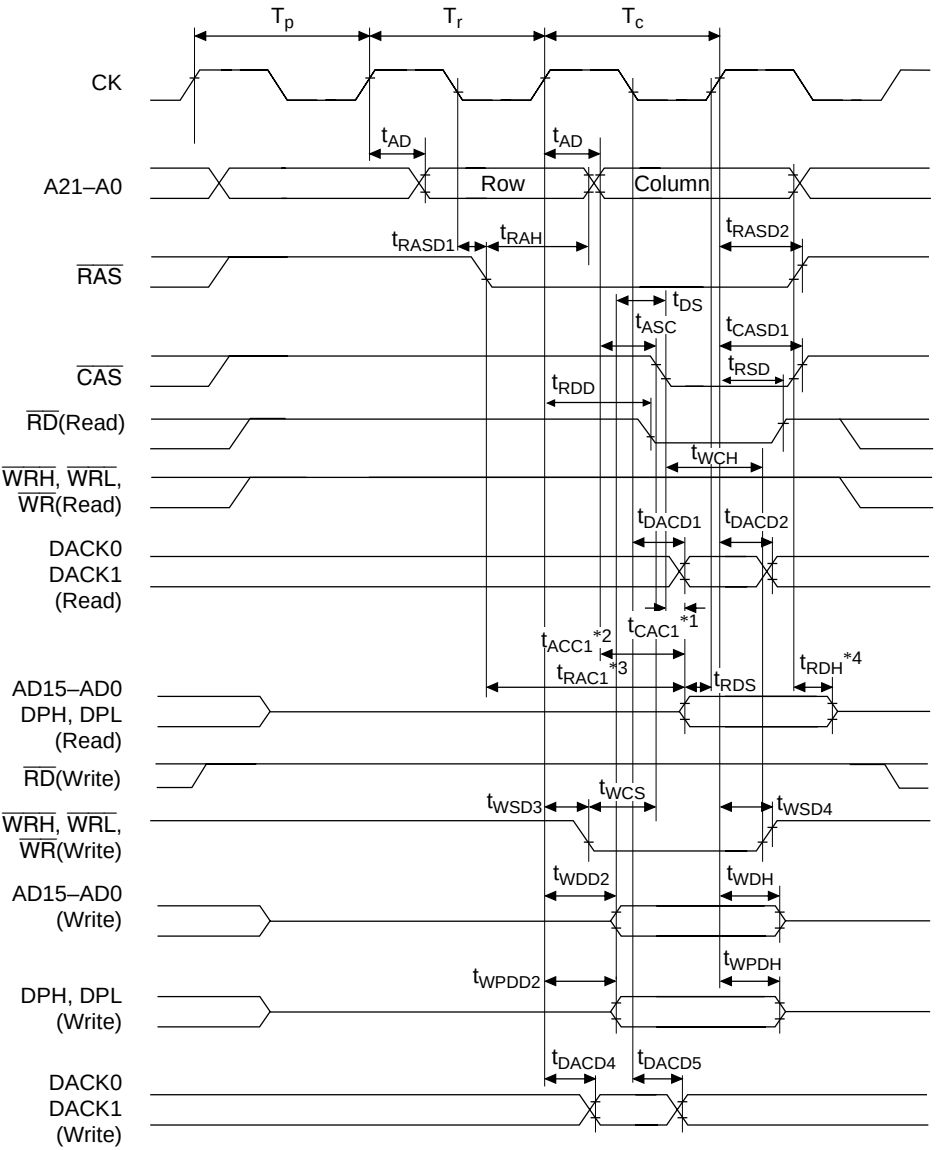
Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n + 1.65) - 35$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 35$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) – t_{RDS}.
3. t_{RDH} is measured from A21-A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.22 Basic Bus Cycle: Two-State Access



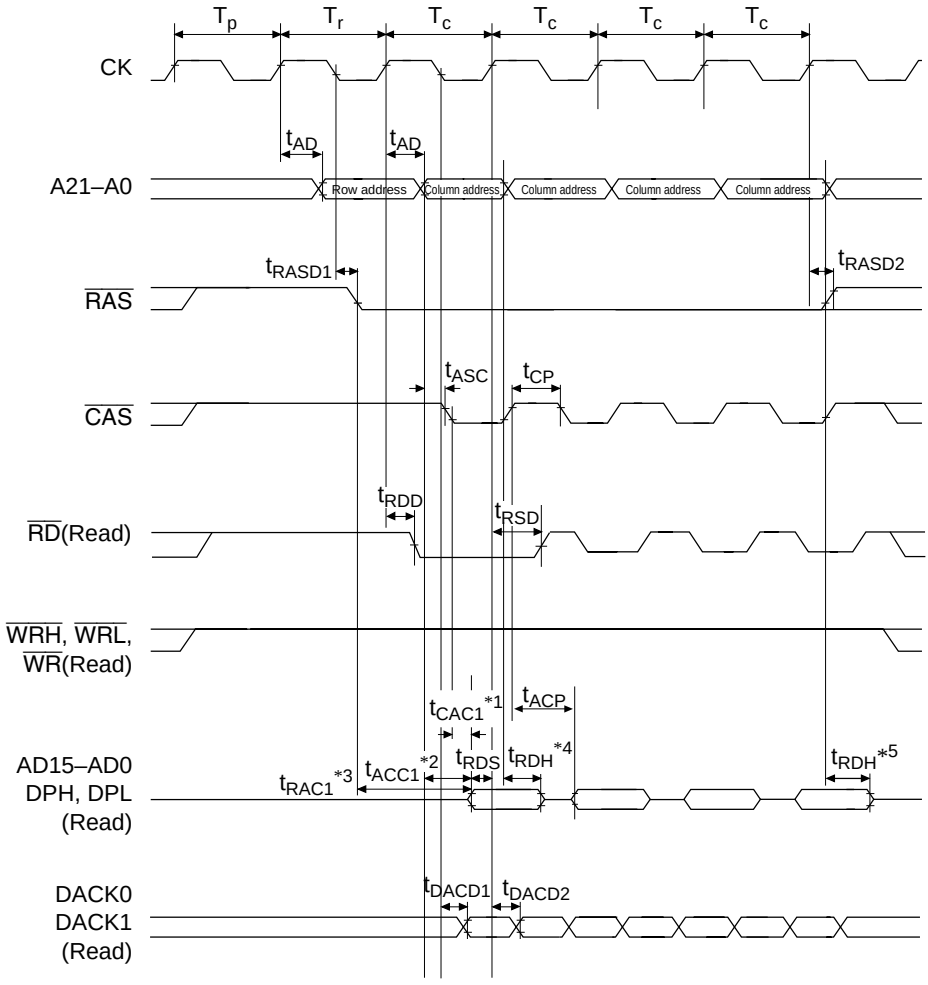
Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n + 1.65) - 35$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 35$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.
2. For t_{ACC2}, use tcyc $\times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

Figure 20.23 Basic Bus Cycle: Two States + Wait State



Notes: 1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 35$ (for 35% duty) or $t_{cyc} \times 0.5 - 35$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
2. For t_{ACC1}, use $t_{cyc} - 44$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 35$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.24 DRAM Bus Cycle (Short-Pitch, Normal Mode)



Notes: 1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 35$ (for 35% duty) or tcyc $\times$ 0.5 – 35 (for 50% duty) instead of tcyc – t_{AD} – t_{ASC} – t_{RDS}.
It is not necessary to meet the t_{RDS} specification as long as the t_{CAC1} specification is met.
2. For t_{ACC1}, use t_{cyc} – 44 instead of t_{cyc} – t_{AD} – t_{RDS}.
It is not necessary to meet the t_{RDS} specification as long as the t_{ACC1} specification is met.
3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 35$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
It is not necessary to meet the t_{RDS} specification as long as the t_{RAC1} specification is met.
4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.
5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.25 (a) DRAM Bus Cycle (Short-Pitch, High-Speed Page Mode: Read)

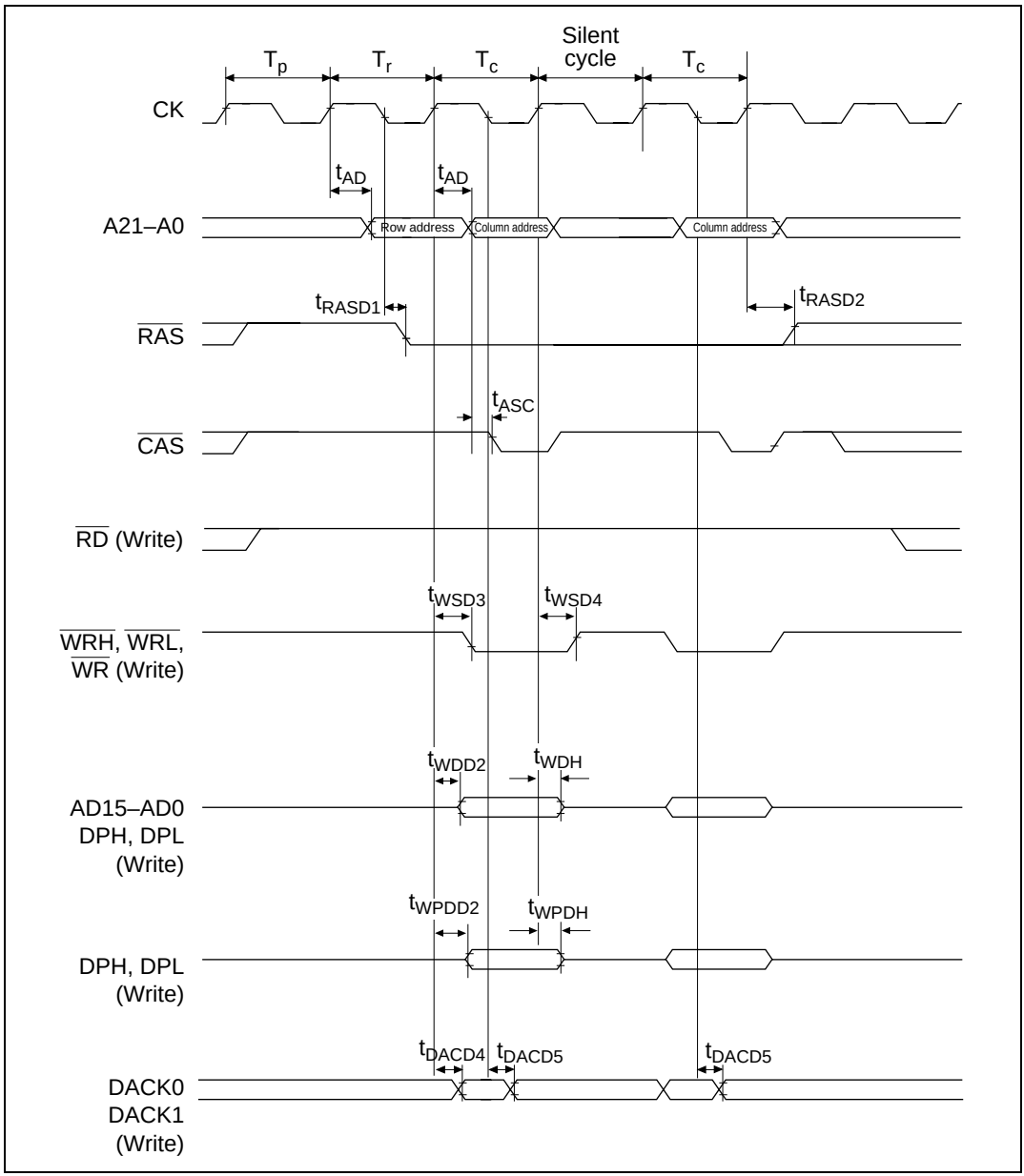
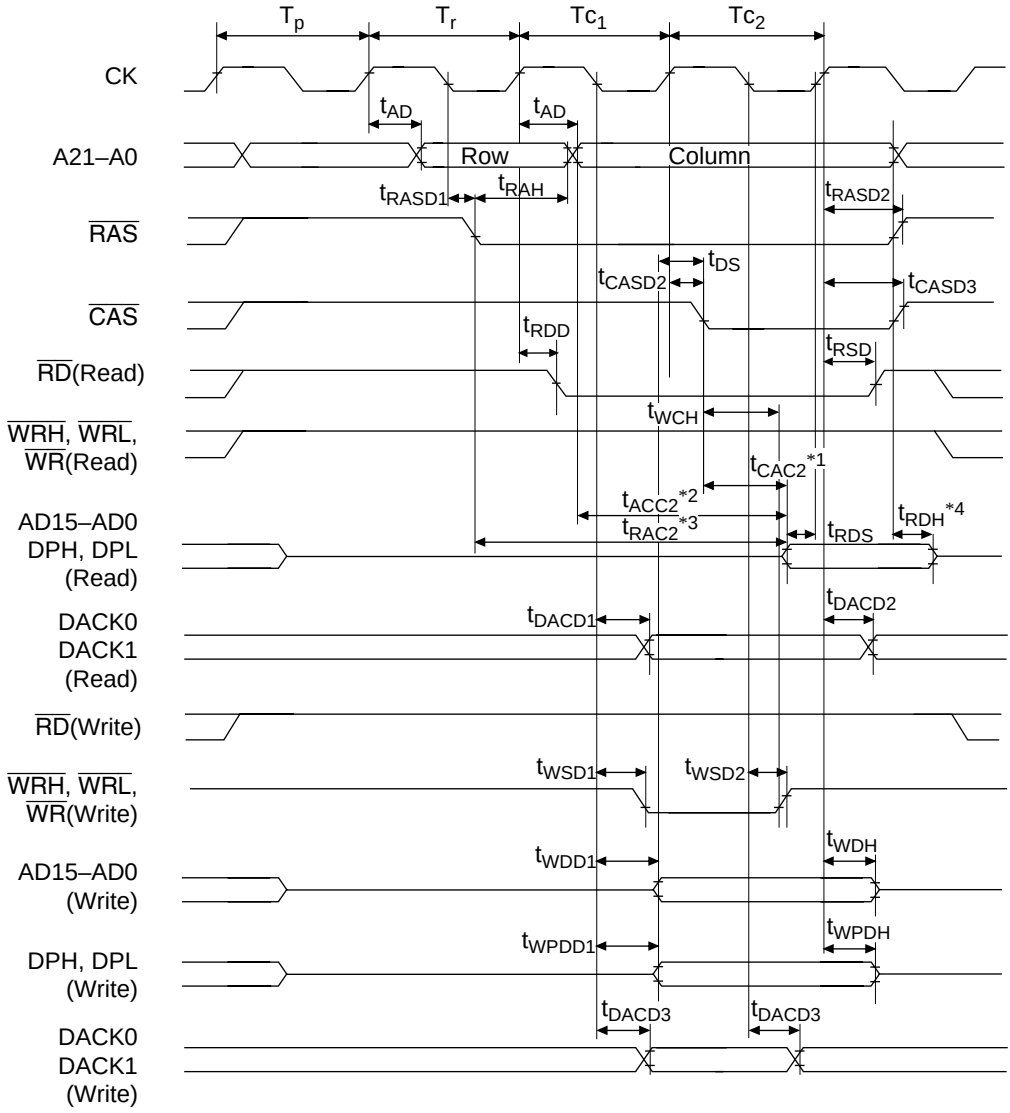


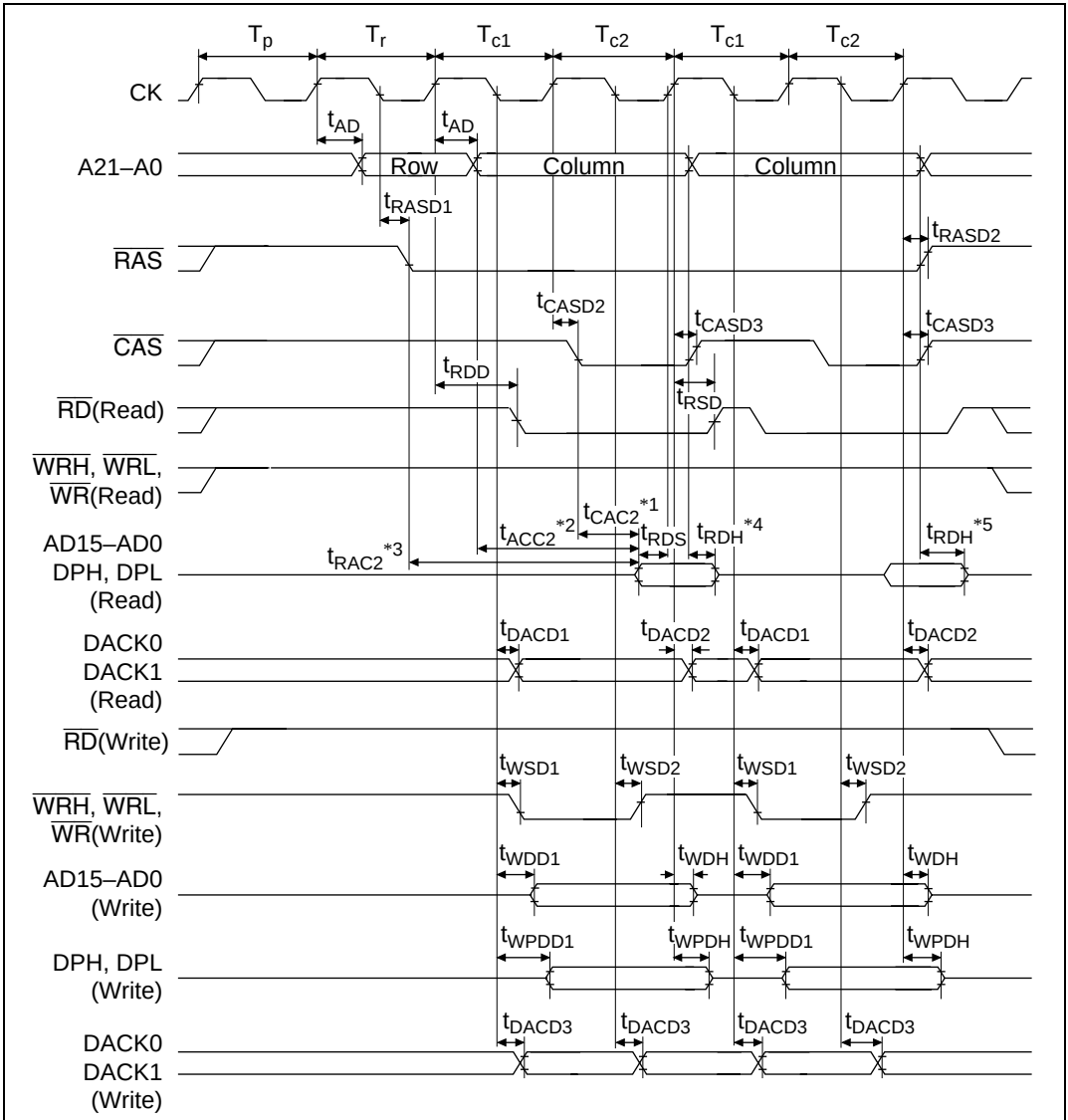
Figure 20.25 (b) DRAM Bus Cycle (Short-Pitch, High-Speed Page Mode: Write)

Note: For details of the silent cycle, see section 8.5.5, DRAM Burst Mode.



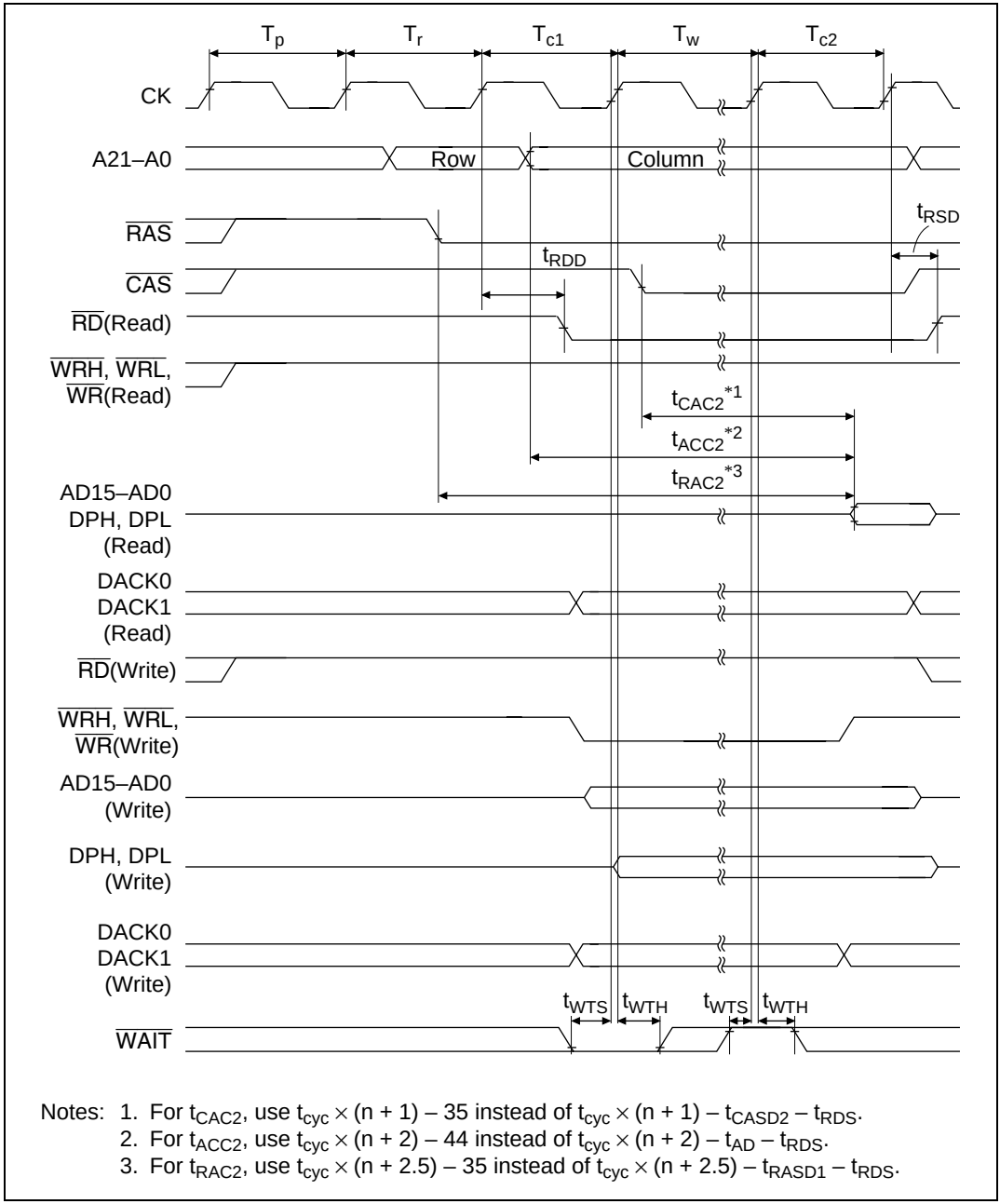
Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 35$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 35$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0, $\overline{CAS}$, or $\overline{RAS}$, whichever is negated first.

Figure 20.26 DRAM Bus Cycle: (Long-Pitch, Normal Mode)



Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 35$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 35$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD2} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.
5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$ whichever is negated first.

Figure 20.27 DRAM Bus Cycle: (Long-Pitch, High-Speed Page Mode)



Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 35$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 35$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.

Figure 20.28 DRAM Bus Cycle: (Long-Pitch, High-Speed Page Mode + Wait State)

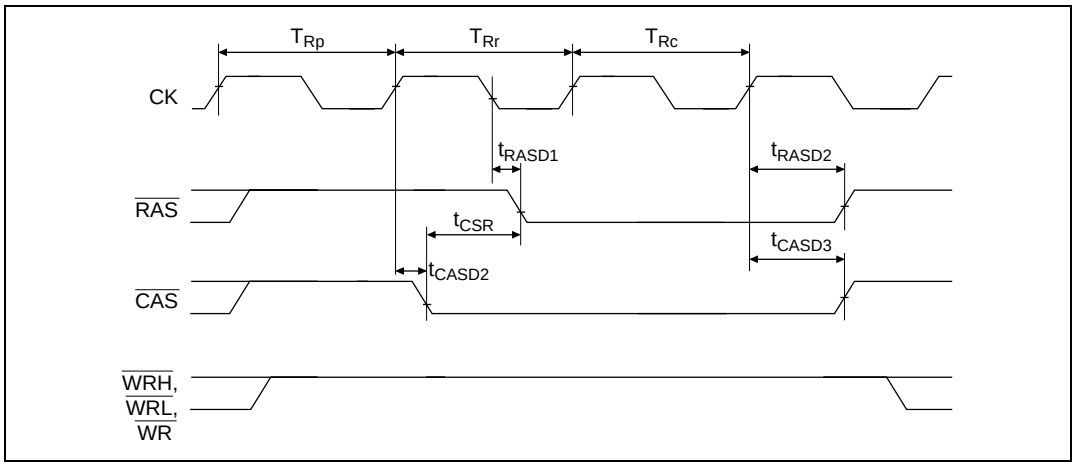


Figure 20.29 CAS-before-RAS Refresh (Short-Pitch)

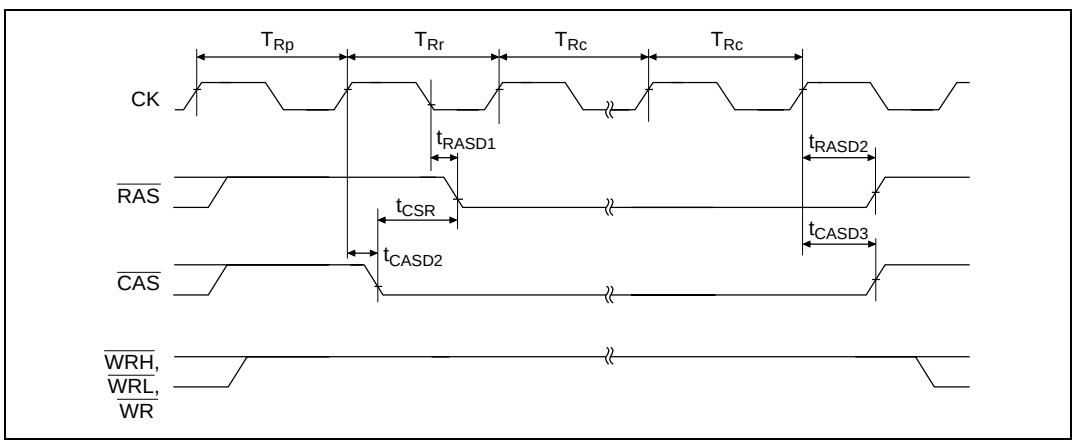


Figure 20.30 CAS-before-RAS Refresh (Long-Pitch)

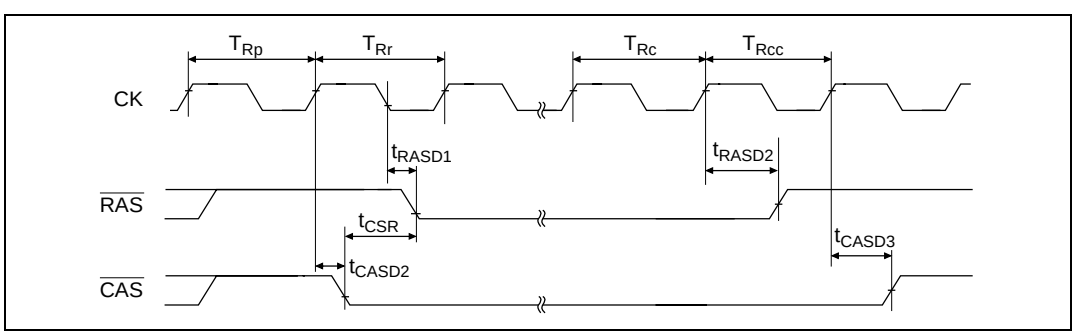


Figure 20.31 Self-Refresh

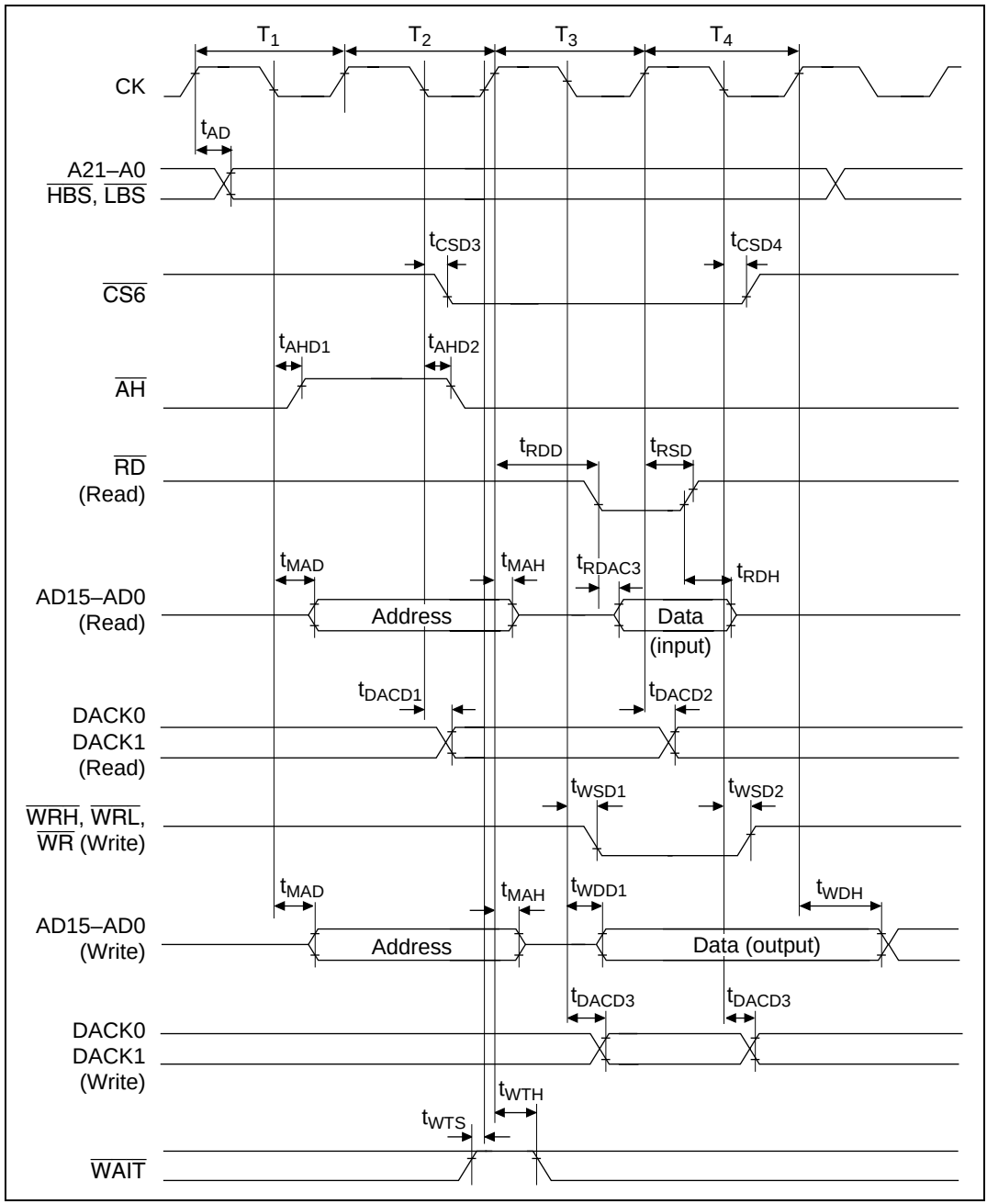


Figure 20.32 Address/Data Multiplex I/O Bus Cycle

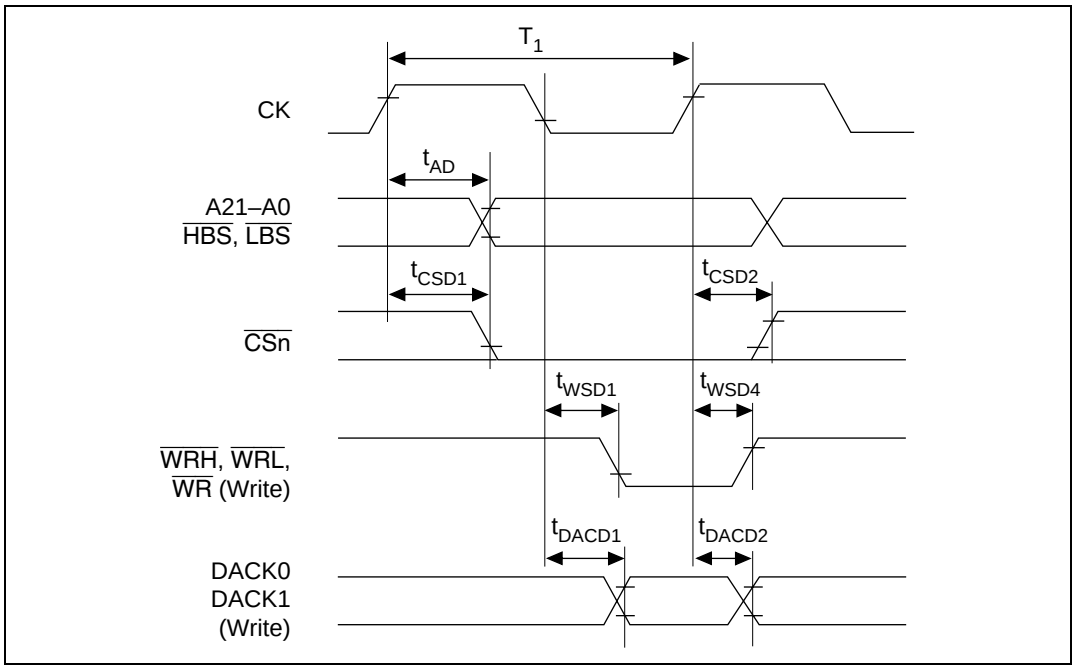


Figure 20.33 DMA Single Transfer/One-State Access Write

(4) DMAC Timing

Table 20.8 DMAC Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		Case A		Case B			
		12.5 MHz		20 MHz			
Item	Symbol	Min	Max	Min	Max	Unit	Figure
$\overline{DREQ0}$, $\overline{DREQ1}$ setup time	t_{DRQS}	80	—	27	—	ns	20.34
$\overline{DREQ0}$, $\overline{DREQ1}$ hold time	t_{DRQH}	30	—	30	—	ns	
$\overline{DREQ0}$, $\overline{DREQ1}$ Pulse width	t_{DRQW}	1.5	—	1.5	—	t_{cyc}	20.35

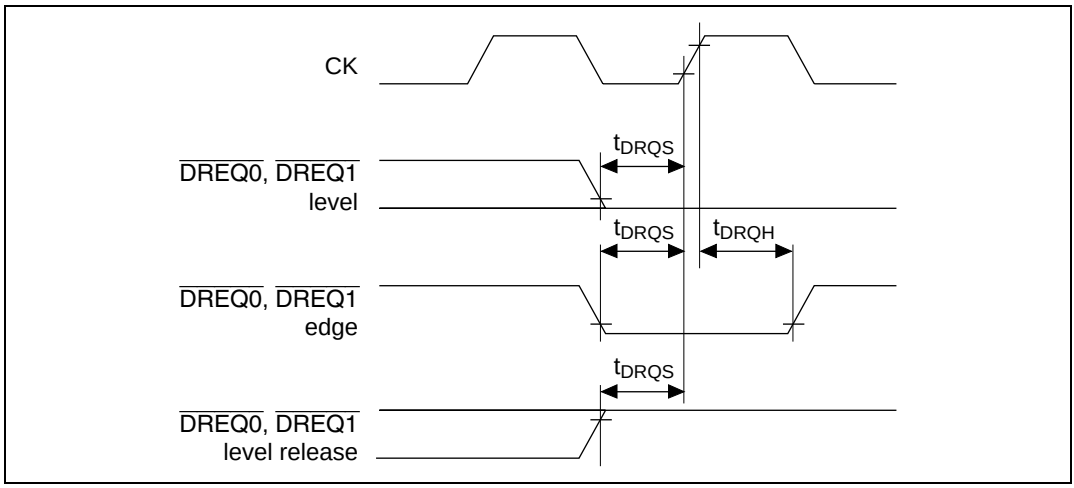


Figure 20.34 $\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ Input Timing (1)

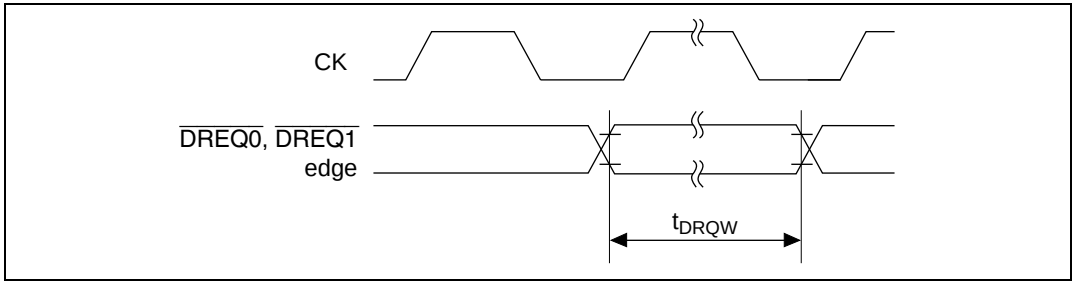


Figure 20.35 $\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ Input Timing (2)

(5) 16-bit Integrated Timer Pulse Unit Timing

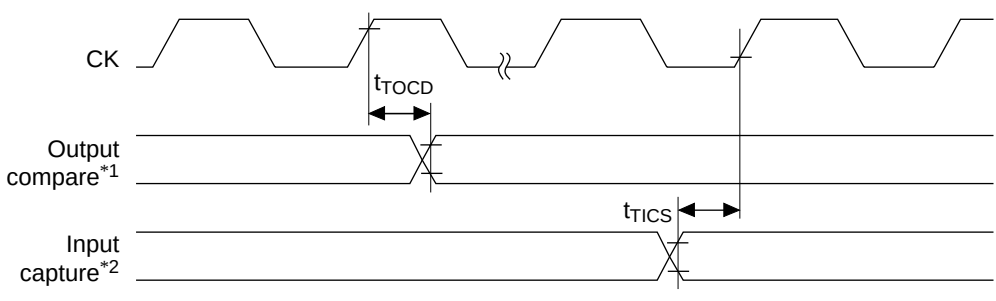
Table 20.9 16-bit Integrated Timer Pulse Unit Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		Case A		Case B			
		12.5 MHz		20 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Figure**
Output compare delay time	t_{TOCD}	—	100	—	100	ns	20.36
Input capture setup time	t_{TICS}	50	—	35	—	ns	
Timer clock input setup time	t_{TCKS}	50	—	50	—	ns	20.37
Timer clock pulse width (single edge)	$t_{TCKWH/L}$	1.5	—	1.5	—	t_{cyc}	
Timer clock pulse width (both edges)	$t_{TCKWL/L}$	2.5	—	2.5	—	t_{cyc}	



Notes: 1. TIOCA0-TIOCA4, TIOCB0-TIOCB4, TOCXA4, TOCXB4
2. TIOCA0-TIOCA4, TIOCB0-TIOCB4

Figure 20.36 ITU Input/Output Timing

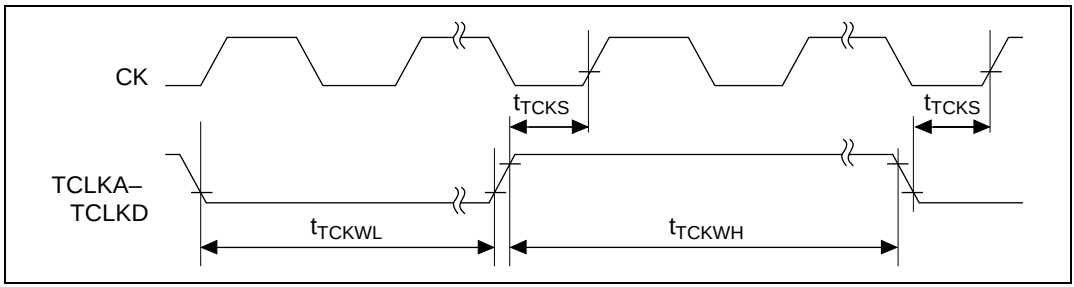


Figure 20.37 ITU Clock Input Timing

(6) Programmable Timing Pattern Controller and I/O Port Timing

Table 20.10 Programmable Timing Pattern Controller and I/O Port Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 12.5 MHz, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 20 MHz, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		Cases A and B			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Figure**
Port output delay time	t_{PWD}	—	100	ns	20.38
Port input hold time	t_{PRH}	50	—	ns	
Port input setup time	t_{PRS}	50	—	ns	

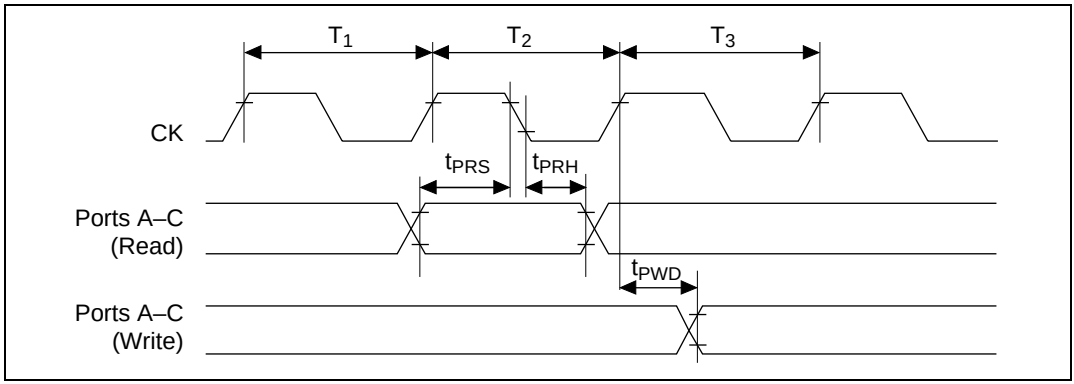


Figure 20.38 Programmable Timing Pattern Controller Output Timing

(7) Watchdog Timer Timing

Table 20.11 Watchdog Timer Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		Cases A and B			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Figure**
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	100	ns	20.39

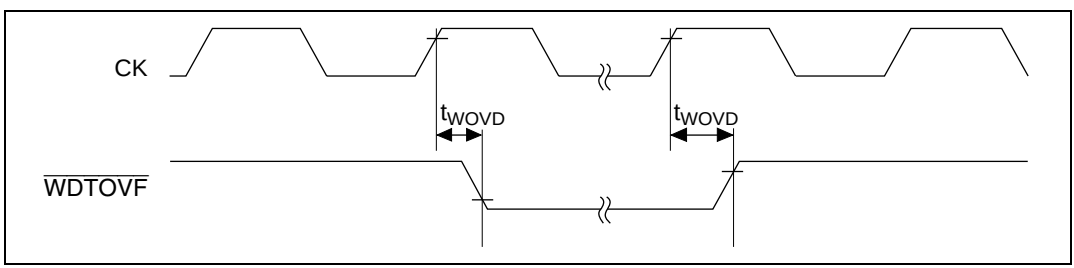


Figure 20.39 Watchdog Timer Output Timing

(8) Serial Communication Interface Timing

Table 20.12 Serial Communication Interface Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 12.5 MHz, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, f = 20 MHz, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		Cases A and B			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Figure**
Input clock cycle	t_{scyc}	4	—	t_{cyc}	20.40
Input clock cycle (synchronous mode)	t_{scyc}	6	—	t_{cyc}	
Input clock pulse width	t_{sckw}	0.4	0.6	t_{scyc}	
Input clock rise time	t_{sckr}	—	1.5	t_{cyc}	
Input clock fall time	t_{sckf}	—	1.5	t_{cyc}	
Transmit data delay time (synchronous mode)	t_{TXD}	—	100	ns	20.41
Receive data setup time (synchronous mode)	t_{RXS}	100	—	ns	
Receive data hold time (synchronous mode)	t_{RXH}	100	—	ns	

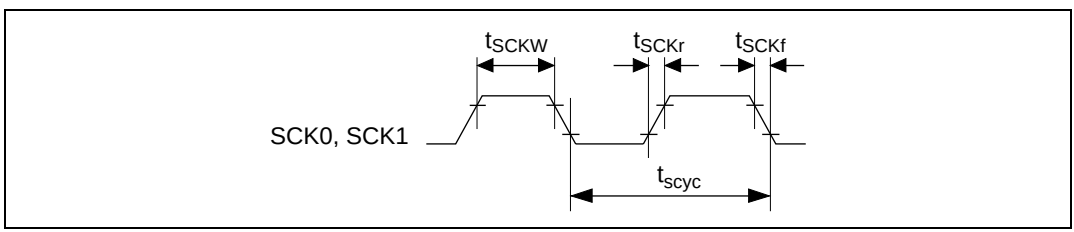


Figure 20.40 Input Clock Timing

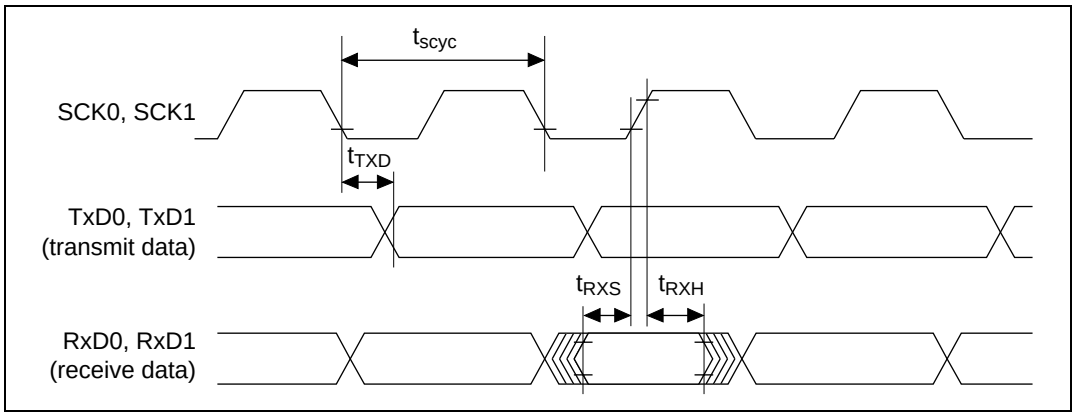


Figure 20.41 SCI I/O Timing (Synchronous Mode)

(9) A/D Converter Timing

Table 20.13 A/D Converter Timing

Case A: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 MHz, Ta = –20 to +75°C*

Case B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

			Cases A and B				
Item		**Symbol**	**Min**	**typ**	**Max**	**Unit**	**Figure**
External trigger input pulse width		t_{TRGW}	2.0	—	—	t_{cyc}	20.42
External trigger input start delay time		t_{TRGS}	50	—	—	ns	
A/D conversion start delay time	CKS = 0	t_D	10	—	17	t_{cyc}	20.43
	CKS = 1		6	—	9	t_{cyc}	
Input sampling time	CKS = 0	t_{SPL}	—	64	—	t_{cyc}	
	CKS = 1		—	32	—	t_{cyc}	
A/D conversion time	CKS = 0	t_{CONV}	259	—	266	t_{cyc}	
	CKS = 1		131	—	134	t_{cyc}	

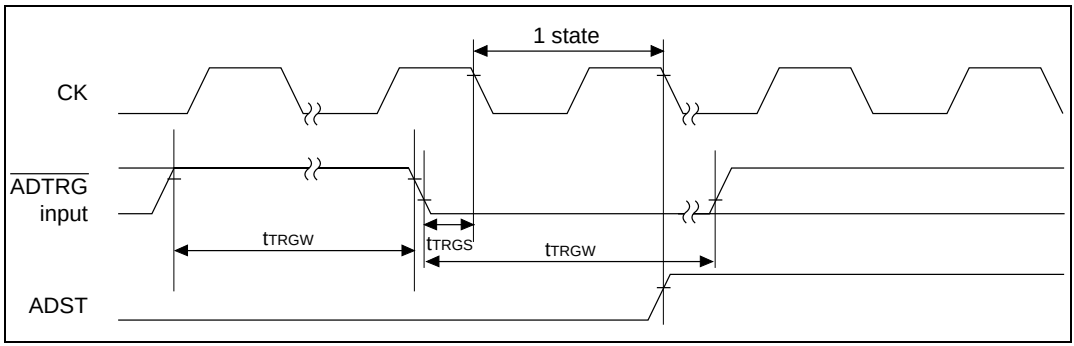


Figure 20.42 External Trigger Input Timing

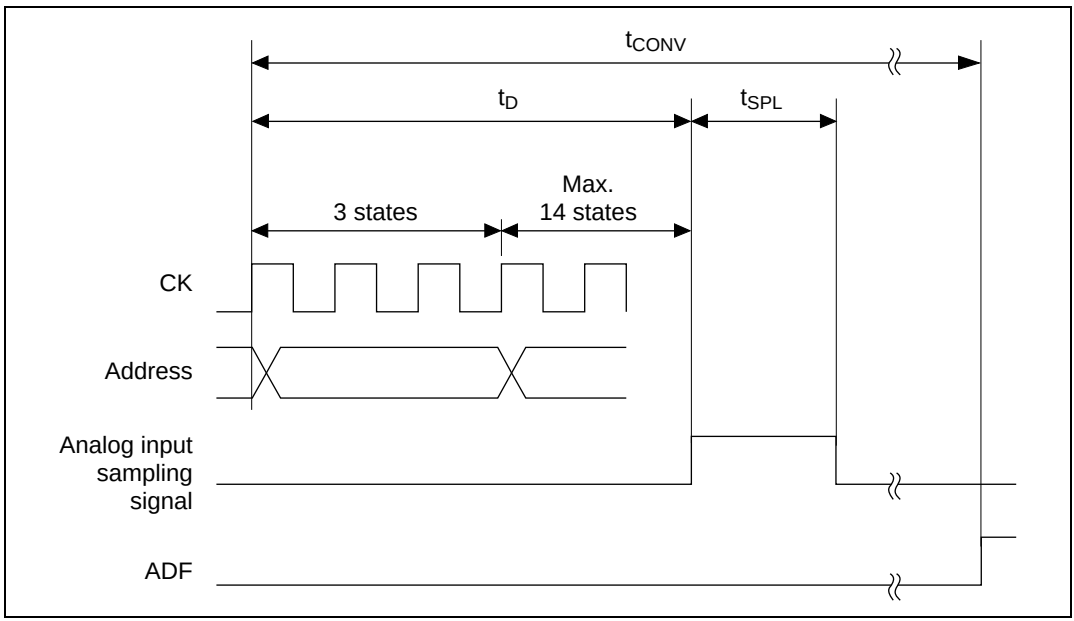
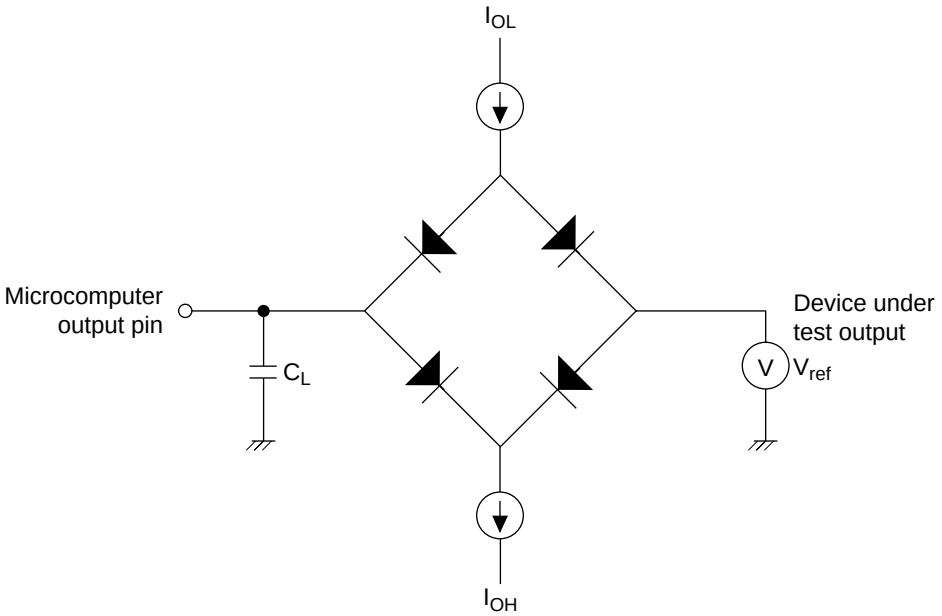


Figure 20.43 Analog Conversion Timing

(10) AC Characteristics Test Conditions



C_L is set as follows for each pin.
30pF: CK, $\overline{\text{CASH}}$, $\overline{\text{CASL}}$, $\overline{\text{CS0}}$–$\overline{\text{CS7}}$, $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, $\overline{\text{AH}}$, $\overline{\text{IRQOUT}}$, $\overline{\text{RAS}}$, DACK0, DACK1
50pF: A21–A0, AD15–AD0, DPH, DPL, $\overline{\text{RD}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{HBS}}$, $\overline{\text{LBS}}$, $\overline{\text{WR}}$
70pF: All port outputs and supporting module output pins other than the above.
I_{OL} and I_{OH} values are as shown in section 20.1.2, DC Characteristics, and table 20.3, Permitted Output Current Values.

Figure 20.44 Output Load Circuit

20.1.4 A/D Converter Characteristics

Table 20.14 A/D Converter Characteristics (1)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

	12.5 MHz			20 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	bit
Conversion time	—	—	11.2	—	—	6.7	µS
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	3	—	—	3	kΩ
Nonlinearity error	—	—	±3	—	—	±3	LSB
Offset error	—	—	±3	—	—	±3	LSB
Full-scale error	—	—	±3	—	—	±3	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±4	—	—	±4	LSB

Table 20.14 A/D Converter Characteristics (2)

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, AV_{CC} = V_{CC} ±10%, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

	12.5 MHz			
Item	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	bit
Conversion time	—	—	11.2	µS
Analog input capacitance	—	—	20	pF
Permissible signal-source impedance	—	—	3	kΩ
Nonlinearity error	—	—	±4.0	LSB
Offset error	—	—	±4.0	LSB
Full-scale error	—	—	±4.0	LSB
Quantization error	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	LSB

20.2 SH7034B 3.3 V 12.5 MHz Version and 20 MHz Version*[1] Electrical Characteristics

20.2.1 Absolute Maximum Ratings

Table 20.15 shows the absolute maximum ratings.

Table 20.15 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.3 to +4.6	V
Input voltage (except port C)	V_{in}	–0.3 to V_{CC} + 0.3	V
Input voltage (port C)	V_{in}	–0.3 to AV_{CC} + 0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.6	V
Analog reference voltage	AV_{ref}	–0.3 to AV_{CC} + 0.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75*[2]	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Operating the chip in excess of the absolute maximum rating may result in permanent damage.

Notes: 1. ROMless products only for 20 MHz version
2. Regular-specification products; for wide-temperature-range products, Topr = –40 to +85°C

20.2.2 DC Characteristics

Table 20.16 lists DC characteristics. Table 20.18 lists the permissible output current values.

Usage Conditions:

- Do not release AV_{CC}, AV_{ref} and AV_{SS} when the A/D converter is not in use. Connect AV_{CC} and AV_{ref} to V_{CC} and AV_{SS} to V_{SS}.
- The current consumption value is measured under conditions of V_{IH} min = V_{CC} – 0.5 V and V_{IL} max = 0.5 V with no load on any output pin and the on-chip pull-up MOS off.
- Even when the A/D converter is not used or is in standby mode, connect AV_{CC} and AV_{ref} to the power voltage(V_{CC}).

Table 20.16 DC Characteristics

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 12.5 to 20 MHz*1, Ta = –20 to +75°C*2

Notes: 1. ROMless products only for 20 MHz version
2. Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input high-level voltage	EXTAL	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	Port C		$V_{CC} \times 0.7$	—	AV_{CC} + 0.3	V	
	Other input pins		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
Input low-level voltage	Other Schmidt trigger input pins	V_{IL}	–0.3	—	$V_{CC} \times 0.2$	V	
Schmidt trigger input voltage	$\overline{RES}$, NMI, MD2–MD0, PA13–10, PA2, PA0, PB7–PB0	V_T^+	$V_{CC} \times 0.9$	—	—	V	
		V_T^-	—	—	$V_{CC} \times 0.1$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input leakage current	$\overline{RES}$	|Iin|	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	NMI, MD2–MD0		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	Port C		—	—	1.0	µA	Vin = 0.5 to AV_{CC} – 0.5 V
3-state leakage current (off state)	Ports A and B, $\overline{CS3}$–$\overline{CS0}$, A21–A0, AD15–AD0	$\|I_{TSI}\|$	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	PA3	–Ip	20	—	300	µA	Vin = 0V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.7	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
			—	—	1.2	V	I_{OL} = 8 mA

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	$\overline{RES}$	Cin	—	—	30	pF	Vin = 0 V Input signal f = 1 MHz Ta = 25°C
	NMI		—	—	30	pF	
	All other input pins		—	—	20	pF	
Current consumption	Ordinary operation	I_{CC}	—	25	—	mA	f = 12.5 MHz
			—	35	60	mA	f = 20 MHz
	Sleep		—	20	—	mA	f = 12.5 MHz
			—	30	40	mA	f = 20 MHz
	Standby		—	0.1	5	µA	Ta ≤ 50°C
			—	—	10	µA	50°C < Ta
Analog power supply current	Ordinary operation, Sleep	AI_{CC}	—	0.5	1	mA	
	Standby		—	0.1	5	µA	
Reference power supply current	Ordinary operation, Sleep	AI_{ref}	—	0.5	1	mA	
	Standby		—	0.1	5	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Usage Notes:

1. If the A/D converter is not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open. Connect AV_{CC} and AV_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IH} min = V_{CC} - 0.5 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. When the A/D converter is not used, and in standby mode, AV_{CC} and AV_{ref} must still be connected to the power supply (V_{CC}).
4. The Characteristic-related performance values, operating margins, noise margins, noise emissions, etc., of this LSI are different from HD6417034A, etc. Caution is therefore required in carrying out system design, when switching from ZTAT version.

Table 20.17 Permitted Output Current Values

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		12.5 MHz			20 MHz			
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Output low-level permissible current (per pin)	I_{OL}	—	—	10	—	—	10	mA
Output low-level permissible current (total)	$\sum I_{OL}$	—	—	80	—	—	80	mA
Output high-level permissible current (per pin)	$-I_{OH}$	—	—	2.0	—	—	2.0	mA
Output high-level permissible current (total)	$-\sum I_{OH}$	—	—	25	—	—	25	mA

Caution: To ensure reliability of the chip, do not exceed the output current values given in table 20.17.

20.2.3 AC Characteristics

The following AC timing chart represents the AC characteristics, not signal functions. For signal functions, see the explanation in the text.

(1) Clock Timing

Table 20.18 Clock Timing

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		12.5 MHz		20 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Figures**
EXTAL input high level pulse width	t_{EXH}	22	—	15	—	ns	20.45
EXTAL input low level pulse width	t_{EXL}	22	—	15	—	ns	
EXTAL input rise time	t_{EXr}	—	10	—	5	ns	
EXTAL input fall time	t_{EXf}	—	10	—	5	ns	
Clock cycle time	t_{cyc}	80	500	50	250	ns	20.45, 20.46
Clock high pulse width	t_{CH}	30	—	20	—	ns	20.46
Clock low pulse width	t_{CL}	30	—	20	—	ns	
Clock rise time	t_{Cr}	—	10	—	5	ns	
Clock fall time	t_{Cf}	—	10	—	5	ns	
Reset oscillation settling time	t_{OSC1}	10	—	10	—	ms	20.47
Software standby oscillation settling time	t_{OSC2}	10	—	10	—	ms	

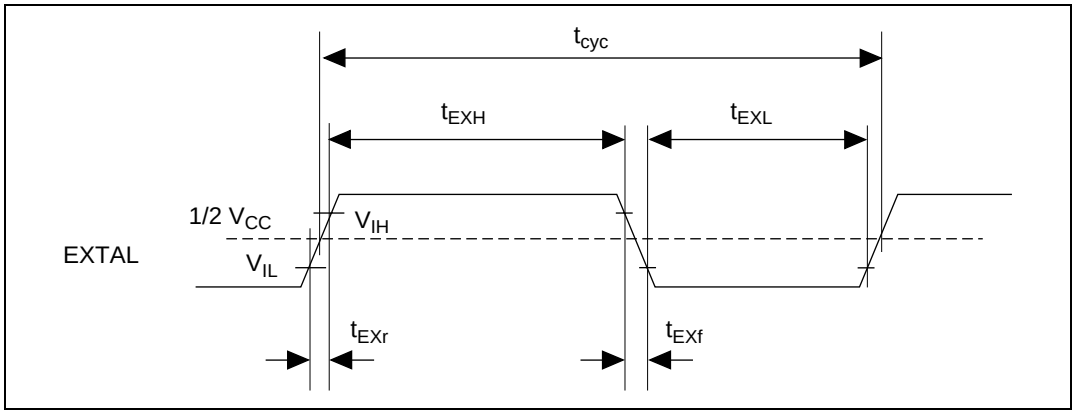


Figure 20.45 EXTAL Input Timing

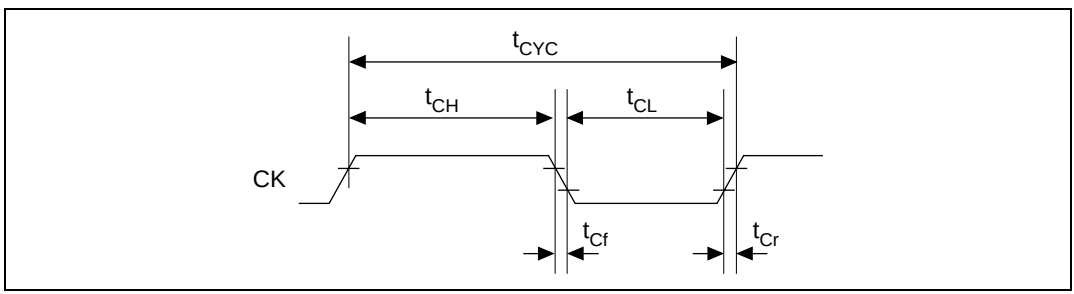


Figure 20.46 System Clock Timing

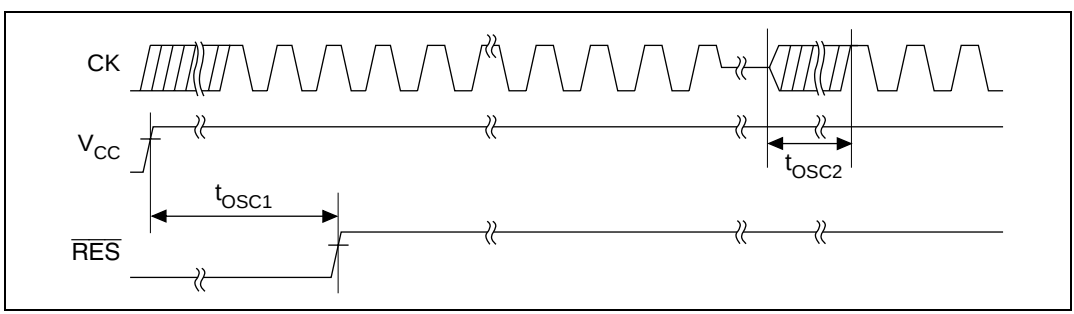


Figure 20.47 Oscillation Settling Time

(2) Control Signal Timing

Table 20.19 Control Signal Timing

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		12.5 MHz		20 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Figure**
$\overline{RES}$ setup time	t_{RESS}	320	—	200	—	ns	20.48
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI reset setup time	t_{NMIRS}	320	—	200	—	ns	
NMI reset hold time	t_{NMIRH}	320	—	200	—	ns	
NMI setup time	t_{NMIS}	160	—	100	—	ns	20.49
NMI hold time	t_{NMIH}	80	—	50	—	ns	
$\overline{IRQ0}$–$\overline{IRQ7}$ setup time (edge detection)	t_{IRQES}	160	—	100	—	ns	
$\overline{IRQ0}$–$\overline{IRQ7}$ setup time (level detection)	t_{IRQLS}	160	—	100	—	ns	
$\overline{IRQ0}$–$\overline{IRQ7}$ hold time	t_{IRQEH}	80	—	50	—	ns	
$\overline{IRQOUT}$ output delay time	t_{IRQOD}	—	80	—	50	ns	20.50
Bus request setup time	t_{BRQS}	80	—	50	—	ns	20.51
Bus acknowledge delay time 1	t_{BACD1}	—	80	—	50	ns	
Bus acknowledge delay time 2	t_{BACD2}	—	80	—	50	ns	
Bus 3-state delay time	t_{BZD}	—	80	—	50	ns	

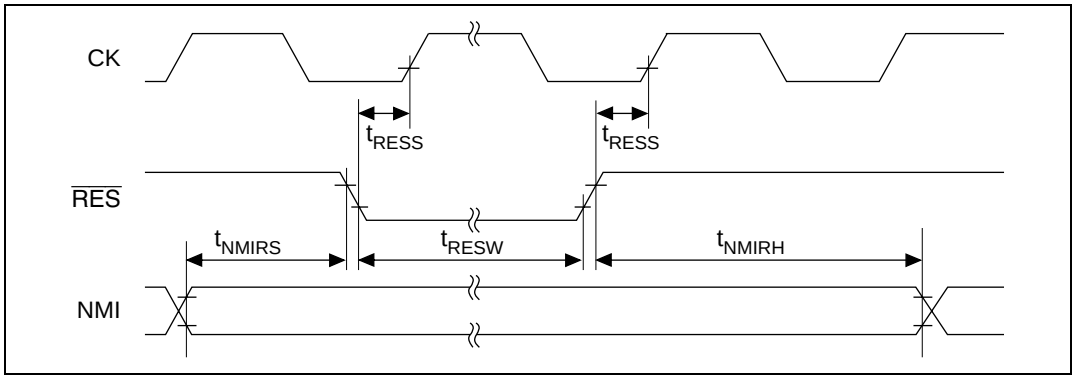


Figure 20.48 Reset Input Timing

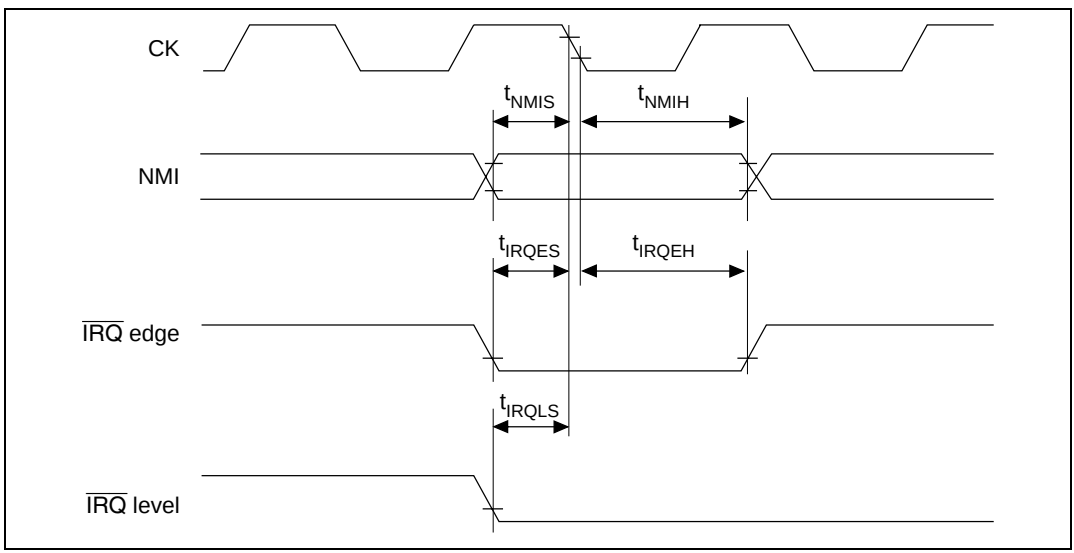


Figure 20.49 Interrupt Signal Input Timing

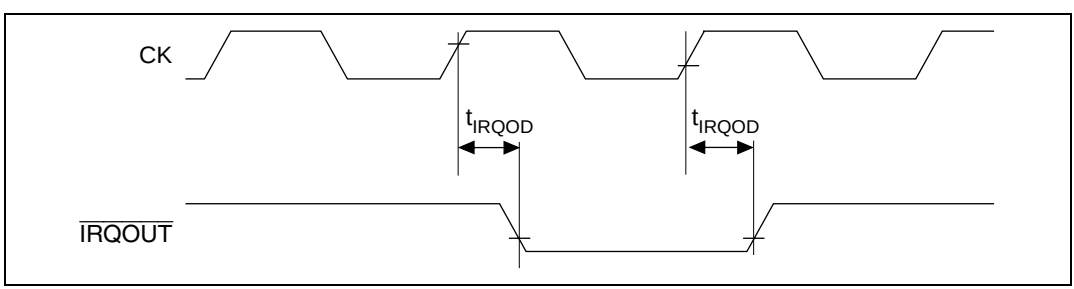


Figure 20.50 Interrupt Signal Output Timing

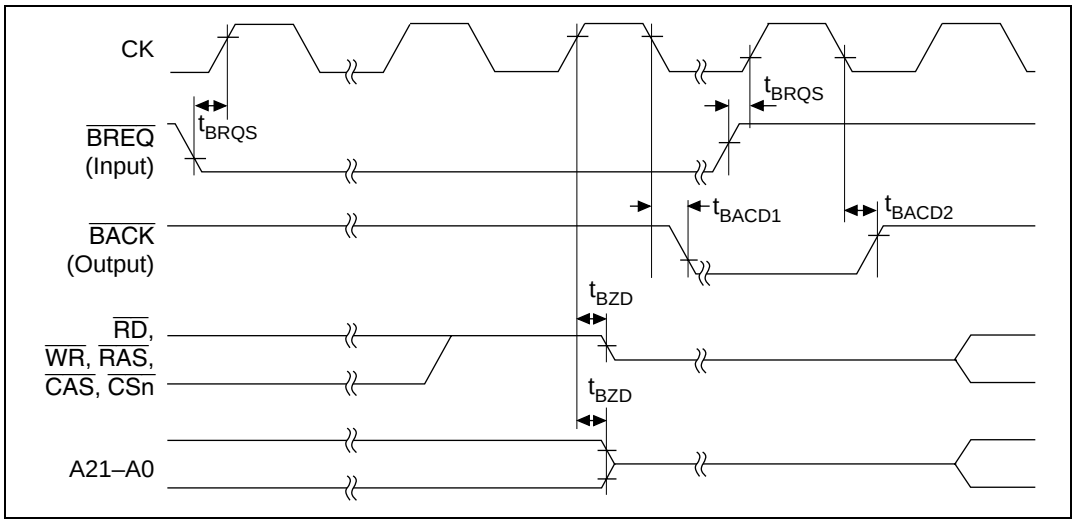


Figure 20.51 Bus Release Timing

(3) Bus Timing

Tables 20.20 show the bus timing.

Table 20.20 Bus Timing (1)

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 20 MHz*1, Ta = –20 to +75°C*2

Notes: 1. ROMless products
2. Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item		Symbol	Min	Max	Unit	Figures
Address delay time		t_{AD}	—	20*1	ns	20.52, 20.53, 20.55–20.58, 20.63, 20.64
$\overline{CS}$ delay time 1		t_{CSD1}	—	25	ns	20.52, 20.53, 20.64
$\overline{CS}$ delay time 2		t_{CSD2}	—	25	ns	
$\overline{CS}$ delay time 3		t_{CSD3}	—	25	ns	20.63
$\overline{CS}$ delay time 4		t_{CSD4}	—	25	ns	
Access time 1*6 from read strobe	35% duty*2	t_{RDAC1}	$t_{cyc} \times 0.65 - 20$	—	ns	20.52
	50% duty		$t_{cyc} \times 0.5 - 20$	—	ns	
Access time 2*6 from read strobe	35% duty*2	t_{RDAC2}	$t_{cyc} \times (n+1.65) - 20$*3	—	ns	20.53, 20.54
	50% duty		$t_{cyc} \times (n+1.5) - 20$*3	—	ns	
Access time 3*6 from read strobe	35% duty*2	t_{RDAC3}	$t_{cyc} \times (n+0.65) - 20$*3	—	ns	20.63
	50% duty		$t_{cyc} \times (n+0.5) - 20$*3	—	ns	
Read strobe delay time		t_{RSD}	—	20	ns	20.52, 20.53, 20.55–20.59, 20.63
Read data setup time		t_{RDS}	15	—	ns	20.52, 20.53, 20.55–20.58, 20.63
Read data hold time		t_{RDH}	0	—	ns	
Write strobe delay time 1		t_{WSD1}	—	20	ns	20.53, 20.57, 20.58, 20.63, 20.64
Write strobe delay time 2		t_{WSD2}	—	20	ns	20.53, 20.57, 20.58, 20.63
Write strobe delay time 3		t_{WSD3}	—	20	ns	20.55, 20.56
Write strobe delay time 4		t_{WSD4}	—	20	ns	20.55, 20.56, 20.64

Item	Symbol	Min	Max	Unit	Figures
Write data delay time 1	t_{WDD1}	—	35	ns	20.53, 20.57, 20.58, 20.63
Write data delay time 2	t_{WDD2}	—	20	ns	20.55, 20.56
Write data hold time	t_{WDH}	0	—	ns	20.53, 20.55–20.58
Parity output delay time 1	t_{WPDD1}	—	40	ns	20.53, 20.57, 20.58
Parity output delay time 2	t_{WPDD2}	—	20	ns	20.55, 20.56
Parity output hold time	t_{WPDH}	0	—	ns	20.53, 20.55–20.58
Wait setup time	t_{WTS}	10	—	ns	20.54, 20.59, 20.63
Wait hold time	t_{WTH}	6	—	ns	
Read data access time 1*6	t_{ACC1}	$t_{cyc} - 30$*4	—	ns	20.52, 20.55, 20.56
Read data access time 2*6	t_{ACC2}	$t_{cyc} \times (n+2) - 30$*3	—	ns	20.53, 20.54, 20.57–20.59
$\overline{RAS}$ delay time 1	t_{RASD1}	—	20	ns	20.55–20.58, 20.60–20.62
$\overline{RAS}$ delay time 2	t_{RASD2}	—	30	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	—	20	ns	20.55
$\overline{CAS}$ delay time 2*7	t_{CASD2}	—	20	ns	20.57, 20.58, 20.60–20.62
$\overline{CAS}$ delay time 3*7	t_{CASD3}	—	20	ns	
Column address setup time	t_{ASC}	0	—	ns	20.55, 20.56
Read data access time from $\overline{CAS}$ 1*6 (35% duty*2)	t_{CAC1}	$t_{cyc} \times 0.65 - 19$	—	ns	
Read data access time from $\overline{CAS}$ 1*6 (50% duty)	t_{CAC1}	$t_{cyc} \times 0.5 - 19$	—	ns	
Read data access time from $\overline{CAS}$ 2*6	t_{CAC2}	$t_{cyc} \times (n+1) - 25$*3	—	ns	20.57–20.59
Read data access time from $\overline{RAS}$ 1*6	t_{RAC1}	$t_{cyc} \times 1.5 - 20$	—	ns	20.55, 20.56
Read data access time from $\overline{RAS}$ 2*6	t_{RAC2}	$t_{cyc} \times (n+2.5) - 20$*3	—	ns	20.57–20.59
High-speed page mode $\overline{CAS}$ precharge time	t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.56

Item		Symbol	Min	Max	Unit	Figures
$\overline{AH}$ delay time 1		t_{AHD1}	—	20	ns	20.63
$\overline{AH}$ delay time 2		t_{AHD2}	—	20	ns	
Multiplexed address delay time		t_{MAD}	—	30	ns	
Multiplexed address hold time		t_{MAH}	0	—	ns	
DACK0, DACK1 delay time 1		t_{DACD1}	—	23	ns	20.52, 20.53, 20.55–20.58, 20.63, 20.64
DACK0, DACK1 delay time 2		t_{DACD2}	—	23	ns	
DACK0, DACK1 delay time 3*7		t_{DACD3}	—	20	ns	20.53, 20.57, 20.58, 20.63
DACK0, DACK1 delay time 4		t_{DACD4}	—	20	ns	20.55, 20.56
DACK0, DACK1 delay time 5		t_{DACD5}	—	20	ns	
Read delay time	35% duty*2	t_{RDD}	—	$t_{cyc} \times 0.35 + 12$	ns	20.52, 20.53, 20.55–20.59, 20.63
	50% duty		—	$t_{cyc} \times 0.5 + 15$	ns	
Data setup time for $\overline{CAS}$		t_{DS}	0*5	—	ns	20.55, 20.57
$\overline{CAS}$ setup time for $\overline{RAS}$		t_{CSR}	10	—	ns	20.60–20.62
Row address hold time		t_{RAH}	10	—	ns	20.55, 20.57
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*2	t_{WCS}	0	—	ns	20.55
	50% duty	t_{WCS}	0	—	ns	
Access time from $\overline{CAS}$ precharge*6		t_{ACP}	t_{cyc} –20	—	ns	20.56

Notes: 1. HBS and LBS signals are 25 ns.
2. When frequency is 10 MHz or more.
3. n is the number of wait cycles.
4. Access time from addresses A0 to A21 is tcyc-25 ns.
5. –5ns for parity output of DRAM long-pitch access.
6. It is not necessary to meet the t_{RDS} specification as long as the access time specification is met.
7. In the relationship of t_{CASD2} and t_{CASD3} with respect to t_{DACD3}, a Min-Max combination does not occur because of the logic structure.

Table 20.20 Bus Timing (2)

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 12.5 MHz, Ta = –20 to +75°C*

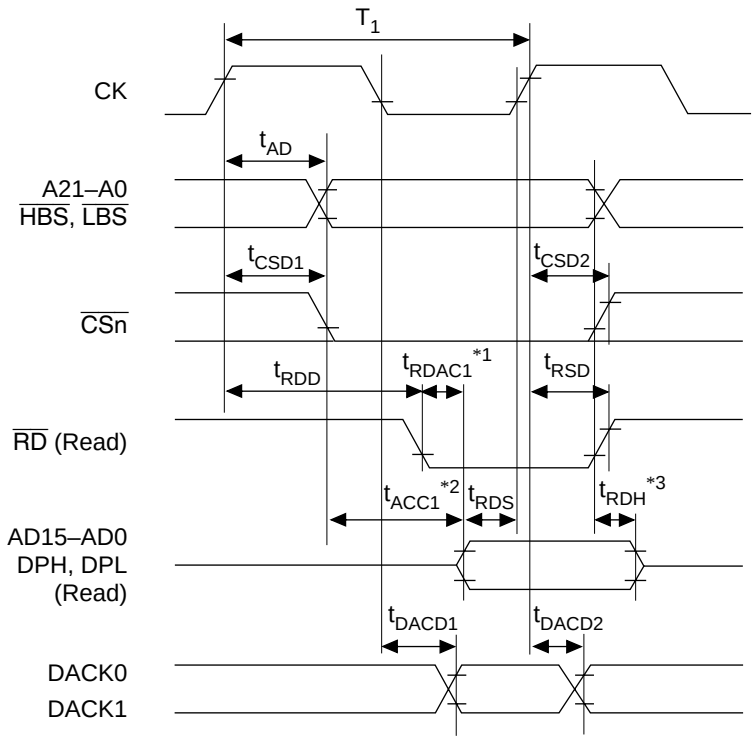
Note: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item		Symbol	Min	Max	Unit	Figures
Address delay time		t_{AD}	—	40	ns	20.52, 20.53, 20.55–20.58, 20.63, 20.64
$\overline{CS}$ delay time 1		t_{CSD1}	—	40	ns	20.52, 20.53, 20.64
$\overline{CS}$ delay time 2		t_{CSD2}	—	40	ns	
$\overline{CS}$ delay time 3		t_{CSD3}	—	40	ns	20.63
$\overline{CS}$ delay time 4		t_{CSD4}	—	40	ns	
Access time 1*4 from read strobe	35% duty*1	t_{RDAC1}	$t_{cyc} \times 0.65 - 35$	—	ns	20.52
	50% duty		$t_{cyc} \times 0.5 - 35$	—	ns	
Access time 2*4 from read strobe	35% duty*1	t_{RDAC2}	$t_{cyc} \times (n+1.65) - 35$*2	—	ns	20.53, 20.54
	50% duty		$t_{cvc} \times (n+1.5) - 35$*2	—	ns	
Access time 3*4 from read strobe	35% duty*1	t_{RDAC3}	$t_{cyc} \times (n+0.65) - 35$*2	—	ns	20.63
	50% duty		$t_{cvc} \times (n+0.5) - 35$*2	—	ns	
Read strobe delay time		t_{RSD}	—	40	ns	20.52, 20.53, 20.55–20.59, 20.63
Read data setup time		t_{RDS}	25	—	ns	20.52, 20.53, 20.55–20.58, 20.63
Read data hold time		t_{RDH}	0	—	ns	
Write strobe delay time 1		t_{WSD1}	—	40	ns	20.53, 20.57, 20.58, 20.63, 20.64
Write strobe delay time 2		t_{WSD2}	—	30	ns	20.53, 20.57, 20.58, 20.63
Write strobe delay time 3		t_{WSD3}	—	40	ns	20.55, 20.56
Write strobe delay time 4		t_{WSD4}	—	40	ns	20.55, 20.56, 20.64

Item	Symbol	Min	Max	Unit	Figures
Write data delay time 1	t_{WDD1}	—	70	ns	20.53, 20.57, 20.58, 20.63
Write data delay time 2	t_{WDD2}	—	40	ns	20.55, 20.56
Write data hold time	t_{WDH}	–10	—	ns	20.53, 20.55–20.58, 20.63
Parity output delay time 1	t_{WPDD1}	—	80	ns	20.53, 20.57, 20.58
Parity output delay time 2	t_{WPDD2}	—	40	ns	20.55, 20.56
Parity output hold time	t_{WPDH}	–10	—	ns	20.53, 20.55–20.58
Wait setup time	t_{WTS}	40	—	ns	20.54, 20.59, 20.63
Wait hold time	t_{WTH}	10	—	ns	
Read data access time 1*4	t_{ACC1}	$t_{cyc} - 44$	—	ns	20.52, 20.55, 20.56
Read data access time 2*4	t_{ACC2}	$t_{cyc} \times (n+2) - 44$*2	—	ns	20.53, 20.54, 20.57–20.59
$\overline{RAS}$ delay time 1	t_{RASD1}	—	40	ns	20.55–20.58, 20.60–20.62
$\overline{RAS}$ delay time 2	t_{RASD2}	—	40	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	—	40	ns	20.55
$\overline{CAS}$ delay time 2*5	t_{CASD2}	—	40	ns	20.57, 20.58, 20.60–20.62
$\overline{CAS}$ delay time 3*5	t_{CASD3}	—	40	ns	
Column address setup time	t_{ASC}	0	—	ns	20.55, 20.56
Read data access time from $\overline{CAS}$ 1*4 (35% duty*1)	t_{CAC1}	$t_{cyc} \times 0.65 - 35$	—	ns	
Read data access time from $\overline{CAS}$ 1*4 (50% duty)	t_{CAC1}	$t_{cyc} \times 0.5 - 35$	—	ns	
Read data access time from $\overline{CAS}$ 2*4	t_{CAC2}	$t_{cyc} \times (n+1) - 35$*2	—	ns	20.57–20.59
Read data access time from $\overline{RAS}$ 1*4	t_{RAC1}	$t_{cyc} \times 1.5 - 35$	—	ns	20.55, 20.56
Read data access time from $\overline{RAS}$ 2*4	t_{RAC2}	$t_{cyc} \times (n+2.5) - 35$*2	—	ns	20.57–20.59
High-speed page mode $\overline{CAS}$ precharge time	t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.56

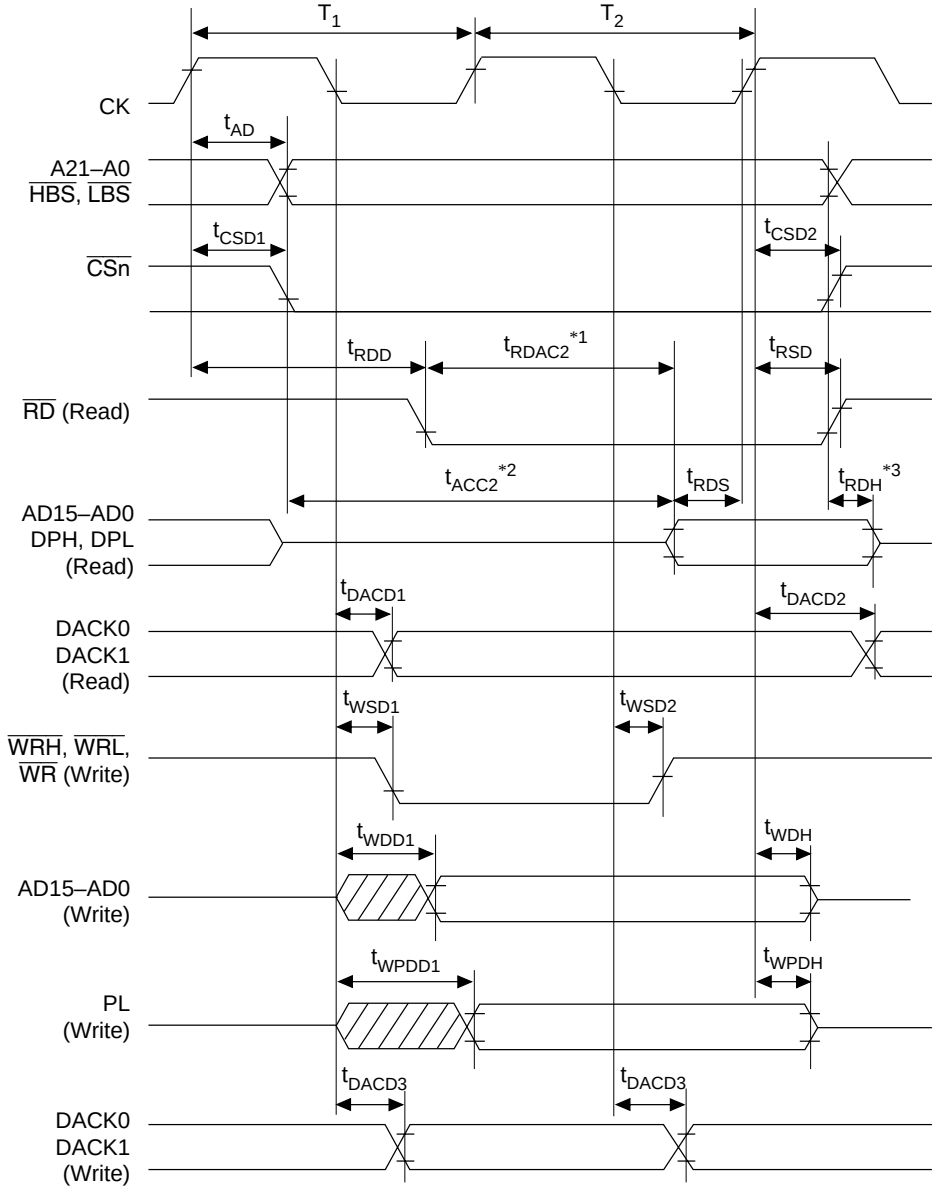
Item		Symbol	Min	Max	Unit	Figures
$\overline{AH}$ delay time 1		t_{AHD1}	—	40	ns	20.63
$\overline{AH}$ delay time 2		t_{AHD2}	—	40	ns	
Multiplexed address delay time		t_{MAD}	—	40	ns	
Multiplexed address hold time		t_{MAH}	–10	—	ns	
DACK0, DACK1 delay time 1		t_{DACD1}	—	40	ns	20.52, 20.53, 20.55–20.58, 20.63, 20.64
DACK0, DACK1 delay time 2		t_{DACD2}	—	40	ns	
DACK0, DACK1 delay time 3*5		t_{DACD3}	—	40	ns	20.53, 20.57, 20.58, 20.63
DACK0, DACK1 delay time 4		t_{DACD4}	—	40	ns	20.55, 20.56
DACK0, DACK1 delay time 5		t_{DACD5}	—	40	ns	
Read delay time	35% duty*1	t_{RDD}	—	$t_{cyc} \times 0.35 + 35$	ns	20.52, 20.53, 20.55–20.59, 20.63
	50% duty		—	$t_{cyc} \times 0.5 + 35$	ns	
Data setup time for $\overline{CAS}$		t_{DS}	0*3	—	ns	20.55, 20.57
$\overline{CAS}$ setup time for $\overline{RAS}$		t_{CSR}	10	—	ns	20.60–20.62
Row address hold time		t_{RAH}	10	—	ns	20.55, 20.57
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*1	t_{WCS}	0	—	ns	20.55
	50% duty		0	—	ns	
Access time from $\overline{CAS}$ precharge*4		t_{ACP}	t_{cyc} –20	—	ns	20.56

Notes: 1. When frequency is 10 MHz or more.
2. n is the number of wait cycles.
3. –5ns for parity output of DRAM long-pitch access.
4. If the access time is satisfied, t_{RDS} need not be satisfied.
5. In the relationship between t_{CASD2} and t_{CASD3} for t_{DACD3}, the pair of Min-Max is not exist in the logical structure.



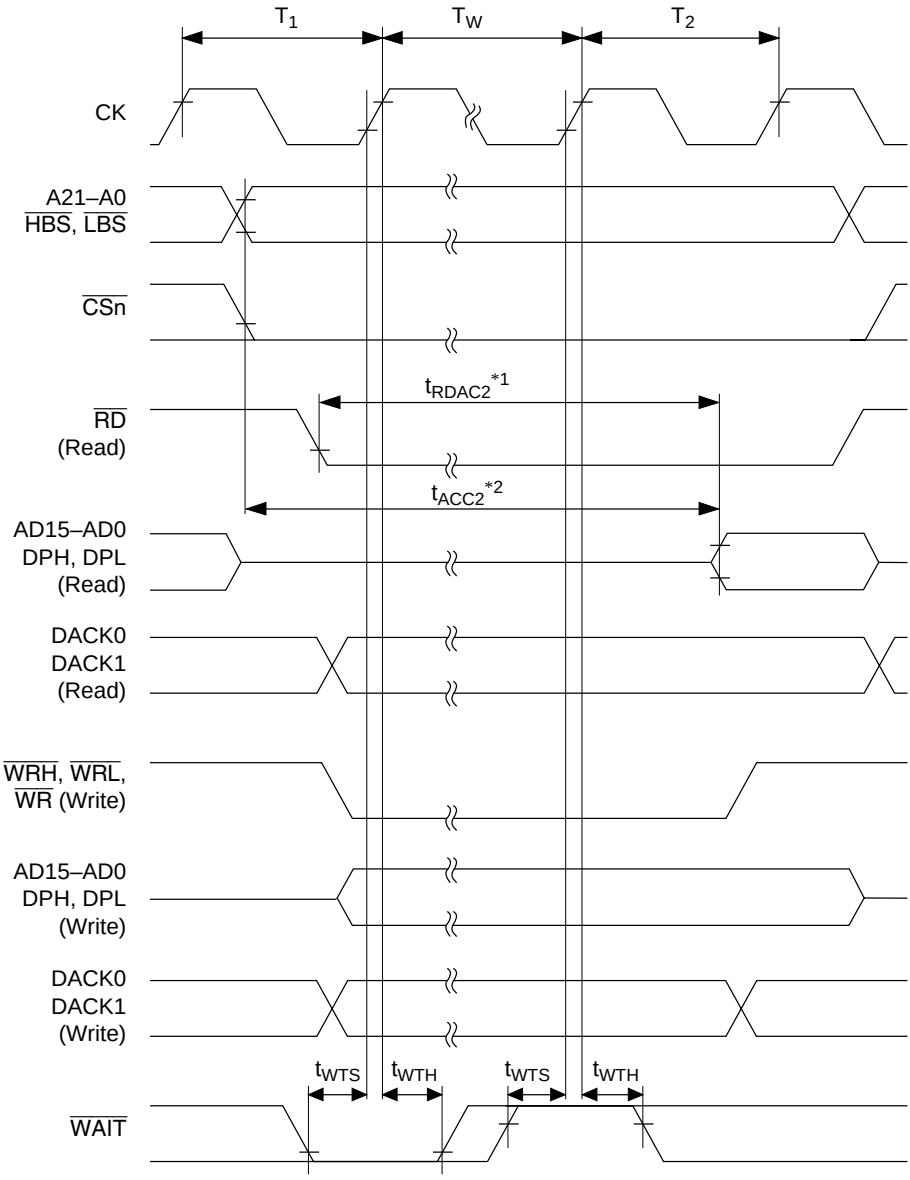
Notes: 1. For t_{RDAC1}, use $t_{cyc} \times 0.65 - 20$ (for 35% duty) or $t_{cyc} \times 0.5 - 20$ (for 50% duty) instead of $t_{cyc} - t_{RDD} - t_{RDS}$.
2. For t_{ACC1}, use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD}$ (or t_{CSD1}) – t_{RDS}.
3. t_{RDH} is measured from A21–A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.52 Basic Bus Cycle: One-State Access



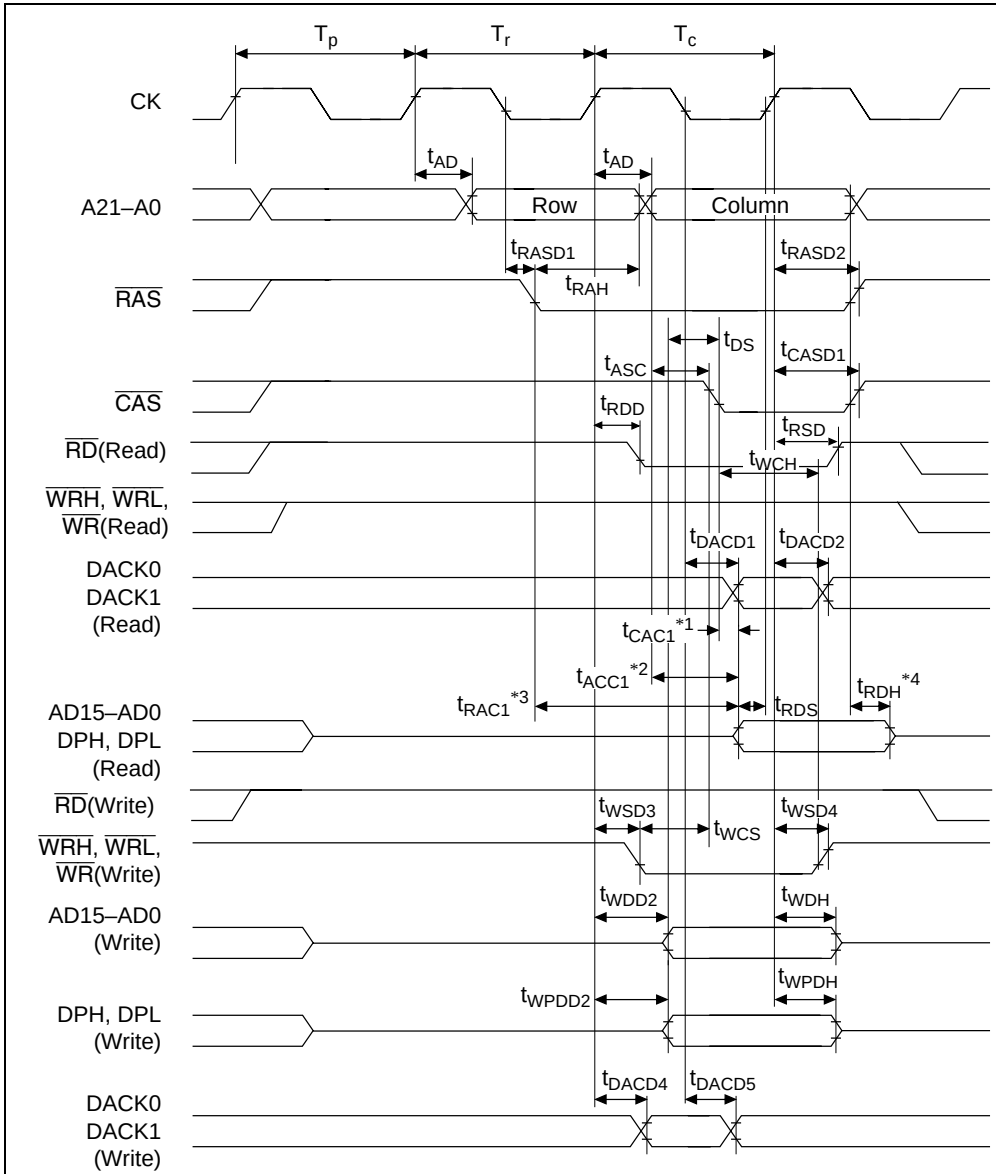
Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n + 1.65) - 20$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 20$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) – t_{RDS}.
3. t_{RDH} is measured from A21–A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.53 Basic Bus Cycle: Two-State Access



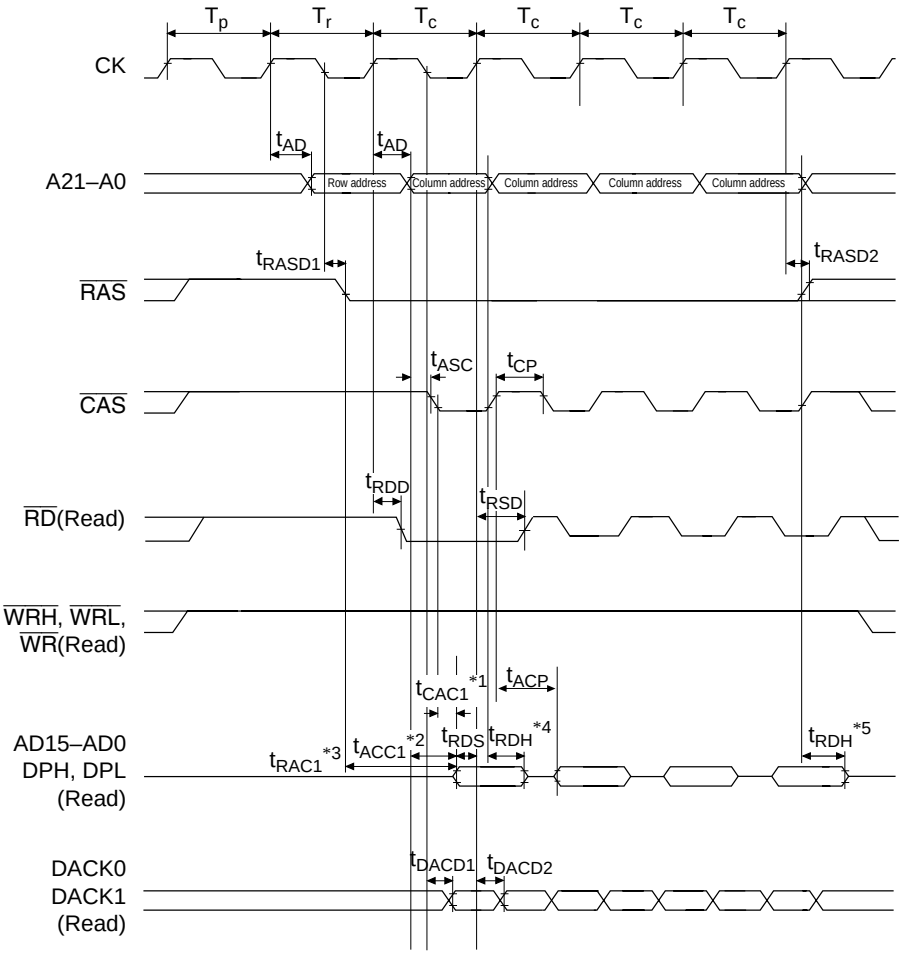
Notes: 1. For t_{RDAC2}, use $t_{cyc} \times (n+1.65) - 20$ (for 35% duty) or $t_{cyc} \times (n+1.5) - 20$ (for 50% duty) instead of $t_{cyc} \times (n+2) - t_{RDD} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n+2) - 30$ instead of $t_{cyc} \times (n+2) - t_{AD}$ (or t_{CSD1}) $- t_{RDS}$.

Figure 20.54 Basic Bus Cycle: Two States + Wait State



Notes: 1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 19$ (for 35% duty) or $t_{cyc} \times 0.5 - 19$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
2. For t_{ACC1}, use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 20$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.55 DRAM Bus Cycle (Short-Pitch, Normal Mode)



Notes: 1. For t_{CAC1}, use $t_{cyc} \times 0.65 - 19$ (for 35% duty) or $t_{cyc} \times 0.5 - 19$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
It is not necessary to meet the t_{RDS} specification as long as the t_{CAC1} specification is met.

2. For t_{ACC1}, use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
It is not necessary to meet the t_{RDS} specification as long as the t_{ACC1} specification is met.

3. For t_{RAC1}, use $t_{cyc} \times 1.5 - 20$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
It is not necessary to meet the t_{RDS} specification as long as the t_{RAC1} specification is met.

4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.

5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.56 (a) DRAM Bus Cycle (Short-Pitch, High-Speed Page Mode: Read)

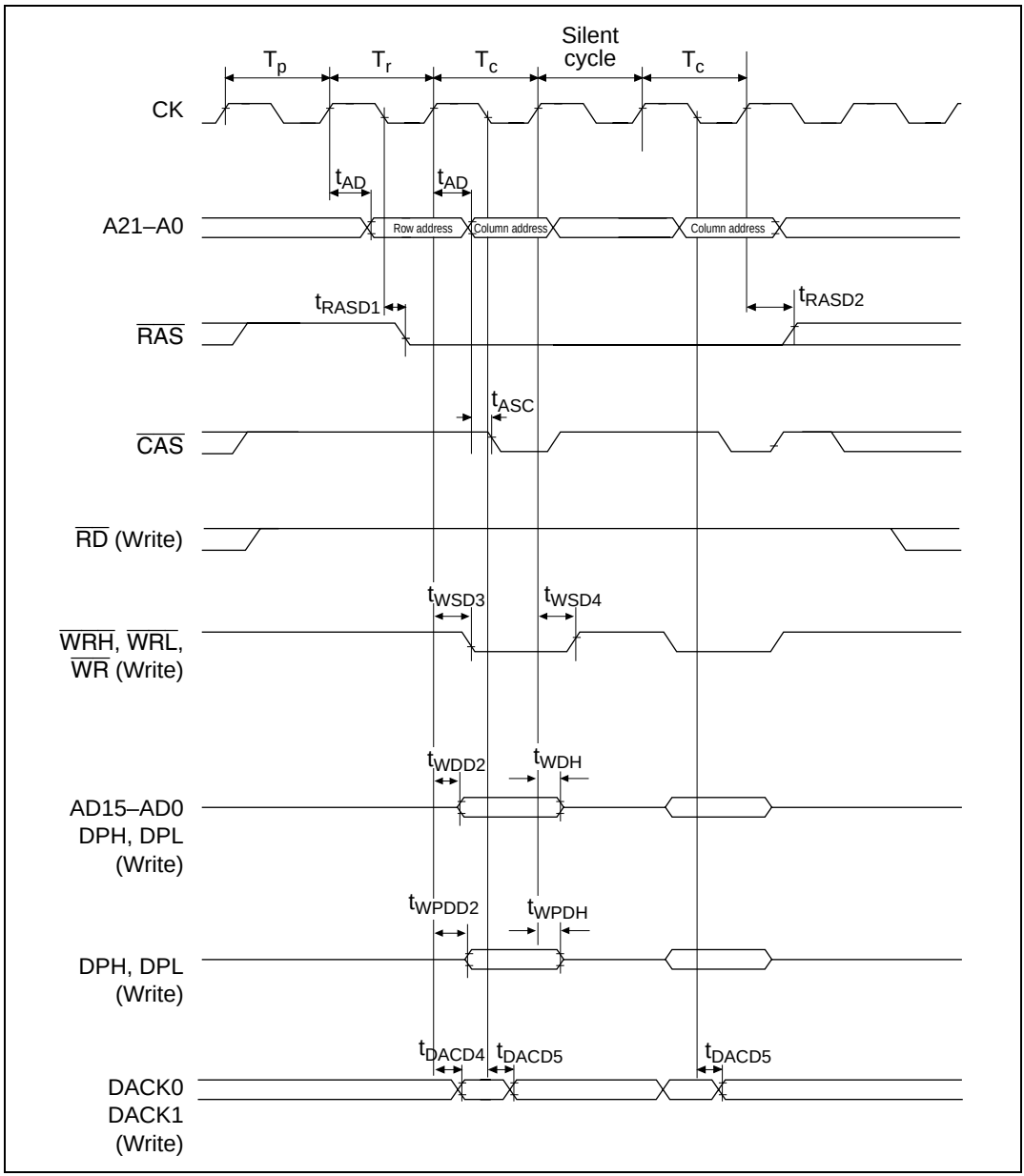
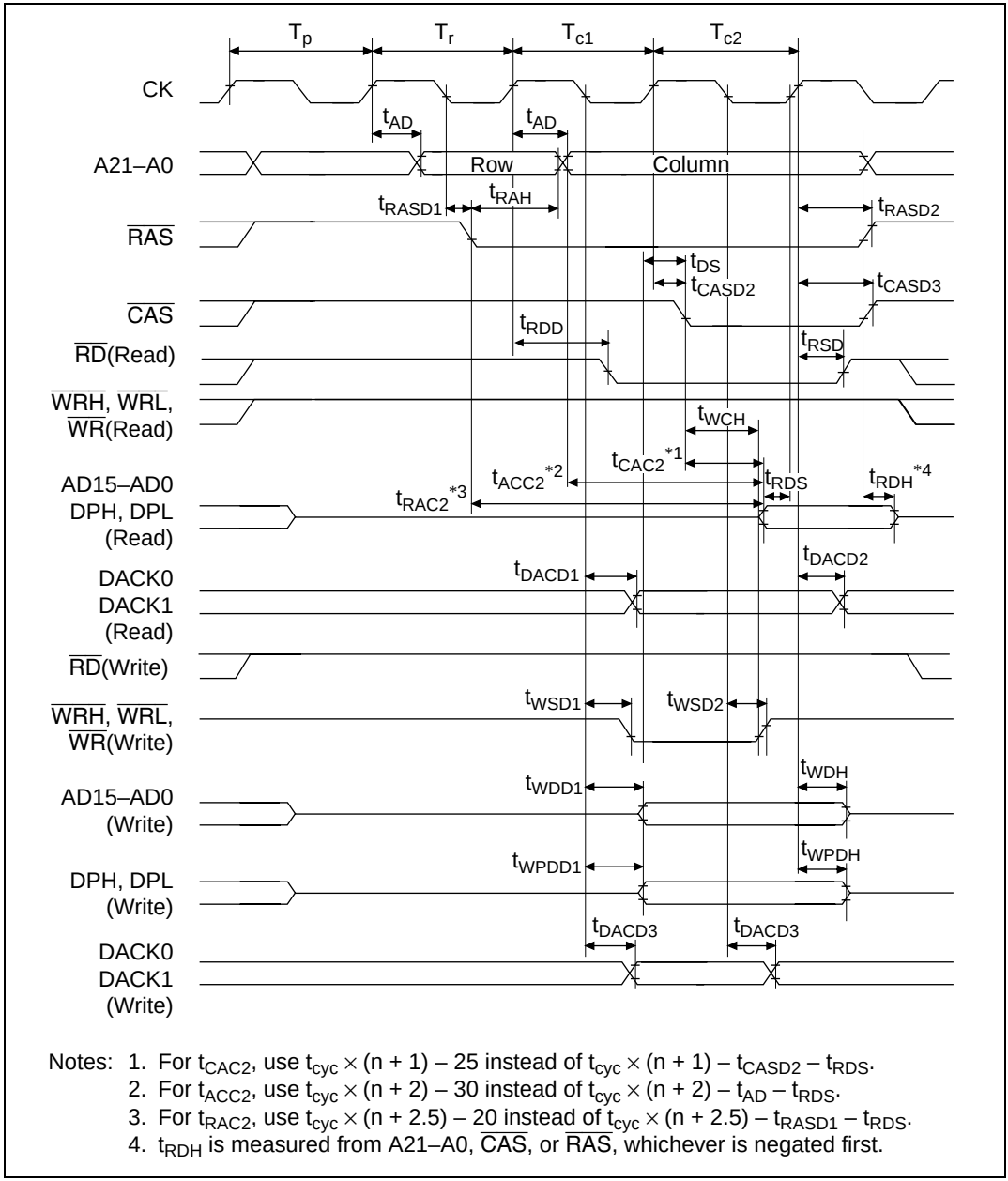


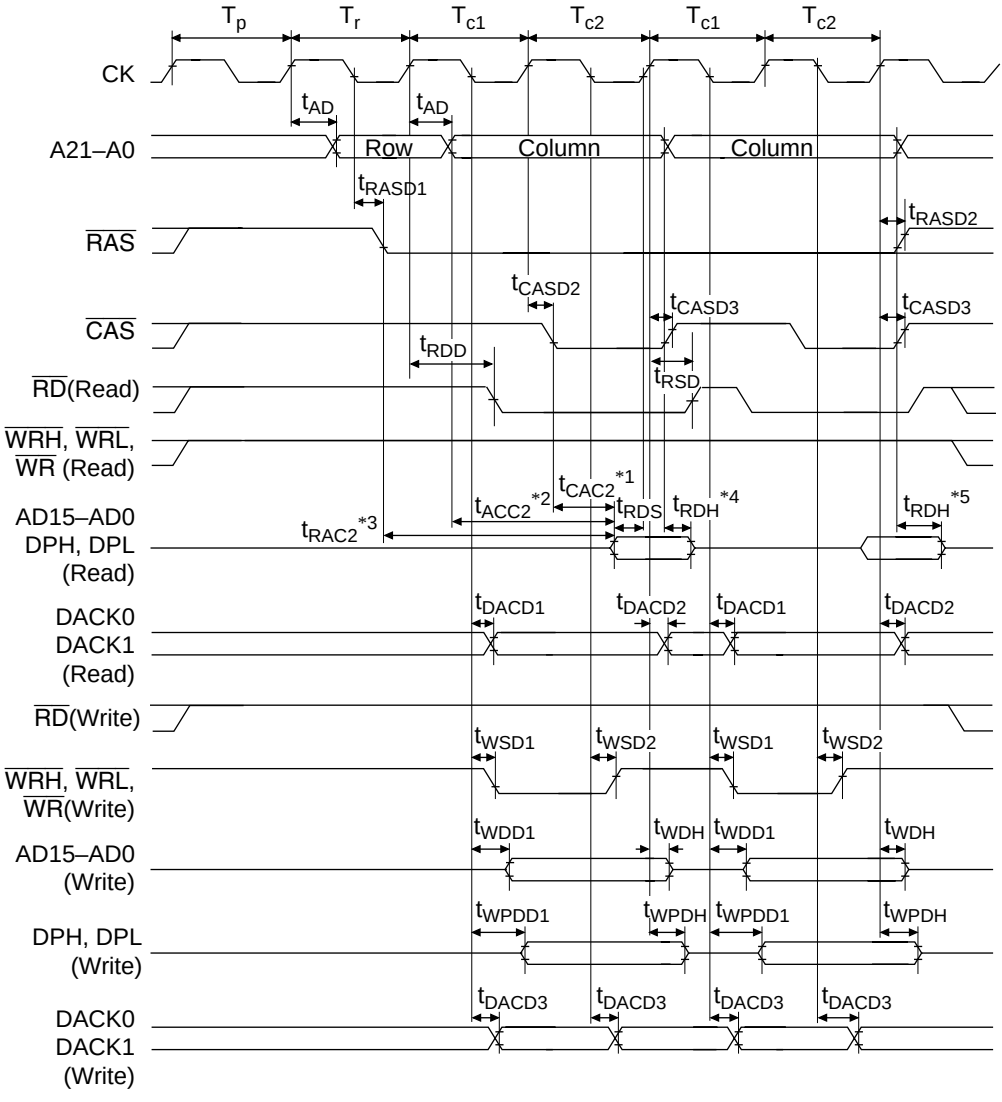
Figure 20.56 (b) DRAM Bus Cycle (Short-Pitch, High-Speed Page Mode: Write)

Note: For details of the silent cycle, see section 8.5.5, DRAM Burst Mode.



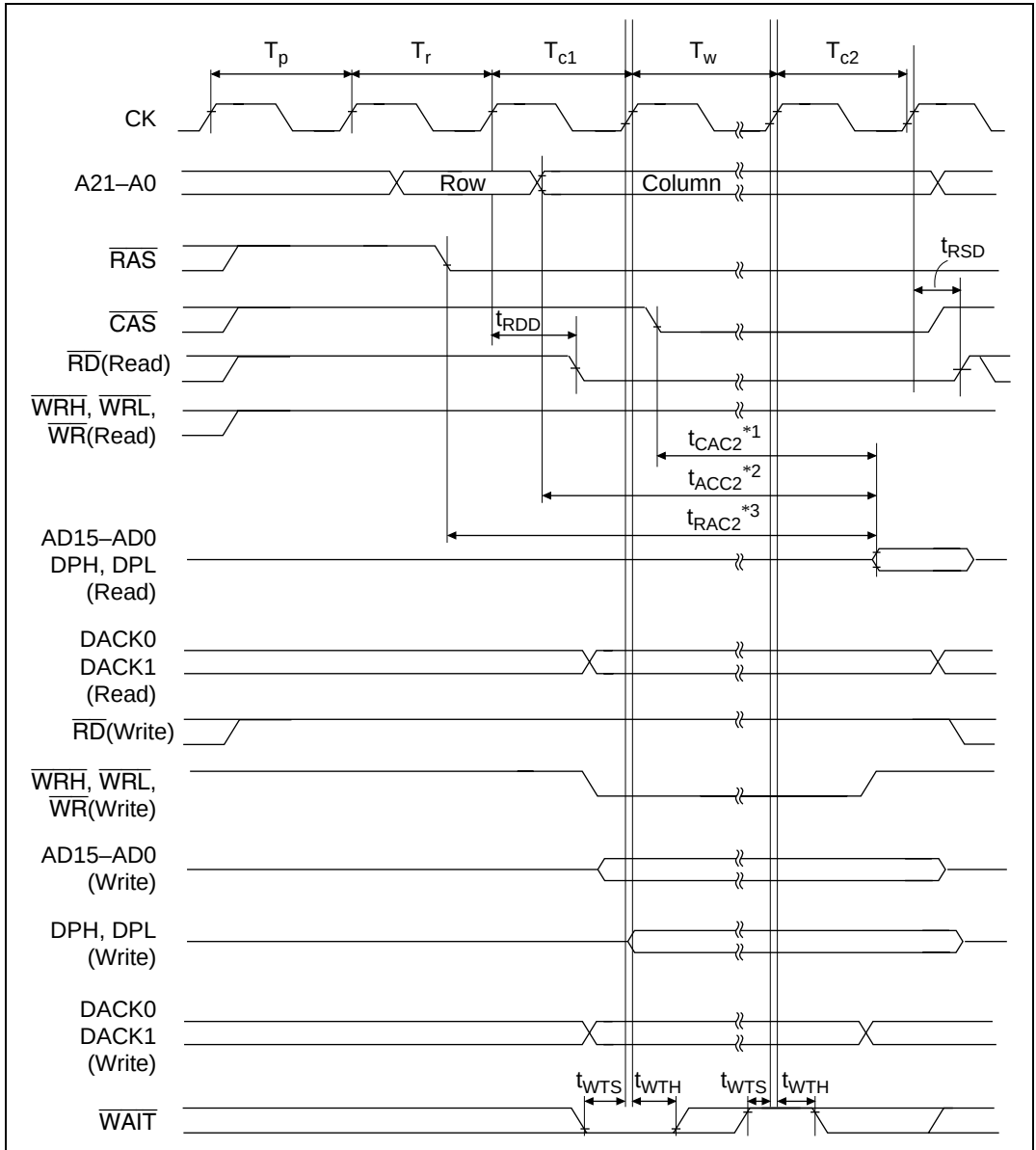
Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0, $\overline{CAS}$, or $\overline{RAS}$, whichever is negated first.

Figure 20.57 DRAM Bus Cycle: (Long-Pitch, Normal Mode)



Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD2} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0 or $\overline{CAS}$, whichever is negated first.
5. t_{RDH} is measured from A21–A0, $\overline{RAS}$, or $\overline{CAS}$ whichever is negated first.

Figure 20.58 DRAM Bus Cycle: (Long-Pitch, High-Speed Page Mode)



Notes: 1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.

Figure 20.59 DRAM Bus Cycle: (Long-Pitch, High-Speed Page Mode + Wait State)

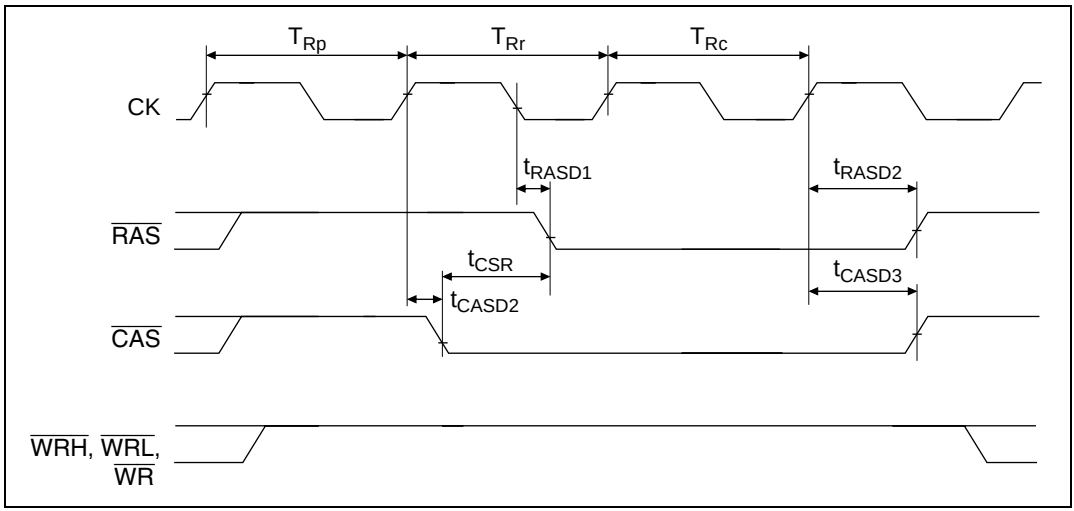


Figure 20.60 CAS-before-RAS Refresh (Short-Pitch)

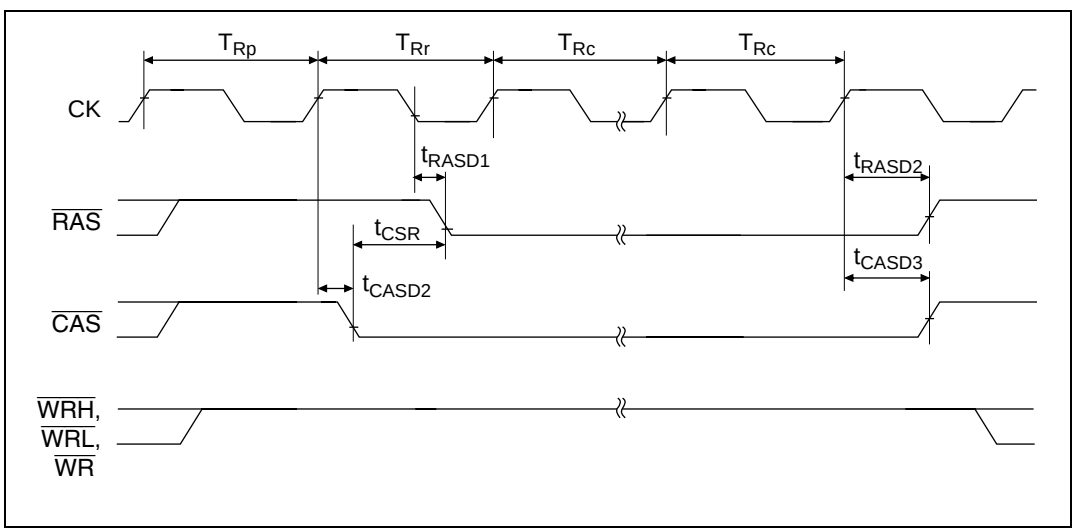


Figure 20.61 CAS-before-RAS Refresh (Long-Pitch)

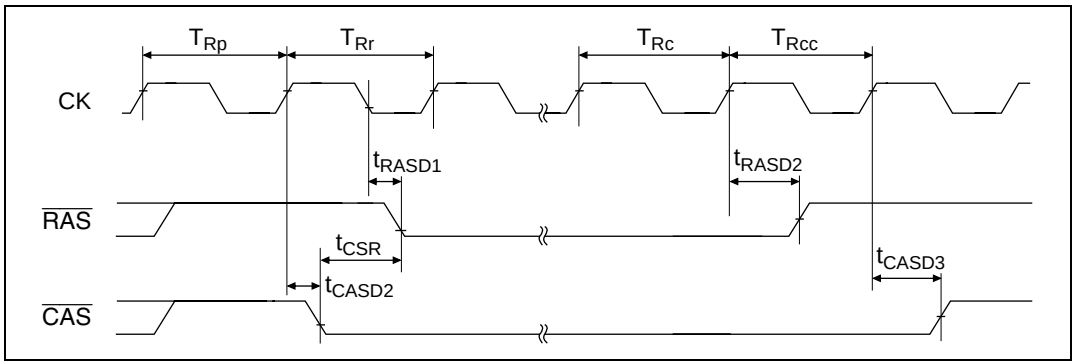


Figure 20.62 Self-Refresh

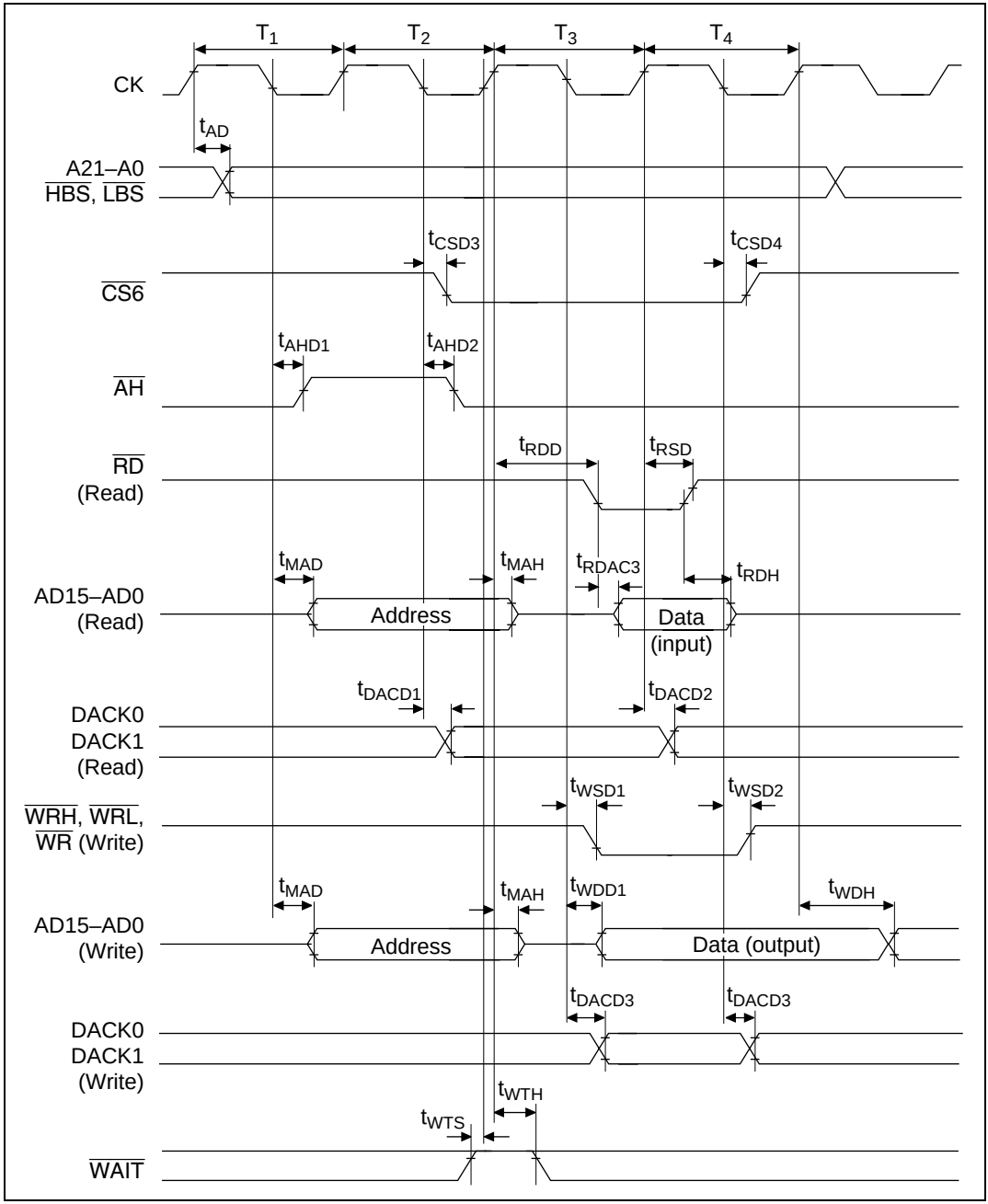


Figure 20.63 Address/Data Multiplex I/O Bus Cycle

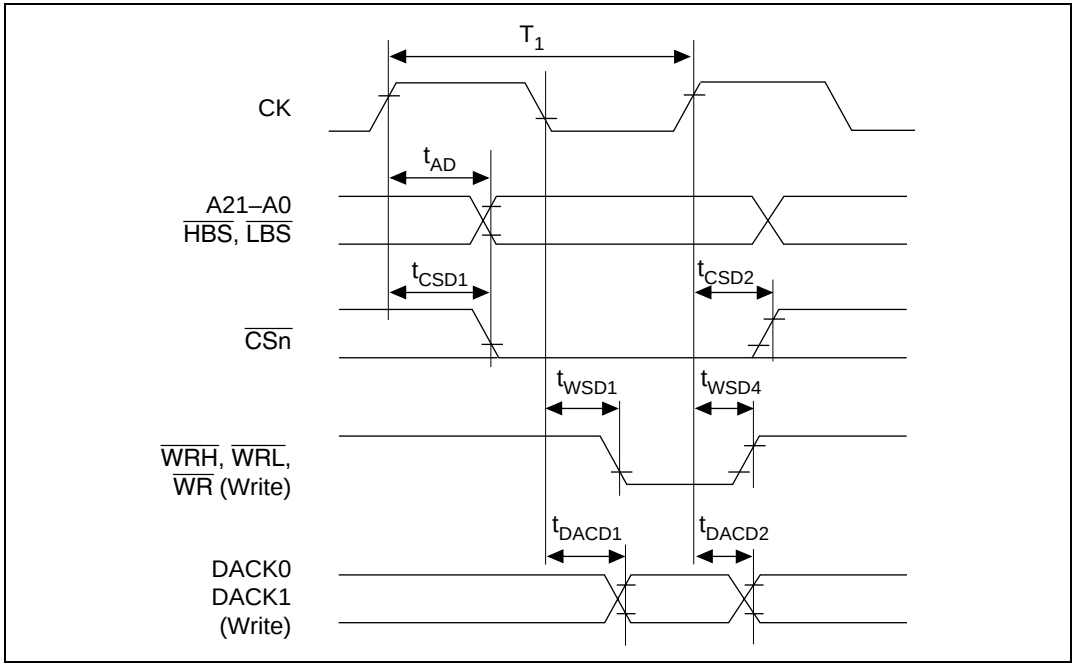


Figure 20.64 DMA Single Transfer/One-State Access Write

(4) DMAC Timing

Table 20.21 DMAC Timing

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Notes: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		12.5 MHz		20 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Figure**
$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ setup time	t_{DRQS}	80	—	27	—	ns	20.65
$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ hold time	t_{DRQH}	30	—	30	—	ns	
$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ Pulse width	t_{DRQW}	1.5	—	1.5	—	t_{cyc}	20.66

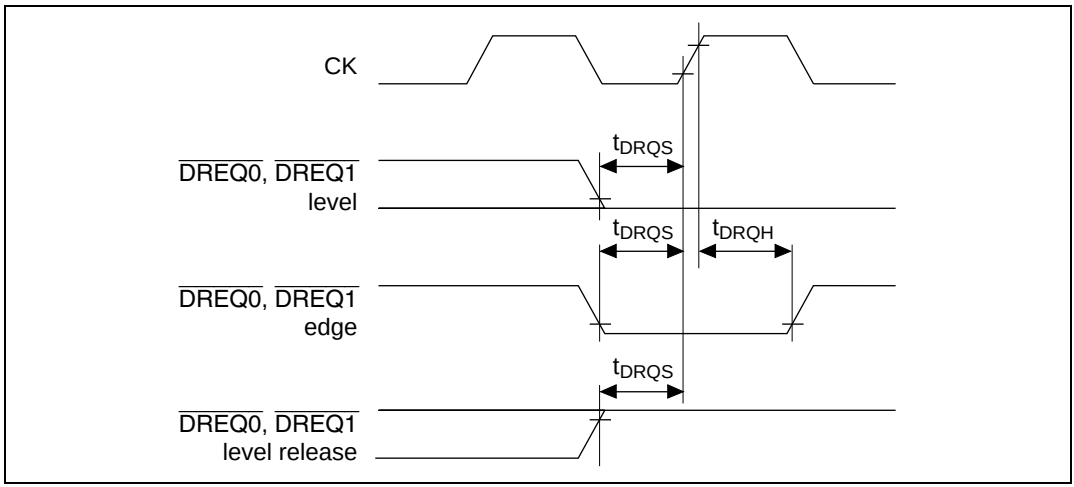


Figure 20.65 DREQ0, DREQ1 Input Timing (1)

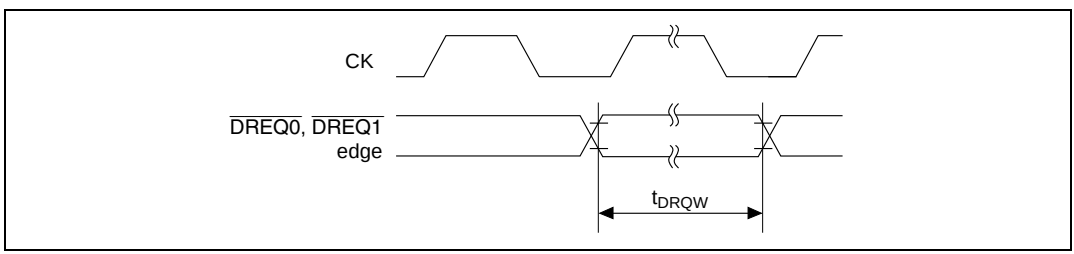


Figure 20.66 DREQ0, DREQ1 Input Timing (2)

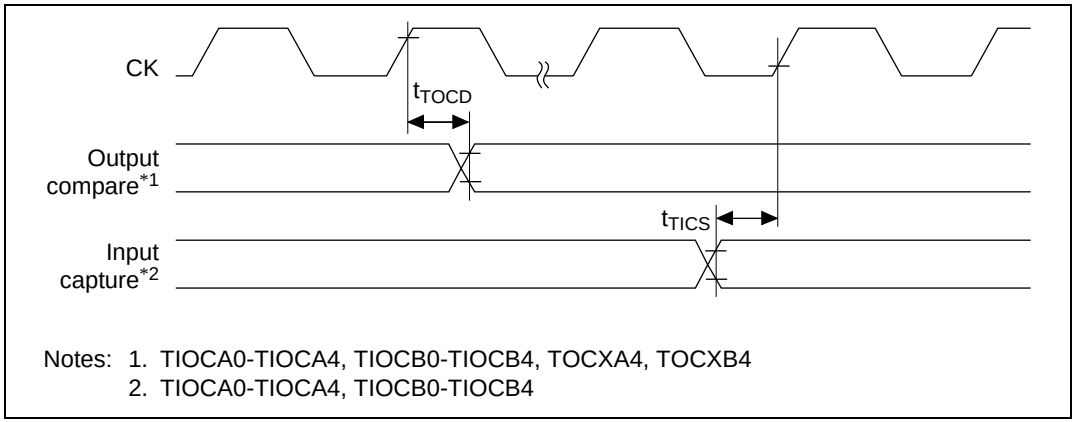
(5) 16-bit Integrated Timer Pulse Unit Timing

Table 20.22 16-bit Integrated Timer Pulse Unit Timing

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Notes: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

		12.5 MHz		20 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Figure**
Output compare delay time	t_{TOCD}	—	100	—	100	ns	20.67
Input capture setup time	t_{TICS}	50	—	35	—	ns	
Timer clock input setup time	t_{TCKS}	50	—	50	—	ns	20.68
Timer clock pulse width (single edge)	$t_{TCKWH/L}$	1.5	—	1.5	—	t_{cyc}	
Timer clock pulse width (both edges)	$t_{TCKWL/L}$	2.5	—	2.5	—	t_{cyc}	



Notes: 1. TIOCA0-TIOCA4, TIOCB0-TIOCB4, TOCXA4, TOCXB4
2. TIOCA0-TIOCA4, TIOCB0-TIOCB4

Figure 20.67 ITU Input/Output Timing

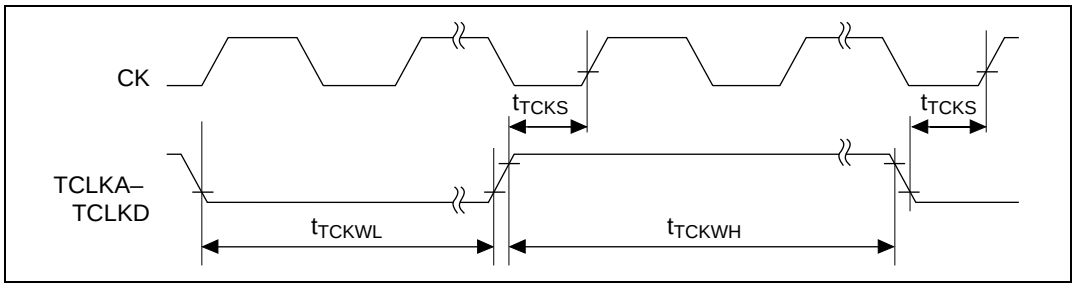


Figure 20.68 ITU Clock Input Timing

(6) Programmable Timing Pattern Controller and I/O Port Timing

Table 20.23 Programmable Timing Pattern Controller and I/O Port Timing

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 12.5 to 20 MHz*1, Ta = –20 to +75°C*2

Notes: 1. ROMless products only for 20 MHz version
2. Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item	Symbol	Min	Max	Unit	Figure
Port output delay time	t_{PWD}	—	100	ns	20.69
Port input hold time	t_{PRH}	50	—	ns	
Port input setup time	t_{PRS}	50	—	ns	

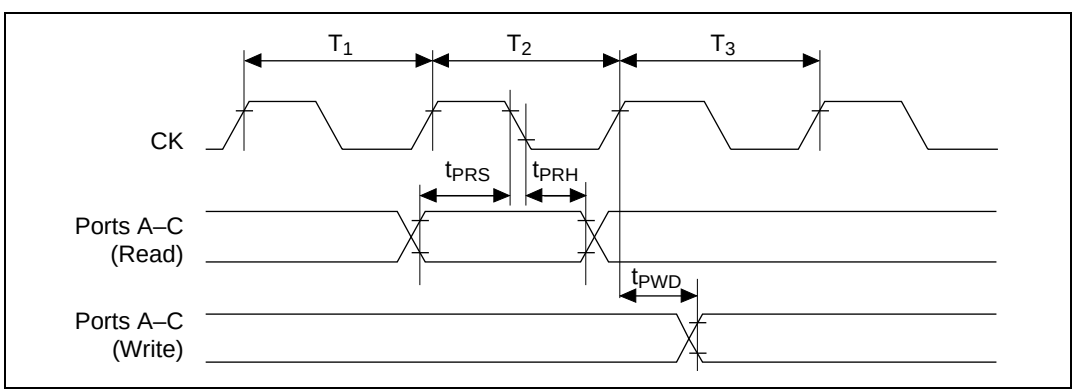


Figure 20.69 Programmable Timing Pattern Controller Output Timing

(7) Watchdog Timer Timing

Table 20.24 Watchdog Timer Timing

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 12.5 to 20 MHz*1, Ta = –20 to +75°C*2

Notes: 1. ROMless products only for 20 MHz version
2. Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item	Symbol	Min	Max	Unit	Figure
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	100	ns	20.70

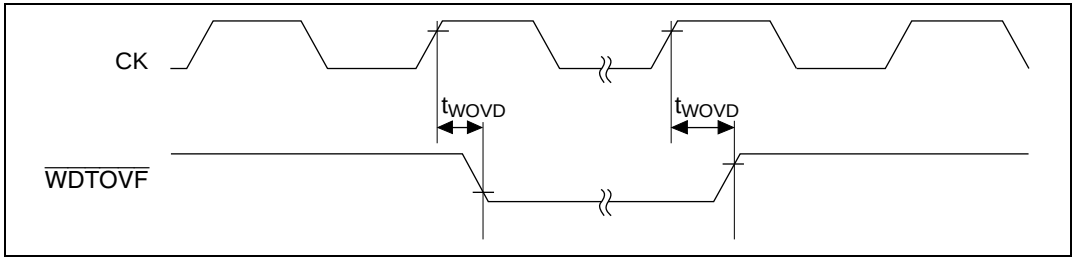


Figure 20.70 Watchdog Timer Output Timing

(8) Serial Communication Interface Timing

Table 20.25 Serial Communication Interface Timing

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 12.5 to 20 MHz*1, Ta = –20 to +75°C*2

Notes: 1. ROMless products only for 20 MHz version
2. Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item	Symbol	Min	Max	Unit	Figure
Input clock cycle	t_{scyc}	4	—	t_{cyc}	20.71
Input clock cycle (synchronous mode)	t_{scyc}	6	—	t_{cyc}	
Input clock pulse width	t_{SCKW}	0.4	0.6	t_{scyc}	
Input clock rise time	t_{SCKr}	—	1.5	t_{cyc}	
Input clock fall time	t_{SCKf}	—	1.5	t_{cyc}	
Transmit data delay time (synchronous mode)	t_{TXD}	—	100	ns	20.72
Receive data setup time (synchronous mode)	t_{RXS}	100	—	ns	
Receive data hold time (synchronous mode)	t_{RXH}	100	—	ns	

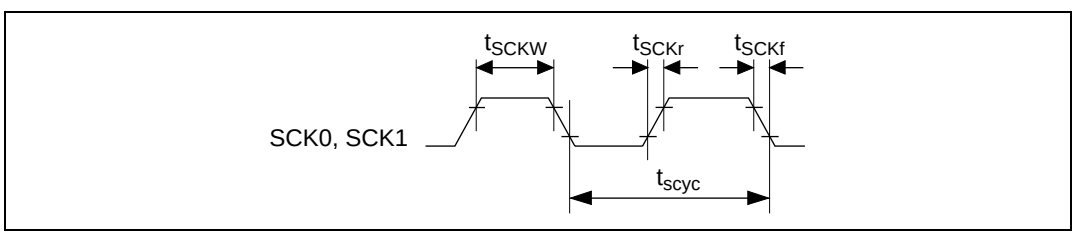


Figure 20.71 Input Clock Timing

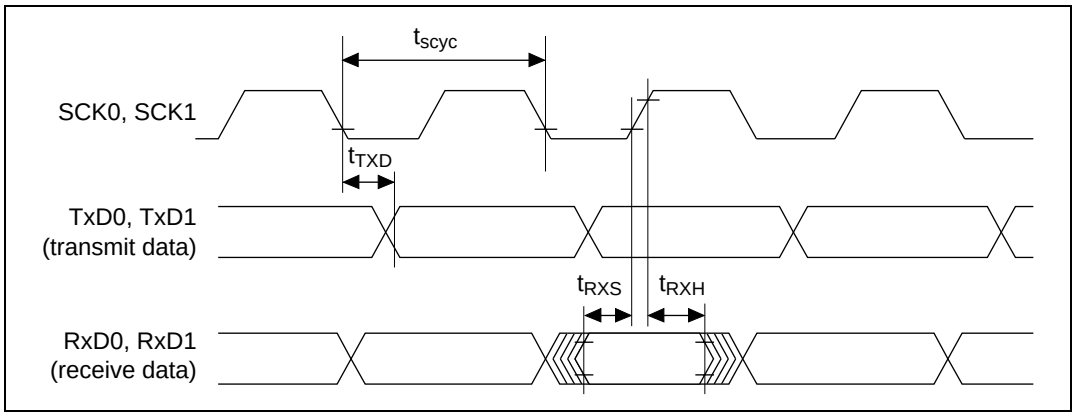


Figure 20.72 SCI I/O Timing (Synchronous Mode)

(9) A/D Converter Timing

Table 20.26 A/D Converter Timing

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, φ = 12.5 to 20 MHz*1, Ta = –20 to +75°C*2

Notes: 1. ROMless products only for 20 MHz version
2. Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

Item		Symbol	Min	typ	Max	Unit	Figure
External trigger input pulse width		t_{TRGW}	2.0	—	—	t_{cyc}	20.73
External trigger input start delay time		t_{TRGS}	50	—	—	ns	
A/D conversion start delay time	CKS = 0	t_D	10	—	17	t_{cyc}	20.74
	CKS = 1		6	—	9	t_{cyc}	
Input sampling time	CKS = 0	t_{SPL}	—	64	—	t_{cyc}	
	CKS = 1		—	32	—	t_{cyc}	
A/D conversion time	CKS = 0	t_{CONV}	259	—	266	t_{cyc}	
	CKS = 1		131	—	134	t_{cyc}	

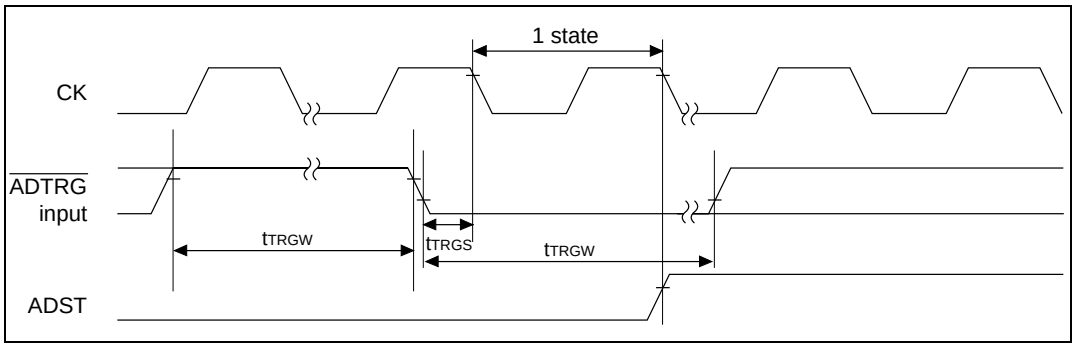


Figure 20.73 External Trigger Input Timing

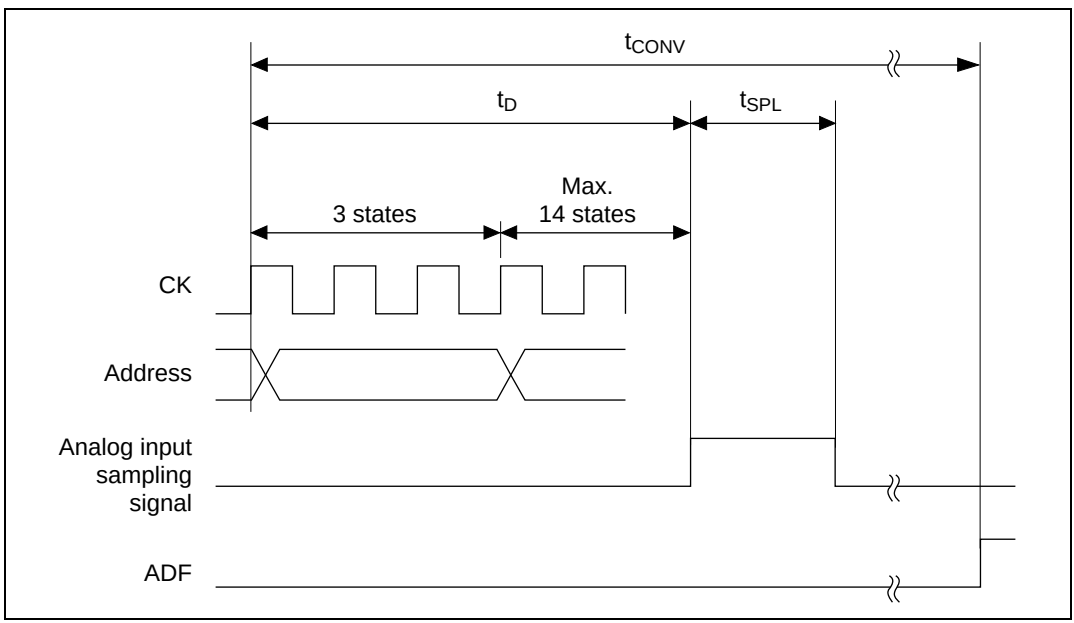
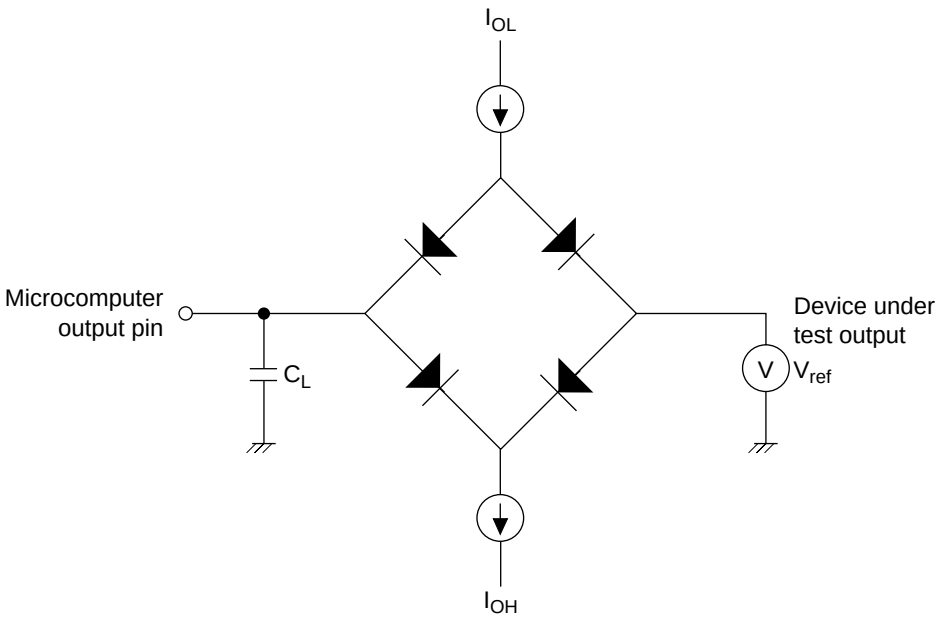


Figure 20.74 Analog Conversion Timing

(10) AC Characteristics Test Conditions



C_L is set as follows for each pin.
30pF: CK, $\overline{\text{CASH}}$, $\overline{\text{CASL}}$, $\overline{\text{CS0}}$–$\overline{\text{CS7}}$, $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, $\overline{\text{AH}}$, $\overline{\text{IRQOUT}}$, $\overline{\text{RAS}}$, DACK0, DACK1
50pF: A21–A0, AD15–AD0, DPH, DPL, $\overline{\text{RD}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{HBS}}$, $\overline{\text{LBS}}$, $\overline{\text{WR}}$
70pF: All port outputs and supporting module output pins other than the above.
I_{OL} and I_{OH} values are as shown in section 20.2.2, DC Characteristics, and table 20.17, Permitted Output Current Values.

Figure 20.75 Output Load Circuit

20.2.4 A/D Converter Characteristics

Table 20.27 A/D Converter Characteristics

Conditions: V_{CC} = 3.3 V ±0.3V, AV_{CC} = 3.3 V ±0.3V, AV_{CC} = V_{CC} ±0.3V, AV_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C*

Notes: * Regular-specification products; for wide-temperature-range products, Ta = –40 to +85°C

	12.5 MHz			20 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	bit
Conversion time	—	—	11.2	—	—	6.7	µS
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	1	—	—	1	kΩ
Nonlinearity error*	—	—	±4.0	—	—	±4.0	LSB
Offset error*	—	—	±4.0	—	—	±4.0	LSB
Full-scale error*	—	—	±4.0	—	—	±4.0	LSB
Quantization error*	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	LSB

Note: * Reference value

Appendix A On-Chip Supporting Module Registers

A.1 List of Registers

The addresses and bit names of the on-chip supporting module registers are listed below. 16- and 32-bit registers are shown as two or four levels of 8 bits each.

Table A.1 8-Bit Access Space (8-Bit and 16-Bit Accessible, 32-Bit Access Disabled)

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFE00–H'5FFFEBF	—	—	—	—	—	—	—	—	—	—
H'5FFFEC0	SMR0	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI (channel 0)
H'5FFFEC1	BRR0									
H'5FFFEC2	SCR0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'5FFFEC3	TDR0									
H'5FFFEC4	SSR0	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
H'5FFFEC5	RDR0									
H'5FFFEC6	—	—	—	—	—	—	—	—	—	
H'5FFFEC7	—	—	—	—	—	—	—	—	—	
H'5FFFEC8	SMR1	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI (channel 1)
H'5FFFEC9	BRR1									
H'5FFFECA	SCR1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'5FFFECB	TDR1									
H'5FFFECC	SSR1	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
H'5FFFECD	RDR1									
H'5FFFECE–H'5FFFEDF	—	—	—	—	—	—	—	—	—	
H'5FFFEE0	ADDRAH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D
H'5FFFEE1	ADDRAL	AD1	AD0	—	—	—	—	—	—	
H'5FFFEE2	ADDRBH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
H'5FFFEE3	ADDRBL	AD1	AD0	—	—	—	—	—	—	
H'5FFFEE4	ADDRCH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
H'5FFFEE5	ADDRCL	AD1	AD0	—	—	—	—	—	—	
H'5FFFEE6	ADDRDH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
H'5FFFEE7	ADDRDL	AD1	AD0	—	—	—	—	—	—	
H'5FFFEE8	ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0	
H'5FFFEE9	ADCR	TRGE	—	—	—	—	—	—	—	
H'5FFFEEA–H'5FFFEEF	—	—	—	—	—	—	—	—	—	

Table A.2 16-bit Access Space (In Principle, 8-Bit, 16-Bit and 32-Bit Accessible)

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFF00	TSTR*[1]	—	—	—	STR4	STR3	STR2	STR1	STR0	ITU (channels 0–4 shared)
H'5FFFF01	TSNC*[1]	—	—	—	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	
H'5FFFF02	TMDR*[1]	—	MDF	FDIR	PWM4	PWM3	PWM2	PWM1	PWM0	
H'5FFFF03	TFCR*[1]	—	—	CMD1	CMD0	BFB4	BFA4	BFB3	BFA3	
H'5FFFF04	TCR0*[1]	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	ITU (channel 0)
H'5FFFF05	TIOR0*[1]	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
H'5FFFF06	TIER0*[1]	—	—	—	—	—	OVIE	IMIEB	IMIEA	
H'5FFFF07	TSR0*[1]	—	—	—	—	—	OVF	IMFB	IMFA	
H'5FFFF08	TCNT0									
H'5FFFF09										
H'5FFFF0A	GRA0									
H'5FFFF0B										
H'5FFFF0C	GRB0									
H'5FFFF0D										
H'5FFFF0E	TCR1*[1]	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	ITU (channel 1)
H'5FFFF0F	TIORL*[1]	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
H'5FFFF10	TIERI*[1]	—	—	—	—	—	OVIE	IMIEB	IMIEA	
H'5FFFF11	TSR1*[1]	—	—	—	—	—	OVF	IMFB	IMFA	
H'5FFFF12	TCNT1									
H'5FFFF13										
H'5FFFF14	GRA1									
H'5FFFF15										
H'SFFFF16	GRB1									
H'5FFFF17										
H'5FFFF18	TCR2*[1]	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	ITU (channel 2)
H'5FFFF19	TIOR2*[1]	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
H'5FFFF1A	TIER2*[1]	—	—	—	—	—	OVIE	IMIEB	IMIEA	
H'5FFFF1B	TSR2*[1]	—	—	—	—	—	OVF	IMFB	IMFA	
H'5FFFF1C	TCNT2									
H'5FFFF1D										
H'5FFFF1E	GRA2									
H'5FFFF1F										
H'5FFFF20	GRB2									
H'5FFFF21										

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFF22	TCR3*[1]	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	ITU (channel 3)
H'5FFFF23	TIOR3*[1]	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
H'5FFFF24	TIER3*[1]	—	—	—	—	—	OVIE	IMIEB	IMIEA	
H'5FFFF25	TSR3*[1]	—	—	—	—	—	OVF	IMFB	IMFA	
H'5FFFF26	TCNT3									
H'5FFFF27										
H'5FFFF28	GRA3									
H'5FFFF29										
H'5FFFF2A	GRB3									
H'5FFFF2B										
H'5FFFF2C	BRA3									
H'5FFFF2D										
H'5FFFF2E	BRB3									
H'5FFFF2F										
H'5FFFF31	TOCR*[1]	—	—	—	—	—	—	OLS4	OLS3	ITU (channels 0–4 shared)
H'5FFFF32	TCR4*[1]	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	ITU (channel 4)
H'5FFFF33	TIOR4*[1]	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
H'5FFFF34	TIER4*[1]	—	—	—	—	—	OVIE	IMIEB	IMIEA	
H'5FFFF35	TSR4*[1]	—	—	—	—	—	OVF	IMFB	IMFA	
H'5FFFF36	TCNT4									
H'5FFFF37										
H'5FFFF38	GRA4									
H'5FFFF39										
H'5FFFF3A	GRB4									
H'5FFFF3B										
H'5FFFF3C	BRA4									
H'5FFFF3D										
H'5FFFF3E	BRB4									
H'5FFFF3F										

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFF40	SAR0*5									DMAC channel 0
H'5FFFF41										
H'5FFFF42										
H'5FFFF43										
H'5FFFF44	DAR0*5									
H'5FFFF45										
H'5FFFF46										
H'5FFFF47										
H'5FFFF48	DMAOR*2	—	—	—	—	—	—	PR1	PR0	
H'5FFFF49		—	—	—	—	—	AE	NMIF	DME	
H'5FFFF4A	TCR0*5									
H'5FFFF4B										
H'5FFFF4C	—	—	—	—	—	—	—	—	—	
H'5FFFF4D	—	—	—	—	—	—	—	—	—	
H'5FFFF4E	CHCR0	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H'5FFFF4F		AM	AL	DS	TM	TS	IE	TE	DE	
H'5FFFF50	SAR1*5									DMAC channel 1
H'5FFFF51										
H'5FFFF52										
H'5FFFF53										
H'5FFFF54	DAR1*5									
H'5FFFF55										
H'5FFFF56										
H'5FFFF57										
H'5FFFF58	—	—	—	—	—	—	—	—	—	
H'5FFFF59	—	—	—	—	—	—	—	—	—	
H'5FFFF5A	TCR1*5									
H'5FFFF5B										
H'5FFFF5C	—	—	—	—	—	—	—	—	—	
H'5FFFF5D	—	—	—	—	—	—	—	—	—	
H'5FFFF5E	CHCR1	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H'5FFFF5F		AM	AL	DS	TM	TS	IE	TE	DE	

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFF60	SAR2*5									DMAC channel 2
H'5FFFF61										
H'5FFFF62										
H'5FFFF63										
H'5FFFF64	DAR2*5									
H'5FFFF65										
H'5FFFF66										
H'5FFFF67										
H'5FFFF68	—	—	—	—	—	—	—	—	—	
H'5FFFF69	—	—	—	—	—	—	—	—	—	
H'5FFFF6A	TCR2*5									
H'5FFFF6B										
H'5FFFF6C	—	—	—	—	—	—	—	—	—	
H'5FFFF6D	—	—	—	—	—	—	—	—	—	
H'5FFFF6E	CHCR2	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H'5FFFF6F		AM	AL	DS	TM	TS	IE	TE	DE	
H'5FFFF70	SAR3*5									DMAC channel 3
H'5FFFF71										
H'5FFFF72										
H'5FFFF73										
H'5FFFF74	DAR3*5									
H'5FFFF75										
H'5FFFF76										
H'5FFFF77										
H'5FFFF78	—	—	—	—	—	—	—	—	—	
H'5FFFF79	—	—	—	—	—	—	—	—	—	
H'5FFFF7A	TCR3*5									
H'5FFFF7B										
H'5FFFF7C	—	—	—	—	—	—	—	—	—	
H'5FFFF7D	—	—	—	—	—	—	—	—	—	
H'5FFFF7E	CHCR3	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H5FFFF7F		AM	AL	DS	TM	TS	IE	TE	DE	

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFF80–H'5FFFF83	—	—	—	—	—	—	—	—	—	INTC
H'5FFFF84	IPRA									
H'5FFFF85										
H'5FFFF86	IPRB									
H'5FFFF87										
H'5FFFF88	IPRC									
H'5FFFF89										
H'5FFFF8A	IPRD									
H'5FFFF8B										
H'5FFFF8C	IPRE									
H'5FFFF8D										
H'5FFFF8E	ICR	NMIL	—	—	—	—	—	—	NMIE	
H'5FFFF8F		IRQ0S	IRQ1S	IRQ2S	IRQ3S	IRQ4S	IRQ5S	IRQ6S	IRQ7S	
H'5FFFF90	BARH	BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24	UBC
H'5FFFF91		BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16	
H'5FFFF92	BARL	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8	
H'5FFFF93		BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
H'5FFFF94	BAMRH	BAM31	BAM30	BAM29	BAM28	BAM27	BAM26	BAM25	BAM24	
H'5FFFF95		BAM23	BAM22	BAM21	BAM20	BAM19	BAM18	BAM17	BAM16	
H'5FFFF96	BAMRL	BAM15	BAM14	BAM13	BAM12	BAM11	BAM10	BAM9	BAM8	
H'5FFFF97		BAM7	BAM6	BAM5	BAM4	BAM3	BAM2	BAM1	BAM0	
H'5FFFF98	BBR	—	—	—	—	—	—	—	—	
H'5FFFF99		CD1	CD0	ID1	ID0	RW1	RW0	SZ1	SZ0	
H'5FFFF9A–H'5FFFF9F	—	—	—	—	—	—	—	—	—	

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFFA0	BCR	DRAME	IOE	WARP	RDDTY	BAS	—	—	—	BSC
H'5FFFFA1		—	—	—	—	—	—	—	—	
H'5FFFFA2	WCR1	RW7	RW6	RW5	RW4	RW3	RW2	RW1	RW0	
H'5FFFFA3		—	—	—	—	—	—	WW1	—	
H'5FFFFA4	WCR2	DRW7	DRW6	DRW5	DRW4	DRW3	DRW2	DRW1	DRW0	
H'5FFFFA5		DWW7	DWW6	DWW5	DWW4	DWW3	DWW2	DWW1	DWW0	
H'5FFFFA6	WCR3	WPU	A02LW1	A02LW0	A6LW1	A6LW0	—	—	—	
H'5FFFFA7		—	—	—	—	—	—	—	—	
H'5FFFFA8	DCR	CW2	RASD	TPC	BE	CDTY	MXE	MXC1	MXC0	
H'5FFFFA9		—	—	—	—	—	—	—	—	
H'5FFFFAA	PCR	PEF	PFRC	PEO	PCHK1	PCHK0				
H'5FFFFAB		—	—	—	—	—	—	—	—	
H'5FFFFAC	RCR	—	—	—	—	—	—	—	—	
H'5FFFFAD		RFSHE	RMODE	RLW1	RLW0	—	—	—	—	
H'5FFFFAE	RTCSR	—	—	—	—	—	—	—	—	
H'5FFFFAF		CMF	CMIE	CKS2	CKS1	CKS0				
H'5FFFFB0	RTCNT	—	—	—	—	—	—	—	—	
H'5FFFFB1										
H'5FFFFB2	RTCOR	—	—	—	—	—	—	—	—	
H'5FFFFB3										
H'5FFFFB4–H'5FFFFB7	—	—	—	—	—	—	—	—	—	
H'5FFFFB8	TCSR*[3]	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0	WDT
H'5FFFFB9	TCNT*[3]									
H'5FFFFBA	—	—	—	—	—	—	—	—	—	
H'5FFFFBB	RSTCSR*[3]	WOVF	RSTE	RSTS	—	—	—	—	—	
H'5FFFFBC	SBYCR	SBY	HIZ	—	—	—	—	—	—	Power down state
H'5FFFFBD–H'5FFFFBF	—	—	—	—	—	—	—	—	—	—

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFFC0	PADR	PA15 DR	PA14 DR	PA13 DR	PA12 DR	PA11 DR	PA10 DR	PA9 DR	PA8 DR	Port A
H'5FFFFC1		PA7 DR	PA6 DR	PA5 DR	PA4 DR	PA3 DR	PA2 DR	PA1 DR	PA0 DR	
H'5FFFFC2	PBDR	PB15 DR	PB14 DR	PB13 DR	PB12 DR	PB11 DR	PB10 DR	PB9 DR	PB8 DR	Port B
H'5FFFFC3		PB7 DR	PB6 DR	PB5 DR	PB4 DR	PB3 DR	PB2 DR	PB1 DR	PB0 DR	
H'5FFFFC4	PAIOR	PA15 IOR	PA14 IOR	PA13 IOR	PA12 IOR	PA11 IOR	PA10 IOR	PA9 IOR	PA8 IOR	PFC
H'5FFFFC5		PA7 IOR	PA6 IOR	PA5 IOR	PA4 IOR	PA3 IOR	PA2 IOR	PA1 IOR	PA0 IOR	
H'5FFFFC6	PBIOR	PB15 IOR	PB14 IOR	PB13 IOR	PB12 IOR	PB11 IOR	PB10 IOR	PB9 IOR	PB8 IOR	
H'SFFFFC7		PB7 IOR	PB6 IOR	PB5 IOR	PB4 IOR	PB3 IOR	PB2 IOR	PB1 IOR	PB0 IOR	
H'5FFFFC8	PACR1	PA15 MD1	PA15 MD0	PA14 MD1	PA14 MD0	PA13 MD1	PA13 MD0	PA12 MD1	PA12 MD0	
H'5FFFFC9		PA11 MD1	PA11 MD0	PA10 MD1	PA10 MD0	PA9 MD1	PA9 MD0	—	PA8 MD	
H'5FFFFCA	PACR2	—	PA7 MD	—	PA6 MD	—	PA5 MD	—	PA4 MD	
H'5FFFFCB		PA3 MD1	PA3 MD0	PA2 MD1	PA2 MD0	PA1 MD1	PA1 MD0	PA0 MD1	PA0 MD0	
H'5FFFFCC	PBCR1	PB15 MD1	PB15 MD0	PB14 MD1	PB14 MD0	PB13 MD1	PB13 MD0	PB12 MD1	PB12 MD0	
H'5FFFFCD		PB11 MD1	PB11 MD0	PB10 MD1	PB10 MD0	PB9 MD1	PB9 MD0	PB8 MD1	PB8 MD0	
H'5FFFFCE	PBCR2	PB7 MD1	PB7 MD0	PB6 MD1	PB6 MD0	PB5 MD1	PB5 MD0	PB4 MD1	PB4 MD0	
H'5FFFFCF		PB3 MD1	PB3 MD0	PB2 MD1	PB2 MD0	PB1 MD1	PB1 MD0	PB0 MD1	PB0 MD0	
H'5FFFFD0	PCDR	—	—	—	—	—	—	—	—	Port C
H'5FFFFD1		PC7 DR	PC6 DR	PC5 DR	PC4 DR	PC3 DR	PC2 DR	PC1 DR	PC0 DR	

		Bit Name								
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Module**
H'5FFFFD2–H'5FFFFED	—	—	—	—	—	—	—	—	—	PFC
H'5FFFFEE	CASCR	CASHMD1	CASHMD0	CASLMD1	CASLMD0	—	—	—	—	
H'5FFFFEF		—	—	—	—	—	—	—	—	TPC
H'5FFFFF0	TPMR	—	—	—	—	G3NOV	G2NOV	G1NOV	G0NOV	
H'5FFFFF1	TPCR	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0	
H'5FFFFF2	NDERB	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8	
H'5FFFFF3	NDERA	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0	
H'5FFFFF4	NDRB*[4]	NDR15	NDR14	NDR13	NDR12	—	—	—	—	
H'5FFFFF5	NDRA*[4]	NDR7	NDR6	NDR5	NDR4	—	—	—	—	
H'5FFFFF6	NDRB*[4]	—	—	—	—	NDR11	NDR10	NDR9	NDR8	
H'5FFFFF7	NDRA*[4]	—	—	—	—	NDR3	NDR2	NDR1	NDR0	
H'5FFFFF8–H'5FFFFFF	—	—	—	—	—	—	—	—	—	

Notes
1. Only 8-bit accessible. 16-bit and 32-bit access disabled.
2. Register shared by all channels.
3. Address for read. For writing, the addresses are H'5FFFFB8 for TCR and TCNT and H'5FFFFBA for RSTCSR. For more information, see section 12, Watchdog Timer (WDT), particularly section 12.2.4, Notes on Register Access.
4. When the output triggers for TPC output group 0 and TPC output group 1 set by TPCR are the same, the NDRA address is H'5FFFFF5; when the output triggers are different, the NDRA address for group 0 is H'5FFFFF7 and the NDRA address for group 1 is H'5FFFFF5. Likewise, when the output triggers for TPC output group 2 and TPC output group 3 set by TPCR are the same, the NDRB address is H'5FFFFF4; when the output triggers are different, the NDRB address for group 2 is H'5FFFFF6 and the NDRB address for group 3 is H'5FFFFF4.
5. 16-bit and 32-bit accessible. 8-bit access disabled.

A.2 Register Tables

A.2.1 Serial Mode Register (SMR) SCI

Start Address: H'5FFFEC0 (channel 0), H'5FFFEC8 (channel 1)

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.3 SMR Bit Functions

Bit	Bit name	Value*	Description	
7	Communication mode (C/$\overline{A}$)	0	Asynchronous mode	(Initial value)
		1	Synchronous mode	
6	Character length (CHR)	0	8-bit data	(Initial value)
		1	7-bit data	
5	Parity enable (PE)	0	Parity bit addition and check disable	(Initial value)
		1	Parity bit addition and check enable	
4	Parity mode (O/$\overline{E}$)	0	Even parity	(Initial value)
		1	Odd parity	
3	Stop bit length (STOP)	0	1 stop bit	(Initial value)
		1	2 stop bits	
2	Multiprocessor mode (MP)	0	Multiprocessor function disabled	(Initial value)
		1	Multiprocessor function selected	
1,0	Clock select 1, 0 (CKS1, CKS0)	0	0 ϕ clock	(Initial value)
		0	1 ϕ/4 clock	
		1	0 ϕ/16 clock	
		1	1 ϕ/64 clock	

Note: * When 2 or more bits are treated as a group, the left side is the upper bit and the right the lower bit.

A.2.2 Bit Rate Register (BRR) SCI

Start Address: H'5FFFEC1 (channel 0), H'5FFFEC9 (channel 1)

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.4 BBR Bit Functions

Bit	Bit name	Description
7–0	(Bit rate setting)	Set serial transmission/reception bit rate

A.2.3 Serial Control Register (SCR) SCI

Start Address: H'5FFFEC2 (channel 0), H'5FFFECA (channel 1)

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.5 SCR Bit Functions

Bit	Bit Name	Value		Description	
7	Transmit interrupt enable (TIE)	0		Transmit data-empty interrupt request (TXI) disabled (Initial value)	
		1		Transmit data-empty interrupt request (TXI) enabled	
6	Receive interrupt enable (RIE)	0		Receive-data-full interrupt request (RXI) and receive-error interrupt request (ERI) disabled (Initial value)	
		1		Receive-data-full interrupt request (RXI) and receive-error interrupt request (ERI)	
5	Transmit enable (TE)	0		Transmission disabled (Initial value)	
		1		Transmission enabled	
4	Receive enable (RE)	0		Reception disabled (Initial value)	
		1		Reception enabled	
3	Multiprocessor interrupt enable (MPIE)	0		Multiprocessor interrupts disabled (normal receive operation) (Initial value) Clear conditions: (1) MPIE bit cleared to zero; (2) When data the MPB = 1 is received	
		1		Multiprocessor interrupts enabled. Disables receive interrupts (RXI), receive error interrupts (ERI), and setting of RDRF, FER, and ORER flags in SSR until data with a “1” multiprocessor bit is received	
2	Transmit end interrupt enable (TEIE)	0		Transmit interrupt requests (TEI) disabled (Initial value)	
		1		Transmit interrupt requests (TEI) enabled	
1	Clock enable 1 (CKE1)	0	0	Asynchronous mode	Internal clock/SCK pin is input pin (input signal ignored) or output pin (output level undetermined) (Initial value)
				Synchronous mode	Internal clock/SCK pin is synchronous clock output (Initial value)
		0	1	Asynchronous mode	Internal clock/SCK pin is clock output
				Synchronous mode	Internal clock/SCK pin is serial clock output
0	Clock enable 0 (CKE0)	1	0	Asynchronous mode	External clock/SCK pin is clock input
				Synchronous mode	External clock/SCK pin is serial clock input
		1	1	Asynchronous mode	External clock/SCK pin is clock input
				Synchronous mode	External clock/SCK pin is serial clock input

A.2.4 Transmit Data Register (TDR) SCI

Start Address: H'5FFFEC3 (channel 0), H'5FFFECB (channel 1)

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.6 TDR Bit Functions

Bit	Bit name	Description
7–0	(Transmit data storage)	Store data for serial transmission

A.2.5 Serial Status Register (SSR) SCI

Start Address: H'5FFFEC4 (channel 0), H'5FFFECC (channel 1)

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only 0 can be written, to clear the flags.

Table A.7 SSR Bit Functions

Bit	Bit name	Value	Description
7	Transmit data register empty (TDRE)	0	Indicates that valid transmit data has been written to TDR Clear Conditions: (1) 0 written in TDRE after reading TDRE = 1; (2) Data written to TDR by DMAC
		1	Indicates that there is no valid transmit data in TDR (Initial value) Set Conditions: (1) Reset or standby mode; (2) TE bit of SCR is 0; (3) Data transferred to TSR from TDR and data writing to TDR enabled
6	Receive data register full (RDRF)	0	Indicates that there is no valid receive data stored in RDR (Initial value) Clear Conditions: (1) Reset or standby mode; (2) 0 written in RDRF after reading RDRF = 1; (3) Data read in RDR by DMAC
		1	Indicates that valid receive data is stored in RDR Set Conditions: Serial reception ends normally and receive data is transferred to RDR from RSR
5	Overrun error (ORER)	0	Indicates that reception is in progress or has ended normally (Initial value) Clear Conditions: (1) Reset or standby mode; (2) 0 written in ORER after reading ORER = 1
		1	Indicates that an overrun error occurred in reception Set Conditions: The next serial reception ends while RDRF = 1
4	Framing error (FER)	0	Indicates that reception is in progress or has ended normally (Initial value) Clear Conditions: (1) Reset or standby mode; (2) 0 written in FER after reading FER = 1
		1	Indicates that a framing error occurred in reception Set Conditions: When the stop bit at the end of the receive data when the SCI finishes receiving has been checked to see if it is 1 and the stop bit is 0
3	Parity error (PER)	0	Indicates that reception is in progress or has ended normally (Initial value) Clear Conditions: (1) Reset or standby mode; (2) 0 written in PER after reading PER = 1
		1	Indicates that a parity error occurred in reception Set Conditions: When the number of 1's in the receive data and parity bit together during reception is not consistent with the even/odd parity setting specified in the O/$\overline{E}$ bit of the serial mode register (SMR)

Bit	Bit name	Value	Description
2	Transmit end (TEND)	0	Indicates that transmission is in progress Clear Conditions: (1) 0 written in TDRE after reading TDRE = 1; (2) Data written to TDR by DMAC
		1	Indicates that transmission has ended (Initial value) Set Conditions: (1) Reset or standby mode; (2) TE bit in SCR is 0; (3) TDRE = 1 when the final bit of a 1-byte serial transmit character is transmitted
1	Multiprocessor bit (MPB)	0	Indicates that data with multiprocessor bit = 0 has been received (Initial value)
		1	Indicates that data with multiprocessor bit = 1 has been received
0	Multiprocessor bit transfer (MPBT)	0	0 transmitted as the multiprocessor bit (Initial value)
		1	1 transmitted as the multiprocessor bit

A.2.6 Receive Data Register (RDR) SCI

Start Address: H'5FFFEC5 (channel 0), H'5FFFECD (channel 1)

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bit	Bit name	Description
7–0	(Receive serial data storage)	Store the serial data received

A.2.7 A/D Data Register AH–DL (ADDRAH–ADDRL) A/D

Start Address: H'5FFFEE0, H'5FFFEE1, H'5FFFEE2, H'5FFFEE3, H'5FFFEE4, H'5FFFEE5, H'5FFFEE6, H'5FFFEE7

Bus Width: 8/16

Bit	15	14	13	12	11	10	9	8
	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
	AD1	AD0	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Table A.8 ADDRAH–ADDRL Bit Functions

Bit	Bit name	Description
15–8	A/D data 9–2	Stores upper 8 bits of A/D conversion result
7,6	A/D data 1, 0	Stores upper 2 bits of A/D conversion result

A.2.8 A/D Control/Status Register (ADCSR) A/D

Start Address: H'5FFFEF8

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	0	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Only 0 can be written, to clear the flag.

Table A.9 ADCSR Bit Functions

Bit	Bit name	Value	Description
7	A/D end flag (ADF)	0	Clear conditions: (1) 0 written in ADF after reading ADF = 1; (2) DMAC started by ADI interrupt and A/D converter register is accessed (Initial value)
		1	Set Conditions: (1) Single mode: A/D conversion ends; (2) Scan mode: A/D conversion of all channels set has ended
6	A/D interrupt enable (ADF)	0	Interrupt requested by A/D conversion (ADI) disabled (Initial value)
		1	Interrupt requested by A/D conversion (ADI) enabled
5	A/D start (ADST)	0	Disable A/D conversion (Initial value)
		1	(1) Single mode: Start A/D conversion and when conversion ends, automatically cleared to zero; (2) Scan mode: Start A/D conversion and sequentially continue converting the selected channels until cleared to 0 by software, reset, or standby mode
4	Scan mode (SCAN)	0	Single mode (Initial value)
		1	Scan mode
3	Clock select (CKS)	0	Conversion time = 236 cycles (max) (Initial value)
		1	Conversion time = 134 cycles (max)

2–0	Channel select 2–0	CH2	CH1	CH0	Single mode	Scan mode
		0	0	0	AN0 (Initial value)	AN0 (Initial value)
				1	AN1	AN0, AN1
			1	0	AN2	AN0–AN2
				1	AN3	AN0–AN3
		1	0	0	AN4	AN4
				1	AN5	AN4, AN5
			1	0	AN6	AN4–AN6
				1	AN7	AN4–AN7

A.2.9 A/D Control Register (ADCR) A/D

Start Address: H'5FFFEE9

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	TRGE	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

Table A.10 ADCR Bit Functions

Bit	Bit name	Value	Description
7	Trigger enable bit (TRGE)	0	Start of A/D conversion by external trigger disabled (Initial value)
		1	Start of A/D conversion by rising edge of external conversion trigger input pin ($\overline{\text{ADTRG}}$) enabled

A.2.10 Timer Start Register (TSTR) ITU

Start Address: H'5FFFF00

Bus Width: 8

Bit	7	6	5	4	3	2	1	0
	—	—	—	STR4	STR3	STR2	STR1	STR0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Table A.11 TSTR Bit Functions

Bit	Bit name	Value	Description	
4	Counter start 4 (STR4)	0	Count operation of TCNT4 stops	(Initial value)
		1	TCNT4 counts	
3	Counter start 3 (STR3)	0	Count operation of TCNT 3 stops	(Initial value)
		1	TCNT3 counts	
2	Counter start 2 (STR2)	0	Count operation of TCNT 2 stops	(Initial value)
		1	TCNT2 counts	
1	Counter start 1 (STR1)	0	Count operation of TCNT 1 stops	(Initial value)
		1	TCNT1 counts	
0	Counter start 0 (STR0)	0	Count operation of TCNT 0 stops	(Initial value)
		1	TCNT0 counts	

A.2.11 Timer Synchronization Register (TSNC) ITU

Start Address: H'5FFFF01

Bus Width: 8

Bit	7	6	5	4	3	2	1	0
	—	—	—	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
Initial value	*	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Note: * Undetermined

Table A.12 TSNC Bit Functions

Bit	Bit name	Value	Description
4	Timer sync 4 (SYNC4)	0	Independent operation of channel 4 timer counter (TCNT4) (Initial value) (Preset/clear of TCNT4 is unrelated to other channels)
		1	Channel 4 operation is synchronous. TCNT4 sync preset/sync clear enabled.
3	Timer sync 3 (SYNC3)	0	Independent operation of channel 3 timer counter (TCNT3) (Initial value) (Preset/clear of TCNT3 is unrelated to other channels)
		1	Channel 3 operation is synchronous. TCNT3 sync preset/sync clear enabled.
2	Timer sync 2 (SYNC2)	0	Independent operation of channel 2 timer counter (TCNT2) (Initial value) (Preset/clear of TCNT2 is unrelated to other channels)
		1	Channel 2 operation is synchronous. TCNT2 sync preset/sync clear enabled.
1	Timer sync 1 (SYNC1)	0	Independent operation of channel 1 timer counter (TCNT1) (Initial value) (Preset/clear of TCNT1 is unrelated to other channels)
		1	Channel 1 operation is synchronous. TCNT1 sync preset/sync clear enabled.
0	Timer sync 0 (SYNC0)	0	Independent operation of channel 0 timer counter (TCNT0) (Initial value) (Preset/clear of TCNT0 is unrelated to other channels)
		1	Channel 0 operation is synchronous. TCNT0 sync preset/sync clear enabled.

A.2.12 Timer Mode Register (TMDR) ITU

Start Address: H'5FFFF02

Bus Width: 8

Bit	7	6	5	4	3	2	1	0
	—	MDF	FDIR	PWM4	PWM3	PWM2	PWM1	PWM0
Initial value	*	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Undetermined

Table A.13 TMDR Bit Functions

Bit	Bit name	Value	Description
6	Phase counting mode (MDF)	0	Channel 2 operates normally (Initial value)
		1	Channel 2 in phase count mode
5	Flag direction (FDIR)	0	OVF of TSR2 set to 1 when TCNT2 overflows or underflows (Initial value)
		1	OVF in TSR2 set to 1 when TCNT2 overflows
4	PWM mode 4 (PWM4)	0	Channel 4 operates normally (Initial value)
		1	Channel 4 in PWM mode
3	PWM mode 3 (PWM3)	0	Channel 3 operates normally (Initial value)
		1	Channel 3 in PWM mode
2	PWM mode 2 (PWM2)	0	Channel 2 operates normally (Initial value)
		1	Channel 2 in PWM mode
1	PWM mode 1 (PWM1)	0	Channel 1 operates normally (Initial value)
		1	Channel 1 in PWM mode
0	PWM mode 0 (PWM0)	0	Channel 0 operates normally (Initial value)
		1	Channel 0 in PWM mode

A.2.13 Timer Function Control Register (TFCR) ITU

Start Address: H'5FFFF03

Bus Width: 8

Bit	7	6	5	4	3	2	1	0
	—	—	CMD1	CMD0	BFB4	BFA4	BFB3	BFA3
Initial value	*	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Undetermined

Table A.14 TFCR Bit Functions

Bit	Bit name	Value		Description	
5,4	Combination modes 1, 0 (CMD1, CMD0)	0	0	Channel 3 and 4 operate normally	(Initial value)
		0	1	Channel 3 and 4 operate normally	
		1	0	Channels 3 and 4 are combined to operate in complementary PWM mode	
		1	1	Channels 3 and 4 are combined to operate in reset-synchronized PWM mode	
3	Buffer mode B4 (BFB4)		0	GRB4 operates normally	(Initial value)
			1	Buffer operation of GRB4 and BRB4	
2	Buffer mode A4 (BFA4)		0	GRA4 operates normally	(Initial value)
			1	Buffer operation of GRA4 and BRA4	
1	Buffer mode B3 (BFB3)		0	GRB3 operates normally	(Initial value)
			1	Buffer operation of GRB3 and BRB3	
0	Buffer mode A3 (BFA3)		0	GRA3 operates normally	(Initial value)
			1	Buffer operation of GRA3 and BRA3	

A.2.14 Timer Control Registers 0–4 (TCR0–TCR4) ITU

Start Address: H'5FFFF04 (channel 0), H'5FFFF0E (channel 1), H'5FFFF18 (channel 2), H'5FFFF22 (channel 3), H'5FFFF32 (channel 4)

Bus Width: 8

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	*	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Undetermined

Table A.15 TCR0–TCR4 Bit Functions

Bit	Bit name	Value			Description	
6,5	Counter clear 1, 0 (CCLR1, CCLR0)	0	0		TCNT clear disabled	(Initial value)
		0	1		TCNT cleared upon GRA compare match/input capture	
		1	0		TCNT cleared upon GRB compare match/input capture	
		1	1		Synchronized clear. TCNT cleared in synchronization with counter clear of other timers operating in sync	
4,3	Clock edge 1, 0 (CKEG1, CKEG0)	0	0		Count on rising edge	(Initial value)
		0	1		Count on falling edge	
		1	*		Count on both rising and falling edges	
2–0	Timer prescaler 2–0 (TPSC2–TPSC0)	0	0	0	Internal clock: Count on ϕ	(Initial value)
		0	0	1	Internal clock: Count on $\phi/2$	
		0	1	0	Internal clock: Count on $\phi/4$	
		0	1	1	Internal clock: Count on $\phi/8$	
		1	0	0	External clock A: Count on TCLKA pin input	
		1	0	1	External clock B: Count on TCLKB pin input	
		1	1	0	External clock C: Count on TCLKC pin input	
		1	1	1	External clock D: Count on TCLKD pin input	

Note: * 0 or 1

A.2.15 Timer I/O Control Registers 0–4 (TIOR0–TIOR4) ITU

Start Address: H'5FFFF05 (channel 0), H'5FFFF0F (channel 1), H'5FFFF19 (channel 2), H'5FFFF23 (channel 3), H'5FFFF33 (channel 4)

Bus Width: 8

Bit	7	6	5	4	3	2	1	0
	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
Initial value	*	0	0	0	1	0	0	0
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Note: * Undetermined

Table A.16 TIO0–TIO4 Bit Functions

Bit	Bit name	Value	Description	
6–4	I/O control B2–0 (IOB2–IOB0)	0 0 0	GRB is output compare register	Pin output due to compare match disabled (Initial value)
		0 0 1		0 output on GRB compare match
		0 1 0		1 output on GRB compare match
		0 1 1		Toggle output on GRB compare match (1 output on channel 2 only)
		1 0 0	GRB is input capture register	Input capture to GRB on rising edge
		1 0 1		Input capture to GRB on falling edge
		1 1 *		Input capture on both rising and falling edges
2–0	I/O control A2–0 (IOA2–IOA0)	0 0 0	GRA is output compare register	Pin output due to compare match disabled (Initial value)
		0 0 1		0 output on GRA compare match
		0 1 0		1 output on GRA compare match
		0 1 1		Toggle output on GRA compare match (1 output on channel 2 only)
		1 0 0	GRA is input capture register	Input capture to GRA on rising edge
		1 0 1		Input capture to GRA on falling edge
		1 1 *		Input capture on both rising and falling edges

Note: * 0 or 1

A.2.16 Timer Interrupt Enable Registers 0–4 (TIER0–TIER4) ITU

Start Address: H'5FFFF06 (channel 0), H'5FFFF10 (channel 1), H'5FFFF1A (channel 2), H'5FFFF24 (channel 3), H'5FFFF34 (channel 4),

Bus Width: 8

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	OVIE	IMIEB	IMIEA
Initial value	*	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	R/W	R/W	R/W

Note: * Undetermined

Table A.17 TIER0–TIER4 Bit Functions

Bit	Bit name	Value	Description
2	Overflow interrupt enable (OVIE)	0	Interrupt request by OVF (OVI) disabled (Initial value)
		1	Interrupt request by OVF (OVI) enabled
1	Input capture/compare match interrupt enable B (IMIEB)	0	Interrupt request by IMFB (IMIB) disabled (Initial value)
		1	Interrupt request by IMFB (IMIB) enabled
0	Input capture/compare match interrupt enable A (IMIEA)	0	Interrupt request by IMFA (IMIA) disabled (Initial value)
		1	Interrupt request by IMFA (IMIA) enabled

A.2.17 Timer Status Registers 0–4 (TSR0–TSR4) ITU

Start Address: H'5FFFF07 (channel 0), H'5FFFF11 (channel 1), H'5FFFF1B (channel 2), H'5FFFF25 (channel 3), H'5FFFF35 (channel 4),

Bus Width: 8

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	OVF	IMFB	IMFA
Initial value	*1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	R/(W)*2	R/(W)*2	R/(W)*2

Notes: 1. Undetermined
2. Only 0 can be written, to clear the flag.

Table A.18 TSR0–TSR4 Bit Functions

Bit	Bit name	Value	Description
2	Overflow flag (OVF)	0	Clear conditions: 0 is written in OVF after reading OVF = 1 (Initial value)
		1	Set conditions: TCNT value overflows (H'FFFF → H'0000) or underflows (H'FFFF → H'0000)
1	Input capture/compare match flag B (IMFB)	0	Clear conditions: 0 is written in IMFB after reading IMFB = 1 (Initial value)
		1	Set conditions: (1) When GRB is functioning as the output compare register, and TCNT = GRB; (2) When GRB is functioning as the input capture register, and the TCNT value is transferred to GRB by the input capture signal
0	Input capture/compare match flag A (IMFA)	0	Clear conditions: 0 is written in IMFA after reading IMFA = 1 (Initial value)
		1	Set conditions: (1) When GRA is functioning as the output compare register, and TCNT = GRA; (2) When GRA is functioning as the input capture register, and the TCNT value is transferred to GRA by the input capture signal

A.2.18 Timer Counter 0–4 (TCNT0–TCNT4) ITU

Start Address: H'5FFFF08 (channel 0), H'5FFFF12 (channel 1), H'5FFFF1C (channel 2), H'5FFFF26 (channel 3), H'5FFFF36 (channel 4)

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.19 TCNT0–TCNT4 Bit Functions

Bit	Bit name	Description
15–0	(Count value)	Count input clocks

A.2.19 General Registers A0–4 (GRA0–GRA4) ITU

Start Address: H'5FFFF0A (channel 0), H'5FFFF14 (channel 1), H'5FFFF1E (channel 2), H'5FFFF28 (channel 3), H'5FFFF38 (channel 4)

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.20 GRA0–GRA4 Bit Functions

Bit	Bit name	Description
15–0	Registers used for both output compare and input capture	Output compare register: Set with compare match output Input capture register: Stores the TCNT value when the input capture signal is generated

A.2.20 General Registers B0–4 (GRB0–GRB4) ITU

Start Address: H'5FFFF0C (channel 0), H'5FFFF16 (channel 1), H'5FFFF20 (channel 2), H'5FFFF2A (channel 3), H'5FFFF3A (channel 4)

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.21 GRB0–GRB4 Bit Functions

Bit	Bit name	Description
15–0	Registers used for both output compare and input capture	Output compare register: Set with compare match output Input capture register: Stores the TCNT value when the input capture signal is generated

A.2.21 Buffer Registers A3, 4 (BRA3, BRA4) ITU

Start Address: H'5FFFF2C (channel 3), H'5FFFF3C (channel 4)

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.22 BRA3, BRA4 Bit Functions

Bit	Bit name	Description
15–0	Buffer registers used for output compare/input capture	Output compare register: Transfers to GRA the value stored up to compare match generation Input capture register: Stores the value stored in GRA up to input capture signal generation

A.2.22 Buffer Registers B3, 4 (BRB3, BRB4) ITU

Start Address: H'5FFFF2E (channel 3), H'5FFFF3E (channel 4)

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.23 BRB3, BRB4 Bit Functions

Bit	Bit name	Description
15–0	Buffer registers used for output compare/input capture	Output compare register: Transfers to GRB the value stored up to compare match generation Input capture register: Stores the value stored in GRB up to input capture signal generation

A.2.23 Timer Output Control Register (TOCR) ITU

Start Address: H'5FFFF31

Bus Width: 8

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	OLS4	OLS3
Initial value	*	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	R/W	R/W

Note: * Undetermined

Table A.24 TOCR Bit Functions

Bit	Bit name	Value	Description
1	Output level select 4 (OLS4)	0	Reverse output of TIOCA3, TIOCA4, TIOCB4
		1	Direct output of TIOCA3, TIOCA4, TIOCB4 (Initial value)
0	Output level select 3 (OLS3)	0	Reverse output of TIOCB3, TOCXA4, TOCXB4
		1	Direct output of TIOCB3, TOCXA4, TOCXB4 (Initial value)

A.2.24 DMA Source Address Registers 0–3 (SAR0–SAR3) DMAC

Start Address: H'5FFFF40 (channel 0), H'5FFFF50 (channel 1), H'5FFFF60 (channel 2), H'5FFFF70 (channel 3)

Bus Width: 16/32

Bit	31	30	29	28	27	26	25	24
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Undetermined

Table A.25 SAR0–SAR3 Bit Functions

Bit	Bit name	Description
31–0	(Specifies transfer source address)	Specifies the address of the DMA transfer source

A.2.25 DMA Destination Address Registers 0–3 (DAR0–DAR3) DMAC

Start Address: H'5FFFF44 (channel 0), H'5FFFF54 (channel 1), H'5FFFF64 (channel 2), H'5FFFF74 (channel 3)

Bus Width: 16/32

Bit	31	30	29	28	27	26	25	24
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Undetermined

Table A.26 DAR0–DAR3 Bit Functions

Bit	Bit name	Description
31–0	(Specifies transfer destination address)	Specifies the address of the DMA transfer destination

A.2.26 DMA Transfer Count Registers 0–3 (TCR0–TCR3) DMAC

Start Address: H'5FFFF4A (channel 0), H'5FFFF5A (channel 1), H'5FFFF6A (channel 2), H'5FFFF7A (channel 3)

Bus Width: 16/32

Bit	15	14	13	12	11	10	9	8
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Undetermined

Table A.27 TCR0–TCR3 Bit Functions

Bit	Bit name	Description
15–0	(Specifies number of DMA transfers)	Specifies the number of DMA transfers (bytes or words). During DMA transfer, indicates the number of transfers remaining.

A.2.27 DMA Channel Control Registers 0–3 (CHCR0–CHCR3) DMAC

Start Address: H'5FFFF4E (channel 0), H'5FFFF5E (channel 1), H'5FFFF6E (channel 2), H'5FFFF7E (channel 3)

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	AM	AL	DS	TM	TS	IE	TE	DE
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*2	R/W*2	R/W*2	R/W	R/W	R/W	R/(W)*1	R/W

Notes: 1. Only 0 can be written, to clear the flag.
2. Writing is valid only for CHCR0 and CHCR1.

Table A.28 CHCR0–CHCR3 Bit Functions

Bit	Bit name	Value	Description
15,14	Destination address mode bits 1, 0 (DM1, DM0)	0 0	Destination address is fixed (Initial value)
		0 1	Destination address incremented (+1 for byte transfer; +2 for word transfer)
		1 0	Destination address decremented (–1 for byte transfer; –2 for word transfer)
		1 1	Reserved (cannot be set)
13,12	Source address mode bits 1, 0 (SM1, SM0)	0 0	Source address is fixed (Initial value)
		0 1	Source address incremented (+1 for byte transfer; +2 for word transfer)
		1 0	Source address decremented (–1 for byte transfer; –2 for word transfer)
		1 1	Reserved (cannot be set)
11–8	Resource select bits 3–0 (RS3–RS0)	0 0 0 0	$\overline{\text{DREQ}}$ (external request[*1]) (Initial value) (Dual address mode)
		0 0 0 1	Reserved (cannot be set)
		0 0 1 0	$\overline{\text{DREQ}}$ (external request[*1]) (Single address mode[*2])
		0 0 1 1	$\overline{\text{DREQ}}$ (external request[*1]) (Single address mode[*3])
		0 1 0 0	RXIO (transfer request by receive-data-full interrupt of on-chip SCI0)[*4]
		0 1 0 1	TXIO (transfer request by transmit-data-empty interrupt of on-chip SCI0)[*4]
		0 1 1 0	RXI1 (transfer request by receive-data-full interrupt of on-chip SCI1)[*4]
		0 1 1 1	TXI1 (transfer request by transmit-data-empty interrupt of on-chip SCI1)[*4]
		1 0 0 0	IMIA0 (input capture A/compare match A interrupt request of on-chip ITU0)[*4]
		1 0 0 1	IMIA1 (input capture A/compare match A interrupt request of on-chip ITU1)[*4]
		1 0 1 0	IMIA2 (input capture A/compare match A interrupt request of on-chip ITU2)[*4]

Bit	Bit name	Value	Description
11–8	Resource select bits 3–0 (RS3–RS0) (cont)	1 0 1 1	IMIA3 (input capture A/compare match A interrupt request of on-chip ITU3)*4
		1 1 0 0	Auto request (transfer request automatically generated within DMAC)*4
		1 1 0 1	ADI (A/D conversion end interrupt request of on-chip A/D converter)
		1 1 1 0	Reserved (cannot be set)
		1 1 1 1	Reserved (cannot be set)
7	Acknowledge mode bit (AM)*1	0	DACK output in read cycle (Initial value)
		1	DACK output in write cycle
6	Acknowledge level bit (AL)*1	0	DACK is active-high signal (Initial value)
		1	DACK is active-low signal
5	$\overline{\text{DREQ}}$ select bit (DS)*1	0	$\overline{\text{DREQ}}$ detected at low (Initial value)
		1	$\overline{\text{DREQ}}$ detected on falling edge
4	Transfer bus mode bit (TM)	0	Cycle-steal mode (Initial value)
		1	Burst mode
3	Transfer size bit (TS)	0	Byte (8 bits) (Initial value)
		1	Word (16 bits)
2	Interrupt enable bit (IE)	0	Interrupt request disabled (Initial value)
		1	Interrupt request enabled
1	Transfer end flag bit (TE)	0	DMA transferring or DMA transfer halted (Initial value) Clear Conditions: TE bit read and then 0 written in TE
		1	DMA transfer ends normally
0	DMA enable bit (DE)	0	DMA transfer disabled (Initial value)
		1	DMA transfer enabled

Notes: 1. Only valid in channels 0 and 1.
2. Transfer to external device from memory mapped external device or external memory with DACK.
3. Transfer from external device to memory mapped external device or external memory with DACK.
4. Dual address mode.

A.2.28 DMA Operation Registers (DMAOR) DMAC

Start Address: H'5FFFF48

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	PR1	PR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	AE	NMIF	DME
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	R/(W)*	R/(W)*	R/W

Note: * Only 0 can be written, to clear the flag.

Table A.29 DMAOR Bit Functions

Bit	Bit name	Value	Description
9,8	Priority mode bits 1, 0 (PR1,PR0)	0 0	Priority order is fixed (Initial value) (Channel 0 > channel 3 > channel 2 > channel 1)
		0 1	Priority order is fixed (Channel 1 > channel 3 > channel 2 > channel 0)
		1 0	Round-robin priority order (Immediately after reset: Channel 0 > channel 3 > channel 2 > channel 1)
		1 1	External-pin-alternating mode priority order (Immediately after reset: Channel 3 > channel 2 > channel 1 > channel 0)
2	Address error flag bit (AE)	0	No errors caused by DMAC (Initial value) Clear Condition: Write 0 in AE after reading AE
		1	Address error caused by DMAC
1	NMI flag bit (NMIF)	0	No NMI interrupt (Initial value) Clear Condition: Write 0 in NMIF after reading NMIF
		1	NMI interrupt generated
0	DMA master enable bit (DME)	0	DMA transfer disabled for all channels (Initial value)
		1	DMA transfer enabled for all channels

A.2.29 Interrupt Priority Setting Register A (IPRA) INTC

Start Address: H'5FFFF84

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.30 IPRA Bit Functions

Bit	Bit name	Description
15–12	(Set IRQ0 priority level)	Sets the IRQ0 priority level value
11–8	(Set IRQ1 priority level)	Sets the IRQ1 priority level value
7–4	(Set IRQ2 priority level)	Sets the IRQ2 priority level value
3–0	(Set IRQ3 priority level)	Sets the IRQ3 priority level value

A.2.30 Interrupt Priority Setting Register B (IPRB) INTC

Start Address: H'5FFFF86

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.31 IPRB Bit Functions

Bit	Bit name	Description
15–12	(Set IRQ4 priority level)	Sets the IRQ4 priority level value
11–8	(Set IRQ5 priority level)	Sets the IRQ5 priority level value
7–4	(Set IRQ6 priority level)	Sets the IRQ6 priority level value
3–0	(Set IRQ7 priority level)	Sets the IRQ7 priority level value

A.2.31 Interrupt Priority Setting Register C (IPRC) INTC

Start Address: H'5FFFF88

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.32 IPRC Bit Functions

Bit	Bit name	Description
15–12	(Set DMAC0 and DMAC1 priority levels)	Sets the DMAC0 and DMAC1 priority level values
11–8	(Set DMAC2 and DMAC3 priority levels)	Sets the DMAC2 and DMAC3 priority level values
7–4	(Set ITU0 priority level)	Sets the ITU0 priority level value
3–0	(Set ITU1 priority level)	Sets the ITU1 priority level value

A.2.32 Interrupt Priority Setting Register D (IPRD) INTC

Start Address: H'5FFFF8A

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.33 IPRD Bit Functions

Bit	Bit name	Description
15–12	(Set ITU2 priority level)	Sets the ITU2 priority level value
11–8	(Set ITU3 priority level)	Sets the ITU3 priority level value
7–4	(Set ITU4 priority level)	Sets the ITU4 priority level value
3–0	(Set SCI0 priority level)	Sets the SCI0 priority level value

A.2.33 Interrupt Priority Setting Register E (IPRE) INTC

Start Address: H'5FFFF8C

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
					—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Table A.34 IPRE Bit Functions

Bit	Bit name	Description
15–12	(Set SCI1 priority level)	Sets the SC1 priority level value
11–8	(Set PRT*1 and A/D priority levels)	Sets the PRT*1 and A/D priority level values
7–4	(Set WDT and REF*2 priority levels)	Sets the WDT and REF*2 priority level value

Notes 1. PRT: Parity control section within the bus state controller. See section 8, Bus State Controller (BSC), for more information.

2. REF: DRAM refresh control section within the bus state controller. See section 8, Bus State Controller (BSC), for more information.

A.2.34 Interrupt Control Register (ICR) INTC

Start Address: H'5FFFF8E

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	NMIL	—	—	—	—	—	—	NMIE
Initial value	*	0	0	0	0	0	0	0
Read/Write	R	—	—	—	—	—	—	R/W

Bit	7	6	5	4	3	2	1	0
	IRQ0S	IRQ1S	IRQ2S	IRQ3S	IRQ4S	IRQ5S	IRQ6S	IRQ7S
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * NMI pin input high: 1
NMI pin input low: 0

Table A.35 ICR Bit Functions

Bit	Bit Name	Value	Description
15	NMI input level (NMIL)	0	Low input to NMI pin
		1	High input to NMI pin
8	NMI edge select (NMIE)	0	Interrupt request sensed at falling edge of NMI input (Initial value)
		1	Interrupt request sensed at rising edge of NMI input
7–0	IRQ0–7 sense select (IRQ0–IRQ7)	0	Interrupt request sensed at $\overline{\text{IRQ}}$ input low level (Initial value)
		1	Interrupt request sensed at $\overline{\text{IRQ}}$ input falling edge

A.2.35 Break Address Register H (BARH) UBC

Start Address: H'5FFFF90

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.36 BARH Bit Functions

Bit	Bit name	Description
15–0	Set break address bits 31–16 (BA31–BA16)	Specifies the upper end (bits 31–16) of the address which is the break condition

A.2.36 Break Address Register L (BARL) UBC

Start Address: H'5FFFF92

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.37 BARL Bit Functions

Bit	Bit name	Description
15–0	Set break address bits 15–0 (BA15–BA0)	Specifies the lower end (bits 15–0) of the address which is the break condition

A.2.37 Break Address Mask Register H (BAMRH) UBC

Start Address: H'5FFFF94

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	BAM31	BAM30	BAM29	BAM28	BAM27	BAM26	BAM25	BAM24
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BAM23	BAM22	BAM21	BAM20	BAM19	BAM18	BAM17	BAM16
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.38 BAMRH Bit Functions

Bit	Bit name	Description
15–0	Break address masks 31–16 (BAM31–BAM16)	Specifies the bits to be masked in the break address specified in BARH

A.2.38 Break Address Mask Register L (BAMRL) UBC

Start Address: H'5FFFF96

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	BAM15	BAM14	BAM13	BAM12	BAM11	BAM10	BAM9	BAM8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BAM7	BAM6	BAM5	BAM4	BAM3	BAM2	BAM1	BAM0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.39 BAMRL Bit Functions

Bit	Bit name	Description
15–0	Break address masks 15–0 (BAM15–BAM0)	Specifies the bits to be masked in the break address specified in BARL

A.2.39 Break Bus Cycle Register (BBR) UBC

Start Address: H'5FFFF98

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
	CD1	CD0	ID1	ID0	RW1	RW0	SZ1	SZ0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.40 BBR Bit Functions

Bit	Bit name	Value		Description
7,6	CPU cycle/DMA cycle select (CD1, CD0)	0	0	User break interrupt not generated (Initial value)
		0	1	CPU cycle is break condition
		1	0	DMA cycle is break condition
		1	1	CPU cycle and DMA cycle are both break conditions
5,4	Instruction fetch/data access select (ID1, ID0)	0	0	User break interrupt not generated (Initial value)
		0	1	Instruction fetch cycle is break condition
		1	0	Data access cycle is break condition
		1	1	Instruction fetch cycle and data access cycle are both break conditions
3,2	Read/write select (RW1, RW0)	0	0	User break interrupt not generated (Initial value)
		0	1	Read cycle is break condition
		1	0	Write cycle is break condition
		1	1	Read cycle and write cycle are both break conditions
1,0	Operand size select (SZ1, SZ0)	0	0	Operand size not included in the break conditions (Initial value)
		0	1	Byte access is break condition
		1	0	Word access is break condition
		1	1	Longword access is break condition

A.2.40 Bus Control Register (BCR) BSC

Start Address: H'5FFFFA0

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	DRAME	IOE	WARP	RDDTY	BAS	—	—	—
Initial value:	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	—	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Table A.41 BCR Bit Functions

Bit	Bit Name	Value	Description
15	DRAM enable (DRAME)	0	Area 1 is external memory space (Initial value)
		1	Area 1 is DRAM space
14	Multiplex I/O enable (IOE)	0	Area 6 is external memory space (Initial value)
		1	Area 6 is address/data multiplex I/O space
13	Warp mode (WARP)	0	Normal mode: External access and internal access not performed simultaneously (Initial value)
		1	Warp mode: External access and internal access performed simultaneously
12	RD duty (RDDTY)	0	$\overline{RD}$ signal high width duty ratio is 50% (Initial value)
		1	$\overline{RD}$ signal high width duty ratio is 35%
11	Byte access select (BAS)	0	$\overline{WRH}$, $\overline{WRL}$, and A0 signals valid (Initial value)
		1	$\overline{WR}$, $\overline{HBS}$, and $\overline{LBS}$ and signals valid

A.2.41 Wait State Control Register 1 (WCR1) BSC

Start Address: H'5FFFA2

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	RW7	RW6	RW5	RW4	RW3	RW2	RW1	RW0
Initial value:	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	WW1	—
Initial value:	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	R/W*	—

Note: * Only write 0 in the WW1 bit when area 1 is DRAM space. When it is external memory space, do not write 0.

Table A.42 WCR Bit Functions

				Number of read cycles				
				External Space		Internal Space		
Bit	Bit Name	Value	$\overline{\text{WAIT}}$ Pin Signal Input	External Memory Space	DRAM Space	Multi-plex I/O	On-Chip Modules	On-Chip ROM, RAM
15–8	Read wait state control (RW7–RW0)	0	Not sampled during read cycle	• Areas 1, 3–5, 7: fixed at 1 cycle • Areas 0, 2, 6: 1 cycle + long wait state	Column address cycle: Fixed at 1 cycle (short-pitch)	Wait state is 4 cycles plus $\overline{\text{WAIT}}$	Fixed at 3 cycles	Fixed at 1 cycle
		1	Sampled during read cycle (Initial value)	• Areas 1, 3–5, 7: wait state is 2 cycles plus $\overline{\text{WAIT}}$ • Areas 0, 2, 6: 1 cycle + long wait state, or wait state from $\overline{\text{WAIT}}$	Column address cycle: Wait state is 2 cycles plus $\overline{\text{WAIT}}$ (long-pitch)*			

			Description	
Bit	Bit Name	Value	DRAM Space (BCRDRAME = 1)	Area 1 External Memory Space (BCRDRAME = 1)
1	Write wait state control (WW1)	0	Column address cycle: 1 cycle (short-pitch)	Setting prohibited
		1	Column address cycle: Wait state is 2 cycles + $\overline{\text{WAIT}}$ (long-pitch) (Initial value)	Wait state is 2 cycles + $\overline{\text{WAIT}}$

Note: * During a CBR refresh, the $\overline{\text{WAIT}}$ signal is ignored and the wait state inserted using the RLW1 and RLW0 bits.

A.2.42 Wait State Control Register 2 (WCR2) BSC

Start Address: H'5FFFFA4

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	DRW7	DRW6	DRW5	DRW4	DRW3	DRW2	DRW1	DRW0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	DWW7	DWW6	DWW5	DWW4	DWW3	DWW2	DWW1	DWW0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.43 WCR2 Bit Functions

			Description			
				Number of Single Mode DMA External Space Cycle States		
Bit	Bit Name	Value	$\overline{\text{WAIT}}$ Pin Signal Input	External Memory Space	DRAM Space	Multiplex I/O
15–8	Single mode DMA memory read wait state control (DRW7–DRW0)	0	Not sampled during single mode DMA memory read cycle	• Areas 1, 3–5, 7: fixed at 1 cycle • Areas 0, 2, 6: 1 cycle + long wait state	Column address cycle: Fixed at 1 cycle (short-pitch)	Wait state is 4 cycles plus $\overline{\text{WAIT}}$
		1	Sampled during single mode DMA memory read cycle (Initial value)	• Areas 1, 3–5, 7: wait state is 2 cycles plus $\overline{\text{WAIT}}$ • Areas 0, 2, 6: 1 cycle + long wait state, or wait state from $\overline{\text{WAIT}}$	Column address cycle: Wait state is 2 cycles plus $\overline{\text{WAIT}}$ (long-pitch)	
7–0	Single mode DMA memory write wait state control (DWW7–DWW0)	0	Not sampled during single mode DMA memory write cycle	• Areas 1, 3–5, 7: fixed at 1 cycle • Areas 0, 2, 6: 1 cycle + long wait state	Column address cycle: Fixed at 1 cycle (short-pitch)	Wait state is 4 cycles plus $\overline{\text{WAIT}}$
		1	Sampled during single mode DMA memory write cycle (Initial value)	• Areas 1, 3–5, 7: wait state is 2 cycles plus $\overline{\text{WAIT}}$ • Areas 0, 2, 6: 1 cycle + long wait state, or wait state from $\overline{\text{WAIT}}$	Column address cycle: Wait state is 2 cycles plus $\overline{\text{WAIT}}$ (long-pitch)	

A.2.43 Wait State Control Register 3 (WCR3) BSC

Start Address: H'5FFFFA6

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	WPU	A02LW1	A02LW0	A6LW1	A6LW0	—	—	—
Initial value	1	1	1	1	1	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	—	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Table A.44 WCR3 Bit Functions

Bit	Bit Name	Value		Description	
15	Wait pin pull-up control (WPU)	0		$\overline{\text{WAIT}}$ pin not pulled up	
		1		$\overline{\text{WAIT}}$ pin pulled up	(Initial value)
14,13	Areas 0 and 2 long wait insert 1, 0 (A02LW1, A02LW0)	0	0	1-cycle long wait state inserted	
		0	1	2-cycle long wait state inserted	
		1	0	3-cycle long wait state inserted	
		1	1	4-cycle long wait state inserted	(Initial value)
12,11	Area 6 long wait insert 1, 0 (A6LW1, A6LW0)	0	0	1-cycle long wait state inserted	
		0	1	2-cycle long wait state inserted	
		1	0	3-cycle long wait state inserted	
		1	1	4-cycle long wait state inserted	(Initial value)

A.2.44 DRAM Area Control Register (DCR) BSC

Start Address: H'5FFFA8

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	CW2	RASD	TPC	BE	CDTY	MXE	MXC1	MXC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Table A.45 DCR Bit Functions

Bit	Bit Name	Value	Description
15	2-CAS system/2-WE system (CW2)	0	2-CAS system: $\overline{\text{CASH}}$, $\overline{\text{CASL}}$, and $\overline{\text{WRL}}$ signals are valid (Initial value)
		1	2-WE system: $\overline{\text{CASL}}$, $\overline{\text{WRH}}$, and $\overline{\text{WRL}}$ signals are valid
14	RAS down (RASD)	0	RAS up mode: Returns $\overline{\text{RAS}}$ signal to high and waits for next DRAM access (Initial value)
		1	RAS down mode: Leaves $\overline{\text{RAS}}$ signal low and waits for next DRAM access
13	Number of RAS pre-charge cycles (TPC)	0	1-cycle pre-charge cycle inserted (Initial value)
		1	2-cycle pre-charge cycle inserted
12	Burst operation enable (BE)	0	Normal mode: Full access (Initial value)
		1	High-speed page mode: Burst operation
11	CAS duty (CDTY)	0	$\overline{\text{CAS}}$ signal high width duty ratio is 50% (Initial value)
		1	$\overline{\text{CAS}}$ signal high width duty ratio is 35%
10	Multiplex enable (MXE)	0	Row address and column address not multiplexed (Initial value)
		1	Row address and column address multiplexed
9,8	Multiplex shift count 1,0 (MXC1, MXC0)		Row address shift (MXE = 1) / Row address for comparison during burst (MXE = 0 or 1)
		0 0	8 bits (Initial value) / A27–A8 (Initial value)
		0 1	9 bits / A27–A9
		1 0	10 bits / A27–A10
		1 1	Reserved / Reserved

A.2.45 Parity Control Register (PCR) BSC

Start Address: H'5FFFFAA

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	PEF	PFRC	PEO	PCHK1	PCHK0	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	—	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Table A.46 PCR Bit Functions

Bit	Bit Name	Value		Description	
15	Parity error flag (PEF)	0		No parity error	(Initial value)
				Clear Condition: PEF read, then 0 written in PEF	
		1		Parity error occurred	
14	Parity forced output (PFRC)	0		No forced parity output	(Initial value)
		1		Forced high-level output	
13	Parity polarity (PEO)	0		Even parity	(Initial value)
		1		Odd parity	
12,11	Parity check enable 1, 0 (PCHK1, PCHK0)	0	0	Parity not checked or generated	(Initial value)
		0	1	Parity checked and generated in DRAM space	
		1	0	Parity checked and generated in DRAM space and area 2	
		1	1	Reserved	

A.2.46 Refresh Control Register (RCR) BSC

Start Address: H'5FFFFAC

Bus Width: 8/16/32 (read), 16 (write)

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
	RFSHE	RMODE	RLW1	RLW0	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Table A.47 RCR Bit Functions

Bit	Bit Name	Value		Description	
7	Refresh control (RFSHE)	0		No refresh control (RTCNT can be used as an interval timer)	(Initial value)
		1		Refresh control	
6	Refresh mode (RMODE)	0		CAS-before-RAS refresh performed	(Initial value)
		1		Self-refresh performed	
5,4	Wait state insertion CBR refresh 1,0 (RLW1, RLW0)	0	0	1-cycle wait state inserted	(Initial value)
		0	1	2-cycle wait state inserted	
		1	0	3-cycle wait state inserted	
		1	1	4-cycle wait state inserted	

A.2.47 Refresh Timer Control/Status Register (RTCSR) BSC

Start Address: H'5FFFAE

Bus Width: 8/16/32 (read), 16 (write)

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
	CMF	CMIE	CKS2	CKS1	CKS0	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	—	—	—

Table A.48 RSTCR Bit Functions

Bit	Bit Name	Value			Description	
7	Compare match flag (CMF)	0			RTCNT and RTCOR values do not match	(Initial value)
					Clear Condition: CMF read, then 0 written in CMF	
		1			RTCNT and RTCOR values match	
6	Compare match interrupt enable (CMIE)	0			Compare match interrupt (CMI) disabled	(Initial value)
		1			Compare match interrupt (CMI) enabled	
5–3	Clock select 2–0 (CKS2–CKS0)	0	0	0	Clock input disabled	(Initial value)
		0	0	1	ϕ/2	
		0	1	0	ϕ/8	
		0	1	1	ϕ/32	
		1	0	0	ϕ/128	
		1	0	1	ϕ/512	
		1	1	0	ϕ/2048	
		1	1	1	ϕ/4096	

A.2.48 Refresh Timer Counter (RTCNT) BSC

Start Address: H'5FFFFB0

Bus Width: 8/16/32 (read), 16 (write)

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.49 RTCNT Bit Functions

Bit	Bit Name	Description
7–0	(Count value)	Input clock count value

A.2.49 Refresh Timer Constant Register (RTCOR) BSC

Start Address: H'5FFFFB2

Bus Width: 8/16/32 (read), 16 (write)

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.50 RTCOR Bit Functions

Bit	Bit Name	Description
7–0	(Compare match cycle)	Set with compare match cycle

A.2.50 Timer Control/Status Register (TCSR) WDT

Start Address: H'5FFFFB8

Bus Width: 8 (read), 16 (write)

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/(W)*	R/W	R/W	—	—	R/W	R/W	R/W

Note: * Only 0 can be written, to clear the flag.

Table A.51 TCSR Bit Functions

Bit	Bit Name	Value	Description	
7	Overflow flag (OVF)	0	No TCNT overflow in interval timer mode (Initial value)	
			Clear Condition: OVF read, then 0 written in OVF	
		1	TCNT overflow generated in interval timer mode	
6	Timer mode select (WT/$\overline{IT}$)	0	Interval timer mode: When TCNT overflows, interval timer interrupt (ITI) request sent to CPU (Initial value)	
		1	Watchdog timer mode: When TCNT overflows, $\overline{WDTOVF}$ signal is output externally*	
5	Timer enable (TME)	0	Timer disable: TCNT initialized at H'00 and count-up halted (Initial value)	
		1	Timer enable: TCNT starts counting up. When TCNT overflows, a $\overline{WDTOVF}$ signal or interrupt is generated	
2–0	Clock select 2–0 (CKS2–CKS0)		Clock	Overflow cycle (ϕ=20 MHz)
		0 0 0	ϕ/2 (Initial value)	25.6 µs
		0 0 1	ϕ/64	819.2 µs
		0 1 0	ϕ/128	1.6 ms
		0 1 1	ϕ/256	3.3 ms
		0 0 0	ϕ/512	6.6 ms
		0 0 1	ϕ/1024	13.1 ms
		0 1 0	ϕ/4096	52.4 ms
		0 1 1	ϕ/8192	104.9 ms

Note: * When the RSTE bit in RSTCSR is 1, an internal reset signal is also generated simultaneously with the $\overline{WDTOVF}$ signal when TCNT overflows in watchdog timer mode.

A.2.51 Timer Counter (TCNT) WDT

Start Address: H'5FFFFB9 (read), H'5FFFFB8 (write)

Bus Width: 8 (read), 16 (write)

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.52 TCNT Bit Functions

Bit	Bit Name	Description
7–0	Count value	Input clock count value

A.2.52 Reset Control/Status Register (RSTCSR) WDT

Start Address: H'5FFFFBB (read), H'5FFFFBA (write)

Bus Width: 8 (read), 16 (write)

Bit	7	6	5	4	3	2	1	0
	WOVF	RSTE	RSTS	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/(W)*	R/W	R/W	—	—	—	—	—

Note: * Only 0 can be written, to clear the flag.

Table A.53 RSTCSR Bit Functions

Bit	Bit Name	Value	Description
7	Watchdog timer overflow flag (WOVF)	0	No TCNT overflow in watchdog timer mode (Initial value) Clear Condition: WOVF read, then 0 written in WOVF
		1	TCNT overflow generated in watchdog timer mode
6	Reset enable (RSTE)	0	No internal reset when TCNT overflows* (Initial value)
		1	Internal reset when TCNT overflows
5	Reset select (RSTS)	0	Power-on reset (Initial value)
		1	Manual reset

Note: * The microprocessor is not reset internally, but TCNT and TCSR within the WDT are reset.

A.2.53 Standby Control Register (SBYCR) Power-Down State

Start Address: H'5FFFFBC

Bus Width: 8/16/32

Bit	7	6	5	4	3	2	1	0
	SBY	HIZ	—	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/W	R/W	—	—	—	—	—	—

Table A.54 SBYCR Bit Functions

Bit	Bit Name	Value	Description
7	Standby (SBY)	0	Shift to sleep mode on execution of SLEEP instruction (Initial value)
		1	Shift to standby mode on execution of SLEEP instruction
6	Port high impedance (HIZ)	0	Pin states held in standby mode (Initial value)
		1	Pins change to high impedance in standby mode

A.2.54 Port A Data Register (PADR) Port A

Start Address: H'5FFFFC0

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	PA15DR	PA14DR	PA13DR	PA12DR	PA11DR	PA10DR	PA9DR	PA8DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.55 PADR Bit Functions

PAIOR	Pin Function	Read	Write
0	General input	Pin status	Can write to PADR, but this does not affect pin status
	All other	Pin status	Can write to PADR, but this does not affect pin status
1	General input	PADR value	Value written is output from pin
	All other	PADR value	Can write to PADR, but this does not affect pin status

A.2.55 Port B Data Register (PBDR) Port B

Start Address: H'5FFFFC2

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	PB15DR	PB14DR	PB13DR	PB12DR	PB11DR	PB10DR	PB9DR	PB8DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.56 Bit Functions

PBIOR	Pin Function	Read	Write
0	General input	Pin status	Can write to PBDR, but this does not affect pin status
	TPn	Pin status	Cannot write
	All other	Pin status	Can write to PBDR, but this does not affect pin status
1	General input	PBDR value	Value written is output from pin
	TPn	PBDR value	Cannot write
	All other	PBDR value	Can write to PBDR, but this does not affect pin status

A.2.56 Port C Data Register (PCDR) Port C

Start Address: H'5FFFFD0

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

Table A.57 PCDR Bit Functions

Pin I/O	Pin Function	Read	Write
Input	General input	Pin status	Ignored (no affect on pin status)
	ANn	1	Ignored (no affect on pin status)

A.2.57 Port A I/O Register (PAIOR) PFC

Start Address: H'5FFFFC4

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	PA15 IOR	PA14 IOR	PA13 IOR	PA12 IOR	PA11 IOR	PA10 IOR	PA9 IOR	PA8 IOR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PA7 IOR	PA6 IOR	PA5 IOR	PA4 IOR	PA3 IOR	PA2 IOR	PA1 IOR	PA0 IOR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.58 PAIOR Bit Functions

Bit	Bit Name	Value	Description
15–0	Port A I/O (PA15IOR–PA0IOR)	0	Input (Initial value)
		1	Output

A.2.58 Port B I/O Register (PBIOR) PFC

Start Address: H'5FFFFC6

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	PB15 IOR	PB14 IOR	PB13 IOR	PB12 IOR	PB11 IOR	PB10 IOR	PB9 IOR	PB8 IOR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB7 IOR	PB6 IOR	PB5 IOR	PB4 IOR	PB3 IOR	PB2 IOR	PB1 IOR	PB0 IOR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.59 PBIOR Bit Functions

Bit	Bit Name	Value	Description
15–0	Port B I/O (PB15IOR–PB0IOR)	0	Input (Initial value)
		1	Output

A.2.59 Port A Control Register 1 (PACR1) PFC

Start Address: H'5FFFFC8

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	PA15 MD1	PA15 MD0	PA14 MD1	PA14 MD0	PA13 MD1	PA13 MD0	PA12 MD1	PA12 MD0
Initial value	0	0	1	1	0	0	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PA11 MD1	PA11 MD0	PA10 MD1	PA10 MD0	PA9 MD1	PA9 MD0	—	PA8 MD
Initial value	0	0	0	0	0	0	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	—	R/W

Table A.60 PACR1 Bit Functions

Bit	Bit Name	Value		Description
15,14	PA15 mode bits 1,0 (PA15MD1, PA15MD0)	0	0	General-purpose input/output (PA15) (Initial value)
		0	1	Interrupt request input ($\overline{\text{IRQ3}}$)
		1	0	Reserved
		1	1	DMA transfer request input ($\overline{\text{DREQ1}}$)
13,12	PA14 mode bits 1,0 (PA14MD1, PA14MD0)	0	0	General-purpose input/output (PA14)
		0	1	Interrupt request input ($\overline{\text{IRQ2}}$)
		1	0	Reserved
		1	1	DMA transfer request acknowledge output ($\overline{\text{DACK1}}$) (Initial value)
11,10	PA13 mode bits 1,0 (PA13MD1, PA13MD0)	0	0	General-purpose input/output (PA13) (Initial value)
		0	1	Interrupt request input (IRQ1)
		1	0	ITU timer clock input (TCLKB)
		1	1	DMA transfer request input (DREQ0)
9,8	PA12 mode bits 1,0 (PA12MD1, PA12MD0)	0	0	General-purpose input/output (PA12)
		0	1	Interrupt request input (IRQ0)
		1	0	ITU timer clock input (TCKLA)
		1	1	DMA transfer request acknowledge output (DACK0) (Initial value)
7,6	PA11 mode bits 1,0 (PA11MD1, PA11MD0)	0	0	General-purpose input/output (PA11) (Initial value)
		0	1	High data bus parity input/output (DPH)
		1	0	ITU input capture input/output compare output (TIOCB1)
		1	1	Reserved
5,4	PA10 mode bits 1,0 (PA10MD1, PA10MD0)	0	0	General-purpose input/output (PA10) (Initial value)
		0	1	Low data bus parity input/output (DPL)
		1	0	ITU input capture input/output compare output (TIOCA1)
		1	1	Reserved
3,2	PA9 mode bits 1,0 (PA9MD1, PA9MD0)	0	0	General-purpose input/output (PA9) (Initial value)
		0	1	Address hold output ($\overline{\text{AH}}$)
		1	0	A/D conversion trigger input ($\overline{\text{ADTRG}}$)
		1	1	Interrupt request output ($\overline{\text{IRQOUT}}$)
0	PA8 mode bit (PA8MD)	0		General-purpose input/output (PA8) (Initial value)
		1		Bus request input ($\overline{\text{BREQ}}$)

A.2.60 Port A Control Register 2 (PACR2) PFC

Start Address: H'5FFFFCA

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	—	PA7MD	—	PA6MD	—	PA5MD	—	PA4MD
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	R/W	—	R/W	—	R/W	—	R/W

Bit	7	6	5	4	3	2	1	0
	PA3MD1	PA3MD0	PA2MD1	PA2MD0	PA1MD1	PA1MD0	PA0MD1	PA0MD0
Initial value	1	0	0	1	0	1	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.61 PACR2 Bit Functions

Bit	Bit Name	Value		Description
14	PA7 mode bit (PA7MD)	0		General-purpose input/output (PA7)
		1		Bus request acknowledge output ($\overline{\text{BACK}}$) (Initial value)
12	PA6 mode bit (PA6MD)	0		General-purpose input/output (PA6)
		1		Read output ($\overline{\text{RD}}$) (Initial value)
10	PA5 mode bit (PA5MD)	0		General-purpose input/output (PA5)
		1		High write output ($\overline{\text{WRH}}$) or low byte strobe output ($\overline{\text{LBS}}$) (Initial value)
8	PA4 mode bit (PA4MD)	0		General-purpose input/output (PA4)
		1		Low write output ($\overline{\text{WRL}}$) or write output ($\overline{\text{WR}}$)(Initial value)
7,6	PA3 mode bits 1,0 (PA3MD1, PA3MD0)	0	0	General-purpose input/output (PA3)
		0	1	Chip select output ($\overline{\text{CS7}}$)
		1	0	Wait state input ($\overline{\text{WAIT}}$) (Initial value)
		1	1	Reserved
5,4	PA2 mode bits 1,0 (PA2MD1, PA2MD0)	0	0	General-purpose input/output (PA2)
		0	1	Chip select output ($\overline{\text{CS6}}$) (Initial value)
		1	0	ITU input capture input/output compare output (TIOCB0)
		1	1	Reserved
3,2	PA1 mode bits 1,0 (PA1MD1, PA1MD0)	0	0	General-purpose input/output (PA1)
		0	1	Chip select output ($\overline{\text{CS5}}$) (Initial value)
		1	0	Row address strobe output ($\overline{\text{RAS}}$)
		1	1	Reserved
1,0	PA0 mode bits 1,0 (PA0MD1, PA0MD0)	0	0	General-purpose input/output (PA0)
		0	1	Chip select output ($\overline{\text{CS4}}$) (Initial value)
		1	0	ITU input capture input/output compare output (TIOCA0)
		1	1	Reserved

A.2.61 Port B Control Register 1 (PBCR1) PFC

Start Address: H'5FFFFCC

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	PB15 MD1	PB15 MD0	PB14 MD1	PB14 MD0	PB13 MD1	PB13 MD0	PB12 MD1	PB12 MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB11 MD1	PB11 MD0	PB10 MD1	PB10 MD0	PB9 MD1	PB9 MD0	PB8 MD1	PB8 MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.62 PBCR1 Bit Functions

Bit	Bit Name	Value		Description	
15,14	PB15 mode bits 1,0 (PB15MD1, PB15MD0)	0	0	General-purpose input/output (PB15)	(Initial value)
		0	1	Interrupt request input ($\overline{\text{IRQ7}}$)	
		1	0	Reserved	
		1	1	Timing pattern output (TP15)	
13,12	PB14 mode bits 1,0 (PB14MD1, PB14MD0)	0	0	General-purpose input/output (PB14)	(Initial value)
		0	1	Interrupt request input ($\overline{\text{IRQ6}}$)	
		1	0	Reserved	
		1	1	Timing pattern output (TP14)	
11,10	PB13 mode bits 1,0 (PB13MD1, PB13MD0)	0	0	General-purpose input/output (PB13)	(Initial value)
		0	1	Interrupt request input ($\overline{\text{IRQ5}}$)	
		1	0	Serial clock input/output (SCK1)	
		1	1	Timing pattern output (TP13)	
9,8	PB12 mode bits 1,0 (PB12MD1, PB12MD0)	0	0	General-purpose input/output (PB12)	(Initial value)
		0	1	Interrupt request input ($\overline{\text{IRQ4}}$)	
		1	0	Serial clock input/output (SCK0)	
		1	1	Timing pattern output (TP12)	
7,6	PB11 mode bits 1,0 (PB11MD1, PB11MD0)	0	0	General-purpose input/output (PB11)	(Initial value)
		0	1	Reserved	
		1	0	Transmit data input (TxD1)	
		1	1	Timing pattern output (TP11)	
5,4	PB10 mode bits 1,0 (PB10MD1, PB10MD0)	0	0	General-purpose input/output (PB10)	(Initial value)
		0	1	Reserved	
		1	0	Receive data input (RxD1)	
		1	1	Timing pattern output (TP10)	
3,2	PB9 mode bits 1,0 (PB9MD1, PB9MD0)	0	0	General-purpose input/output (PB9)	(Initial value)
		0	1	Reserved	
		1	0	Transmit data input (TxD0)	
		1	1	Timing pattern output (TP9)	
1,0	PB8 mode bits 1,0 (PB8MD1, PB8MD0)	0	0	General-purpose input/output (PB8)	(Initial value)
		0	1	Reserved	
		1	0	Receive data input (RxD0)	
		1	1	Timing pattern output (TP8)	

A.2.62 Port B Control Register 2 (PBCR2) PFC

Start Address: H'5FFFFCE

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	PB7MD1	PB7MD0	PB6MD1	PB6MD0	PB5MD1	PB5MD0	PB4MD1	PB4MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	PB3MD1	PB3MD0	PB2MD1	PB2MD0	PB1MD1	PB1MD0	PB0MD1	PB0MD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.63 PBCR2 Bit Functions

Bit	Bit Name	Value		Description	
15,14	PB7 mode bits 1,0 (PB7MD1, PB7MD0)	0	0	General-purpose input/output (PB7)	(Initial value)
		0	1	ITU timer clock input (TCLKD)	
		1	0	ITU output compare output (TOCXB4)	
		1	1	Timing pattern output (TP7)	
13,12	PB6 mode bits 1,0 (PB6MD1, PB6MD0)	0	0	General-purpose input/output (PB6)	(Initial value)
		0	1	ITU timer clock input (TCLKC)	
		1	0	ITU output compare output (TOCXA4)	
		1	1	Timing pattern output (TP6)	
11,10	PB5 mode bits 1,0 (PB5MD1, PB5MD0)	0	0	General-purpose input/output (PB5)	(Initial value)
		0	1	Reserved	
		1	0	ITU input capture input/output compare output (TIOCB4)	
		1	1	Timing pattern output (TP5)	
9,8	PB4 mode bits 1,0 (PB4MD1, PB4MD0)	0	0	General-purpose input/output (PB4)	(Initial value)
		0	1	Reserved	
		1	0	ITU input capture input/output compare output (TIOCA4)	
		1	1	Timing pattern output (TP4)	
7,6	PB3 mode bits 1,0 (PB3MD1, PB3MD0)	0	0	General-purpose input/output (PB3)	(Initial value)
		0	1	Reserved	
		1	0	ITU input capture input/output compare output (TIOCB3)	
		1	1	Timing pattern output (TP3)	
5,4	PB2 mode bits 1,0 (PB2MD1, PB2MD0)	0	0	General-purpose input/output (PB2)	(Initial value)
		0	1	Reserved	
		1	0	ITU input capture input/output compare output (TIOCA3)	
		1	1	Timing pattern output (TP2)	
3,2	PB1 mode bits 1,0 (PB1MD1, PB1MD0)	0	0	General-purpose input/output (PB1)	(Initial value)
		0	1	Reserved	
		1	0	ITU input capture input/output compare output (TIOCB2)	
		1	1	Timing pattern output (TP1)	
1,0	PB0 mode bits 1,0 (PB0MD1, PB0MD0)	0	0	General-purpose input/output (PB0)	(Initial value)
		0	1	Reserved	
		1	0	ITU input capture input/output compare output (TIOCA2)	
		1	1	Timing pattern output (TP0)	

A.2.63 Column Address Strobe Pin Control Register (CASCR) PFC

Start Address: H'5FFFFEE

Bus Width: 8/16/32

Bit	15	14	13	12	11	10	9	8
	CASH MD1	CASH MD0	CASL MD1	CASL MD0	—	—	—	—
Initial value	0	1	0	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

Table A.64 CASCR Bit Functions

Bit	Bit Name	Value		Description	
15,14	CASH mode bits 1,0 (CASHMD1, CASHMD0)	0	0	Reserved	
		0	1	Chip select output ($\overline{CS1}$)	(Initial value)
		1	0	Column address strobe output ($\overline{CASH}$)	
		1	1	Reserved	
13,12	CASL mode bits 1,0 (CASLMD1, CASLMD0)	0	0	Reserved	
		0	1	Chip select output ($\overline{CS3}$)	(Initial value)
		1	0	Column address strobe output ($\overline{CASL}$)	
		1	1	Reserved	

A.2.64 TPC Output Mode Register (TPMR) TPC

Start Address: H'5FFFF0

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	G3NOV	G2NOV	G1NOV	G0NOV
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Table A.65 TPMR Bit Functions

Bit	Bit Name	Value	Description
3	Group 3 non-overlap (G3NOV)	0	TPC output group 3 operates normally (the output value is updated at every compare match A of the selected ITU) (Initial value)
		1	TPC output group 3 operates in non-overlap mode (1 output and 0 output can be performed independently upon compare matches A and B of the selected ITU)
2	Group 2 non-overlap (G2NOV)	0	TPC output group 2 operates normally (the output value is updated at every compare match A of the selected ITU) (Initial value)
		1	TPC output group 2 operates in non-overlap mode (1 output and 0 output can be performed independently upon compare matches A and B of the selected ITU)
1	Group 1 non-overlap (G1NOV)	0	TPC output group 1 operates normally (the output value is updated at every compare match A of the selected ITU) (Initial value)
		1	TPC output group 1 operates in non-overlap mode (1 output and 0 output can be performed independently upon compare matches A and B of the selected ITU)
0	Group 0 non-overlap (G0NOV)	0	TPC output group 0 operates normally (the output value is updated at every compare match A of the selected ITU) (Initial value)
		1	TPC output group 0 operates in non-overlap mode (1 output and 0 output can be performed independently upon compare matches A and B of the selected ITU)

A.2.65 TPC Output Control Register (TPCR) TPC

Start Address: H'5FFFF1

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.66 TPCR Bit Functions

Bit	Bit Name	Value		Description
7,6	Group 3 compare match select 1, 0 (G3CMS1, G3CMS0)	0	0	The output trigger of TPC output group 3 (pins TP15–TP12) is the ITU channel 0 compare match
		0	1	The output trigger of TPC output group 3 (pins TP15–TP12) is the ITU channel 1 compare match
		1	0	The output trigger of TPC output group 3 (pins TP15–TP12) is the ITU channel 2 compare match
		1	1	The output trigger of TPC output group 3 (pins TP15–TP12) is the ITU channel 3 compare match*
5,4	Group 2 compare match select 1, 0 (G2CMS1, G2CMS0)	0	0	The output trigger of TPC output group 2 (pins TP11–TP8) is the ITU channel 0 compare match
		0	1	The output trigger of TPC output group 2 (pins TP11–TP8) is the ITU channel 1 compare match
		1	0	The output trigger of TPC output group 2 (pins TP11–TP8) is the ITU channel 2 compare match
		1	1	The output trigger of TPC output group 2 (pins TP11–TP8) is the ITU channel 3 compare match*
3,2	Group 1 compare match select 1, 0 (G1CMS1, G1CMS0)	0	0	The output trigger of TPC output group 1 (pins TP7–TP4) is the ITU channel 0 compare match
		0	1	The output trigger of TPC output group 1 (pins TP7–TP4) is the ITU channel 1 compare match
		1	0	The output trigger of TPC output group 1 (pins TP7–TP4) is the ITU channel 2 compare match
		1	1	The output trigger of TPC output group 1 (pins TP7–TP4) is the ITU channel 3 compare match*
1,0	Group 0 compare match select 1, 0 (G0CMS1, G0CMS0)	0	0	The output trigger of TPC output group 0 (pins TP3–TP0) is the ITU channel 0 compare match
		0	1	The output trigger of TPC output group 0 (pins TP3–TP0) is the ITU channel 1 compare match
		1	0	The output trigger of TPC output group 0 (pins TP3–TP0) is the ITU channel 2 compare match
		1	1	The output trigger of TPC output group 0 (pins TP3–TP0) is the ITU channel 3 compare match*

Note: * Initial value

A.2.66 Next Data Enable Register A (NDERA) TPC

Start Address: H'5FFFFF3

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.67 NDERA Bit Functions

Bit	Bit Name	Value	Description
7–0	Next data enable 7–0 (NDER7–NDER0)	0	Disable TPC output TP7–TP0 disabled (Initial value) (Transfer from NDR7–NDR0 to PB7–PB0 disabled)
		1	TPC output TP7–TP0 enabled (Transfer from NDR7–NDR0 to PB7–PB0 enabled)

A.2.67 Next Data Enable Register B (NDERB) TPC

Start Address: H'5FFFFF2

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.68 NDERB Bit Functions

Bit	Bit Name	Value	Description
7–0	Next data enable 7–0 (NDER15–NDER8)	0	TPC output TP15–TP8 disabled (Initial value) (Transfer from NDR15–NDR8 to PB15–PB8 disabled)
		1	TPC output TP15–TP8 enabled (Transfer from NDR15–NDR8 to PB15–PB8 enabled)

A.2.68 Next Data Register A (NDRA) TPC

(When the Output Triggers of TPC Output Groups 0 and 1 are the Same)

Start Address: H'5FFFF5

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.69 NDRA Bit Functions

Bit	Bit Name	Description
7–4	Next data 7–4 (NDR7–NDR4)	Stores the next output data for TPC output group 1
3–0	Next data 3–0 (NDR3–NDR0)	Stores the next output data for TPC output group 0

A.2.69 Next Data Register A (NDRA) TPC

(When the Output Triggers of TPC Output Groups 0 and 1 are the Same)

Start Address: H'5FFFF7

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

Table A.70 NDRA Bit Functions

Bit	Bit Name	Description
7–0	Reserved bits	Writing is invalid; always read as 1

A.2.70 Next Data Register A (NDRA) TPC

(When the Output Triggers of TPC Output Groups 0 and 1 are Different)

Start Address: H'5FFFFF5

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Table A.71 NDRA Bit Functions

Bit	Bit Name	Description
7–4	Next data 7–4 (NDR7–NDR4)	Stores the next output data for TPC output group 1

A.2.71 Next Data Register A (NDRA) TPC

(When the Output Triggers of TPC Output Groups 0 and 1 are Different)

Start Address: H'5FFFFF7

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	NDR3	NDR2	NDR1	NDR0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Table A.72 NDRA Bit Functions

Bit	Bit Name	Description
3–0	Next data 3–0 (NDR3–NDR0)	Stores the next output data for TPC output group 0

A.2.72 Next Data Register B (NDRB) TPC

(When the Output Triggers of TPC Output Groups 2 and 3 are the Same)

Start Address: H'5FFFF4

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table A.73 NDRB Bit Functions

Bit	Bit Name	Description
7–4	Next data 15–12 (NDR15–NDR12)	Stores the next output data for TPC output group 3
3–0	Next data 11–8 (NDR11–NDR8)	Stores the next output data for TPC output group 2

A.2.73 Next Data Register B (NDRB) TPC

(When the Output Triggers of TPC Output Groups 2 and 3 are the Same)

Start Address: H'5FFFF6

Bus Width: 8/16

Module: TPC

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

Table A.74 NDRB Bit Functions

Bit	Bit Name	Description
7–0	Reserved bits	Writing is invalid; always read as 1

A.2.74 Next Data Register B (NDRB) TPC

(When the Output Triggers of TPC Output Groups 2 and 3 are Different)

Start Address: H'5FFFFF4

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Table A.75 NDRB Bit Functions

Bit	Bit Name	Description
7–4	Next data 15–12 (NDR15–NDR12)	Stores the next output data for TPC output group 3

A.2.75 Next Data Register B (NDRB) TPC

(When the Output Triggers of TPC Output Groups 2 and 3 are Different)

Start Address: H'5FFFFF6

Bus Width: 8/16

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	NDR11	NDR10	NDR9	NDR8
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Table A.76 NDRB Bit Functions

Bit	Bit Name	Description
3–0	Next data 11–8 (NDR11–NDR8)	Stores the next output data for TPC output group 2

A.3 Register Status in Reset and Power-Down States

Table A.77 Register Status in Reset and Power-Down States

		Reset State		Power-Down State	
Category	**Abbreviation**	**Power On**	**Manual**	**Standby**	**Sleep**
CPU	R0–R15	Initialized	Initialized	Held	Held
	SR				
	GBR				
	VBR				
	MACH,MACL				
	PR				
	PC				
Interrupt controller (INTC)	IPRA–IPRE	Initialized	Initialized	Held	Held
	ICR				
User break controller (UBC)	BARH,BARL	Initialized	Initialized	Held	Held
	BAMRH,BAMRL				
	BBR				
Bus state controller (BSC)	BCR	Initialized	Held	Held	Held
	WCR1–WCR3				
	DCR				
	RCR				
	RTSCR				
	RTCNT				
	RTCOR				
	PCR				
Direct memory access controller (DMAC)	SAR0–SAR3	Initialized	Initialized	Initialized	Held
	DAR0–DAR3				
	TCR0–TCR3				
	CHCR0–CHCR3				
	DMAOR				

Category	Abbreviation	Reset State		Power-Down State	
		Power On	Manual	Standby	Sleep
16-bit integrated timer pulse unit (ITU)	TSTR	Initialized	Initialized	Initialized	Held
	TSNC				
	TMDA, TMDB				
	TCNT0–TCNT4				
	GRA0–GRA4, GRB0–GRB4				
	BRA3, BRA4. BRB3, BRB4				
	TCR0–TCR4				
	TIOR0–TIOR4				
	TIER0–TIER4				
	TSR0–TSR4				
Programmable timing pattern controller (TPC)	TPMR	Initialized	Initialized	Held	Held
	TPCR				
	NDERA,NDERB				
	NDRA, NDRB				
Watchdog timer (WDT)	TCNT	Initialized	Initialized	Held	Held
	TCSR			*1	
	RSTCR*2			Initialized	
Serial communication interface (SCI)	SMR	Initialized	Initialized	Initialized	Held
	BRR				
	SCR				
	TDR				
	TSR			Held	
	SSR			Initialized	
	RDR				
	RSR			Held	

		Reset State		Power-Down State	
Category	**Abbreviation**	**Power On**	**Manual**	**Standby**	**Sleep**
A/D converter	ADDRA–ADDRD	Initialized	Initialized	Initialized	Held
	ADCSR				
	ADCR				
Pin function controller (PFC)	PAIOR,PBIOR	Initialized	Held	Held	Held
	PACR1,PACR2, PBCR1,PBCR2				
	CASCR				
Parallel I/O ports (I/O)	PADR,PBDR	Initialized	Held	Held	Held
	PCDR	*3	*3	*3	*3
Power-down-state related	SBYCR	Initialized	Initialized	Held	Held

Notes: 1. Bits 7–5 (OVF, WT/IT, TME) are initialized, bits 2–0 (CKS2–CKS0) are held.
2. Not initialized in the case of a reset by the WDT.
3. Bits 15–8 are always undetermined, bits 7–0 always reflect the state of the corresponding pin.

Appendix B Pin States

Table B.1 Pin State In Resets, Power-Down State, and Bus-Released State

		Pin State				
		Reset		Power-Down		Bus
Category	**Pin**	**Power-On**	**Manual**	**Standby**	**Sleep**	**Released**
Clock	CK	O	O	H*[1]	O	O
System control	$\overline{\text{RES}}$	I	I	I	I	I
	$\overline{\text{WDTOVF}}$	H	H	H*[1]	O	O
	$\overline{\text{BREQ}}$	—	I	Z	I	I
	$\overline{\text{BACK}}$	Z	O	Z	O	L
Interrupt	NMI	I	I	I	I	I
	$\overline{\text{IRQ7}}$–$\overline{\text{IRQ0}}$	—	I	Z	I	I
	$\overline{\text{IRQOUT}}$	—	O	O*[1]	H	O
Address bus	A21–A0	H	O	Z	H	Z
Data bus	AD15–AD0	Z	Z	Z	Z	Z
	DPH,DPL	—	Z	Z	Z	Z
Bus control	$\overline{\text{WAIT}}$	I	I*[2]	Z	I*[2]	I*[2]
	$\overline{\text{CS7}}$	—	O	Z	H	Z
	$\overline{\text{CS6}}$–$\overline{\text{CS0}}$	Z	O	Z	H	Z
	$\overline{\text{RD}}$	H	O	Z	H	Z
	$\overline{\text{WRH}}$ ($\overline{\text{LBS}}$),$\overline{\text{WRL}}$ ($\overline{\text{WR}}$)	H	O	Z	H	Z
	$\overline{\text{RAS}}$	—	O	O*[1]	O	Z
	$\overline{\text{CASH}}$,$\overline{\text{CASL}}$	—	O	O	O	Z
	$\overline{\text{AH}}$	—	O	Z	H	Z
Direct memory access controller (DMAC)	$\overline{\text{DREQ0}}$,$\overline{\text{DREQ1}}$	—	I	Z	I	I
	DACK0,DACK1	Z	O	K*[1]	O	O
16-bit integrated timer pulse unit (ITU)	TIOCA0–TIOCA4	—	I	K*[1]	I/O	I/O
	TIOCB0–TIOCB4	—	I	K*[1]	I/O	I/O
	TOCXA4, TOCXB4	—	I	K*[1]	O	O
	TCLKA–TCLKD	—	I	Z	I	I
Timing pattern controller (TPC)	TP15–TP0	—	I	K*[1]	O	O

		Pin State				
		Reset		Power-Down		Bus
Category	Pin	Power-On	Manual	Standby	Sleep	Released
Serial communication interface (SCI)	TxD0–TxD1	—	Z	K*[1]	O	O
	RxD0,RxD1	—	I	Z	I	I
	SCK0,SCK1	—	I	Z	I/O	I/O
A/D converter	AN7–AN0	Z	Z	Z	I	I
	$\overline{\text{ADTRG}}$	—	I	Z	I	I
I/O ports	PA14, PA12, PA7–PA0	—	I/O	K*[1]	I/O	I/O
	PA15, PA13, PA11–PA8, PB15–PB0	Z	I/O	K*[1]	I/O	I/O
	PC7–PC0	Z	I	Z	I	I

—: One of the multiplexed pin functions is allocated, but the pin functions in the reset state are different.

I: Input

O: Output

H: High

L: Low

Z: High impedance

K: Input pins are high-impedance, output pins hold their state.

Notes: 1. When the port high impedance bit (HIZ) in the standby control register (SBYCR) is set to 1, the output pins become high-impedance.

2. When the pin pull-up control bit (WPU) in the wait state control register (WCR3) is set to 1, the $\overline{\text{WAIT}}$ pin is pulled up, but if set to 0, it is not pulled up.

The following table shows the states of bus control pins and external bus pins in accesses of various address spaces.

Table B.2 Pin States in Address Space Accesses

				On-Chip Peripheral Modules			
					16-Bit Space		
Pin Name		On-Chip ROM Space	On-Chip RAM Space	8-Bit Space	Upper Byte	Lower Byte	Word
$\overline{CS7}$–$\overline{CS0}$		High	High	High	High	High	High
$\overline{RAS}$		High	High	High	High	High	High
$\overline{CASH}$		High	High	High	High	High	High
$\overline{CASL}$		High	High	High	High	High	High
$\overline{AH}$		Low	Low	Low	Low	Low	Low
$\overline{RD}$	R	High	High	High	High	High	High
	W	—	High	High	High	High	High
$\overline{WRH}$/$\overline{LBS}$	R	High	High	High	High	High	High
	W	—	High	High	High	High	High
$\overline{WRL}$/$\overline{WR}$	R	High	High	High	High	High	High
	W	—	High	High	High	High	High
A0/$\overline{HBS}$		A0	A0	A0	A0	A0	A0
A21–A1		Address	Address	Address	Address	Address	Address
AD15–AD8		High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
AD7–AD0		High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
DPH		High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
DPL		High-Z	High-Z	High-Z	High-Z	High-Z	High-Z

R: Read
W: Write

		Address/Data Multiplex I/O Space						
			16-Bit Space					
			WRH, WRL, A0 System			WR, HBS, LBS System		
Pin Name		8-Bit Space	Upper Byte	Lower Byte	Word	Upper Byte	Lower Byte	Word
$\overline{CS7}$, $\overline{CS5}$–$\overline{CS0}$		High	High	High	High	High	High	High
$\overline{CS6}$		Low	Low	Low	Low	Low	Low	Low
$\overline{RAS}$		High	High	High	High	High	High	High
$\overline{CASH}$		High	High	High	High	High	High	High
$\overline{CASL}$		High	High	High	High	High	High	High
$\overline{AH}$		$\overline{AH}$	$\overline{AH}$	$\overline{AH}$	$\overline{AH}$	$\overline{AH}$	$\overline{AH}$	$\overline{AH}$
$\overline{RD}$	R	Low	Low	Low	Low	Low	Low	Low
	W	High	High	High	High	High	High	High
$\overline{WRH}$/$\overline{LBS}$	R	—*	High	High	High	High	Low	Low
	W	—*	Low	High	Low	High	Low	Low
$\overline{WRL}$/$\overline{WR}$	R	High	High	High	High	High	High	High
	W	Low	High	Low	Low	Low	Low	Low
A0/$\overline{HBS}$		A0	Low	High	Low	Low	High	Low
A21–A1		Address	Address	Address	Address	Address	Address	Address
AD15–AD8		High-Z	Address/ data	Address	Address/ data	Address/ data	Address	Address/ data
AD7–AD0		Address/ data	Address	Address/ data	Address/ data	Address	Address/ data	Address/ data

R: Read

W: Write

$\overline{AH}$: When addresses are output from AD15–AD0, an address hold signal is output.

Note: * Cannot be used; available only for 16-bit space access.

		DRAM Space						
			16-Bit Space					
			2-CAS System			2-WE System		
Pin Name		8-Bit Space	Upper Byte	Lower Byte	Word	Upper Byte	Lower Byte	Word
$\overline{CS7}$–$\overline{CS2}$, $\overline{CS0}$		High	High	High	High	High	High	High
$\overline{CS1}$		Low	—	—	—	Low	Low	Low
$\overline{RAS}$		$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$
$\overline{CASH}$		High	$\overline{CASH}$	High	$\overline{CASH}$	High	High	High
$\overline{CASL}$		$\overline{CAS}$	High	$\overline{CASL}$	$\overline{CASL}$	$\overline{CASL}$	$\overline{CASL}$	$\overline{CASL}$
$\overline{AH}$		Low	Low	Low	Low	Low	Low	Low
$\overline{RD}$	R	Low	Low	Low	Low	Low	Low	Low
	W	High	High	High	High	High	High	High
$\overline{WRH}$	R	High	High	High	High	High	High	High
	W	High	High	High	High	Low	High	Low
$\overline{WRL}$	R	High	High	High	High	High	High	High
	W	Low	Low	Low	Low	High	Low	Low
A0		A0	A0	A0	A0	A0	A0	A0
A21–A1		Address	Address	Address	Address	Address	Address	Address
AD15–AD8		High-Z	Data	High-Z	Data	Data	High-Z	Data
AD7–AD0		Data	High-Z	Data	Data	High-Z	Data	Data
DPH		High-Z	Parity	High-Z	Parity	Parity	High-Z	Parity
DPL		Parity	High-Z	Parity	Parity	High-Z	Parity	Parity

R: Read

W: Write

—: The $\overline{CS1}$ pin is used as the $\overline{CASH}$ signal output pin.

$\overline{RAS}$: When a row address is output from A21–A0, an address strobe signal is output.

$\overline{CAS}$: When a column address is output from A21–A0, an address strobe signal is output.

$\overline{CASH}$: When a column address is output from A21–A0 during an upper byte access, an address strobe signal is output.

$\overline{CASL}$: When a column address is output from A21–A0 during a lower byte access, an address strobe signal is output.

Parity: When a DRAM space parity check is selected with the parity check enable bits (PCHK1,PCHK0) in the parity control register (PCR), this pin is used as the parity pin.

		External Memory Space						
			16-Bit Space					
			WRH, WRL, A0 System			WR, HBS, LBS System		
Pin Name		8-Bit Space	Upper Byte	Lower Byte	Word	Upper Byte	Lower Byte	Word
$\overline{CS7}$–$\overline{CS0}$		Valid	Valid	Valid	Valid	Valid	Valid	Valid
$\overline{RAS}$		High	High	High	High	High	High	High
$\overline{CASH}$		High	High	High	High	High	High	High
$\overline{CASL}$		High	High	High	High	High	High	High
$\overline{AH}$		Low	Low	Low	Low	Low	Low	Low
$\overline{RD}$	R	Low	Low	Low	Low	Low	Low	Low
	W	High	High	High	High	High	High	High
$\overline{WRH}$/$\overline{LBS}$	R	—*	High	High	High	High	Low	Low
	W	—*	Low	High	Low	High	Low	Low
$\overline{WRL}$/$\overline{WR}$	R	High	High	High	High	High	High	High
	W	Low	High	Low	Low	Low	Low	Low
A0/$\overline{HBS}$		A0	A0	A0	A0	Low	High	Low
A21–A1		Address	Address	Address	Address	Address	Address	Address
AD15–AD8		High-Z	Data	High-Z	Data	Data	High-Z	Data
AD7–AD0		Data	High-Z	Data	Data	High-Z	Data	Data
DPH		High-Z	Parity	High-Z	Parity	Parity	High-Z	Parity
DPL		Parity	High-Z	Parity	Parity	High-Z	Parity	Parity

R: Read

W: Write

Valid: Chip select signal for the area accessed is low; other chip select signals are high.

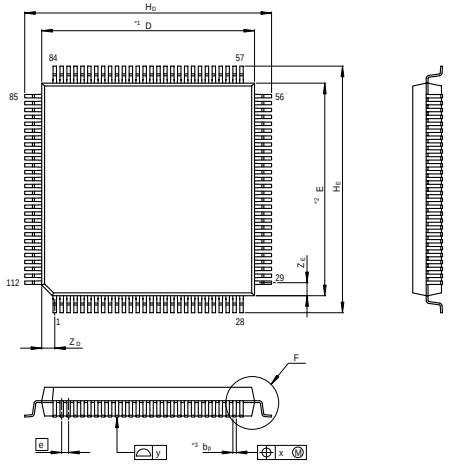
Parity: When an area 2 parity check is selected with the parity check enable bits (PCHK1, PCHK0) in the parity control register (PCR), this pin is used as the parity pin.

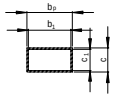
Note: * Cannot be used; available only for 16-bit space access.

Appendix C Package Dimensions

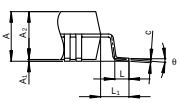
Figure C.1 and figure C.2 show the package dimensions of the SH microcomputer.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP112-20x20-0.65	PRQP0112JA-A	FP-112/FP-112V	2.4g





Terminal cross section



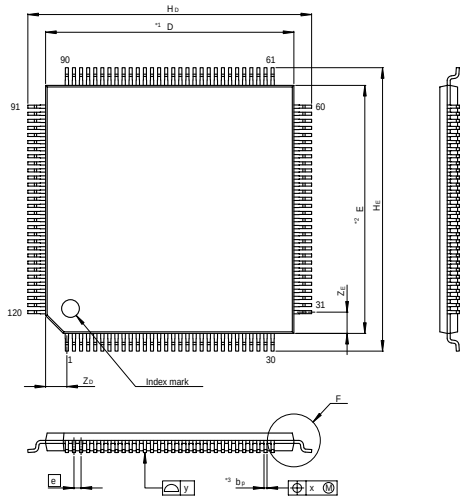
Detail F

NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	20	—
E	—	20	—
A_2	—	2.70	—
H_D	22.9	23.2	23.5
H_E	22.9	23.2	23.5
A	—	—	3.05
A_A	0.00	0.10	0.25
b_p	0.24	0.32	0.40
b_1	—	0.30	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.23	—
Z_E	—	1.23	—
L	0.5	0.8	1.1
L_1	—	1.6	—

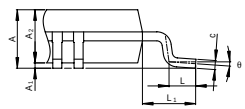
Figure C.1 Package Dimensions (PRQP0112JA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TQFP120-14x14-0.40	PTQP0120LA-A	TFP-120/TFP-120V	0.5g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	14	—
E	—	14	—
A_2	—	1.00	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.20
A_1	0.00	0.10	0.20
b_p	0.12	0.17	0.22
b_1	—	0.15	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.4	—
x	—	—	0.07
y	—	—	0.10
Z_D	—	1.20	—
Z_E	—	1.20	—
L	0.4	0.5	0.6
L_1	—	1.0	—

Figure C.2 Package Dimensions (PTQP0120LA-A)

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Hardware Manual
SH7032, SH7034

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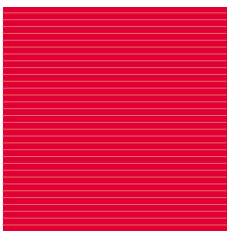
SH7032, SH7034
Hardware Manual



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